National Semiconductor

400039 Rev. 1

CMOS Logic Databook

- *MM54HC/74HC/54HCT/74HCT High Speed CMOS Family*
- *CD4000 Family*
- *MM54C/74C Family*
- *Surface Mount*

For Information on FACT™ (Fairchild Advanced CMOS Technology) logic, see the FACT DATABOOK



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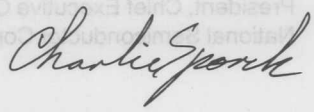
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CMOS LOGIC
DATABOOK

1988 Edition

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Introduction

This comprehensive databook provides information on National Semiconductor's advanced CMOS logic families MM54HC/74HC high speed, CD4000 and MM54C/74HC. The MM54HC/74HC family utilizes microCMOS technology to achieve the input and power supply characteristics of CMOS with the high speed and large output drive of low power Schottky. The MM54HC/74HC family has the same pinout as equivalent 54LS/74LS; in addition, many popular CD4000 series logic functions are offered where no equivalent TTL function exists.

The MM54HCT/74HCT is a subfamily of MM54HC/74HC offering TTL inputs. These MM54HCT/74HCT devices offer convenient TTL level translation to CMOS for those places in the system where only TTL levels are provided.

The CD4000 series is National Semiconductor's extensive line of CD40XXB and CD45XXB series devices. These parts meet the standard JEDEC "B-Series" specifications.

The popular MM54C/74C series logic family metal-gate CMOS technology is pin-for-pin and function-for-function equivalent to the 54/74 family of TTL devices. Unique special function LSI devices in this family are compatible with MM54HC/74HC and CD4000 series.

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Section 1

CMOS AC Switching Test Circuits and Timing Waveforms

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National Semiconductor

AC Parameter Definitions

f_{MAX} Operating frequency. This is the fastest speed that a circuit can be toggled.

t_{PHL} Propagation delay from input to output; output going high to low.

t_{PLH} Propagation delay from input to output; output going low to high.

t_{PZH} Enable propagation delay time. This is measured from the input to the output going to an active high level from TRI-STATE®.

t_{PZL} Enable propagation delay time. This is measured from the input to the output going to an active low level from TRI-STATE.

t_{PHZ} Disable propagation delay time to the output going from an active high level to TRI-STATE.

t_{PLZ} Disable propagation delay time to the output going from an active low level to TRI-STATE.

t_W Input signal pulse width.

t_S Input setup time. This is the time that data must be present prior to clocking input transitioning.

t_H Input hold time. This is the time that data must remain after clocking input has transitioned.

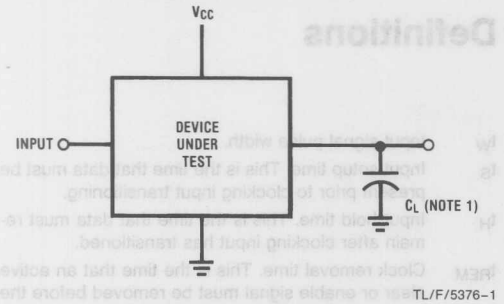
t_{REM} Clock removal time. This is the time that an active clear or enable signal must be removed before the clock input transitions. (Sometimes called recovery time.)

t_r Input signal rise time.

t_f Input signal fall time.

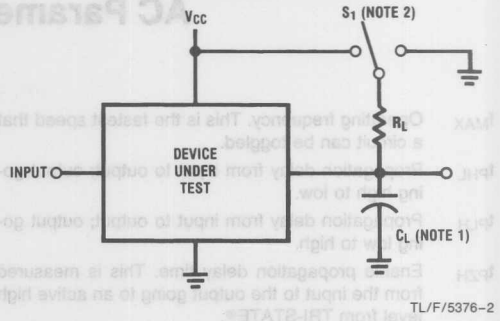
t_{TLH} Output rise time (transition time low to high).

t_{THL} Output fall time (transition time high to low).



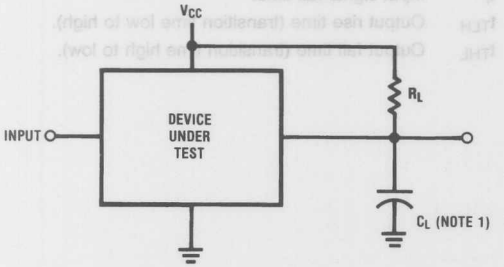
TL/F/5376–1

Output Tests (Notes 2 and 3)



TL/F/5376–2

Test Circuit for Open Drain Outputs



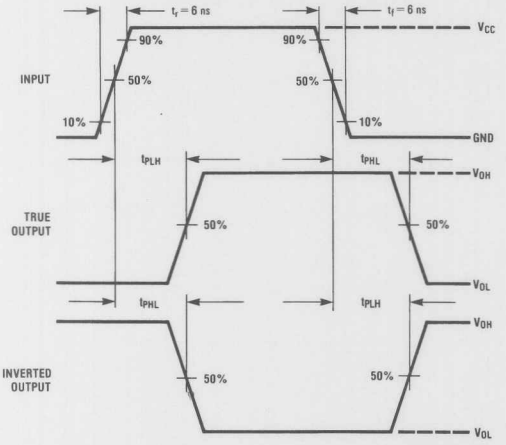
TL/F/5376–3

Note 1: C_L includes load and test jig capacitance. See data sheets for values.

Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

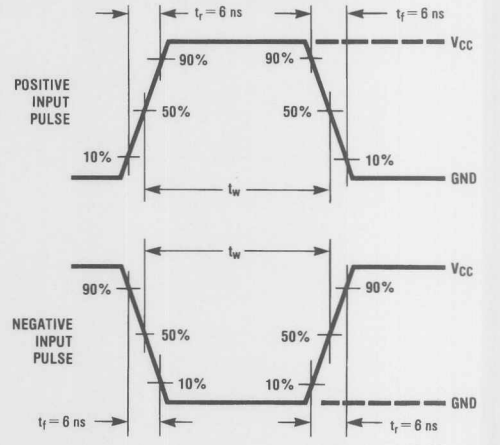
Note 3: For open drain devices S1 = V_{CC} and measurements are same as t_{PZL} and t_{PLZ}.

Propagation Delay Waveforms



TL/F/5376–4

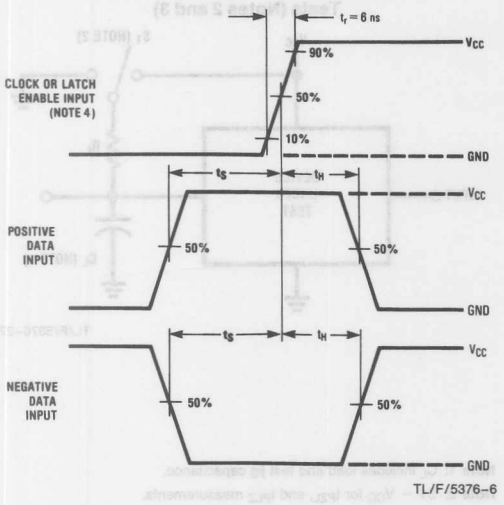
Input Pulse Width Waveforms



TL/F/5376–5

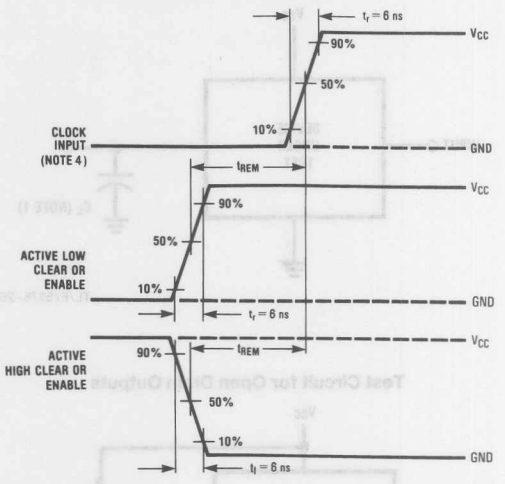
MM54HC/MM74HC AC Switching Test Circuits and Timing Waveforms (Continued)

Setup and Hold Time Waveforms



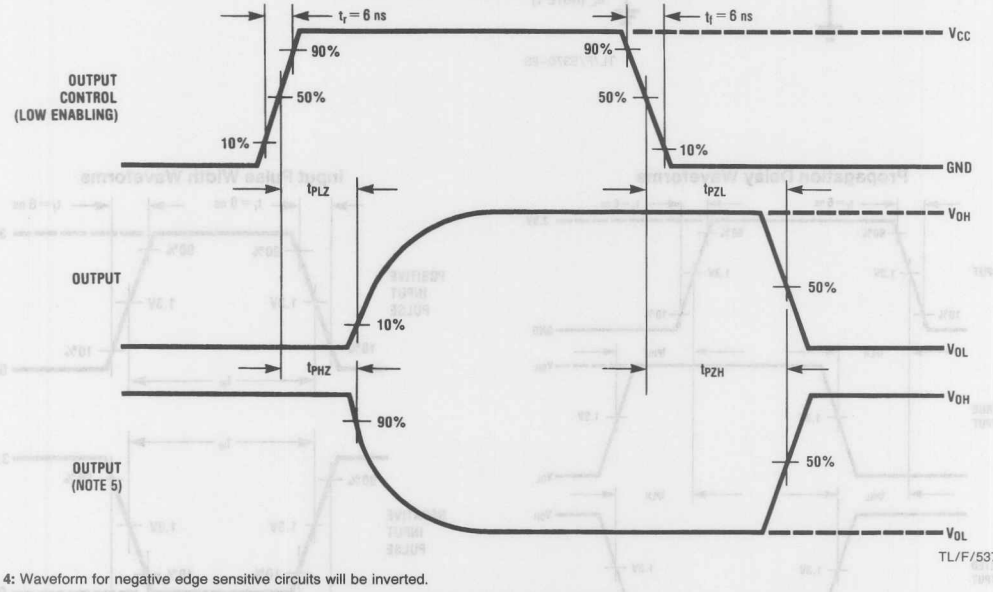
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Removal Time Waveforms



TL/F/5376–7

TRI-STATE Output Enable and Disable Waveforms



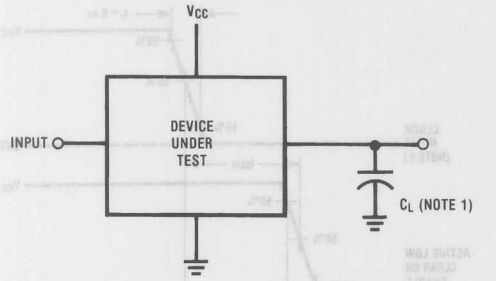
TL/F/5376–8

Note 4: Waveform for negative edge sensitive circuits will be inverted.

Note 5: This waveform is applicable to both TRI-STATE and open drain switching time measurements.

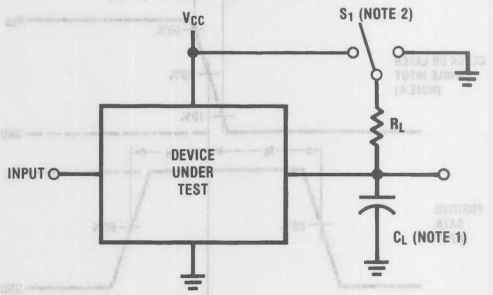
MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms

Test Circuit for Push Pull Outputs



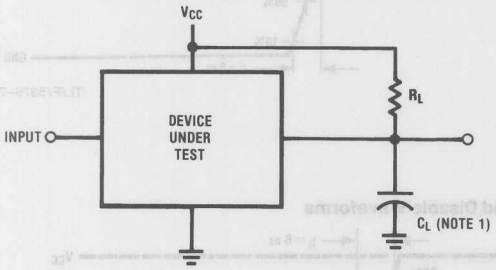
TL/F/5376–26

Test Circuit for TRI-STATE and Open Drain Output Tests (Notes 2 and 3)



TL/F/5376–27

Test Circuit for Open Drain Outputs



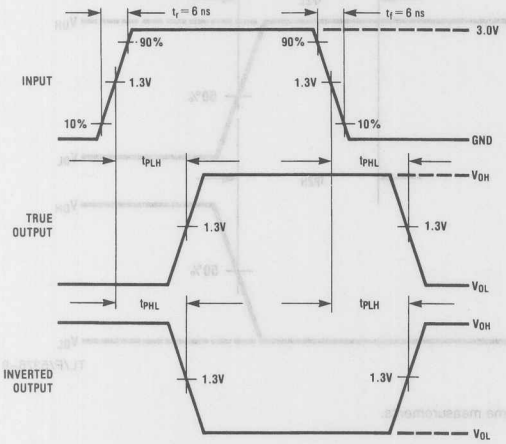
TL/F/5376–28

Note 1: C_L includes load and test jig capacitance.

Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

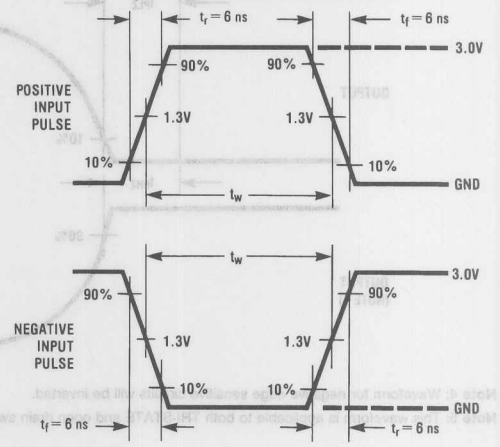
Note 3: For open drain circuits S1 = V_{CC} and measurements are the same as t_{PZL} and t_{PLZ}.

Propagation Delay Waveforms



TL/F/5376–9

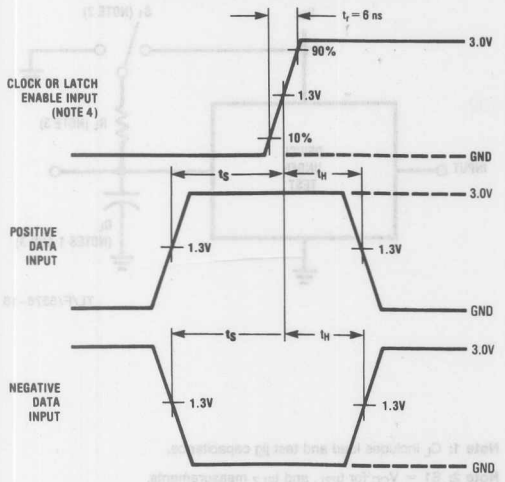
Input Pulse Width Waveforms



TL/F/5376–10

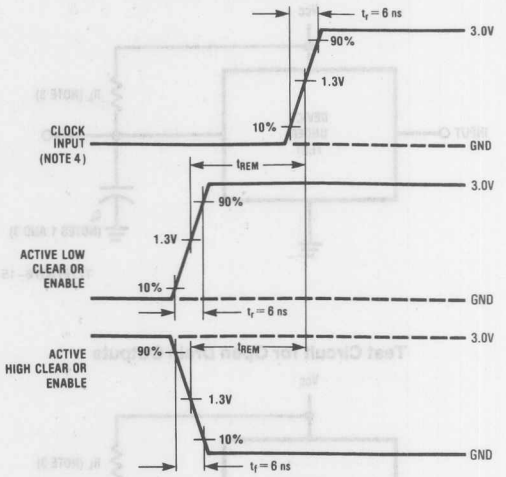
MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms (Continued)

Setup and Hold Time Waveforms



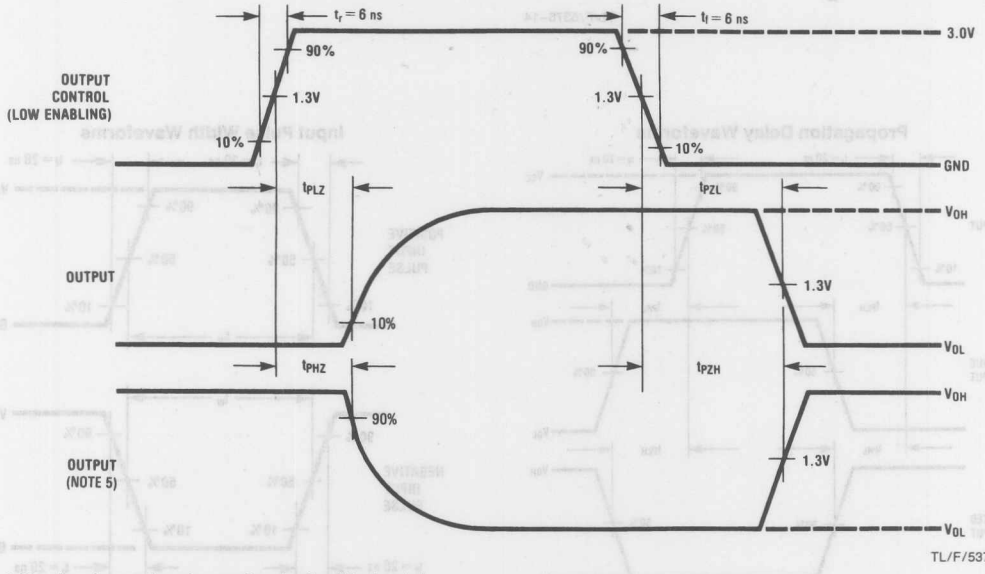
TL/F/5376–11

Removal Time Waveforms



TL/F/5376–12

TRI-STATE Output Enable and Disable Waveforms



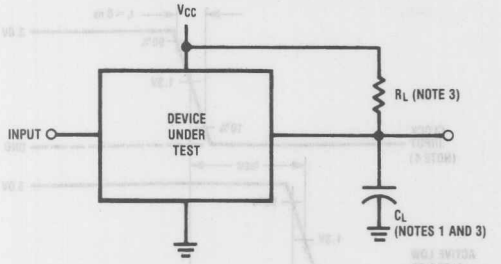
TL/F/5376–13

Note 4: Waveform for negative edge sensitive circuits will be inverted.

Note 5: This waveform is applicable to both TRI-STATE and open drain switching time measurments.

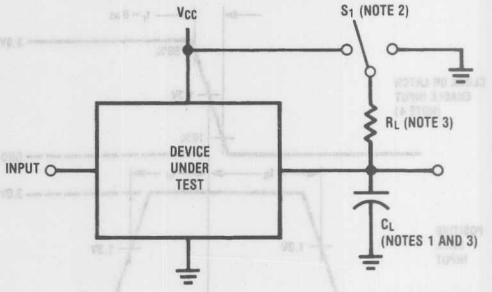
CD4000 AC Switching Test Circuits and Timing Waveforms

Test Circuit for Push Pull Outputs



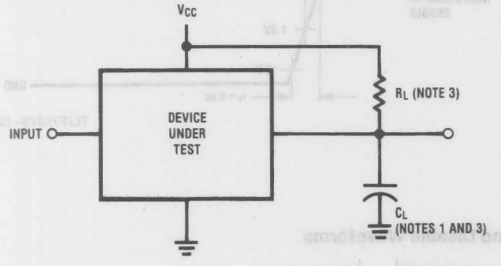
TL/F/5376–15

Test Circuit for TRI-STATE Output Tests



TL/F/5376–16

Test Circuit for Open Drain Outputs



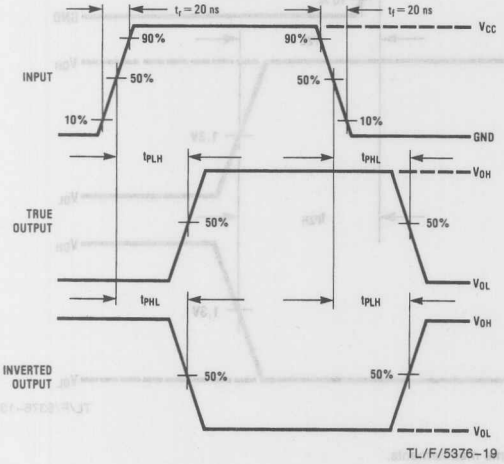
TL/F/5376–14

Note 1: C_L includes load and test jig capacitance.

Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

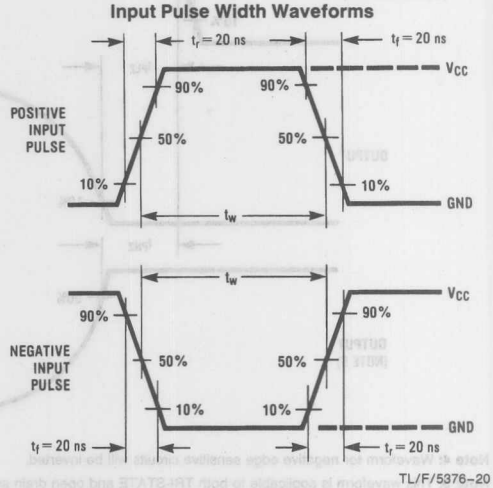
Note 3: See individual data sheet for component values.

Propagation Delay Waveforms



TL/F/5376–19

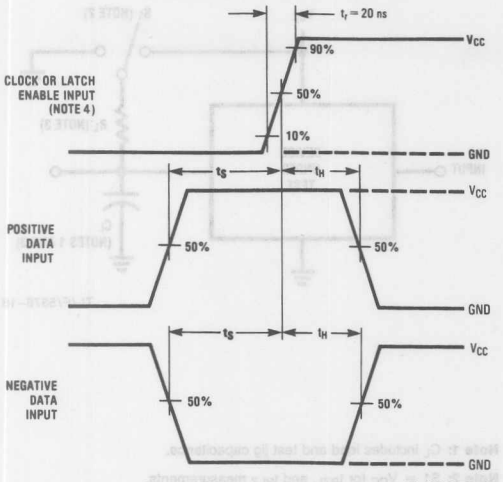
Input Pulse Width Waveforms



TL/F/5376–20

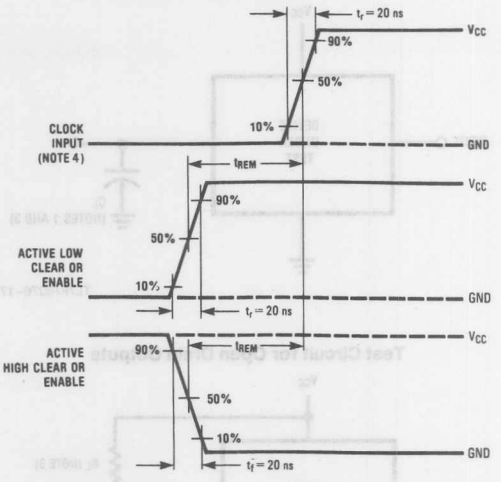
CD4000 AC Switching Test Circuits and Timing Waveforms (Continued)

Setup and Hold Time Waveforms



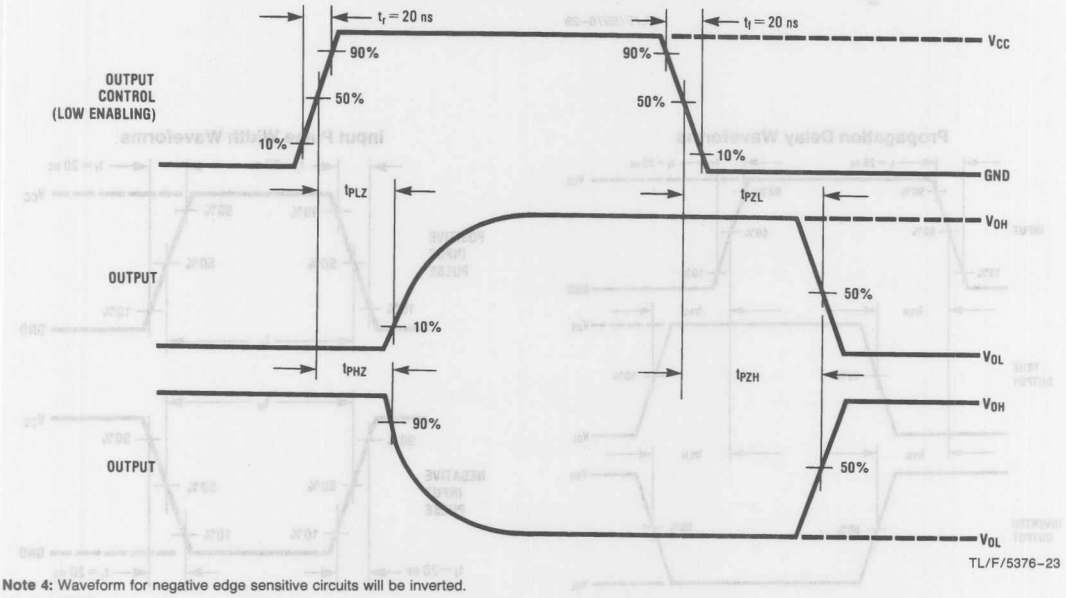
TL/F/5376–21

Removal Time Waveforms



TL/F/5376–22

TRI-STATE Output Enable and Disable Waveforms

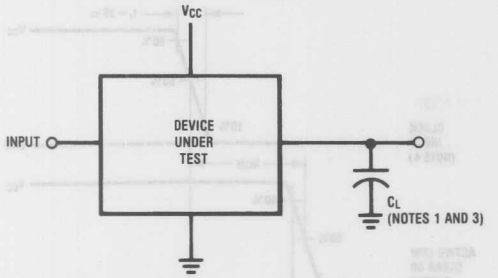


TL/F/5376–23

Note 4: Waveform for negative edge sensitive circuits will be inverted.

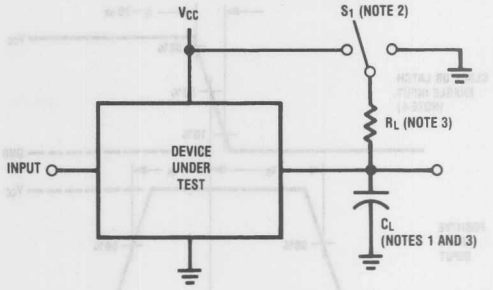
MM54C/MM74C AC Switching Test Circuits and Timing Waveforms

Test Circuit for Push Pull Outputs



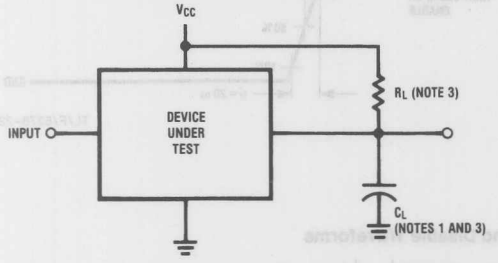
TL/F/5376–17

Test Circuit for TRI-STATE Output Tests



TL/F/5376–18

Test Circuit for Open Drain Outputs



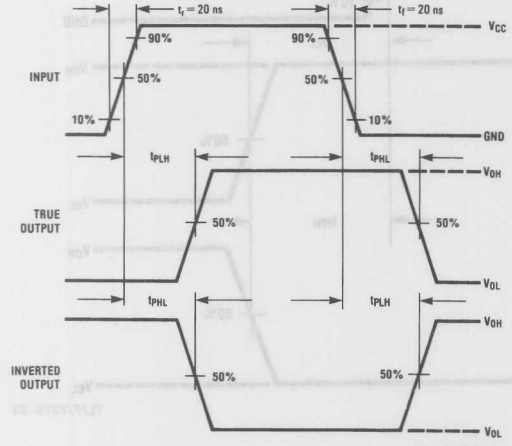
TL/F/5376–29

Note 1: C_L includes load and test jig capacitance.

Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = GND for t_{PZH}, and t_{PHZ} measurements.

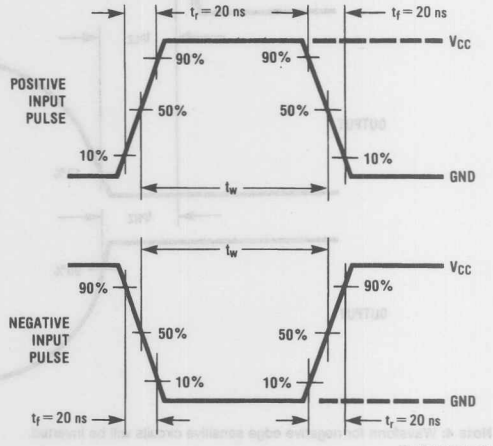
Note 3: See individual data sheet for component values.

Propagation Delay Waveforms



TL/F/5376–24

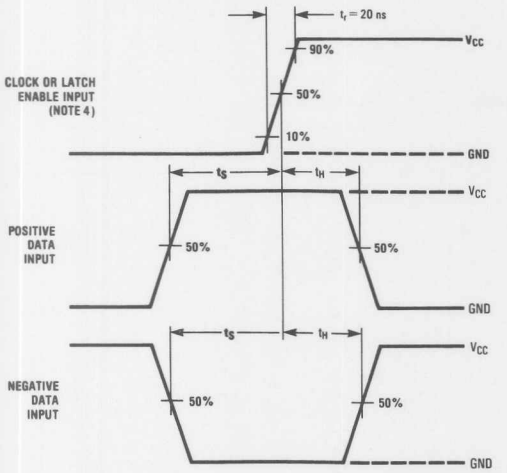
Input Pulse Width Waveforms



TL/F/5376–25

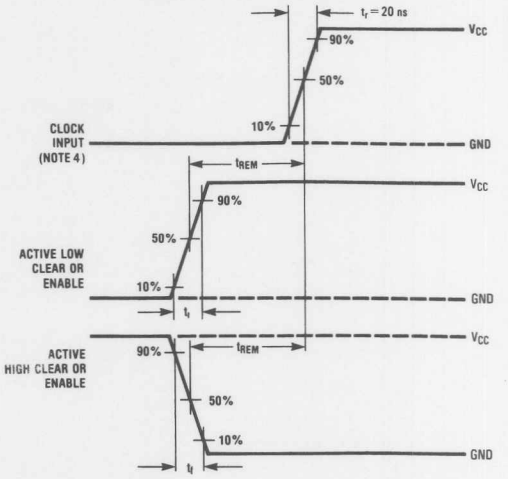
MM54C/MM74C AC Switching Test Circuits and Timing Waveforms (Continued)

Setup and Hold Time Waveforms



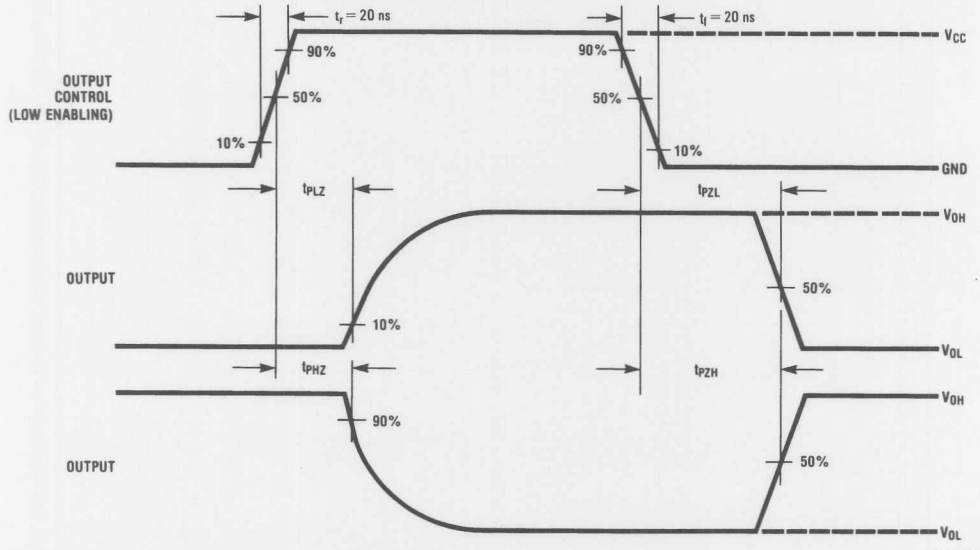
TL/F/5376–30

Removal Time Waveforms



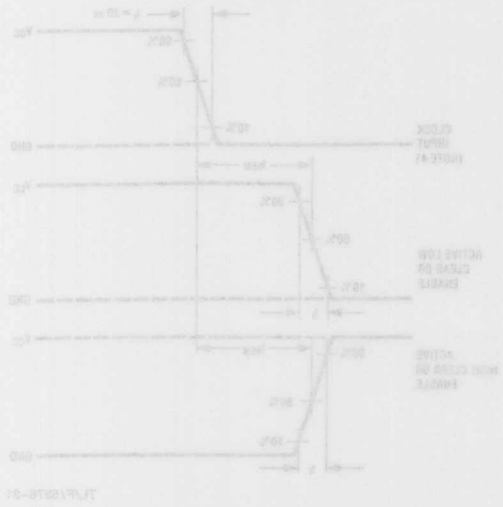
TL/F/5376–31

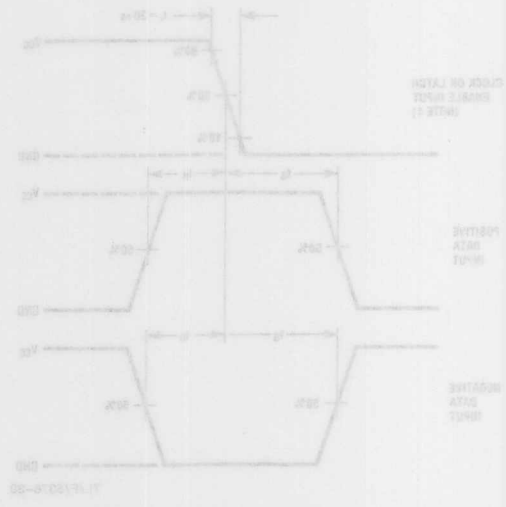
TRI-STATE Output Enable and Disable Waveforms

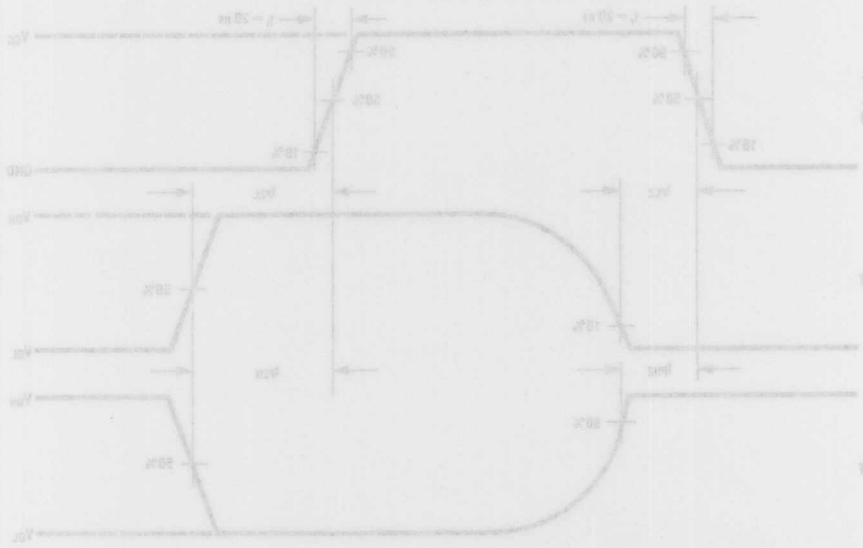


TL/F/5376–32

Note 4: Waveform for negative edge sensitive circuits will be inverted.







Section 2
CMOS Application Notes

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CMOS, the Ideal Logic Family

National Semiconductor
Application Note 77
Stephen Calebotta

INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1 MHz with a 50 pF load is less than 10 mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 ns to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore, cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So, an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that, even at today's prices, CMOS is the most economical choice.

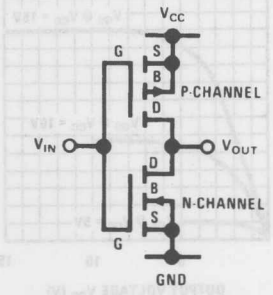
National is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/74C series which National introduced and which will become the industry standard in the near future.

The 54C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is spec'd at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, −55°C to +125°C or 74C, −40°C to +85°C. Table I compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS, a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in *Figure 2-1.* It consists of two MOS enhancement mode transistors, the upper a P-channel type, the lower an N-channel type.



TL/F/6019–1

FIGURE 2-1. Basic CMOS Inverter

The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomenclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device

TABLE I. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters

Family	V_{CC}	V_{IL} Max	I_{IL} Max	V_{IH} Min	I_{IH} 2.4V	V_{OL} Max	I_{OL}	V_{OH} Min	I_{OH}	t_{pd0} Typ	t_{pd1} Typ	P_{DISS}/Gate Static	P_{DISS}/Gate 1 MHz, 50 pF Load
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100 μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	—	3.5	—	0.4	*360 μA	2.4	*100 μA	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	—	8.0	—	1.0	**10 μA	9.0	**10 μA	25	30	0.00003 mW	5 mW

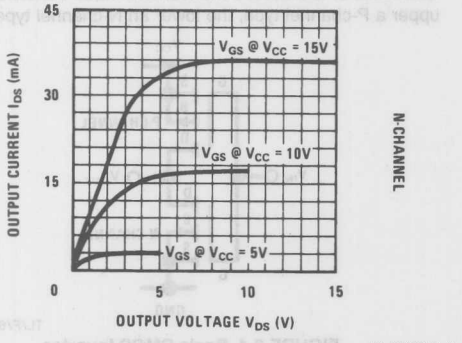
*Assumes interfacing to low power TTL.

**Assumes interfacing to CMOS.

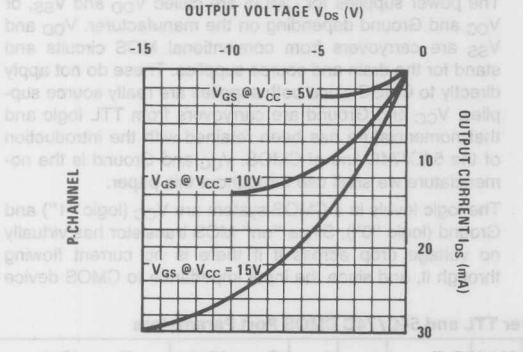
is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. *Figure 2-2* shows the characteristic curves of N-channel and P-channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of V_{GS} = 15V (Gate to Source Voltage) for the N-channel transistor. Note that for a constant drive voltage V_{GS}, the transistor behaves like a current source for V_{DS}'s (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor). For V_{DS}'s below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS}'s, there are similar curves except that the magnitude of the I_{DS}'s are significantly smaller and that in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The P-channel transistor exhibits essentially identical, but complemented, characteristics.



TL/F/6019–2



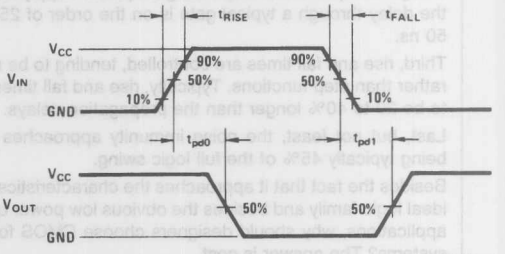
TL/F/6019–3

FIGURE 2-2. Logical "1" Output Voltage vs Source Current

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp-like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in *Figure 2-1*, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P-channel or N-channel transistor is conducting.

Now if we increase V_{CC} and, therefore, V_{GS} the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and, therefore, the rise times and the propagation delays through the inverter as measured in *Figure 2-3* have decreased.

So, we can see that for a given design, and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system. Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit, or any other circuit for that matter, when driving a capacitive load.



TL/F/6019–4

FIGURE 2-3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the VI power dissipated in the CMOS circuit increases with V_{CC} (for V_{CC}'s > $2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC}, the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the J_{DS} currents. Incidently, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and, therefore, the input voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize VI power dissipation.

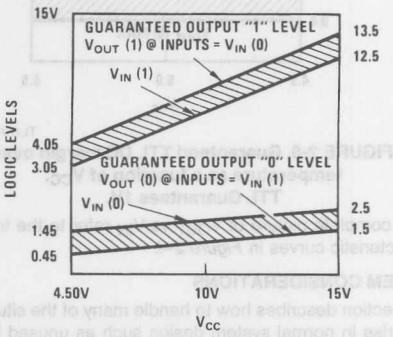
Let's look at the transfer characteristics, *Figure 2-4*, as they vary with V_{CC}. For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages, V_T, to be 2V. If V_{CC} is

less than the threshold voltage of 2V, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly then we are on the curve shown on *Figure 2-4a.* We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages *(Figure 2-4b),* then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ *(Figure 2-4c).* At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds the transfer curves begin to round off *(Figure 2-4d).* As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them, giving the rounded characteristic.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 0.45 V_{CC} or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit. In fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a 0.45 V_{CC} spurious pulse on the clock line would not cause the flop to change state.

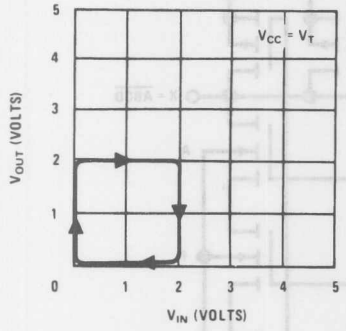
National also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within 0.1 V_{CC} volts of a proper logic level (V_{CC} or Ground), the input can be as much as 0.1 V_{CC} plus 1V away from power supply rail. Shown graphically we have:



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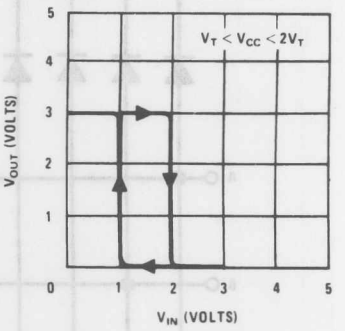
FIGURE 2-5. Guaranteed CMOS DC margin over temperature as a function of V_{CC}. CMOS Guarantees 1V.

This is similar in nature to the standard TTL noise margin spec which is 0.4V.



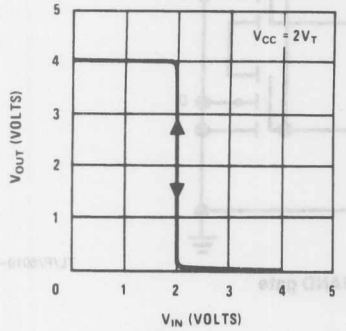
(a)

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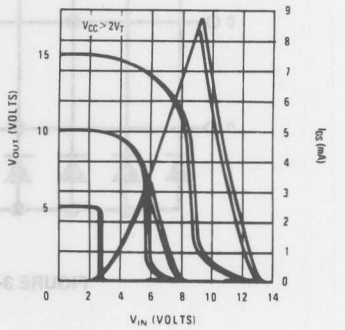
(b)

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(c)

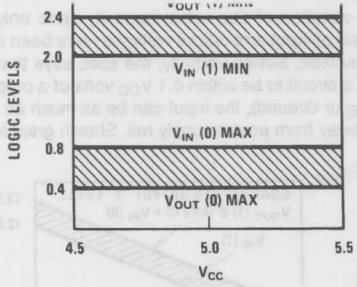
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(d)

TL/F/6019–8

FIGURE 2-4. Transfer Characteristics vs V_{CC}



TL/F/6019–10

FIGURE 2-6. Guaranteed TTL DC margin over temperature as a function of V_{CC}. TTL Guarantees 1V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in *Figure 2-4.*

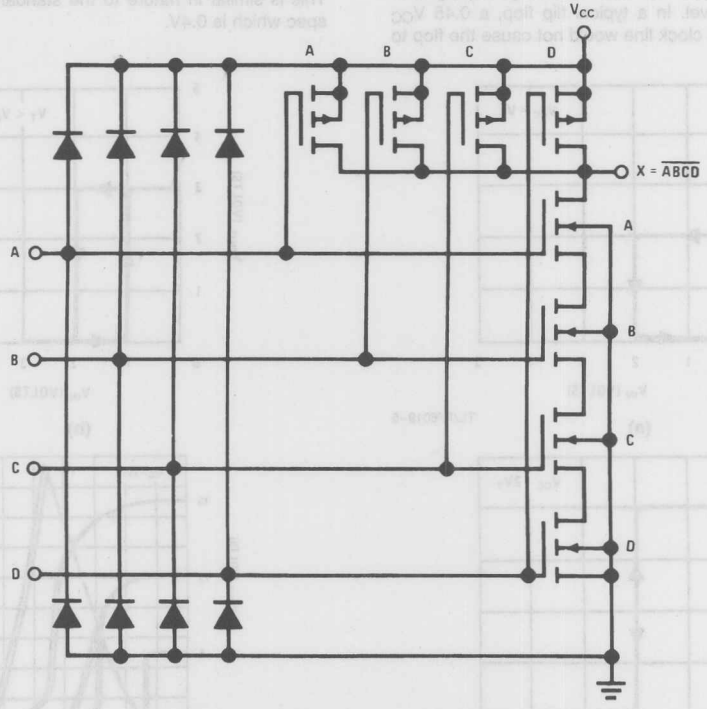
SYSTEM CONSIDERATIONS

This section describes how to handle many of the situations that arise in normal system design such as unused inputs, paralleling circuits for extra drive, data bussing, power considerations and interfaces to other logic families.

Unused inputs: Simply stated, unused inputs should not be left open. Because of the very high impedance ($\sim 10^{12}\Omega$), a input. The choice is not completely arbitrary, however, since there will be an effect on the output drive capability of the circuit in question. Take, for example, a four input NAND gate being used as a two input gate. The internal structure is shown in *Figure 3-1.* Let inputs A and B be the unused inputs.

If we are going to tie the unused inputs to a logic level, inputs A and B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most, only two of the upper transistors could ever be turned on. However, if inputs A and B were tied to input C, the input capacitance would triple, but each time C went low, the upper A, B and C transistors would turn on, tripling the available source current. If input D was low also, all four of the upper transistors would be on.

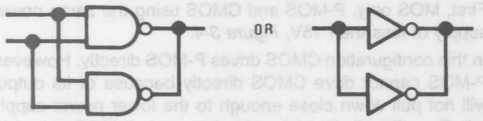
So, tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them, but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates). There is no increase in drive possible through the series transistors. By using this approach, a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.



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FIGURE 3-1. MM74C20 Four Input NAND gate

Parallel gates: Depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in *Figure 3-2.* This insures that there are a number of parallel combinations of the series string of transistors *(Figure 3-1),* thereby increasing drive in that direction also.



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FIGURE 3-2. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

Data bussing: There are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (Part No. CD4016C). Second, and the preferred way, is to use parts specifically designed with a CMOS equivalent of a TRI-STATE® output.

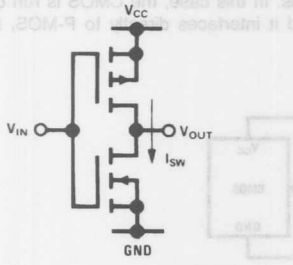
Power supply filtering: Since CMOS can operate over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply voltage required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: To minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the VI power dissipated during switching. In any CMOS device during switching, there is a momentary current path from the power supply to ground, (when $V_{CC} > 2V_T$) *Figure 3-3.*

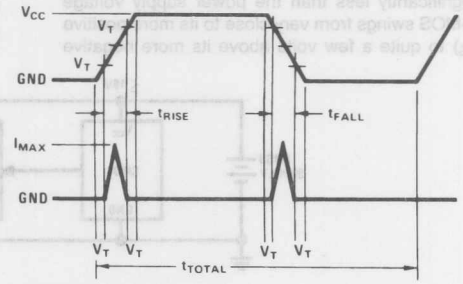
The maximum amplitude of the current is a rapidly increasing function of the input voltage which in turn is a direct function of the power supply voltage. See *Figure 2-4d.*

The actual amount of VI power dissipated by the system is determined by three things: power supply voltage, frequency and input signal rise time. A very important factor is the input rise time. If the rise time is long, power dissipation increases since the current path is established for the entire period that the input signal is passing through the region between the threshold voltages of the upper and lower transistors. Theoretically, if the rise time were zero, no current path would be established and the VI power would be zero. However, with a finite rise time there is always some current flow and this current flow increases rapidly with power supply voltage.

Just a thought about rise time and power dissipation. If a circuit is used to drive many loads, its output rise time will suffer. This will result in an increase in VI power dissipation in every device being driven by that circuit (but not in the drive circuit itself). If power consumption is critical, it may be necessary to improve the rise time of that circuit by buffering or by dividing the loads in order to reduce overall power consumption.



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VI Power is Given By:

$$P_{VI} = V_{CC} \times \frac{1}{2} I_{Max} \times \text{Rise Time to Period Ratio}$$

$$\text{Rise Time to Period Ratio} = \frac{V_{CC} - 2V_T}{V_{CC}} \times \frac{t_{RISE} + t_{FALL}}{t_{TOTAL}}$$

$$\text{Where } \frac{1}{t_{TOTAL}} = \text{Frequency}$$

$$P_{VI} = \tfrac{1}{2} (V_{CC} - 2V_T)\, I_{CC\ Max} (t_{RISE} + t_{FALL})\, \text{FREQ.}$$

FIGURE 3-3. DC Transient Power

So, to summarize the effects of power supply voltage, input voltage, input rise time and output load capacitance on system power dissipation, we can say the following:

1. **Power supply voltage:** CV^2f power dissipation increases as the square of power supply voltage. VI power dissipation increases approximately as the square of the power supply voltage.
2. **Input voltage level:** VI power dissipation increases if the input voltage lies somewhere between Ground plus a threshold voltage and V_{CC} minus a threshold voltage. The highest power dissipation occurs when V_{IN} is at ½ V_{CC}. CV^2f dissipation is unaffected.
3. **Input rise time:** VI power dissipation increases with longer rise times since the DC current path through the device is established for a longer period. The CV^2f power is unaffected by slow input rise times.
4. **Output load capacitance:** The CV^2f power dissipated in a circuit increases directly with load capacitance. VI power in a circuit is unaffected by its output load capacitance. However, increasing output load capacitance will slow down the output rise time of a circuit which in turn will affect the VI power dissipation in the devices it is driving.

INTERFACES TO OTHER LOGIC TYPES

There are two main ideas behind all of the following interfaces to CMOS. First, CMOS outputs should satisfy the current and voltage requirements of the other family's inputs. Second, and probably most important, the other family's outputs should swing as near as possible to the full voltage range of the CMOS power supplies.

P-Channel MOS: There are a number of things to watch for when interfacing CMOS and P-MOS. The first is the power supply set. Most of the more popular P-MOS parts are specified with 17V to 24V power supplies while the maximum power supply voltage for CMOS is 15V. Another problem is that unlike CMOS, the output swing of a push-pull P-MOS output is significantly less than the power supply voltage across it. P-MOS swings from very close to its more positive supply (V_{SS}) to quite a few volts above its more negative supply (V_{DD}). So, even if P-MOS uses a 15V or lower power supply set, its output swing will not go low enough for a reliable interface to CMOS. There are a number of ways to solve this problem depending on the configuration of the system. We will discuss two solutions for systems that are built totally with MOS and one solution for systems that include bipolar logic.

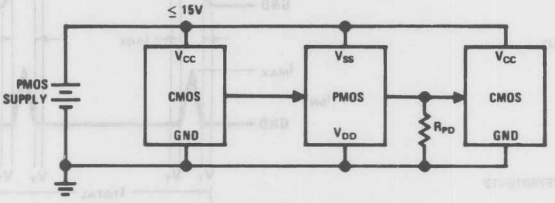
First, MOS only. P-MOS and CMOS using the same power supply of less than 15V, *Figure 3-4.*

In this configuration CMOS drives P-MOS directly. However, P-MOS cannot drive CMOS directly because of its output will not pull down close enough to the lower power supply rail. R_{PD} (R pull down) is added to each P-MOS output to pull it all the way down to the lower rail. Its value is selected such that it is small enough to give the desired RC time constant when pulling down but not so small that the P-MOS output cannot pull it virtually all the way up to the upper power supply rail when it needs to. This approach will work with push-pull as well as open drain P-MOS outputs.

Another approach in a purely MOS system is to build a cheap zener supply to bias up the lower power supply rail of CMOS, *Figure 3-5.*

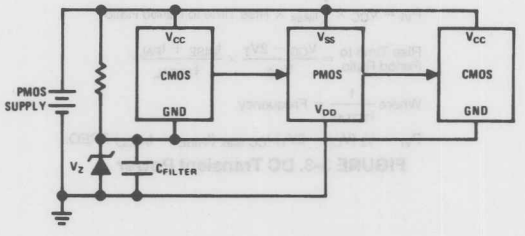
In this configuration the P-MOS supply is selected to satisfy the P-MOS voltage requirement. The bias supply voltage is selected to reduce the total voltage across the CMOS (and therefore its logic swing) to match the minimum swing of the P-MOS outputs. The CMOS can still drive P-MOS directly and now the P-MOS can drive CMOS with no pull-down resistors. The other restrictions are that the total voltage across the CMOS is less than 15V and that the bias supply can handle the current requirements of all the CMOS. This approach is useful if the P-MOS supply must be greater than 15V and the CMOS current requirement is low enough to be done easily with a small discrete component regulator.

If the system has bipolar logic, it will usually have at least two power supplies. In this case, the CMOS is run off the bipolar supply and it interfaces directly to P-MOS, *Figure 3-6.*



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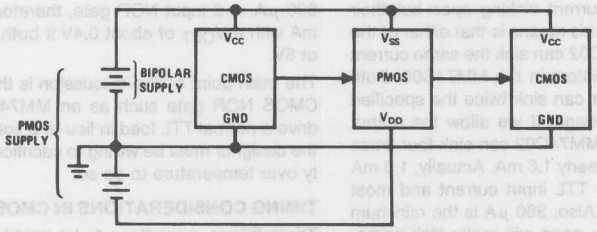
FIGURE 3-4. A One Power Supply System Built Entirely of CMOS and P-MOS



TL/F/6019–16

Use a Bias supply to reduce the voltage across the CMOS to match the logic swing of the P-MOS. Make sure the resulting voltage across the CMOS is less than 15V.

FIGURE 3-5. A P-MOS and CMOS System Where the P-MOS Supply is Greater than 15V



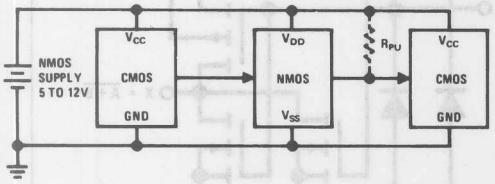
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Run the CMOS from the bipolar supply and interface directly to P-MOS.

FIGURE 3-6. A System with CMOS, P-MOS and Bipolar Logic

N-Channel MOS: Interfacing to N-MOS is somewhat simpler than interfacing to P-MOS although similar problems exist. First, N-MOS requires lower power supplies than P-MOS, being in the range of 5V to 12V. This is directly compatible with CMOS. Second, N-MOS logic levels range from slightly above the lower supply rail to about 1V to 2V below the upper rail.

At the higher power supply voltages, N-MOS and CMOS can be interfaced directly since the N-MOS high logic level will be only about 10 to 20 percent below the upper rail. However, at lower supply voltages the N-MOS output will be down 20 to 40 percent below the upper rail and something may have to be done to raise it. The simplest solution is to add pull up resistors on the N-MOS outputs as shown in *Figure 3-7.*



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Both operate off same supply with pull up resistors optional from N-MOS to CMOS.

FIGURE 3-7. A System with CMOS and N-MOS Only

TTL, LPTTL, DTL: Two questions arise when interfacing bipolar logic families to CMOS. First, is the bipolar family's logic "1" output voltage high enough to drive CMOS directly?

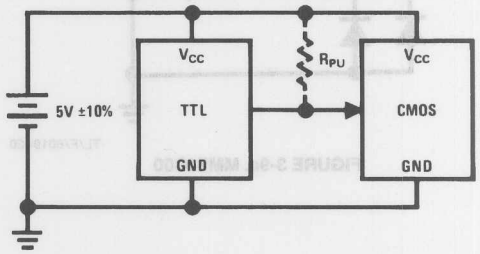
TTL, LPTTL, and DTL can drive 74C series CMOS directly over the commercial temperature range without external pull up resistors. However, TTL and LPTTL cannot drive 4000 series CMOS directly (DTL can) since 4000 series specs do not guarantee that a direct interface with no pull up resistors will operate properly.

DTL and LPTTL manufactured by National (NS LPTTL pulls up one diode drop higher than the LPTTL of other vendors) will also drive 74C directly over the entire military temperature range. LPTTL manufactured by other vendors and standard TTL will drive 74C directly over most of the military temperature range. However, the TTL logic "1" drops to a somewhat marginal level toward the lower end of the military temperature range and a pull up resistor is recommended.

According to the curve of DC margin vs V_{CC} for CMOS in *Figure 2-5,* if the CMOS sees an input voltage greater than $V_{CC} - 1.5V$ ($V_{CC} = 5V$), the output is guaranteed to be less than 0.5V from Ground. The next CMOS element will amplify this 0.5V level to the proper logic levels of V_{CC} or Ground. The standard TTL logic "1" spec is a V_{OUT} min. of 2.4V sourcing a current of 400 μA. This is an extremely conservative spec since a TTL output will only approach a one level of 2.4V under the extreme worst case conditions of lowest temperature, high input voltage (0.8V), highest possible leakage currents (into succeeding TTL devices), and V_{CC} at the lowest allowable ($V_{CC} = 4.5V$).

Under nominal conditions (25°C, $V_{IN} = 0.4V$, nominal leakage currents into CMOS and $V_{CC} = 5V$) a TTL logic "1" will be more like $V_{CC} - 2V_D$, or $V_{CC} - 1.2V$. Varying only temperature, the output will change by two times -2 mV per °C, or -4 mV per °C. $V_{CC} - 1.2V$ is more than enough to drive CMOS reliably without the use of a pull up resistor.

If the system is such that the TTL logic "1" output can drop below $V_{CC} - 1.5V$, use a pull up resistor to improve the logic "1" voltage into the CMOS.



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Pull up resistor, R_{PU}, is needed only at the lower end of the Mil temperature range.

FIGURE 3-8. TTL to CMOS Interface

The second question is, can CMOS sink the bipolar input current and not exceed the maximum value of the bipolar logic zero input voltage? The logic "1" input is no problem.

The LPTTL input current is small enough to allow CMOS to drive two loads directly. Normal power TTL input currents are ten times higher than those in LPTTL and consequently the CMOS output voltage will be well above the input logic "0" maximum of 0.8V. However, by carefully examining the CMOS output specs we will find that a two input NOR gate can drive one TTL load, albeit somewhat marginally. For example, the logical "0" output voltage for both an MM74C00 and MM74C02 over temperature is specified at 0.4V sinking 360 μA (about 420 μA at 25°C) with an input voltage of 4.0V and a V_{CC} of 4.75V. Both schematics are shown in *Figure 3-9.*

Both parts have the same current sinking spec but their structures are different. What this means is that either of the lower transistors in the MM74C02 can sink the same current as the two lower series transistors in the MM74C00. Both MM74C02 transistors together can sink twice the specified current for a given output voltage. If we allow the output voltage to go to 0.8V, then a MM74C02 can sink four times 360 μA, or 1.44 mA which is nearly 1.6 mA. Actually, 1.6 mA is the maximum spec for the TTL input current and most TTL parts run at about 1 mA. Also, 360 μA is the minimum CMOS sink current spec, the parts will really sink somewhere between 360 μA and 540 μA (between 2 and 3 LPTTL input loads). The 360 μA sink current is specified with an input voltage of 4.0V. With an input voltage of 5.0V, the sink current will be about 560 μA over temperature, making it even easier to drive TTL. At room temperature with an input voltage of 5V, a CMOS output can sink about 800 μA. A 2 input NOR gate, therefore, will sink about 1.6 mA with a V_{OUT} of about 0.4V if both NOR gate inputs are at 5V.

The main point of this discussion is that a common 2 input CMOS NOR gate such as an MM74C02 can be used to drive a normal TTL load in lieu of a special buffer. However, the designer must be willing to sacrifice some noise immunity over temperature to do so.

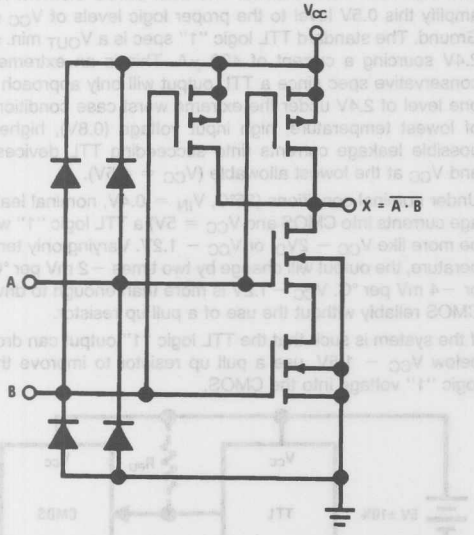


FIGURE 3-9a. MM74C00

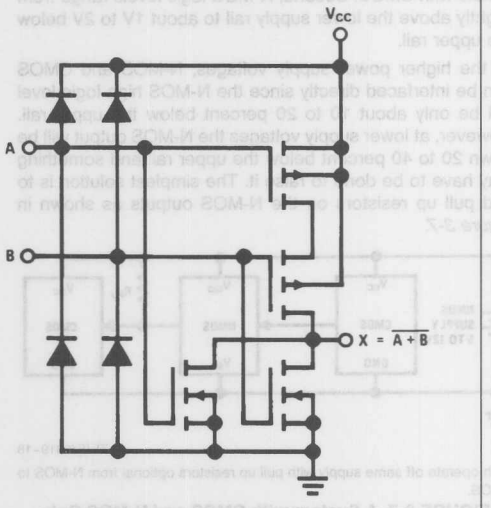


FIGURE 3-9b. MM74C02

TIMING CONSIDERATIONS IN CMOS MSIs

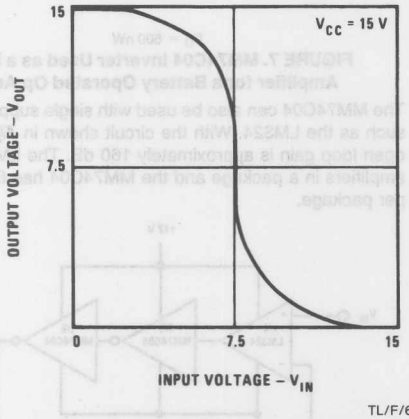
There is one more thing to be said in closing. All the flip-flops used in CMOS designs are genuinely edge sensitive. This means that the J-K flip-flops do not "ones catch" and that some of the timing restrictions that applied to the control lines on MSI functions in TTL have been relaxed in the 74C series.

CMOS Linear Applications

National Semiconductor
Application Note 88

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. *Figure 1* shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristics as shown in *Figure 1.*

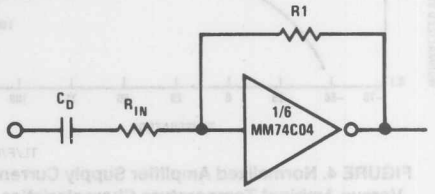


TL/F/6020–1

FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter

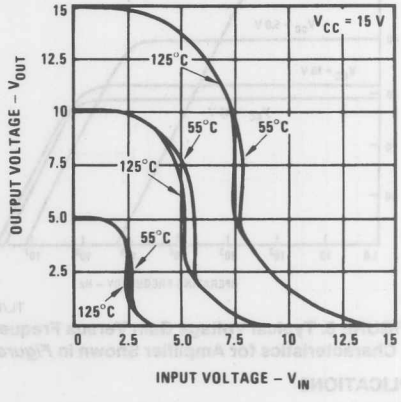
Under AC Conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. *Figure 2* shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.



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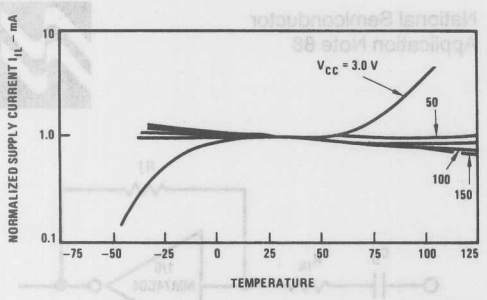
FIGURE 2. A 74CMOS Inverter Biased for Linear Mode Operation



TL/F/6020–3

FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self-biased inverter with supply voltage is shown in *Figure 4.* When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

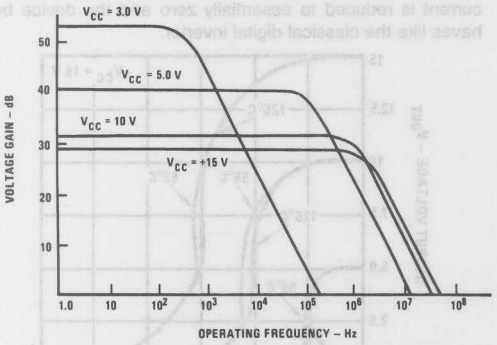


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FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or a dual supply.



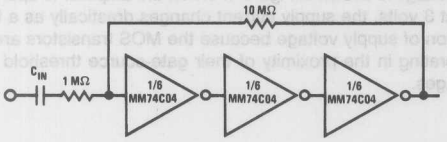
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FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in *Figure 2*

APPLICATIONS

Cascading Amplifiers for Higher Gain

By cascading the basic amplifier block shown in *Figure 2* a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in *Figure 6*) a higher open loop gain is achieved which results in more accurate closed loop gains.

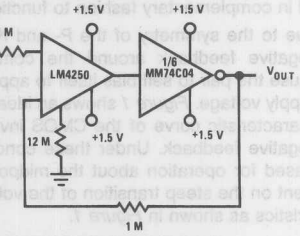


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FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier

Post Amplifier for Op Amps

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in *Figure 7* is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

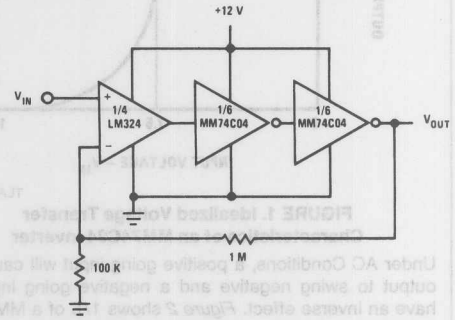


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P_D = 500 nW

FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in *Figure 8,* the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.



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FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA from the V_{CC} supply while the

MM74C02 will supply approximately 10 mA from the negative supply. Shown in *Figure 9* is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

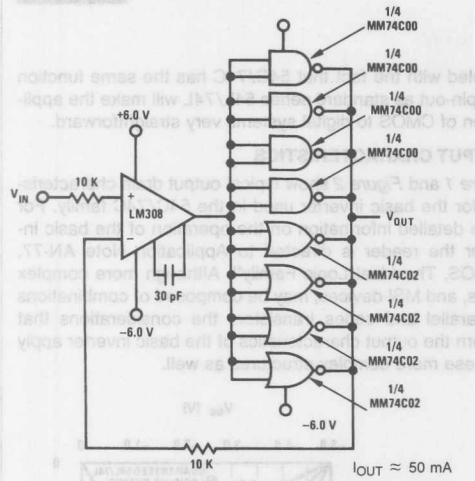


FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive

Other Applications

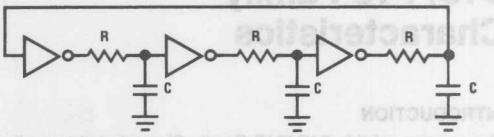
Shown in *Figure 10* is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

Conclusion

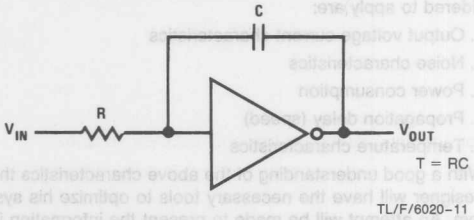
Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.

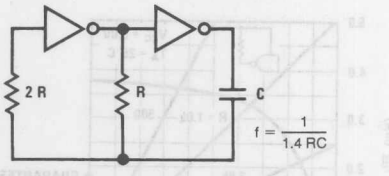
Phase Shift Oscillator Using MM74C04



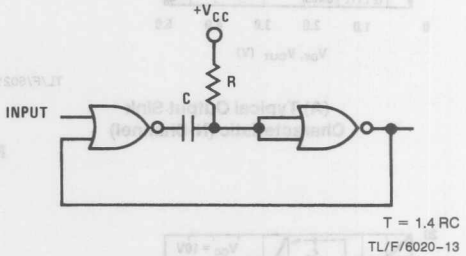
Integrator Using Any Inverting CMOS Gate



Square Wave Oscillator



One Shot



Staircase Generator

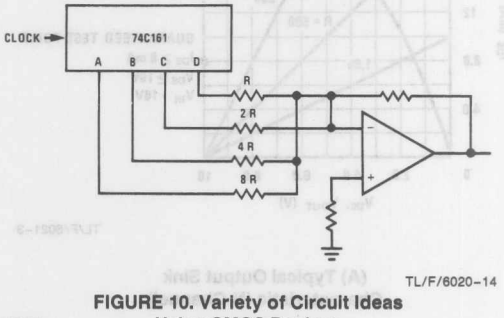


FIGURE 10. Variety of Circuit Ideas Using CMOS Devices

INTRODUCTION

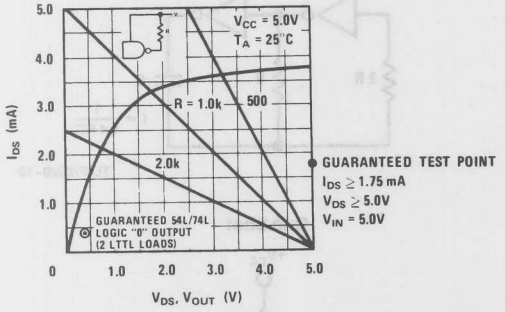
The purpose of this 54C/74C Family Characteristics application note is to set down, in one place, all those characteristics which are common to the devices in the MM54C/MM74C logic family. The characteristics which can be considered to apply are:

1. Output voltage-current characteristics
2. Noise characteristics
3. Power consumption
4. Propagation delay (speed)
5. Temperature characteristics

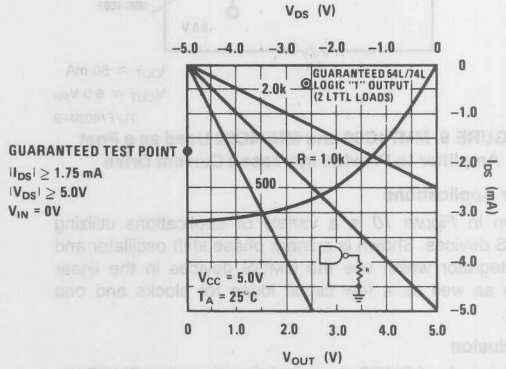
With a good understanding of the above characteristics the designer will have the necessary tools to optimize his system. An attempt will be made to present the information in as simple a manner as possible to facilitate its use. This coupled with the fact that 54C/74C has the same function and pin-out as standard series 54L/74L will make the application of CMOS to digital systems very straightforward.

OUTPUT CHARACTERISTICS

Figure 1 and *Figure 2* show typical output drain characteristics for the basic inverter used in the 54C/74C family. For more detailed information on the operation of the basic inverter the reader is directed to Application Note AN-77, "CMOS, The Ideal Logic Family". Although more complex gates, and MSI devices, may be composed of combinations of parallel and series transistors the considerations that govern the output characteristics of the basic inverter apply to these more complex structures as well.

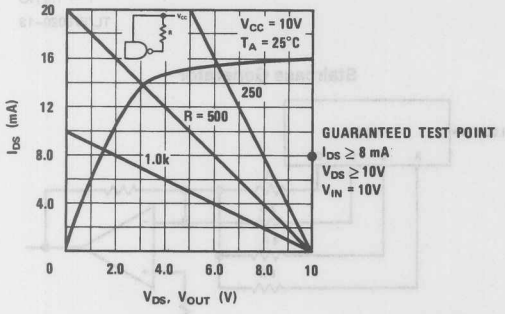


(A) Typical Output Sink Characteristic (N-Channel)

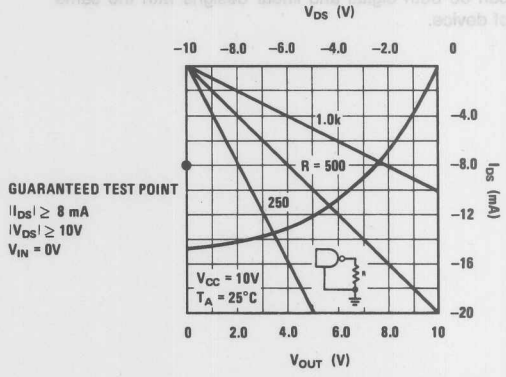


(B) Typical Output Source Characteristic (P-Channel)

FIGURE 1



(A) Typical Output Sink Characteristic (N-Channel)



(B) Typical Output Source Characteristic (P-Channel)

FIGURE 2

The 54C/74C family is designed so that the output characteristics of all devices are matched as closely as possible. To ensure uniformity all devices are tested at four output conditions (see *Figures 1* and *2*). These points are:

V_{CC} = 5.0V	V_{IN} = 5.0V $I_{DS} \geq$ 1.75 mA $V_{DS} \geq$ 5.0V	V_{IN} = 0V $\|I_{DS}\| \geq$ 1.75 mA $\|V_{DS}\| \geq$ 5.0V
V_{CC} = 10V	V_{IN} = 10V $I_{DS} \geq$ 8.0 mA $V_{DS} \geq$ 10V	V_{IN} = 0V $\|I_{DS}\| \geq$ 8.0 mA $\|V_{DS}\| \geq$ 10V

Note that each device data sheet guarantees these points in the table of electrical characteristics.

The output characteristics can be used to determine the output voltage for any load condition. *Figures 1* and *2* show load lines for resistive loads to V_{CC} for sink currents and to GND for source currents. The intersections of this load line with the drain characteristic in question gives the output voltage. For example at V_{CC} = 5.0V, V_{OUT} = 1.5V (typ) with a load of 500Ω to ground.

These figures also show the guaranteed points for driving two 54L/74L standard loads. As can be seen there is typically ample margin at V_{CC} = 5.0V.

In the case where the 54C/74C device is driving another CMOS device the load line is coincident with the I_{DS} = 0 axis and the output will then typically switch to either V_{CC} or ground.

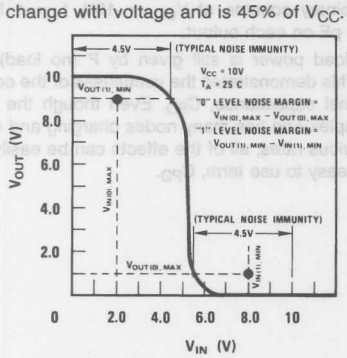
NOISE CHARACTERISTICS

Definition of Terms

Noise Immunity: The noise immunity of a logic element is that voltage which applied to the input will cause the output to change its output state.

Noise Margin: The noise margin of a logic element is the difference between the guaranteed logical "1" ("0") level output voltage and the guaranteed logical "1" ("0") level input voltage.

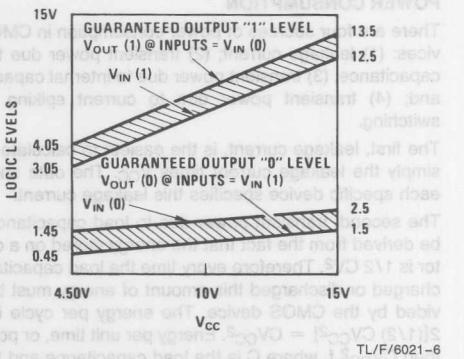
The transfer characteristic of *Figure 3* shows typical noise immunity and guaranteed noise margin for a 54C/74C device operating at V_{CC} = 10V. The typical noise immunity does not change with voltage and is 45% of V_{CC}.



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FIGURE 3. Typical Transfer Characteristics

All 54C/74C devices are guaranteed to have a noise margin of 1.0V or greater over all operating conditions (see *Figure 4*).

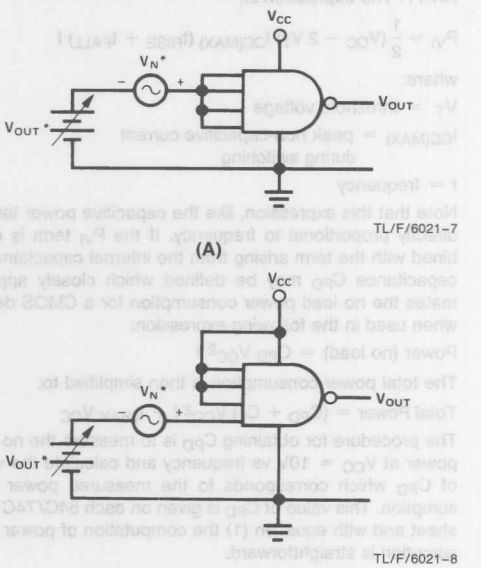


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FIGURE 4. Guaranteed Noise Margin over Temperature vs V_{CC}

Noise immunity is an important device characteristic. However, noise margin is of more use to the designer because it very simply defines the amount of noise a system can tolerate under any circumstances and still maintain the integrity of logic levels.

Any noise specification to be complete must define how measurements are to be made. *Figure 5* indicates two extreme cases; driving all inputs simultaneously and driving one input at a time. Both conditions must be included because each represents one worst case extreme.



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(A)

TL/F/6021–8

*V_{OUT} = $V_{OUT\ (1)\ MIN}$, $V_{OUT\ (0)\ MAX}$
V_N = Allowable Noise Voltage = 1.0V

(B)

FIGURE 5. Noise Margin Test Circuits

To guarantee a noise margin of 1.0V, all 54C/74C devices are tested under both conditions. It is important to note that this guarantees that every node within a system can have 1.0V of noise, in logic "1" or logic "0" state, without malfunctioning. This could not be guaranteed without testing for both conditions in *Figure 5*.

POWER CONSUMPTION

There are four sources of power consumption in CMOS devices: (1) leakage current; (2) transient power due to load capacitance; (3) transient power due to internal capacitance and; (4) transient power due to current spiking during switching.

The first, leakage current, is the easiest to calculate and is simply the leakage current times V_{CC}. The data sheet for each specific device specifies this leakage current.

The second, transient power due to load capacitance, can be derived from the fact that the energy stored on a capacitor is 1/2 CV^2. Therefore every time the load capacitance is charged or discharged this amount of energy must be provided by the CMOS device. The energy per cycle is then $2[(1/2)\ CV_{CC}^2] = CV_{CC}^2$. Energy per unit time, or power, is then $CV_{CC}^2\ f$, where C is the load capacitance and f is the frequency.

The third, transient power due to internal capacitance takes exactly the same form as the load capacitance. Every device has some internal nodal capacitance which must be charged and discharged. This then represents another power term which must be considered.

The fourth, transient power due to switching current, is caused by the fact that whenever a CMOS device goes through a transition, with $V_{CC} \geq 2\ V_T$, there is a time when both N-channel and P-channel devices are both conducting. An expression for this current is derived in Application Note AN-77. The expression is:

$$P_{VI} = \frac{1}{2}(V_{CC} - 2\ V_T)\ I_{CC(MAX)}\ (t_{RISE} + t_{FALL})\ f$$

where:

V_T = threshold voltage

$I_{CC(MAX)}$ = peak non-capacitive current during switching

f = frequency

Note that this expression, like the capacitive power term is directly proportional to frequency. If the P_{VI} term is combined with the term arising from the internal capacitance, a capacitance C_{PD} may be defined which closely approximates the no load power consumption for a CMOS device when used in the following expression:

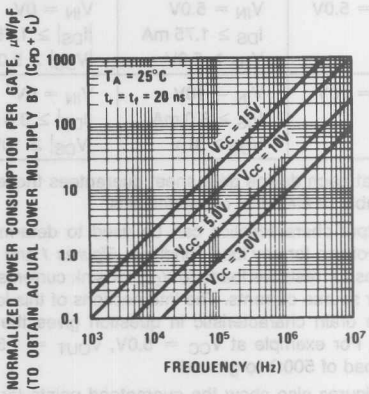
Power (no load) = $C_{PD}\ V_{CC}^2\ f$

The total power consumption is then simplified to:

$$\text{Total Power} = (C_{PD} + C_L)\ V_{CC}^2\ f + I_{LEAK}\ V_{CC} \qquad (1)$$

The procedure for obtaining C_{PD} is to measure the no load power at V_{CC} = 10V vs frequency and calculate the value of C_{PD} which corresponds to the measured power consumption. This value of C_{PD} is given on each 54C/74C data sheet and with equation (1) the computation of power consumption is straightforward.

To simplify the task even further *Figure 6* gives a graph of normalized power vs frequency for different power supply voltages. To obtain actual power consumption find the normalized power for a particular V_{CC} and frequency, then multiply by $C_{PD} + C_L$.



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FIGURE 6. Normalized Typical Power Consumption vs Frequency

As an example let's find the total power consumption for an MM74C00 operating at f = 100 kHz, V_{CC} = 10V and C_L = 50 pF. From the curve, normalized power per gate equals 10 μW/pF. From the data sheet C_{PD} = 12 pF; therefore, actual power per gate is:

$$\frac{\text{power}}{\text{gate}} = \frac{10\ \mu W}{pF} \times (12\ pF + 50\ pF) = \frac{0.62\ mW}{\text{gate}}$$

$$\text{total power} = \frac{\text{no. of gates}}{\text{package}} \times \frac{\text{power}}{\text{gate}} + I_{LEAKAGE} \times V_{CC}$$

$$= 4 \times 0.62\ mW + 0.01\ \mu A \times 10V \cong 2.48\ mW$$

Up to this point the discussion of power consumption has been limited to simple gate functions. Power consumption for an MSI function is more complex but the same technique just derived applies. To demonstrate the technique let's compute the total power consumption of a MM74C161, four bit binary counter, at V_{CC} = 10V, f = 1 MHz and C_L = 50 pF on each output.

The no load power is still given by P (no load) = $C_{PD}\ V_{CC}^2\ f$. This demonstrates the usefulness of the concept of the internal capacitance, C_{PD}. Even though the circuit is very complex and has many nodes charging and discharging at various rates, all of the effects can be easily lumped into one easy to use term, C_{PD}.

Calculation of transient power due to load capacitance is a little more complex since each output is switched at one half the rate of the previous output: Taking this into account the complete expression for power consumption is:

$$P_{TOTAL} = \underbrace{C_{PD}\, V_{CC}^2\, f}_{\text{no load power}} + \underbrace{C_L\, V_{CC}^2\, \frac{f}{2}}_{\text{output power of 1st stage}} + \underbrace{C_L\, V_{CC}^2\, \frac{f}{4}}_{\text{2nd stage}}$$

$$+ \underbrace{C_L\, V_{CC}^2\, \frac{f}{8}}_{\text{3rd stage}} + \underbrace{2\, C_L\, V_{CC}^2\, \frac{f}{16}}_{\text{4th stage \& carry output}} + \underbrace{I_L\, V_{CC}}_{\text{leakage term}}$$

This reduces to:

$$P_{TOTAL} = (C_{PD} + C_L)\, V_{CC}^2\, f + I_L\, V_{CC}$$

From the data sheet C_{PD} = 90 pF and I_L = 0.05 μA. Using *Figure 6* total power is then:

$$P_{TOTAL} = (90\ pF + 50\ pF) \times \frac{100\ \mu W}{pF} +$$

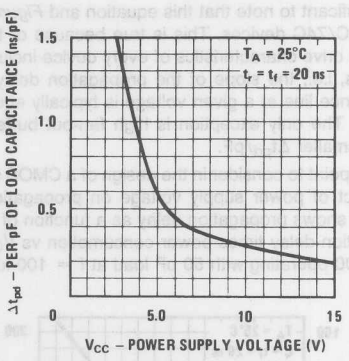
$$0.05 \times 10^{-6} \times 10V \cong 14\ mW$$

This demonstrates that with more complex devices the concept of C_{PD} greatly simplifies the calculation of total power consumption. It becomes an easy task to compute power for different voltages and frequencies by use of *Figure 6* and the equations above.

PROPAGATION DELAY

Propagation delay for all 54C/74C devices is guaranteed with a load of 50 pF *and input rise and fall times of 20 ns.* A 50 pF load was chosen, instead of 15 pF as in the 4000 series, because it is representative of loads commonly seen in CMOS systems. A good rule of thumb, in designing with CMOS, is to assume 10 pF of interwiring capacitance. Operating at the specified propagation delay would allow 5 pF fanout for the 4000 series while 54C/74C has a fanout of 40 pF. A fanout of 5 pF (one gate input) is all but useless, and specified propagation delay would most probably not be realized in an actual system.

Operating at loads other than 50 pF poses a problem since propagation is a function of load capacitance. To simplify the problem *Figure 7* has been generated and gives the slope of the propagation delay vs load capacitance line (Δt_{pd}/pF) as a function of power supply voltage. Because



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FIGURE 7. Typical Propagation Delay per pF of Load Capacitance vs Power Supply

the propagation delay for zero load capacitance is not zero and depends on the internal structure of each device, an offset term must be added that is unique to a particular device type. Since each data sheet gives propagation delay for 50 pF the actual delay for different loads can be computed with the aid of the following equation:

$$t_{pd}\Big|_{C_L = C} = (C - 50)\ pF \times \frac{\Delta t_{pd}}{pF} + t_{pd}\Big|_{C_L = 50\ pF}$$

where:

C = Actual load capacitance

$t_{pd}\Big|_{C_L = 50\ pF}$ = propagation delay with 50 pF load, (specified on each device data sheet)

$\frac{\Delta t_{pd}}{pF}$ = Value obtained from *Figure 7*.

As an example let's compute the propagation delay for an MM74C00 driving 15 pF load and operating with a V_{CC} = 5.0V. The equation gives:

$$t_{pd}\Big|_{C_L = 15\ pF} = (15 - 50)\ pF \times 0.57\frac{ns}{pF} + 50\ ns$$

$$= -20\ ns + 50\ ns = 30\ ns$$

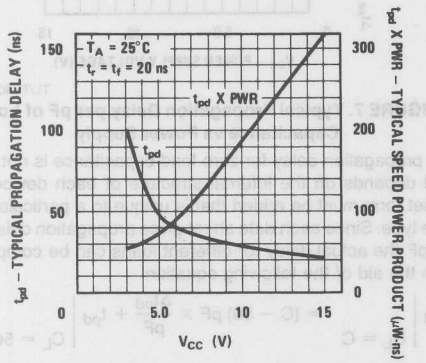
The same formula and curves may be applied to more complex devices. For example the propagation delay from data to output for an MM74C157 operating at V_{CC} = 10V and C_L = 100 pF is:

$$t_{pd}\Big|_{C_L = 100\ pF} = (100 - 50)\ 0.29\ ns + 70\ ns$$

$$= 14.5 + 70 \cong 85\ ns$$

It is significant to note that this equation and *Figure 7* apply to *all* 54C/74C devices. This is true because of the close match in drive characteristics of every device including MSI functions, i.e., the slope of the propagation delay vs load capacitance line at a given voltage is typically equal for all devices. The only exception is high fan-out buffers which have a smaller $\Delta t_{pd}/pF$.

Another point to consider in the design of a CMOS system is the effect of power supply voltage on propagation delay. *Figure 8* shows propagation delay as a function of V_{CC} and propagation delay times power consumption vs V_{CC} for an MM74C00 operating with 50 pF load at f = 100 kHz.



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FIGURE 8. Speed Power Product and Propagation Delay vs V_{CC}

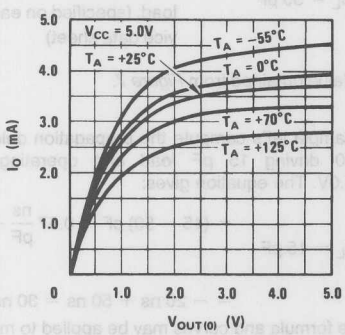
Above V_{CC} = 5.0V note the speed power product curve approaches a straight line. However the t_{pd} curve starts to "flatten out". Going from *V_{CC} = 5.0V to V_{CC} = 10V gives a 40% decrease in propagation delay and going from V_{CC} = 10V to V_{CC} = 15V only decreases propagation delay by 25%.* Clearly for V_{CC} > 10V a small increase in speed is gained by a disproportionate increase in power. Conversely, for small decreases in power below V_{CC} = 5.0V large increases in propagation delay result.

Obviously it is optimum to use the lowest voltage consistent with system speed requirements. However, in general it can be seen from *Figure 8* that the best speed power performance will be obtained in the V_{CC} = 5.0V to V_{CC} = 10V range.

TEMPERATURE CHARACTERISTICS

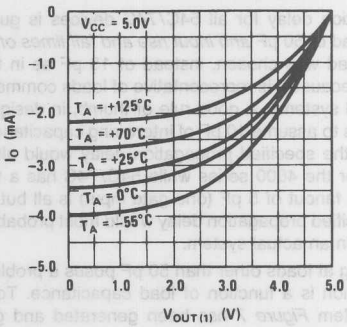
Figures 9 and *10* give temperature variations in drain characteristics for the N-channel and P-channel devices operating at V_{CC} = 5.0V and V_{CC} = 10V respectively. As can be seen from these curves the output sink and source current decreases as temperature increases. The effect is almost linear and can be closely approximated by a temperature coefficient of −0.3% per degree centigrade.

Since the t_{pd} can be entirely attributed to rise and fall time, the temperature dependence of t_{PD} is a function of the rate at which the output load capacitance can be charged and discharged. This in turn is a function of the sink/source current which was shown above to vary as −0.3% per degree centigrade. Consequently we can say that t_{pd} varies as −0.3% per degree centigrade. Actual measurements of t_{pd} with temperature verifies this number.



TL/F/6021–12

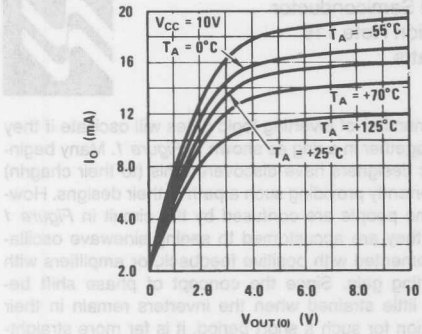
(A) Typical Output Drain Characteristic (N-Channel)



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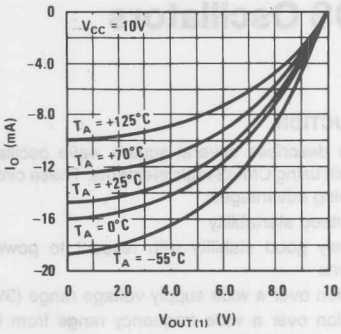
(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 9



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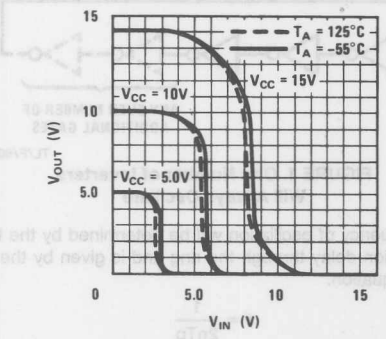
(A) Typical Output Drain Characteristic (N-Channel)



TL/F/6021–15

(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 10



TL/F/6021–16

FIGURE 11. Typical Gate Transfer Characteristics

The drain characteristics of *Figures 9* and *10* show considerable variation with temperature. Examination of the transfer characteristics of *Figure 11* indicates that they are almost independent of temperature. The transfer characteristic is not dependent on temperature because although both the N-channel and P-channel device characteristics change with temperature these changes track each other closely. The proof of this tracking is the temperature independence of the transfer characteristics. Noise margin and maximum/minimum logic levels will then not be dependent on temperature.

As discussed previously power consumption is a function of C_{PD}, C_L, V_{CC}, f and $I_{LEAKAGE}$. All of these terms are essentially constant with temperature except $I_{LEAKAGE}$. However, the leakage current specified on each 54C/74C device applies across the entire temperature range and therefore represents a worst case limit.

CMOS Oscillators

National Semiconductor
Application Note 118
Mike Watts

INTRODUCTION

This note describes several square wave oscillators that can be built using CMOS logic elements. These circuits offer the following advantages:

- Guaranteed startability
- Relatively good stability with respect to power supply variations
- Operation over a wide supply voltage range (3V to 15V)
- Operation over a wide frequency range from less than 1 Hz to about 15 MHz
- Low power consumption (see AN-90)
- Easy interface to other logic families and elements including TTL

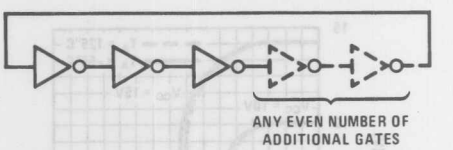
Several RC oscillators and two crystal controlled oscillators are described. The stability of the RC oscillator will be sufficient for the bulk of applications; however, some applications will probably require the stability of a crystal. Some applications that require a lot of stability are:

1. Timekeeping over a long interval. A good deal of stability is required to duplicate the performance of an ordinary wrist watch (about 12 ppm). This is, of course, obtainable with a crystal. However, if the time interval is short and/or the resolution of the timekeeping device is relatively large, an RC oscillator may be adequate. For example: if a stopwatch is built with a resolution of tenths of seconds and the longest interval of interest is two minutes, then an accuracy of 1 part in 1200 (2 minutes × 60 seconds/minute × 10 tenth/second) may be acceptable since any error is less than the resolution of the device.
2. When logic elements are operated near their specified limits. It may be necessary to maintain clock frequency accuracy within very tight limits in order to avoid exceeding the limits of the logic family being used, or in which the timing relationships of clock signals in dynamic MOS memory or shift register systems must be preserved.
3. Baud rate generators for communications equipment.
4. Any system that must interface with other tightly specified systems. Particularly those that use a "handshake" technique in which Request or Acknowledge pulses must be of specific widths.

LOGICAL OSCILLATORS

Before describing any specific circuits, a few words about logical oscillators may clear up some recurring confusion.

Any odd number of inverting logic gates will oscillate if they are tied together in a ring as shown in *Figure 1*. Many beginning logic designers have discovered this (to their chagrin) by inadvertently providing such a path in their designs. However, some people are confused by the circuit in *Figure 1* because they are accustomed to seeing sinewave oscillators implemented with positive feedback, or amplifiers with non-inverting gain. Since the concept of phase shift becomes a little strained when the inverters remain in their linear region for such a short period, it is far more straightforward to analyze the circuit from the standpoint of ideal switches with finite propagation delays rather than as amplifiers with 180° phase shift. It then becomes obvious that a "1" chases itself around the ring and the network oscillates.



TL/F/6022–1

FIGURE 1. Odd Number of Inverters Will Always Oscillate

The frequency of oscillation will be determined by the total propagation delay through the ring and is given by the following equation.

$$f = \frac{1}{2nTp}$$

Where:

f = frequency of oscillation
Tp = Propagation delay per gate
n = number of gates

This is not a practical oscillator, of course, but it does illustrate the maximum frequency at which such an oscillator will run. All that must be done to make this a useful oscillator is to slow it down to the desired frequency. Methods of doing this are described later.

To determine the frequency of oscillation, it is necessary to examine the propagation delay of the inverters. CMOS propagation delay depends on supply voltage and load capacitance. Several curves for propagation delay for National's

74C line of CMOS gates are reproduced in *Figure 2*. From these, the natural frequency of oscillation of an odd number of gates can be determined.

An example may be instructive.

Assume the supply voltage is 10V. Since only one input is driven by each inverter, the load capacitance on each inverter is at most about 8 pF. Examine the curve in *Figure 2c* that is drawn for $V_{CC} = 10V$ and extrapolate it down to 8 pF. We see that the curve predicts a propagation delay of about 17 ns. We can then calculate the frequency of oscillation for three inverters using the expression mentioned above. Thus:

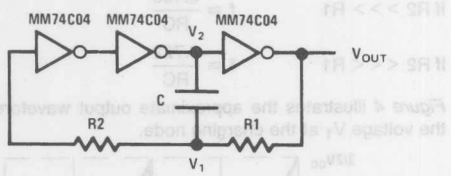
$$f = \frac{1}{2 \times 3 \times 17 \times 10^{-9}} = 9.8\ \text{MHz}$$

Lab work indicates this is low and that something closer to 16 MHz can be expected. This reflects the conservative nature of the curves in *Figure 2*.

Since this frequency is directly controlled by propagation delays, it will vary a great deal with temperature, supply voltage, and any external loading, as indicated by the graphs in *Figure 2*. In order to build a usefully stable oscillator it is necessary to add passive elements that determine oscillation frequency and minimize the effect of CMOS characteristics.

STABLE RC OSCILLATOR

Figure 3 illustrates a useful oscillator made with three inverters. Actually, any inverting CMOS gate or combination of gates could be used. This means left over portions of gate packages can be often used. The duty cycle will be close to 50% and will oscillate at a frequency that is given by the following expression.



TL/F/6022–2

FIGURE 3. Three Gate Oscillator

$$f \cong \frac{1}{2\,R1\,C\left(\frac{0.405\,R2}{R1 + R2} + 0.693\right)}$$

Another form if this expression is:

$$f \cong \frac{1}{2C\,(0.405\,R_{eq} + 0.693\,R1)}$$

Where:

$$R_{eq} = \frac{R1\,R2}{R1 + R2}$$

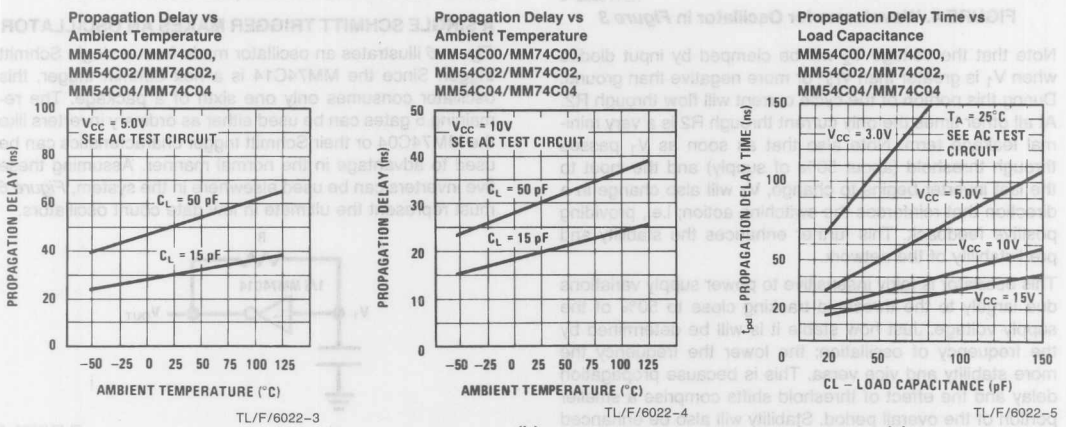


FIGURE 2. Propagation Delay for 74C Gates

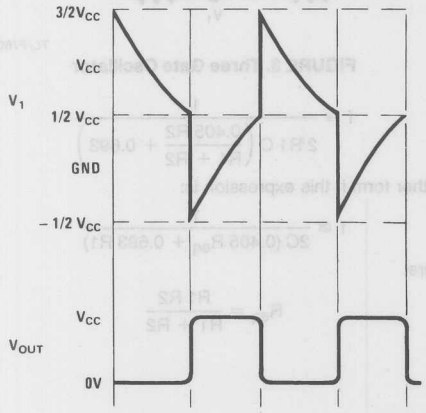
The following three special cases may be useful.

If R1 = R2 = R $\quad f \cong \dfrac{0.559}{RC}$

If R2 >>> R1 $\quad f \cong \dfrac{0.455}{RC}$

If R2 <<< R1 $\quad f \cong \dfrac{0.722}{RC}$

Figure 4 illustrates the approximate output waveform and the voltage V_1 at the charging node.



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FIGURE 4. Waveforms for Oscillator in *Figure 3*

Note that the voltage V_2 will be clamped by input diodes when V_1 is greater than V_{CC} or more negative than ground. During this portion of the cycle current will flow through R2. At all other times the only current through R2 is a very minimal leakage term. Note also that as soon as V_1 passes through threshold (about 50% of supply) and the input to the last inverter begins to change, V_1 will also change in a direction that reinforces the switching action; i.e., providing positive feedback. This further enhances the stability and predictability of the network.

This oscillator is fairly insensitive to power supply variations due largely to the threshold tracking close to 50% of the supply voltage. Just how stable it is will be determined by the frequency of oscillation; the lower the frequency the more stability and vice versa. This is because propagation delay and the effect of threshold shifts comprise a smaller portion of the overall period. Stability will also be enhanced if R1 is made large enough to swamp any variations in the CMOS output resistance.

TWO GATE OSCILLATOR WILL NOT NECESSARILY OSCILLATE

A popular oscillator is shown in *Figure 5a*. The only undesirable feature of this oscillator is that it may not oscillate. This is readily demonstrated by letting the value of C go to zero. The network then degenerates into *Figure 5b*, which obviously will not oscillate. This illustrates that there is some value of C1 that will not force the network to oscillate. The real difference between this two gate oscillator and the three gate oscillator is that the former must be forced to oscillate by the capacitor while the three gate network will always oscillate willingly and is simply slowed down by the capacitor. The three gate network will always oscillate, regardless of the value of C1 but the two gate oscillator will not oscillate when C1 is small.

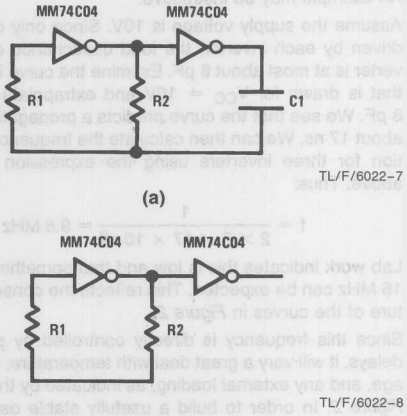


FIGURE 5. Less Than Perfect Oscillator

The only advantage the two gate oscillator has over the three gate oscillator is that it uses one less inverter. This may or may not be a real concern, depending on the gate count in each user's specific application. However, the next section offers a real minimum parts count oscillator.

A SINGLE SCHMITT TRIGGER MAKES AN OSCILLATOR

Figure 6 illustrates an oscillator made from a single Schmitt trigger. Since the MM74C14 is a hex Schmitt trigger, this oscillator consumes only one sixth of a package. The remaining 5 gates can be used either as ordinary inverters like the MM74C04 or their Schmitt trigger characteristics can be used to advantage in the normal manner. Assuming these five inverters can be used elsewhere in the system, *Figure 6* must represent the ultimate in low gate count oscillators.

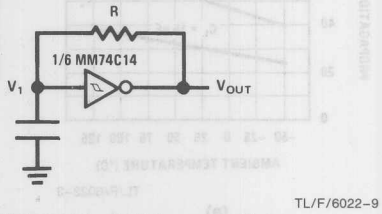
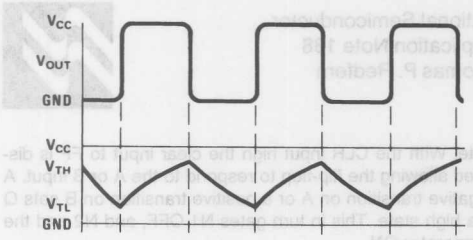


FIGURE 6. Schmitt Trigger Oscillator

Voltage V_1 is depicted in *Figure 7* and changes between the two thresholds of the Schmitt trigger. If these thresholds were constant percentages of V_{CC} over the supply voltage range, the oscillator would be insensitive to variations in V_{CC}. However, this is not the case. The thresholds of the Schmitt trigger vary enough to make the oscillator exhibit a good deal of sensitivity to V_{CC}.

Applications that do not require extreme stability or that have access to well regulated supplies should not be bothered by this sensitivity to V_{CC}. Variations in threshold can be expected to run as high as four or five percent when V_{CC} varies from 5V to 15V.



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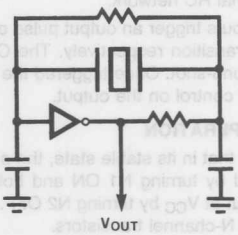
FIGURE 7. Waveforms for Schmitt Trigger Oscillator in *Figure 6*

A CMOS CRYSTAL OSCILLATOR

Figure 8 illustrates a crystal oscillator that uses only one CMOS inverter as the active element. Any odd number of inverters may be used, but the total propagation delay through the ring limits the highest frequency that can be obtained. Obviously, the fewer inverters that are used, the higher the maximum possible frequency.

CONCLUSIONS

A large number of oscillator applications can be implemented with the extremely simple, reliable, inexpensive and versatile CMOS oscillators described in this note. These oscillators consume very little power compared to most other approaches. Each of the oscillators requires less than one full package of CMOS inverters of the MM74C04 variety. Frequently such an oscillator can be built using leftover gates of the MM74C00, MM74C02, MM74C10 variety. Stability superior to that easily attainable with TTL oscillators is readily attained, particularly at lower frequencies. These oscillators are so versatile, easy to build, and inexpensive that they should find their way into many diverse designs.



TL/F/6022–11

FIGURE 8. Crystal Oscillator

Using the CMOS Dual Monostable Multivibrator

National Semiconductor
Application Note 138
Thomas P. Redfern

INTRODUCTION

The MM54C221/MM74C221 is a dual CMOS monostable multivibrator. Each one-shot has three inputs (A, B and CLR) and two outputs (Q and $\overline{Q}$). The output pulse width is set by an external RC network.

The A and B inputs trigger an output pulse on a negative or positive input transition respectively. The CLR input when low resets the one-shot. Once triggered the A and B inputs have no further control on the output.

THEORY OF OPERATION

Figure 1 shows that in its stable state, the one-shot clamps C_{EXT} to ground by turning N1 ON and holds the positive comparator input at V_{CC} by turning N2 OFF. The prefix N is used to denote N-channel transistors.

The signal, G, gating N2 OFF also gates the comparator OFF thereby keeping the internal power dissipation to an absolute minimum. The only power dissipation when in the stable state is that generated by the current through R_{EXT}. The bulk of this dissipation is in R_{EXT} since the voltage drop across N1 is very small for normal ranges of R_{EXT}.

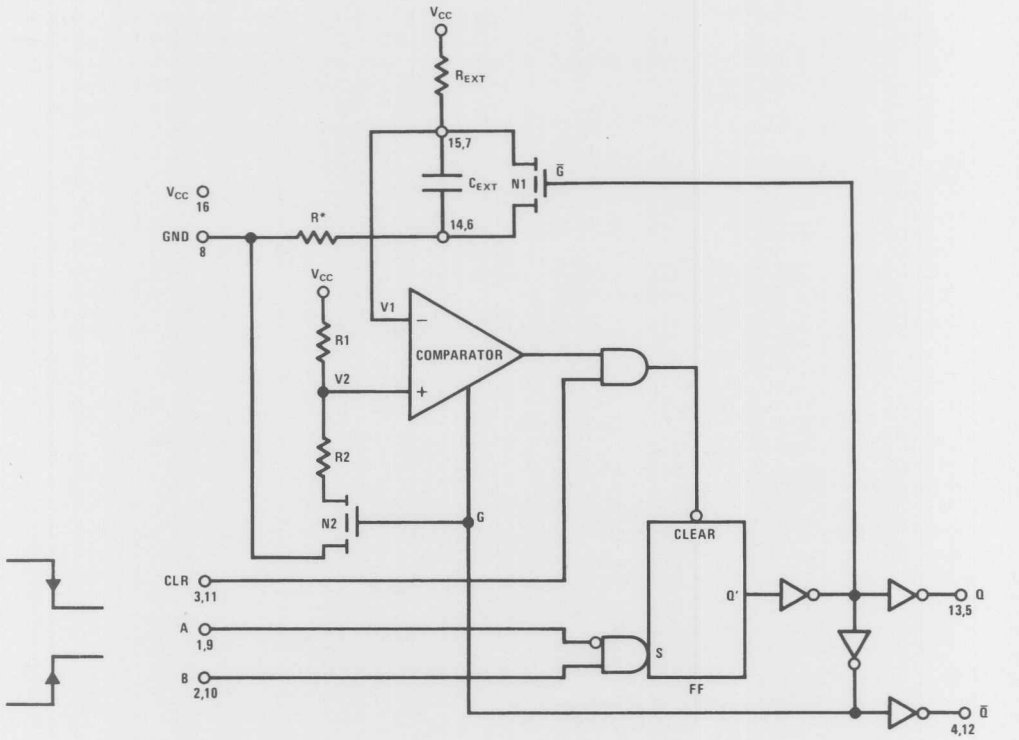
To trigger the one-shot the CLR input must be high.

The gating, G, on the comparator is designed such that the comparator output is high when the one-shot is in its stable state. With the CLR input high the clear input to FF is disabled allowing the flip-flop to respond to the A or B input. A negative transition on A or a positive transition on B sets Q to a high state. This in turn gates N1 OFF, and N2 and the comparator ON.

Gating N2 ON establishes a reference of 0.63 V_{CC} on the comparator's positive input. Since the voltage on C_{EXT} can not change instantaneously V1 = 0V at this time. The comparator then will maintain its one level on the output. Gating N1 OFF allows C_{EXT} to start charging through R_{EXT} toward V_{CC} exponentially.

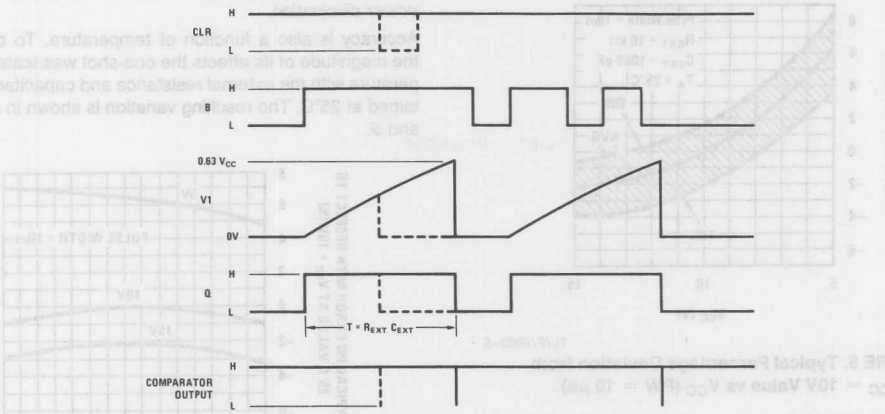
Assuming a perfect comparator (zero offset and infinite gain) when the voltage on C_{EXT}, V1, equals 0.63 V_{CC} the comparator output will go from a high state to a low state resetting Q to a low state. *Figure 2* is a timing diagram summarizing this sequence of events.

This diagram is idealized by assuming zero rise and fall times and zero propagation delay but it shows the basic operation of the one-shot. Also shown is the effect of taking the CLR input low. Whenever CLR goes low FF is reset independent of all other inputs. *Figure 2* also shows that once triggered, the output is independent of any transitions on B (or A) until the cycle is complete.



TL/F/6023–1

FIGURE 1. Monostable Multivibrator Logic Diagram



TL/F/6023–2

FIGURE 2. One-Shot Timing Diagram

The output pulse width is determined by the following equation:

$$V1 = V_{CC}(1 - e^{-T/R_{EXT}C_{EXT}}) = 0.63\,V_{CC} \qquad (1)$$

Solving for t gives:

$$T = R_{EXT}\,C_{EXT}\,\ln(1/0.37) = R_{EXT}\,C_{EXT} \qquad (2)$$

A word of caution should be given in regards to the ground connection of the external capacitor (C_{EXT}). It should always be connected as shown in *Figure 1* to pin 14 or 6 and never to pin 8. This is important because of the parasitic resistor R*. Because of the large discharge current through R*, if the capacitor is connected to pin 8, a four layer diode action can result causing the circuit to latch and possible damage itself.

ACCURACY

There are many factors which influence the accuracy of the one-shot. The most important are:

a. Comparator input offset

b. Comparator gain

c. Comparator time delay

d. Voltage divider R1, R2

e. Delays in logic elements

f. ON impedance of N1 and N2

g. Leakage of N1

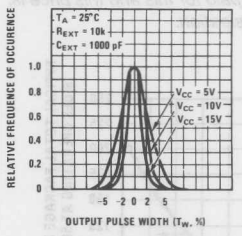
h. Leakage of C_{EXT}

i. Magnitude of R_{EXT} and C_{EXT}

The characteristics of C_{EXT} and R_{EXT} are, of course, not determined by the characteristics of the one-shot. In order to establish the accuracy of the one-shot, devices were tested using an external resistance of 10 kΩ and various capacitors. A resistance of 10 kΩ was chosen because the leakage and ON impedance of transistor N1 have a minimal effect on accuracy with this value of resistance.

Two values of C_{EXT} were chosen, 1000 pF and 0.1 μF. These values give pulse widths of 10 μs and 1000 μs with R_{EXT} = 10 kΩ.

Figures 3 and *4* show the resulting distributions of pulse widths at 25°C for various power supply voltages. Because propagation delays, at the same power supply voltage, are the same independent of pulse width, the shorter the pulse width the more the accuracy is affected by propagation delay. *Figures 3* and *4* clearly show this effect. As pointed out in Application Note AN-90, 54C/74C Family Characteristics, propagation delay is a function of V_{CC}. *Figure 3*, (Pulse Width = 10 μs) shows much greater variation with V_{CC} than *Figure 4* (Pulse Width = 1000 μs). This same information is shown in *Figures 5* and *6* in a different format. In these figures the percent deviation from the average pulse width at 10V V_{CC} is shown vs V_{CC}. In addition to the average value the 10% and 90% points are shown. These percentage points refer to the statistical distribution of pulse width error. As an example, at V_{CC} = 10V for 10 μs pulse width, 90% of the devices have errors of less than +1.7% and 10% have errors less than −2.1%. In other words, 80% have errors between +1.7% and −2.1%.



0% point pulse width:

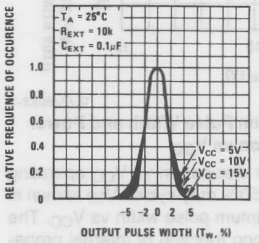
At V_{CC} = 5V, T_W = 10.6 μs
At V_{CC} = 10V, T_W = 10 μs
At V_{CC} = 15V, T_W = 9.8 μs

Percentage of units within 4%:

At V_{CC} = 5V, 90% of units
At V_{CC} = 10V, 95% of units
At V_{CC} = 15V, 98% of units

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FIGURE 3. Typical Pulse Width Distribution for 10 μs Pulse



0% pulse width:

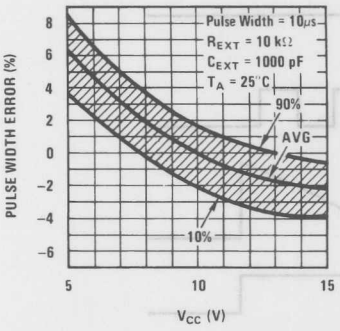
At V_{CC} = 5V, T_W = 1020 μs
At V_{CC} = 10V, T_W = 1000 μs
At V_{CC} = 15V, T_W = 982 μs

Percentage of units within 4%:

At V_{CC} = 5V, 95% of units
At V_{CC} = 10V, 97% of units
At V_{CC} = 15V, 98% of units

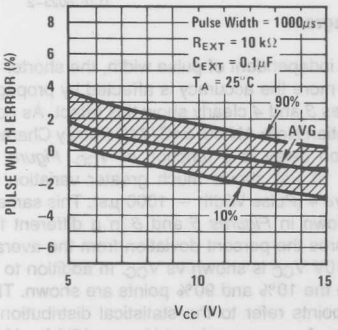
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FIGURE 4. Typical Pulse Width Distribution for 1000 μs Pulse



TL/F/6023–5

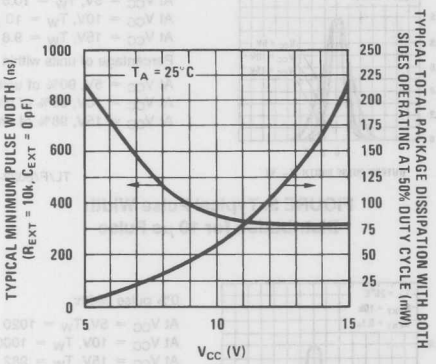
FIGURE 5. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 10 μs)



TL/F/6023–6

FIGURE 6. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 1000 μs)

The minimum error can be obtained by operating at the maximum V_{CC}. A price must be paid for this and this price is, of course, increased power dissipation.

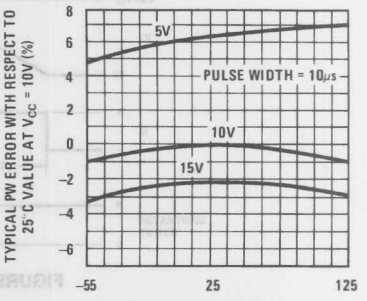


TL/F/6023–7

FIGURE 7. Typical Minimum Pulse Width and Power Dissipation vs V_{CC}

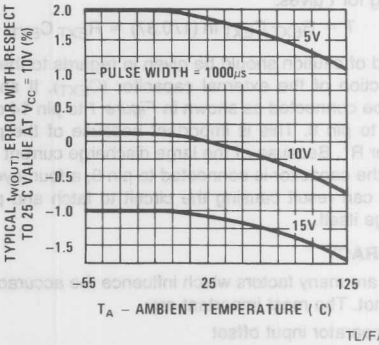
Figure 7 shows typical power dissipation vs V_{CC} operating both sides of the one-shot at 50% duty cycle. Also shown in the same figure is typical minimum pulse width vs V_{CC}. The minimum pulse width is a strong function of internal propagation delays. *It is obvious from these two curves that in creasing V_{CC} beyond 10V will not appreciably improve inaccuracy due to propagation delay but will greatly increase power dissipation.*

Accuracy is also a function of temperature. To determine the magnitude of its effects the one-shot was tested at temperature with the external resistance and capacitance maintained at 25°C. The resulting variation is shown in *Figures 8* and *9*.



TL/F/6023–8

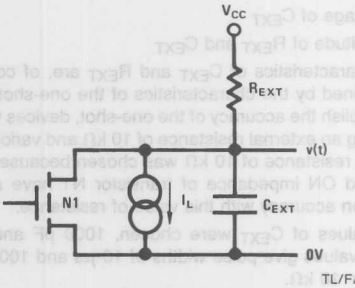
FIGURE 8. Typical Pulse Width Error vs Temperature (PW = 10 μs)



TL/F/6023–9

FIGURE 9. Typical Pulse Width Error vs Temperature (PW = 1000 μs)

Up to this point the external timing resistor, R_{EXT}, has been held fixed at 10 kΩ. In actual applications other values may be necessary to achieve the desired pulse width. The question then arises as to what effect this will have on accuracy.



TL/F/6023–10

FIGURE 10

As R_{EXT} becomes larger and larger the leakage current on transistor N1 becomes an ever increasing problem. The equivalent circuit for this leakage is shown in *Figure 10*.

v(t) is given by:

$$v(t) = (V_{CC} - I_L R_{EXT})\,(1 - e^{-t_L/R_{EXT}\,C_{EXT}})$$

As before, when $v(t) = 0.63\,V_{CC}$, the output will reset. Solving for t_L gives:

$$t_L = R_{EXT}\,C_{EXT}\,\ell n\left(\frac{V_{CC} - I_L R_{EXT}}{0.37\,V_{CC} - I_L R_{EXT}}\right) \qquad (3)$$

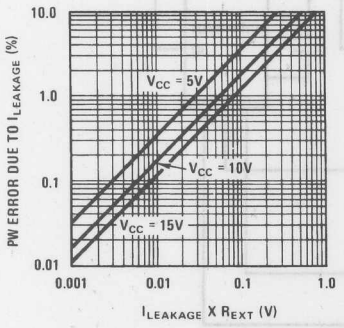
Using T as defined in Equation 2 the pulse width error is:

$$\text{PW Error} = \frac{t_L - T}{T} \times 100\%$$

Substituting Equations 2 and 3 gives:

$$\text{PW Error} = \frac{R_{EXT}\,C_{EXT}\,\ell n\left(\frac{V_{CC} - I_L R_{EXT}}{0.37\,V_{CC} - I_L R_{EXT}}\right) - R_{EXT}\,C_{EXT}\,\ell n(1/0.37)}{R_{EXT}\,C_{EXT}\,\ell n\,(1/0.37)}$$

PW Error is plotted in *Figure 11* for $V_{CC} = 5$, 10 and 15V. As expected, decreasing V_{CC} causes PW Error to increase with fixed I_L. Note that the leakage current, although here assumed to flow through N1, is general and could also be interpreted as leakage through C_{EXT}. See MM54C221/MM74C221 data sheet for leakage limits.



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FIGURE 11. Percentage Pulse Width Error Due to Leakage

To demonstrate the usefulness of *Figure 11* an example will be most helpful. Let us assume that N1 has a leakage of 250×10^{-9}A, C_{EXT} has leakage of 150×10^{-9}A, output pulse width = 0.1 sec and $V_{CC} = 5$V. What $R_{EXT}\,C_{EXT}$ should be used to guarantee an error due to leakage of less than 5%.

From *Figure 11* we see that to meet these conditions R_{EXT} $I_L < 0.14$V.

Then:

$$R_{EXT} < 0.14/(250 + 150) \times 10^{-9}$$
$$< 350\ \text{k}\Omega$$

Choosing standard component values of 250 kΩ and 0.004 μF would satisfy the above conditions.

We have just defined the limitation on the maximum size of R_{EXT}. There is a corresponding limit on the minimum size that R_{EXT} can assume. This is brought about because of the finite ON impedance of N1. As R_{EXT} is made smaller and smaller the amount of voltage across N1 becomes significant. The voltage across N1 is:

$$V_{N1} = V_{CC}\,r_{ON}/(R_{EXT} + r_{ON}) \qquad (4)$$

The output pulse width is defined by:

$$v(t_O) = (V_{CC} - V_{N1})\,(1 - {}^{-t_O}/_{R_{EXT}\,C_{EXT}}) + V_{N1} = 0.63\,V_{CC}$$

Solving for t_O gives:

$$t_O = R_{EXT}\,C_{EXT}\,\ell n\left(\frac{V_{CC} - V_{N1}}{0.37\,V_{CC}}\right)$$

Pulse Width Error is then:

$$\text{PW Error} = \frac{t_O - T}{T} \times 100\%$$

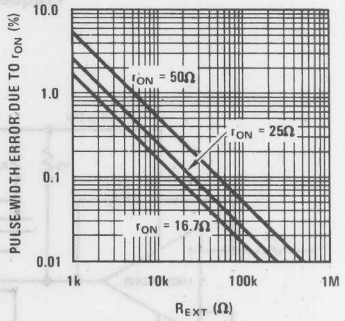
Substituting Equations 2 and 4 gives:

$$= \frac{R_{EXT}\,C_{EXT}\,\ell n\left(\frac{V_{CC} - V_{N1}}{0.37\,V_{CC}}\right) - R_{EXT}\,C_{EXT}\,\ell n\,(1/0.37)}{R_{EXT}\,C_{EXT}\,\ell n\,(1/0.37)}$$

This function is plotted in *Figure 12* for r_{ON} of 50Ω, 25Ω, and 16.7Ω. These are the typical values of r_{ON} for a V_{CC} of 5V, 10V and 15V respectively.

As an example, assume that the pulse width error due to r_{ON} must be less than 0.5% operating at $V_{CC} = 5$V. The typical value of r_{ON} for $V_{CC} = 5$V is 50Ω. Referring to the 50Ω curve in *Figure 12*, R_{EXT} must be greater than 10 kΩ to maintain this accuracy. At $V_{CC} = 10$V, R_{EXT} must be greater than 5 kΩ as can be seen from the 25Ω curve in *Figure 12*.

Although clearly shown in the MM54C221/MM74C221 data sheet, it is worthwhile, for the sake of clarity, to point out that the parasitic capacitance between pins 7(15) and 6(14) is typically 15 pF. This capacitor is in parallel with C_{EXT} and must be taken into account when accuracy is critical.

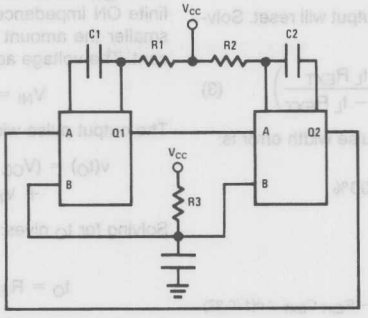


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FIGURE 12. Percentage Pulse Width Error Due to Finite r_{ON} of Transistor N1 vs R_{EXT}

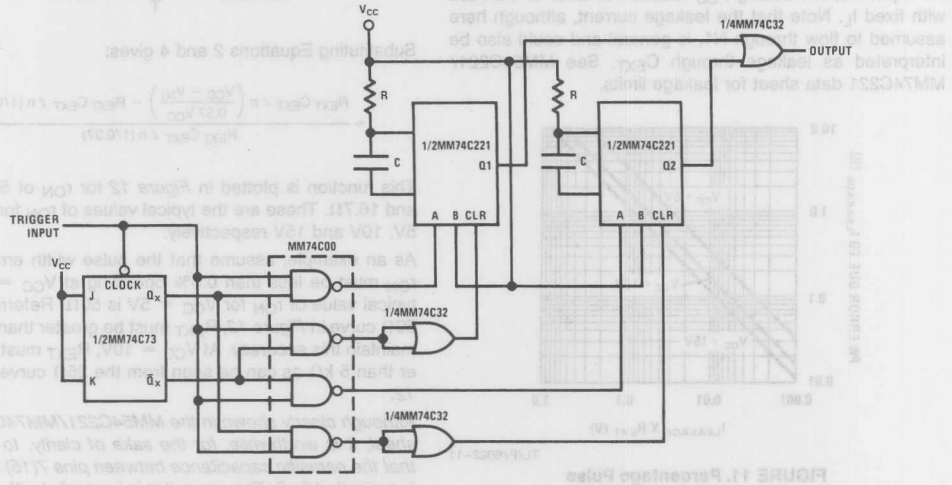
TYPICAL APPLICATIONS

Basic One-Shot Oscillator



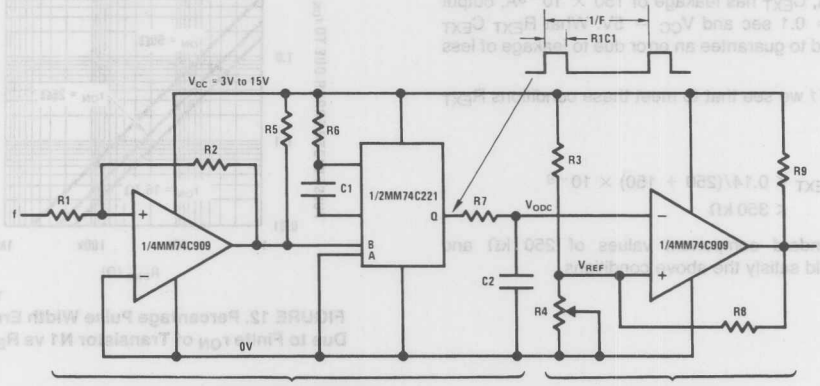
TL/F/6023–13

Retriggerable One-Shot



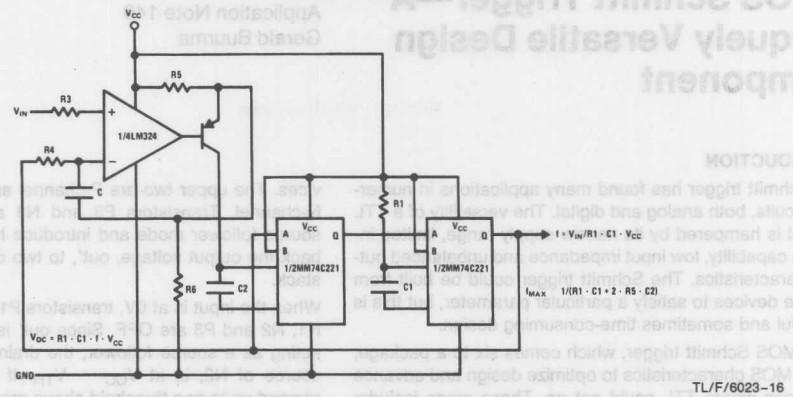
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Frequency Magnitude Comparator



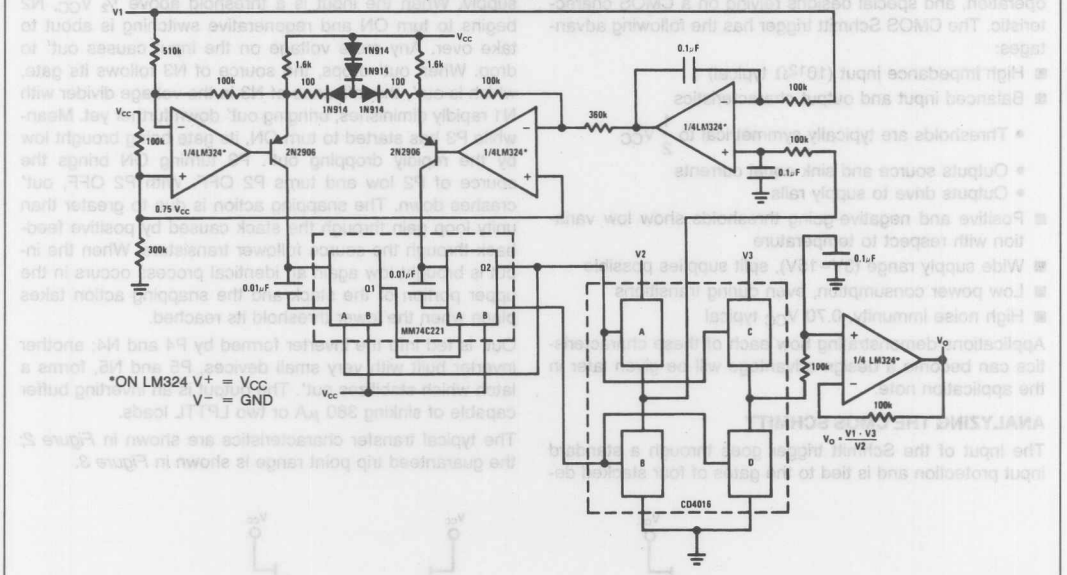
TL/F/6023–15

Linear VCO



TL/F/6023–16

Analog Multiplier/Divider



TL/F/6023–17

Uniquely Versatile Design Component

Gerald Buurma

INTRODUCTION

The Schmitt trigger has found many applications in numerous circuits, both analog and digital. The versatility of a TTL Schmitt is hampered by its narrow supply range, limited interface capability, low input impedance and unbalanced output characteristics. The Schmitt trigger could be built from discrete devices to satisfy a particular parameter, but this is a careful and sometimes time-consuming design.

The CMOS Schmitt trigger, which comes six to a package, uses CMOS characteristics to optimize design and advance into areas where TTL could not go. These areas include: interfacing with op amps and transmission lines, which operate from large split supplies, logic level conversion, linear operation, and special designs relying on a CMOS characteristic. The CMOS Schmitt trigger has the following advantages:

- High impedance input ($10^{12}\Omega$ typical)
- Balanced input and output characteristics
  - Thresholds are typically symmetrical to $\frac{1}{2}$ V_{CC}
  - Outputs source and sink equal currents
  - Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3V–15V), split supplies possible
- Low power consumption, even during transitions
- High noise immunity, 0.70 V_{CC} typical

Applications demonstrating how each of these characteristics can become a design advantage will be given later in the application note.

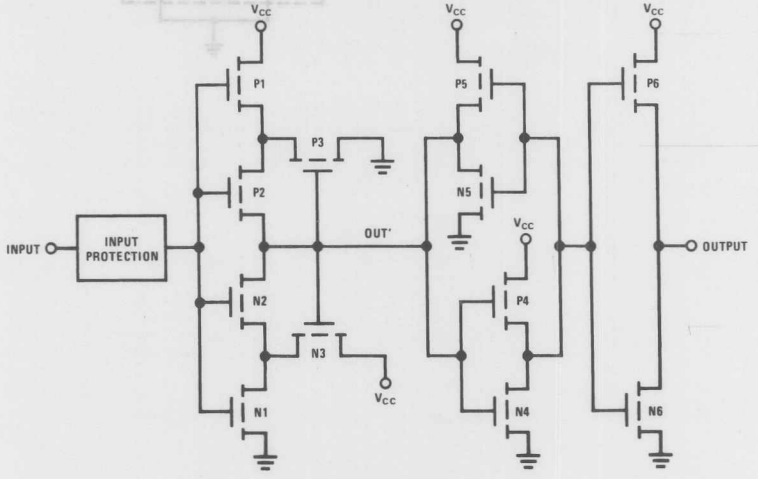
ANALYZING THE CMOS SCHMITT

The input of the Schmitt trigger goes through a standard input protection and is tied to the gates of four stacked devices. The upper two are P-channel and the lower two are N-channel. Transistors P3 and N3 are operating in the source follower mode and introduce hysteresis by feeding back the output voltage, out', to two different points in the stack.

When the input is at 0V, transistors P1 and P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON and acting as a source follower, the drain of N1, which is the source of N2, is at $V_{CC} - V_{TH}$. If the input voltage is ramped up to one threshold above ground transistor N1 begins to turn ON, N1 and N3 both being ON form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold above $\frac{1}{2}$ V_{CC}, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' drops, the source of N3 follows its gate, which is out', the influence of N3 in the voltage divider with N1 rapidly diminishes, bringing out' down further yet. Meanwhile P3 has started to turn ON, its gate being brought low by the rapidly dropping out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to greater than unity loop gain through the stack caused by positive feedback through the source follower transistors. When the input is brought low again an identical process occurs in the upper portion of the stack and the snapping action takes place when the lower threshold its reached.

Out' is fed into the inverter formed by P4 and N4; another inverter built with very small devices, P5 and N5, forms a latch which stabilizes out'. The output is an inverting buffer capable of sinking 360 μA or two LPTTL loads.

The typical transfer characteristics are shown in *Figure 2;* the guaranteed trip point range is shown in *Figure 3.*



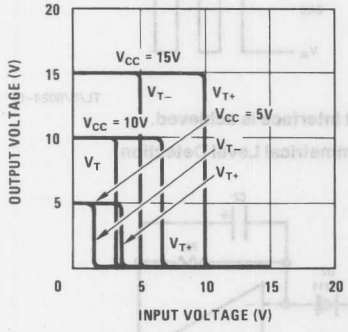
TL/F/6024–1

FIGURE 1. CMOS Schmitt Trigger

WHAT HYSTERESIS CAN DO FOR YOU

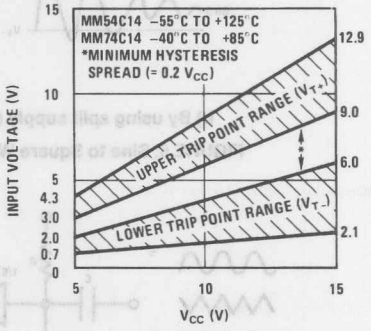
Hysteresis is the difference in response due to the direction of input change. A noisy signal that traverses the threshold of a comparator can cause multiple transitions at the output, if the response time of the comparator is less than the time between spurious effects. A Schmitt trigger has two thresholds: any spurious effects must be greater than the threshold difference to cause multiple transitions. With a CMOS Schmitt at $V_{CC} = 10V$ there is typically 3.6V of threshold difference, enough hysteresis to overcome almost any spurious signal on the input.

A comparator is often used to recover information sent down an unbalanced transmission line. The threshold of the comparator is placed at one half the signal amplitude (See *Figure 4b*). This is done to prevent slicing level distortion. If a 4 μs wide signal is sent down a transmission line a 4 μs wide signal should be received or signal distortion occurs. If the comparator has a threshold above half the signal amplitude, then positive pulses sent are shorter and negative pulses are lengthened (See *Figure 4c*). This is called slicing level distortion. The Schmitt trigger does have a positive offset, V_{T+}, but it also has a negative offset V_{T-}. In CMOS these offsets are approximately symmetrical to half the signal level so a 4 μs wide pulse sent is also recovered (see *Figure 4d*). The recovered pulse is delayed in time but the length is not changed, so noise immunity is achieved and signal distortion is not introduced because of threshold offsets.



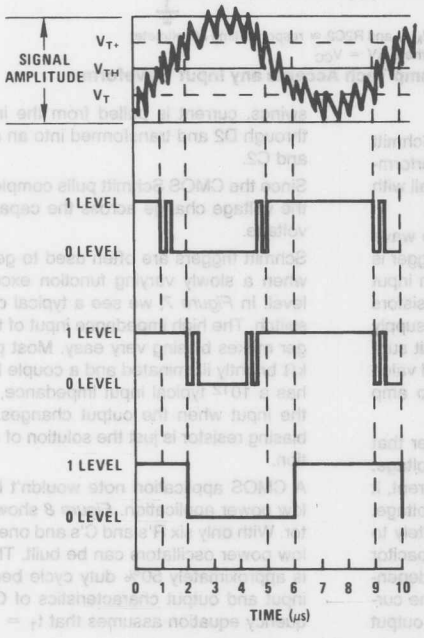
TL/F/6024–2

FIGURE 2. Typical CMOS Transfer Characteristics for Three Different Supply Voltages



TL/F/6024–3

FIGURE 3. Guaranteed Trip Point Range



a) Received signal from transmission line with thresholds at different amplitudes.

b) Recovered signal from comparator with threshold V_{TH} has multiple transitions.

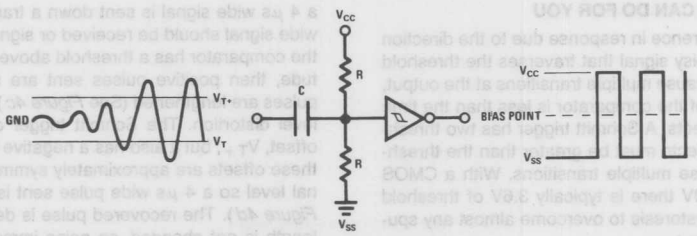
c) Recovered signal from comparator with positive offset on threshold, V_{T+}, positive pulse shorten, negative pulse lengthen.

d) Recovered signal with CMOS Schmitt trigger, V_{T+} and V_T. Restores true waveform.

Recovered signal from Schmitt is same width as comparator with threshold at V_{TH}, and is only delayed in time.

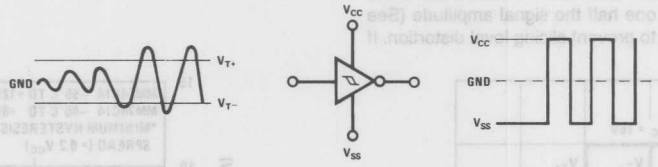
TL/F/6024–4

FIGURE 4. CMOS Schmitt Trigger Ignores Noise



TL/F/6024–5

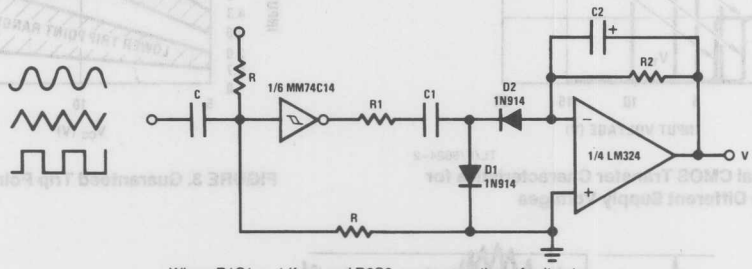
a) Capacitor impedance at lowest operating frequency should be much less than R ‖ R = ½R.



TL/F/6024–6

b) By using split supply (±1.5V to ±7.5V) direct interface is achieved.

FIGURE 5. Sine to Square Wave Converter with Symmetrical Level Detection



Where R1C1 ≅ $1/f_{MAX}$ and R2C2 ≅ response time of voltmeter
V_{OUT} = fR2C1Δ where ΔV = V_{CC}

TL/F/6024–7

FIGURE 6. Diode Dump Tach Accepts any Input Waveform

APPLICATIONS OF THE CMOS SCHMITT

Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

The circuit in *Figure 5a* is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies (see *Figure 5b*). This biases the mean threshold value around zero and makes direct coupling from an op amp output possible.

In *Figure 4*, we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2.

Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage.

Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level. In *Figure 7*, we see a typical circuit, a light activated switch. The high impedance input of the CMOS Schmitt trigger makes biasing very easy. Most photo cells are several kΩ brightly illuminated and a couple MΩ dark. Since CMOS has a 10^{12} typical input impedance, no effects are felt on the input when the output changes. The selection of the biasing resistor is just the solution of a voltage divider equation.

A CMOS application note wouldn't be complete without a low power application. *Figure 8* shows a simple RC oscillator. With only six R's and C's and one Hex CMOS trigger, six low power oscillators can be built. The square wave output is approximately 50% duty cycle because of the balanced input and output characteristics of CMOS. The output frequency equation assumes that $t_1 = t_2 \geq t_{pd0} + t_{pd1}$.

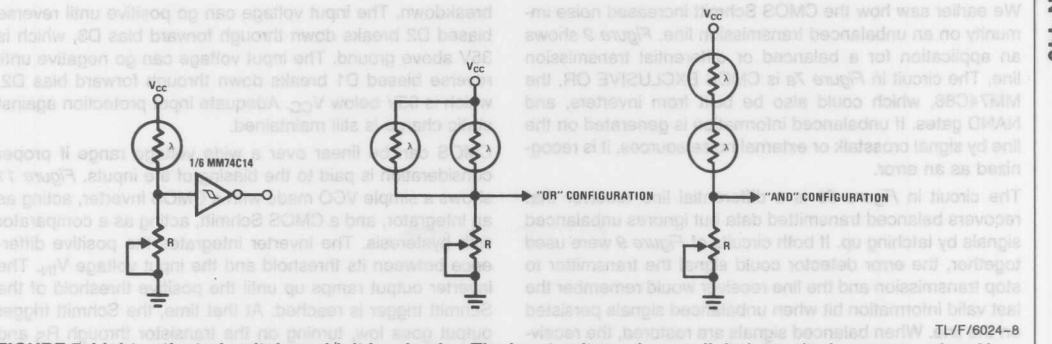
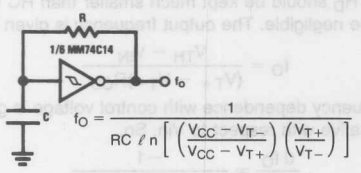


FIGURE 7. Light activated switch couldn't be simpler. The input voltage rises as light intensity increases, when V_{T+} is reached, the output will go low and remain low until the intensity is reduced significantly.



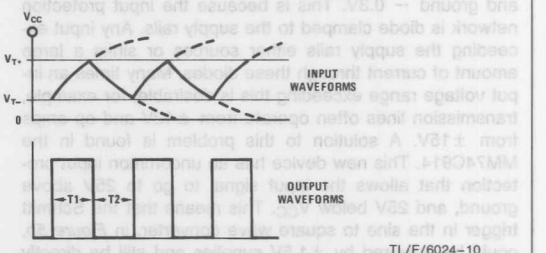
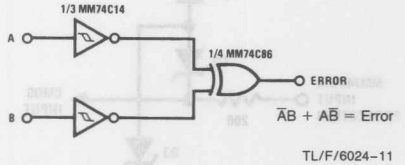


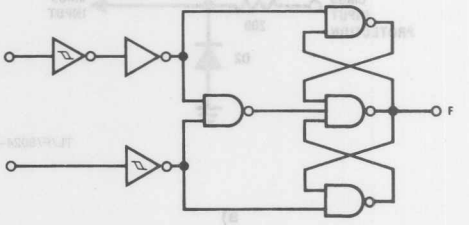
FIGURE 8. Simplest RC Oscillator? Six R's and C's make the CMOS Schmitt into six low power oscillators. Balanced input and output characteristics give the output frequency a typically 50% Duty Cycle.

1/3 MM74C14 Schmitt Trigger
1/6 MM74C04 Inverter
3/4 MM74C00 2-Input NAND
1/3 MM74C10 3-Input NAND



Error is detected when transmission line is unbalanced in either direction.

a) Differential Error Detector



Transmitted data appears at F as long as transmission line is balanced, unbalanced data is ignored and error is detected by above circuit.

b) Differential Line Receiver

Truth Table

A	B	F
0	0	NC
0	1	0
1	0	1
1	1	NC

NC = No Change

FIGURE 9. Increase noise immunity by using the CMOS Schmitt trigger to demodulate a balanced transmission line.

We earlier saw how the CMOS Schmitt increased noise immunity on an unbalanced transmission line. *Figure 9* shows an application for a balanced or differential transmission line. The circuit in *Figure 7a* is CMOS EXCLUSIVE OR, the MM74C86, which could also be built from inverters, and NAND gates. If unbalanced information is generated on the line by signal crosstalk or external noise sources, it is recognized as an error.

The circuit in *Figure 9b* is a differential line receiver that recovers balanced transmitted data but ignores unbalanced signals by latching up. If both circuits of *Figure 9* were used together, the error detector could signal the transmitter to stop transmission and the line receiver would remember the last valid information bit when unbalanced signals persisted on the line. When balanced signals are restored, the receiver can pick up where it left off.

The standard voltage range for CMOS inputs is V_{CC} + 0.3V and ground − 0.3V. This is because the input protection network is diode clamped to the supply rails. Any input exceeding the supply rails either sources or sinks a large amount of current through these diodes. Many times an input voltage range exceeding this is desirable; for example, transmission lines often operate from ±12V and op amps from ±15V. A solution to this problem is found in the MM74C914. This new device has an uncommon input protection that allows the input signal to go to 25V above ground, and 25V below V_{CC}. This means that the Schmitt trigger in the sine to square wave converter, in *Figure 5b*, could be powered by ±1.5V supplies and still be directly compatible with an op amp powered by ±15V supplies.

A standard input protection circuit and the new input protection are shown in *Figure 10*. The diodes shown have a 35V breakdown. The input voltage can go positive until reverse biased D2 breaks down through forward bias D3, which is 35V above ground. The input voltage can go negative until reverse biased D1 breaks down through forward bias D2, which is 35V below V_{CC}. Adequate input protection against static charge is still maintained.

CMOS can be linear over a wide voltage range if proper consideration is paid to the biasing of the inputs. *Figure 11* shows a simple VCO made with a CMOS inverter, acting as an integrator, and a CMOS Schmitt, acting as a comparator with hysteresis. The inverter integrates the positive difference between its threshold and the input voltage V_{IN}. The inverter output ramps up until the positive threshold of the Schmitt trigger is reached. At that time, the Schmitt trigger output goes low, turning on the transistor through R_S and speeding up capacitor C_S. Hysteresis keeps the output low until the integrating capacitor C is discharged through R_D. Resistor R_D should be kept much smaller than RC to keep reset time negligible. The output frequency is given by

$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_{T-})R_{CC}}.$$

The frequency dependence with control voltage is given by the derivative with respect to Vin. So,

$$\frac{d\,f_O}{d\,V_{IN}} = \frac{-1}{(V_{T+} - V_{T-})\,RC},$$

where the minus sign indicates that the output frequency increases as the input is brought further below the inverter threshold. The maximum output frequency occurs when V_{IN} is at ground and the frequency will decrease as V_{IN} is raised up and will finally stop oscillating at the inverter threshold, approximately 0.55 V_{CC}.

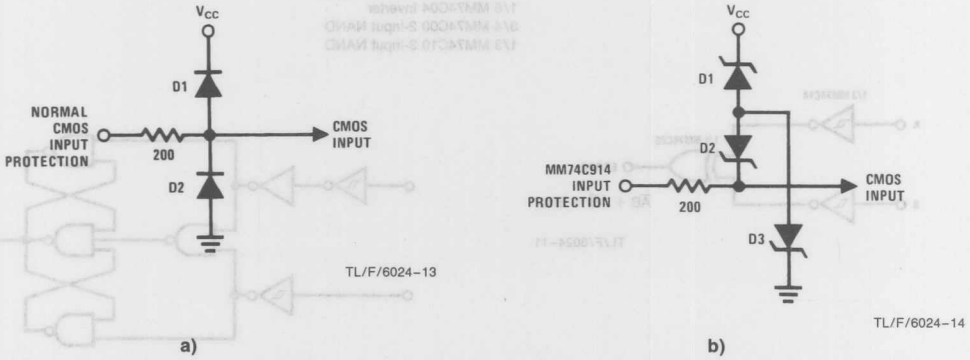
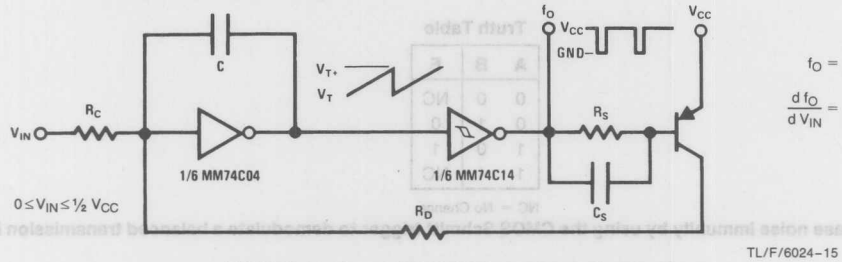


FIGURE 10. Input protection diodes, in a) Normally limit the input voltage swing to 0.3V above V_{CC} and 0.3V below ground. In b) D2 or D1 is reverse biased allowing input swings of 25V above ground or 25V below V_{CC}.



$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_T)\,R_C C}$$

$$\frac{d\,f_O}{d\,V_{IN}} = \frac{-1}{(V_{T+} - V_T)\,R_C C}$$

FIGURE 11. Linear CMOS (Voltage Controller Oscillator)

The pulses from the VCO output are quite narrow because the reset time is much smaller than the integration time. Pulse stretching comes quite naturally to a Schmitt trigger. A one-shot or pulse stretcher made with an inverter and Schmitt trigger is shown in *Figure 12*. A positive pulse coming into the inverter causes its output to go low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged, so the Schmitt input is brought low and the output goes positive. Check the size of the capacitor to make sure that inverter can fully discharge the capacitor in the input pulse time, or

$$I_{SINK\ INVERTER} > \frac{C\,\Delta V}{\Delta T} + \frac{\Delta V}{R}$$

where $\Delta V = V_{CC}$ for CMOS, and ΔT is the input pulse width.

For very narrow pulses, under 100 ns, the capacitor can be omitted and a large resistor will charge up the CMOS gate capacitance just like a capacitor.

When the inverter input returns to zero, the blocking diode prevents the inverter from charging the capacitor and the resistor must charge it from its supply. When the input voltage of the Schmitt reaches V_{T+}, the Schmitt output will go low sometime after the input pulse has gone low.

THE SCHMITT SOLUTION

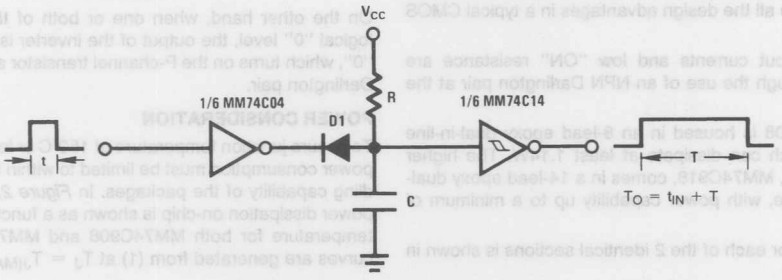
The Schmitt trigger, built from discrete parts, is a careful and sometimes time-consuming design. When introduced in integrated TTL, a few years ago, many circuit designers had renewed interest because it was a building block part. The input characteristics of TTL often make biasing of the trigger input difficult. The outputs don't source as much as they sink, so multivibrators don't have 50% duty cycle, and a limited supply range hampers interfacing with non-5V parts.

The CMOS Schmitt has a very high input impedance with thresholds approximately symmetrical to one half the supply. A high voltage input is available. The outputs sink and source equal currents and pull directly to the supply rails.

A wide threshold range, wide supply range, high noise immunity, low power consumption, and low board space make the CMOS Schmitt a uniquely versatile part.

Use the Schmitt trigger for signal conditioning, restoration of levels, discriminating noisy signals, level detecting with hysteresis, level conversion between logic families, and many other useful functions.

The CMOS Schmitt is one step closer to making design limited only by the imagination of the designer.



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$$T = RC\,\ell n\left(\frac{V_{CC} - V_{BE}}{V_{CC} - V_{T+}}\right) \quad \text{BE SURE THAT } I_{SINK\ INVERTER} > \frac{C\,V_{CC}}{t} + \frac{V_{CC}}{R}$$

FIGURE 12. Pulse Stretcher. A CMOS inverter discharges a capacitor, a blocking diode allows charging through R only. Schmitt trigger output goes low after the RC delay.

Desiging with MM74C908, MM74C918 Dual High Voltage CMOS Drivers

National Semiconductor
Application Note 177
Jen-yen Huang

INTRODUCTION

By combining the merits of both CMOS and bipolar technologies on a single silicon chip, the MM74C908, MM74C918 provides the following distinguished features as general purpose high voltage drivers.

- Wide supply voltage range (3V to 18V)
- High noise immunity (typ 0.45 V_{CC})
- High input impedance (typ $10^{12}\Omega$)
- Extremely low standby power consumption (typ 750 nW at 15V)
- Low output "ON" resistance (typ 8Ω)
- High output drive capability ($I_{OUT} \geq 250$ mA at $V_{OUT} = V_{CC} - 3V$, and $T_J = 65°C$)
- High output "OFF" voltage

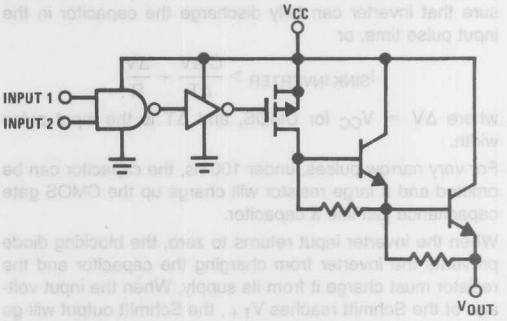
Among these, the first 4 are typical and unique characteristics of CMOS technology which are fully utilized in this circuit to achieve all the design advantages in a typical CMOS system.

The high output currents and low "ON" resistance are achieved through the use of an NPN Darlington pair at the output stage.

The MM74C908 is housed in an 8-lead epoxy dual-in-line package, which can dissipate at least 1.14W. The higher power version, MM74C918, comes in a 14-lead epoxy dual-in-line package, with power capability up to a minimum of 2.27W.

The circuitry for each of the 2 identical sections is shown in *Figure 1*.

With both inputs sitting at logical "1" level, the output of the inverter is also at logical "1", which prevents the P-channel transistor from being turned "ON"; therefore, the output is in its "OFF" state. Only a small amount of leakage current can flow.



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FIGURE 1

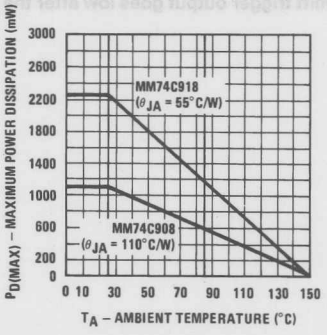
On the other hand, when one or both of the inputs is at logical "0" level, the output of the inverter is also at logical "0", which turns on the P-channel transistor and, hence, the Darlington pair.

POWER CONSIDERATION

To assure junction temperature of 150°C or less, the on-chip power consumption must be limited to within the power handling capability of the packages. In *Figure 2*, the maximum power dissipation on-chip is shown as a function of ambient temperature for both MM74C908 and MM74C918. These curves are generated from (1) at $T_J = T_{J(MAX)} = 150°C$.

$$T_J = T_A + P_D \theta_{jA} \quad (1)$$

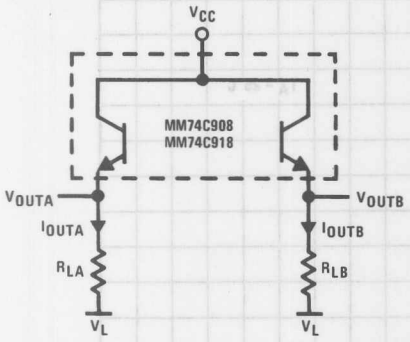
where T_J = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{jA} = thermal resistance between junction and ambient



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FIGURE 2. Maximum Power Dissipation vs Ambient Temperature

A general application circuit for the MM74C908, MM74C918 is as shown in *Figure 3*.



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FIGURE 3

For both sections A and B;

$$I_{OUT} = \frac{V_{CC} - V_L}{R_{ON} + R_L} \quad (2)$$

The device "ON" resistance, R_{ON}, is a function of junction temperature, T_J. The worst-case R_{ON} as a function of T_J is given in (3).

$$R_{ON} = 9[1 + 0.008\,(T_J - 25)] \quad (3)$$

The total power dissipation in the device also consists of normal CMOS power terms (due to leakage current, internal capacitance, switching etc.) which are insignificant compared to the power dissipated at the output stages. Thus, the output power term defines the allowable limits of operation and is given by:

$$PD = P_{DA} + P_{DB} \quad (4)$$
$$= I^2_{OUTA} \times R_{ON} + I^2_{OUTB} \times R_{ON}$$

Given R_{LA} and R_{LB}, (1), (2), (3), (4) can be used to calculate P_D, T_J, etc. through iteration.

For example, let $V_L = 0V$, $V_{CC} = 10V$, $R_{LA} = 100\Omega$, $R_{LB} = 50\Omega$, $T_A = 25°C$, $\theta_{jA} = 110°C/W$.

Assume:

$$R_{ON} = 12.28\Omega$$

By (2):

$$I_{OUTA} = \frac{10}{12.28 + 100} = 0.089A$$

$$I_{OUTB} = \frac{10}{12.28 + 50} = 0.161A$$

By (4):

$$P_D = (0.089)^2 \bullet 12.28 + (0.161)^2 \bullet 12.28 = 0.41W$$

By (1):

$$T_J = 70.5°C$$

And by (3):

$$R_{ON} = 12.28\Omega$$

DESIGN TECHNIQUE

In a typical design, R_L must be chosen to satisy the load requirement (e.g., a minimum current to turn on a relay) and at the same time, the power consumed in the driver package must be kept below its maximum power handling capability.

To minimize the design effort, a graphical technique is developed, which combines all the parameters in one plot, which can be used efficiently to obtain an optimal design.

Assume $T_A = 25°C$ and that both sections of the MM74C908 in *Figure 3* are operating under identical conditions. The maximum allowable package dissipation is:

$$P_D = 2(V_{CC} - V_{OUT}) \times I_{OUT} \quad (6)$$
$$= \frac{1}{110}(150 - T_A) = 1.14W$$

where $T_J = 150°C$, $\theta_{jA} = 110°C/W$ are used in (1) per the data sheet.

Thus, the maximum power allowed in each section is:

$$P_D = (V_{CC} - V_{OUT}) \times I_{OUT} = 0.57W$$

A constant power curve $P_D = 0.57W$ can then be plotted as shown in *Figure 4*. The circuit must operate below this curve. Any voltage-current combination beyond it (in the shaded region) will not guarantee T_J to be lower than 150°C.

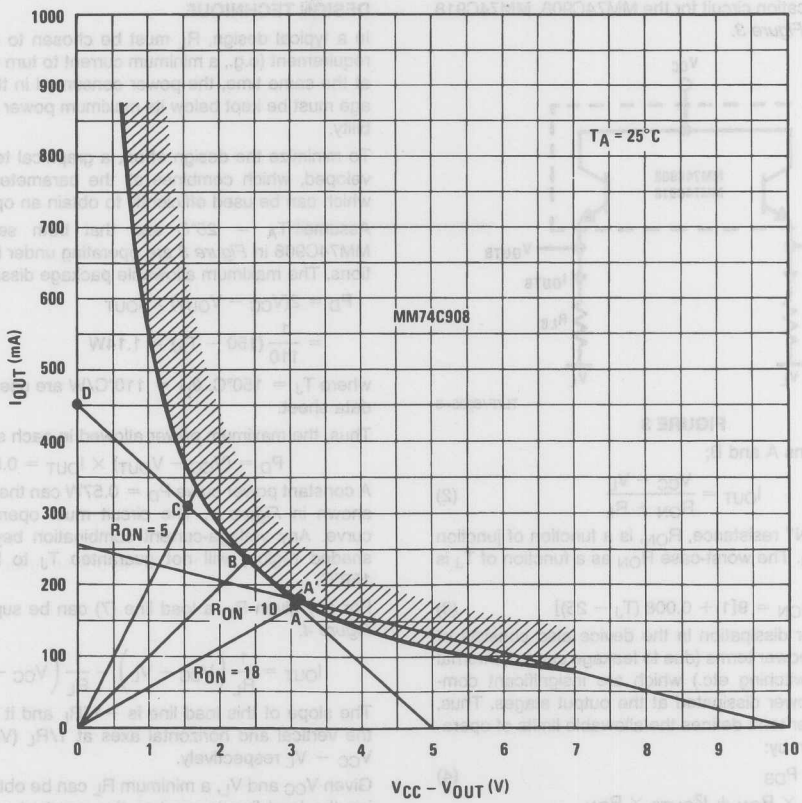
For any given R_L, a load line (7) can be superimposed on *Figure 4*.

$$I_{OUT} = \frac{1}{R_L}\left(V_{CC} - V_L\right) - \frac{1}{R_L}\left(V_{CC} - V_{OUT}\right) \quad (7)$$

The slope of this load line is $-1/R_L$ and it intersects with the vertical and horizontal axes at $1/R_L\,(V_{CC} - V_L)$ and $V_{CC} - V_L$ respectively.

Given V_{CC} and V_L, a minimum R_L can be obtained by drawing the load line tangent to the constant power curve. In *Figure 4*, at $V_{CC} - V_L = 5V$ the line intersects I_{OUT} axis at $I_{OUT} = 450$ mA. Thus, $R_{L(MIN)} = 5V/450\text{ mA} = 11.1\Omega$. Any R_L value below this will move the intersecting point up and cause a section of the load line to extend into the shaded region. Therefore, the junction temperature can exceed $T_{J(MAX)} = 150°C$ in the worst case if the circuit operates on such a section of the load line.

Whether this situation will occur or not is determined by both the value of $V_{CC} - V_L$ and the R_{ON} range of the drivers.



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FIGURE 4

By (3), at $T_J = 150°C$, $R_{ON(MAX)} = 18\Omega$, this is a straight line* passing through the origin with a slope of $I_{OUT}/(V_{CC} - V_{OUT}) = 1/18$ mho and intersects the load line at point A. Similarly, point B and C can be found for typical ($\sim 10\Omega$) and minimum ($\sim 5\Omega$) R_{ON} at $T_J = 150°C$.

For $V_{CC} - V_L = 5V$, the tangent point falls between A and C. Hence, $R_L \geq 11.1\Omega$ calculated above must be satisfied; otherwise, part of the load line within the specified R_{ON} range will extend into the shaded region and therefore, $T_J \geq 150°C$ may occur.

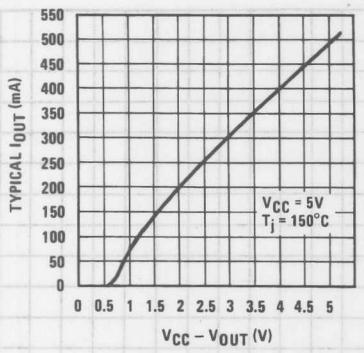
For $V_{CC} - V_L = 10V$, however, a section of the load line can go beyond the $P_D = 0.57W$ curve without affecting the safe operation of the circuit. By inspection of *Figure 4*, the reason is clear—the load line extends into the shaded region only outside of the specified R_{ON} range (to the right of point A'). Within the R_{ON} range, the load line lies below the $P_D = 0.57W$ curve, thus, a safe operation.

To a first approximation**, the section of the load line between A and C is the operating range for the circuit at $V_{CC} - V_L = 5V$ and $R_L = 11.1\Omega$. Hence, the available current and voltage ranges for this circuit are 310 mA $\geq I_{OUT} \geq$ 172 mA and 3.4V $\geq V_{OUT} \geq$ 1.9V, respectively.

Thus, by simply drawing no more than 3 straight lines, one obtains all of the following immediately:

1. All the necessary design information (e.g., minimum R_L, minimum available I_{OUT} and V_{OUT}, etc.)
2. Operating characteristics of the circuit as a whole, including the effect of different R_{ON} values due to process variations, thus, a better insight into the circuit operation.
3. Most importantly, a guarantee that the circuit will be operating in the safe region, ($T_J \leq 150°C$).

For different ambient temperatures or for different power considerations, *Figure 4* can be applied by properly scaling the I_{OUT} axis. (Note that $I_{OUT} \propto T_J - T_A$ and $I_{OUT} \propto P_D$).



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FIGURE 5. Typical I_{OUT} vs Typical V_{OUT}

*Strictly speaking R_{ON} is a non-linear function of I_{OUT}. A typical R_{ON} characteristic at T_J = 150°C is shown in *Figure 5*. The non-linear characteristic near the origin is due to the fact that the output NPN transistor is not saturated. As soon as saturation is reached (I_{OUT} ~ 150 mA) the curve becomes a straight line which extrapolates back to the origin. For practical design purposes, it is sufficient to consider R_{ON} as a linear function of I_{OUT}.

**Note that as the operating point on the load line moves away from the P_D = 0.57W curve (away from the tangent point in this case), the actual junction temperature drops. Therefore, at point A, for example, the device is actually running cooler than T_J = 150°C, even in the worst case. Hence, R_{ON} value drops below 18Ω and the actual operating point is slightly different from A.

To further simplify the design, a family of such curves has been generated as shown in *Figure 6*. Each of these curves corresponds to a particular T_A and P_D (per driver) as indicated, and similar to the P_D = 0.57W curve in *Figure 4*, is generated from (6) by using appropriate T_A values. The application of these curves is illustrated as follows:

Example 1

1. In *Figure 3*, assume that the two drivers in the MM74C908 package are to operate under identical conditions. Find minimum R_L at T_A = 25°C, 45°C, 65°C and 85°C for both $V_{CC} - V_L$ = 5V and $V_{CC} - V_L$ = 10V.

   Then plot $R_{L(MIN)}$ vs T_A.

a) $V_{CC} - V_L$ = 5V

By constructing the load lines tangent to the curves for T_A = 25°C, 45°C, 65°C and 85°C, $R_{L(MIN)}$ for each case can be obtained through the vertical coordinate for the intersection points as shown in *Figure 6*. These are calculated in Table I.

Note that the same results (within graphical error) can be obtained analytically by letting $dR_L/dR_{ON} = 0$. It can be shown that

$$R_{L(MIN)} = \frac{(V_{CC} - V_L)^2}{4X \text{ (Max Power Per Driver)}} \quad (8)$$

b) $V_{CC} - V_L$ = 10V

The $R_{L(MIN)}$ given in (8) may not be a true minimum if the tangent point does not fall inside the specified R_{ON} region. The actual $R_{L(MIN)}$ can be obtained as shown in *Figure 7*. The calculations and results are given in Table II.

Note that the $R_{L(MIN)}$ values in Table II are lower than those given by (8). This corresponds to the section on each of the 4 load lines in *Figure 7* which extends beyond the power limit curve at each associated temperature. However, this section on each load line is outside the specified R_{ON} range. Within the R_{ON} range, load lines are below the power limits; therefore, safe operation is guaranteed.

The $R_{L(MIN)}$ vs T_A plot is as shown in *Figure 8*.

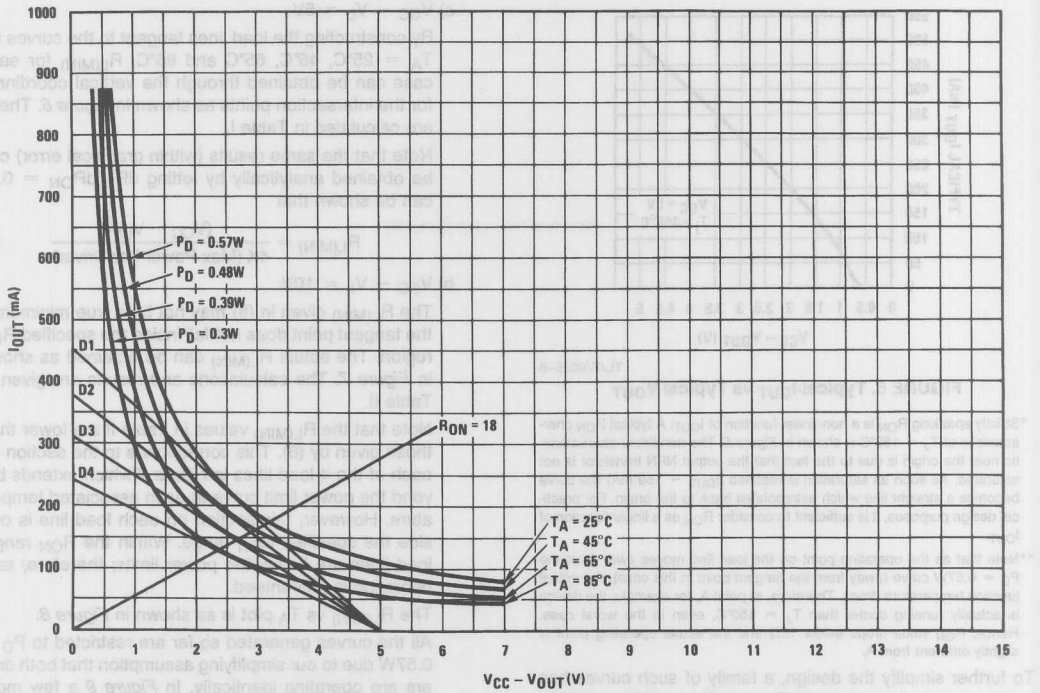
All the curves generated so far are restricted to $P_D \leq$ 0.57W due to our simplifying assumption that both drivers are operating identically. In *Figure 9* a few more curves are added to account for the general situation in which only the restriction $P_{DA} + P_{DB} \leq$ 1.14W is required, (i.e., P_{DA} can be different from P_{DB}). Application of *Figure 9* is illustrated as follows:

TABLE I

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	450	375	310	240
$R_{L(MIN)} = \frac{5}{I_{OUT} \text{ @ D1, 2, 3, 4}}$ (Ω)	11.1	13.3	16.1	20.8

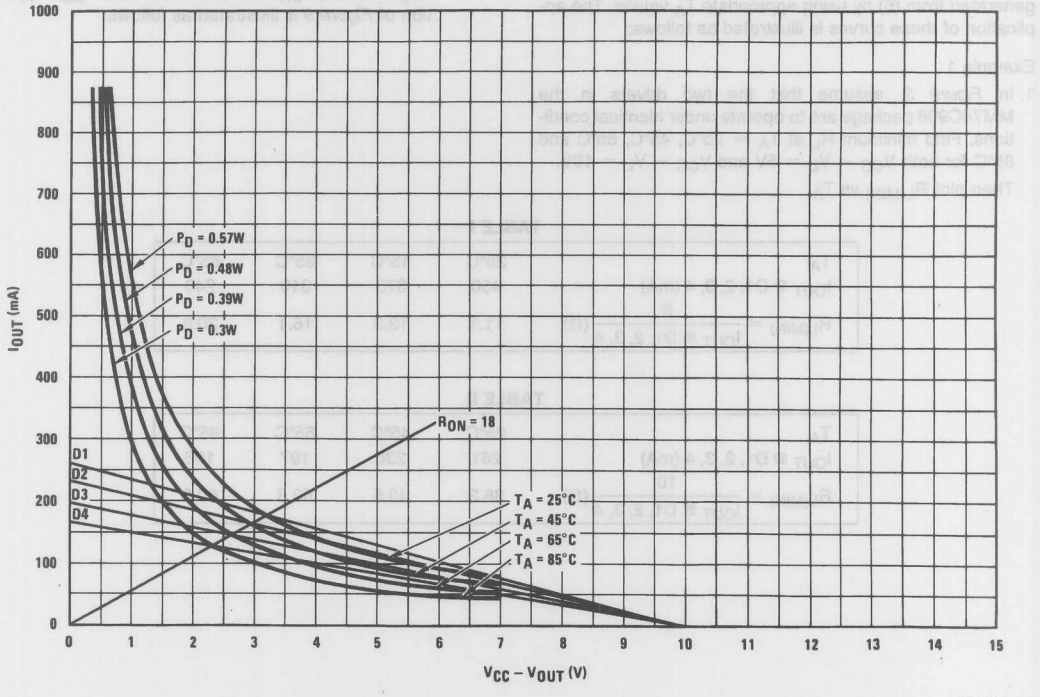
TABLE II

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	261	230	197	166
$R_{L(MIN)} = \frac{10}{I_{OUT} \text{ @ D1, 2, 3, 4}}$ (Ω)	38.3	43.5	50.8	60.2



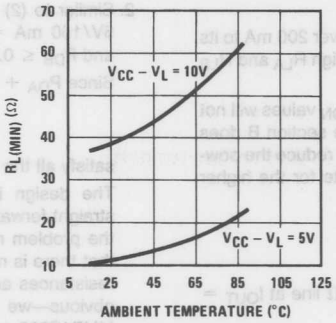
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FIGURE 6



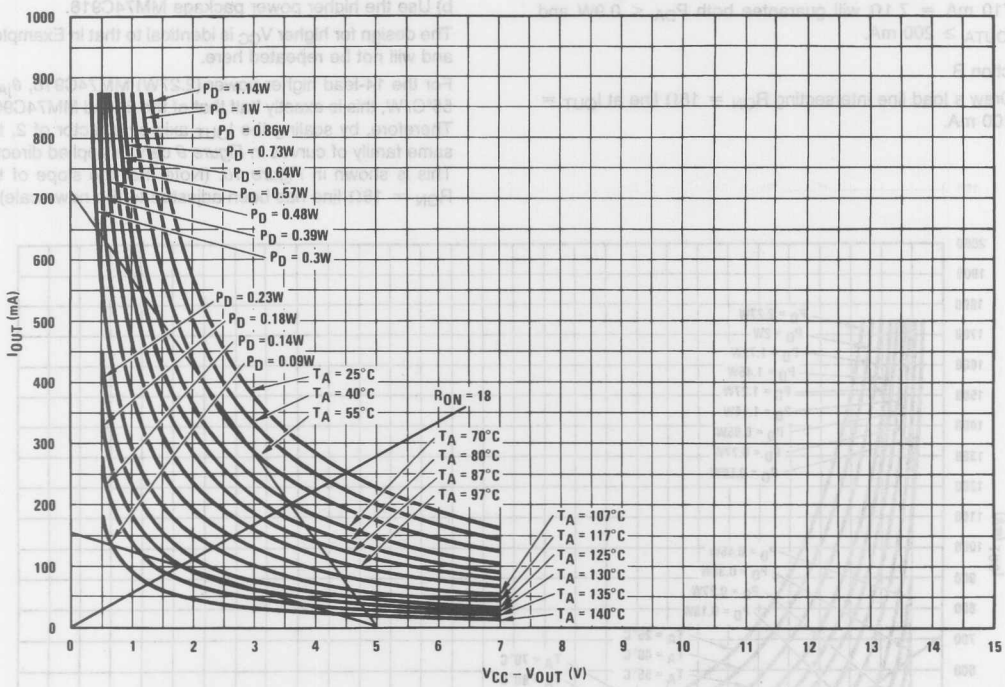
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FIGURE 7



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FIGURE 8



TL/F/6025–9

FIGURE 9

Example 2

In *Figure 3*, assume that driver A has to deliver 200 mA to its load while driver B needs only 100 mA. Design R_{LA} and R_{LB} for $V_{CC} - V_L = 5V$.

By inspection of *Figure 4*, units with high R_{ON} values will not be able to deliver 200 mA. However, since section B does not need the same amount of drive, we can reduce the power consumed in this section to compensate for the higher power (> 0.57W) required in section A.

The design procedure follows:

Section A

1. Draw a load line intersecting $R_{ON} = 18\Omega$ line at $I_{OUT} = 200$ mA.
2. This load line intersects the I_{OUT} axis at $I_{OUT} = 710$ mA and is tangent to $P_{DA} \cong 0.9W$ curve, thus $R_{LA} \cong 5V/710\ mA = 7.1\Omega$ will guarantee both $P_{DA} \leq 0.9W$ and $I_{OUTA} \geq 200$ mA.

Section B

1. Draw a load line intersecting $R_{ON} = 18\Omega$ line at $I_{OUT} = 100$ mA.
2. Similar to (2) above, it is seen immediately that $R_{LB} \cong 5V/150\ mA = 33.3\Omega$ will guarantee $I_{OUTB} \geq 100$ mA and $P_{DB} \leq 0.18W$.

Since $P_{DA} + P_{DB} \leq 0.9 + 0.18 < 1.14W$

$$R_{LA} = 7.1\Omega$$

$$R_{LB} = 33.3\Omega$$

satisfy all the requirements in this problem.

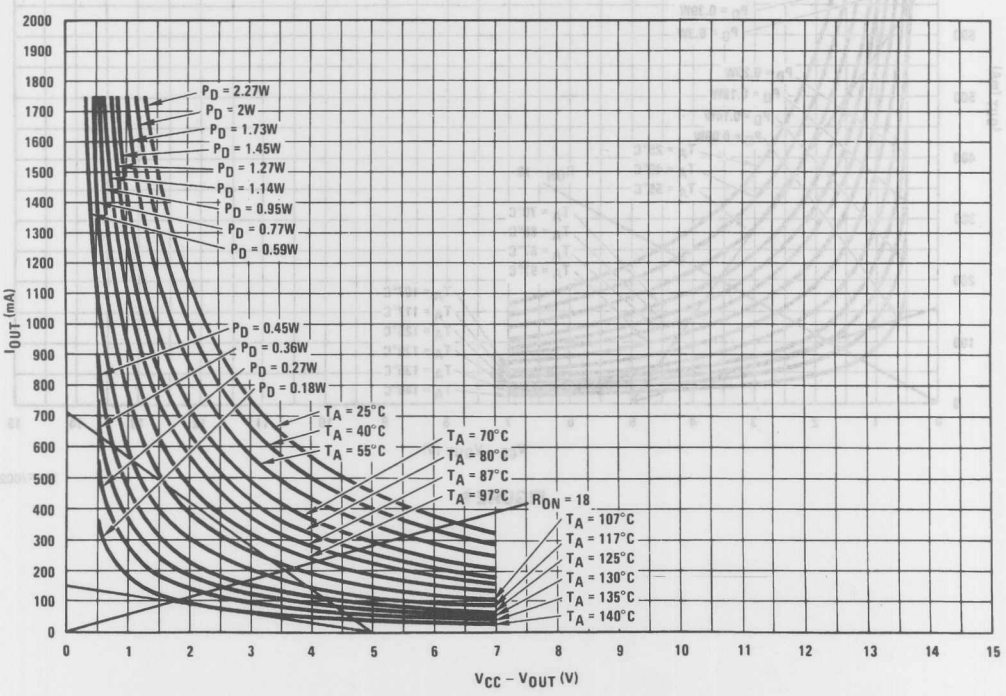
The design in Example 2 illustrated the simple and straight-forward use of the curves and the result meets all the problem requirements. However, it should be noted that there is not much design margin left for tolerance in resistances and other circuit parameters. The reason is obvious—we are pushing at the power limit of the MM74C908 package—and the solutions are simple:

a) Increase V_{CC} supply

b) Use the higher power package MM74C918.

The design for higher V_{CC} is identical to that in Example 2 and will not be repeated here.

For the 14-lead higher power (2.27W) MM74C918, $\theta_{jA} = 55°C/W$, this is exactly half that of the 8-lead MM74C908. Therefore, by scaling the I_{OUT} axis by a factor of 2, the same family of curves in *Figure 9* can be applied directly. This is shown in *Figure 10*. (Note that the slope of the $R_{ON} = 18\Omega$ line has been adjusted to the new scale).



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FIGURE 10

By drawing the same load lines, it is found that:

$$R_{LA} \cong 5V/710\ mA = 7.1\Omega$$

guarantees $P_{DA} \leq 0.9W$

and

$$R_{LB} \cong 5V/150\ mA = 33.3\Omega$$

guarantees $P_{DB} \leq 1.08W$

which is way below the maximum power 2.27W available. Therefore, both R_{LA} and R_{LB} can be lowered to account for tolerance in the resistors. Consider specifically the following example:

Example 3

Assume driver A, B of the MM74C918 have to deliver 250 mA and 150 mA, respectively, to its load. Design R_{LA} and R_{LB} at $V_{CC} - V_L = 10V$.

Driver A

1. In *Figure 11*, draw the load line intersecting $R_{ON} = 18\Omega$ at $I_{OUT} = 250$ mA.
2. This load line intersects the I_{OUT} axis at 450 mA. Thus, by inspection $R_{LA} \cong 10V/450\ mA \cong 22.2\Omega$ guarantees $P_{DA} \leq 1.14W$.

Driver B

1. Draw the load line intersecting $R_{ON} = 18\Omega$ at $I_{OUT} = 150$ mA.
2. This load line intersects the I_{OUT} axis at 210 mA. Thus, by inspection $R_{LB} \cong 10V/210\ mA = 47.6\Omega$ guarantees $P_{DB} \leq 0.4W$.

Since $P_{DA} + P_{DB} \leq 1.14 + 0.4 = 1.8W$, while the package is capable of delivering 2.27W, both R_{LA} and R_{LB} can be lower than the above values and the circuit still operates safely. By picking the closest standard resistance values:

$$R_{LA} = 20\Omega$$

$$R_{LB} = 43\Omega$$

For 5% tolerance in these values,

$$19\Omega \leq R_{LA} \leq 21\Omega$$

$$40.85\Omega \leq R_{LB} \leq 45.15\Omega$$

Thus:

$$I_{OUTA(MIN)} \geq \frac{10V}{18\Omega + 21\Omega} = 256.4\ mA > 250\ mA$$

$$I_{OUTB(MIN)} \geq \frac{10V}{18\Omega + 45.15\Omega} = 158.3\ mA > 150\ mA$$

$$P_{DA(MAX)} \leq \left(\frac{10V}{18\Omega + 19\Omega}\right)^2 \times 18\Omega = 1.31W$$

$$P_{DB(MAX)} \leq \left(\frac{10V}{18\Omega + 40.85\Omega}\right)^2 \times 18\Omega = 9.52W$$

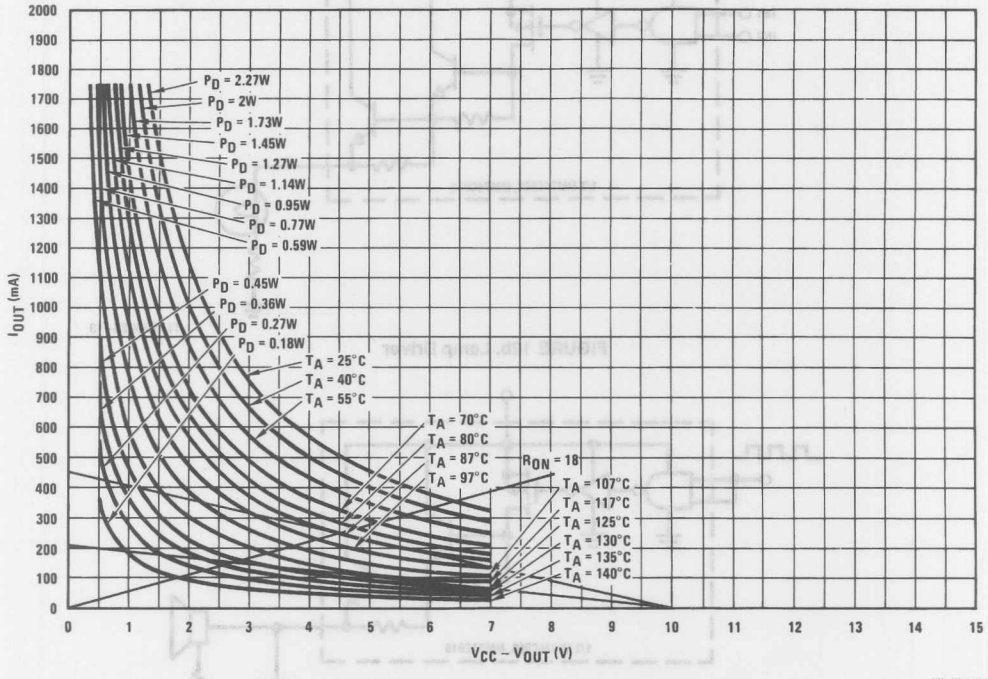
$$P_{DA(MAX)} + P_{DB(MAX)} \leq 1.31 + 0.52 < 2.27W$$

Therefore:

$$R_{LA} = 20\Omega (1.5W, 5\%)$$

$$R_{LB} = 43\Omega\ (1W, 5\%)$$

will guarantee satisfactory performance of the circuit.



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FIGURE 11

APPLICATIONS

Like most other drivers, the MM74C908, MM74C918 can be used to drive relays, lamps, speakers, etc. These are shown in *Figure 12*. (To suppress transient spikes at turn-off, a diode as shown as *Figure 12a* is recommended at the relay coil or any other inductive load.)

However, the MM74C908, MM74C918 offers a unique CMOS feature that is not available in drivers from other logic families—extremely low standby power. At V_{CC} = 15V, power dissipation per package is typically 750 nW when the outputs are not drawing current. Thus, the drivers can be sitting out on line (a telephone line, for example) drawing essentially zero current until activated—an ideal feature for many applications.

The dual feature and the NAND function of the driver design can also be used to advantage as shown in the following applications.

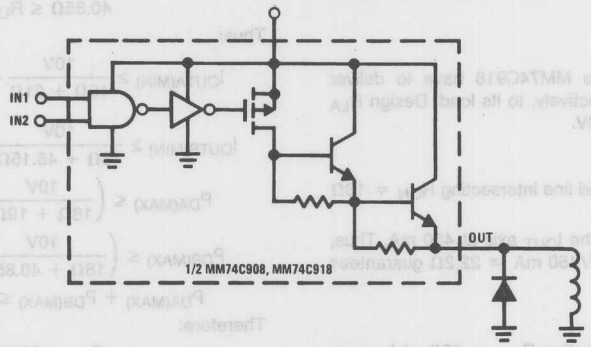


FIGURE 12a. Relay Driver

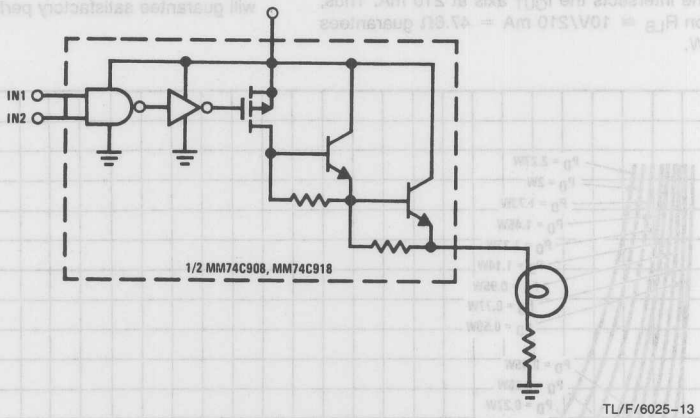


FIGURE 12b. Lamp Driver

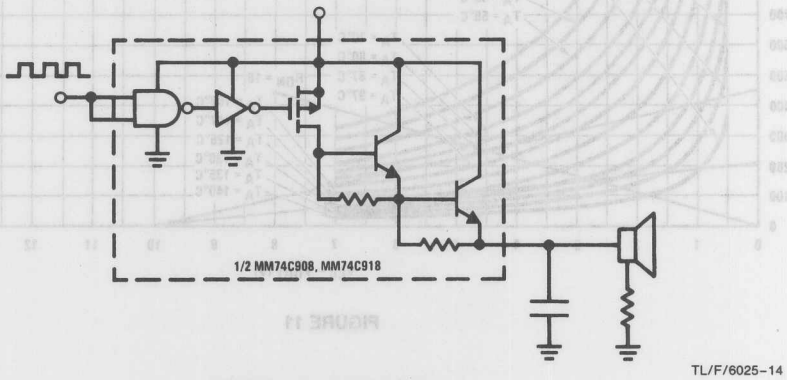


FIGURE 12c. Speaker Driver

In *Figure 13*, the 2 drivers in the package are connected as a Schmitt trigger oscillator, where R1 and R2 are used to generate hysteresis. R3 and C are the inverting feedback timing elements and R4 is the pull-down load for the first driver. Because of its current capability, the circuit can be used to drive an array of LEDs or lamps. If resistor R4 is replaced by an LED (plus a current limiting resistor), the circuit becomes a double flasher with the 2 LEDs flashing out of phase. This is shown in *Figure 14*.

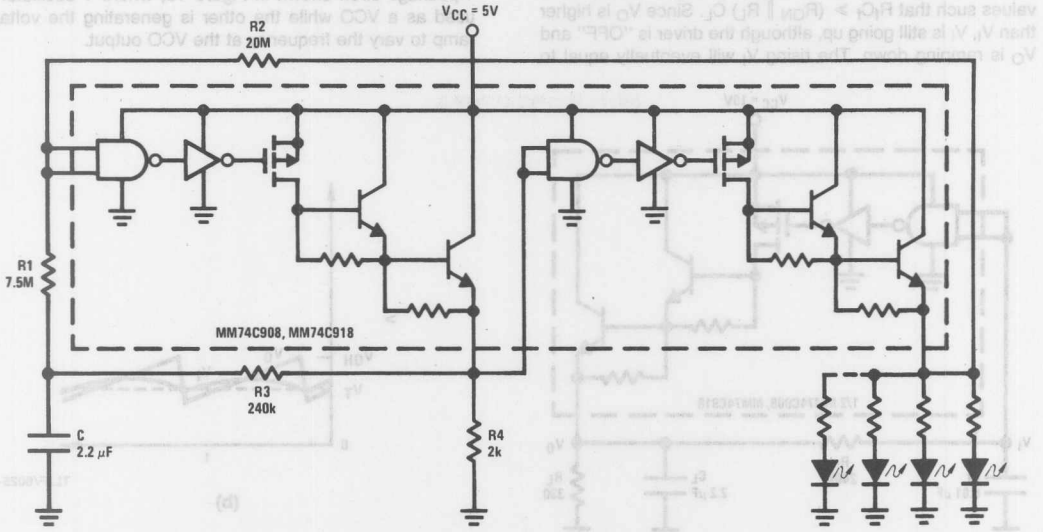


FIGURE 13. High Drive Oscillator/Flasher

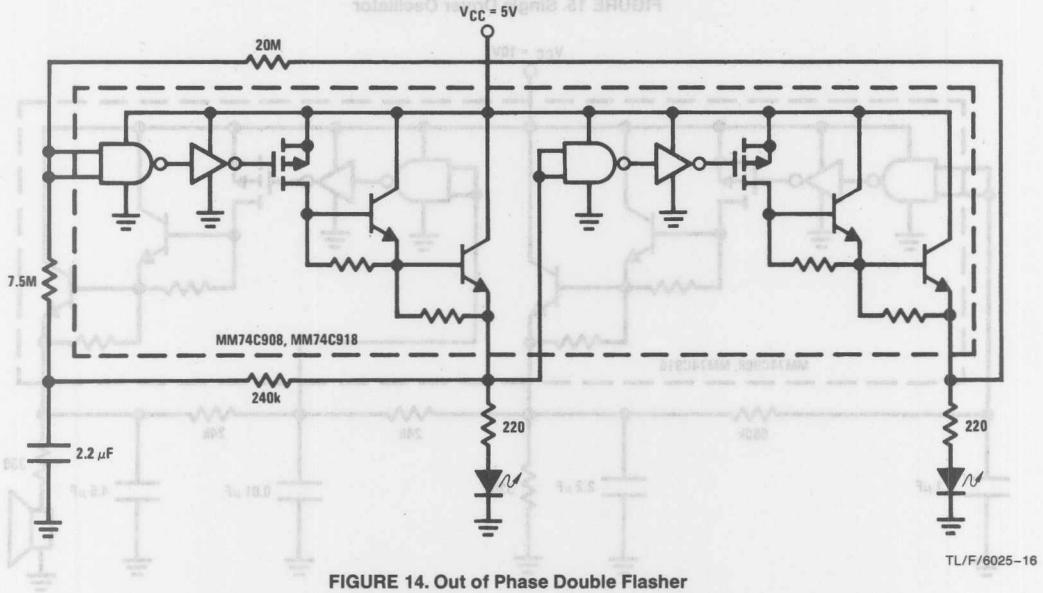


FIGURE 14. Out of Phase Double Flasher

Another oscillator circuit using only 1/2 of the package and 4 passive components is shown in *Figure 15*. Assume V_I is slightly below the input trip point, the driver is "ON" and charging both V_O and V_I until V_I reaches the trip point, V_T, when the driver starts to turn "OFF". V_O can be made much higher than V_I at this instance by adjusting the component values such that $R_f C_f \gg (R_{ON} \parallel R_L) C_L$. Since V_O is higher than V_I, V_I is still going up, although the driver is "OFF" and V_O is ramping down. The rising V_I will eventually equal to the falling V_O, and then start discharging. Then, both V_I and V_O discharge until V_I hits the trip point, V_T, again, when the driver is turned "ON", charging up V_O and subsequently V_I to complete a cycle.

This oscillator is ideal for low cost applications like the 1-package siren shown in *Figure 16*, where 1 oscillator is used as a VCO while the other is generating the voltage ramp to vary the frequency at the VCO output.

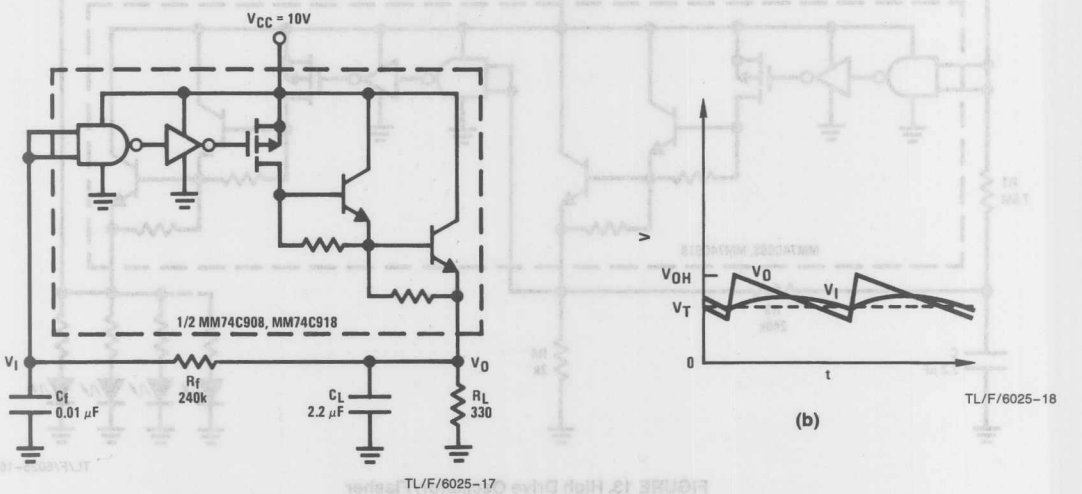


FIGURE 15. Single Driver Oscillator

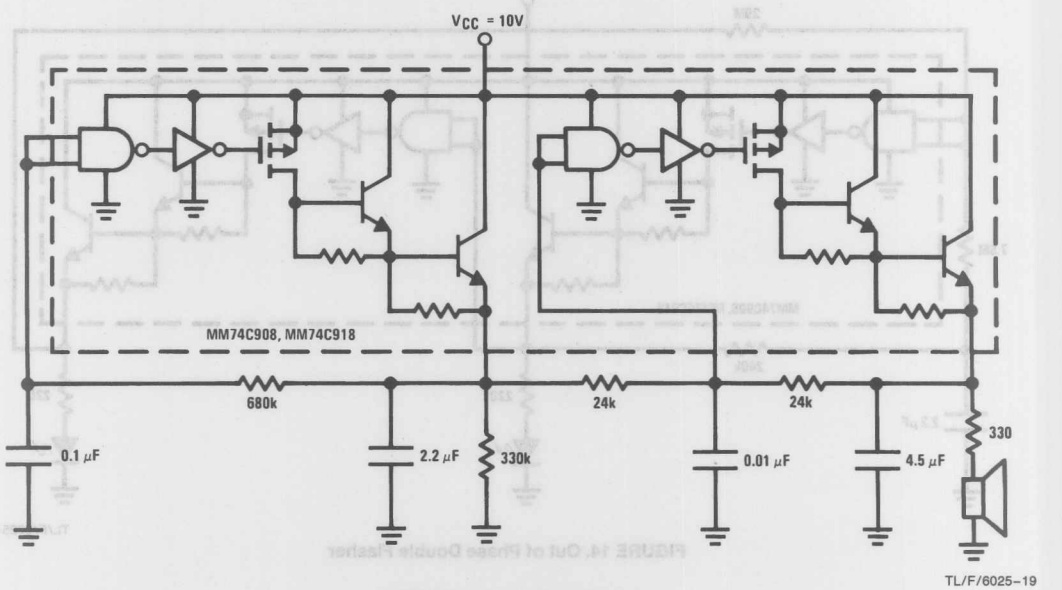
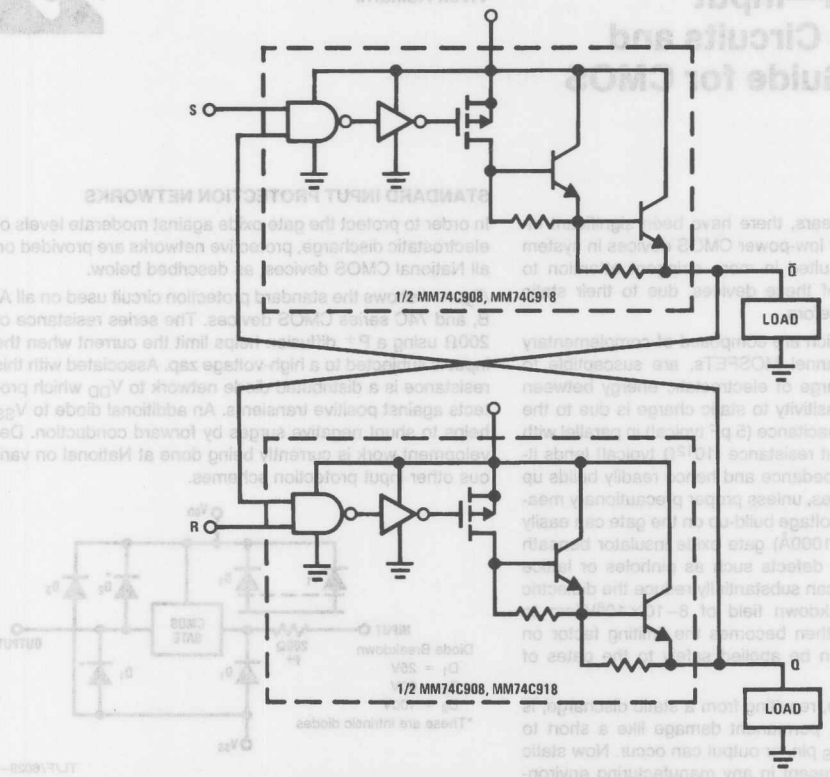


FIGURE 16. Low Cost Siren

The NAND functions at the input can also be used to reduce package count in applications where both high output drive and input NAND features are required. One such example is given in *Figure 17*.



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FIGURE 17. High Drive RS Latch

Protection Circuits and Handling Guide for CMOS Devices

INTRODUCTION

During the past few years, there have been significant increase in the usage of low-power CMOS devices in system designs. This has resulted in more stringent attention to handling techniques of these devices, due to their static sensitivity, than ever before.

All CMOS devices, which are composed of complementary pairs of n- and p-channel MOSFETs, are susceptible to damage by the discharge of electrostatic energy between any two pins. This sensitivity to static charge is due to the fact that gate input capacitance (5 pF typical) in parallel with an extremely high input resistance ($10^{12}\Omega$ typical) lends itself to a high input impedance and hence readily builds up the electrostatic charges, unless proper precautionary measures are taken. This voltage build-up on the gate can easily break down the thin (1000Å) gate oxide insulator beneath the gate metal. Local defects such as pinholes or lattice defects of gate oxide can substantially reduce the dielectric strength from a breakdown field of $8-10\times10^6$V/cm to $3-4\times10^6$V/cm. This then becomes the limiting factor on how much voltage can be applied safely to the gates of CMOS devices.

When a higher voltage, resulting from a static discharge, is applied to the device, permanent damage like a short to substrate, V_{DD} pin, V_{SS} pin, or output can occur. Now static electricity is always present in any manufacturing environment. It is generated whenever two different materials are rubbed together. A person walking across a production floor can generate a charge of thousands of volts. A person working at a bench, sliding around on a stool or rubbing his arms on the work bench can develop a high static potential. Table I shows the results of work done by Speakman[1] on various static potentials developed in a common environment. The ambient relative humidity, of course, has a great effect on the amount of static charge developed, as moisture tends to provide a leakage path to ground and helps reduce the static charge accumulation.

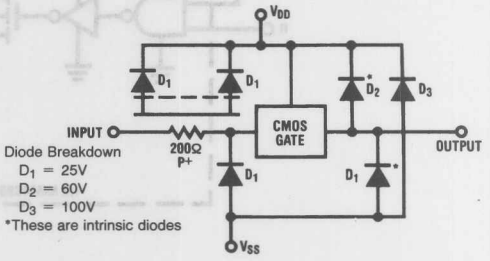
TABLE I. Various Voltages Generated in 15%–30% Relative Humidity (after Speakman[1])

Condition	Most Common Reading (Volts)	Highest Reading (Volts)
Person walking across carpet	12,000	39,000
Person walking across vinyl floor	4,000	13,000
Person working at bench	500	3,000
16-lead DIPs in plastic box	3,500	12,000
16-lead DIPs in plastic shipping tube	500	3,000

STANDARD INPUT PROTECTION NETWORKS

In order to protect the gate oxide against moderate levels of electrostatic discharge, protective networks are provided on all National CMOS devices, as described below.

Figure 1 shows the standard protection circuit used on all A, B, and 74C series CMOS devices. The series resistance of 200Ω using a P^+ diffusion helps limit the current when the input is subjected to a high-voltage zap. Associated with this resistance is a distributed diode network to V_{DD} which protects against positive transients. An additional diode to V_{SS} helps to shunt negative surges by forward conduction. Development work is currently being done at National on various other input protection schemes.

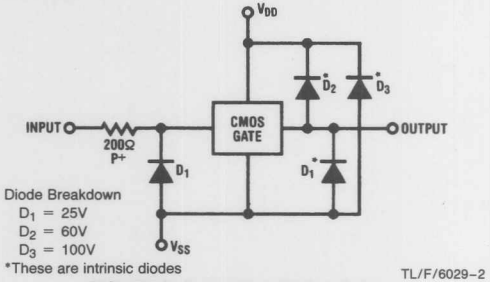


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FIGURE 1. Standard Input Protection Network

OTHER PROTECTIVE NETWORKS

Figure 2 shows the modified protective network for CD4049/4050 buffer. The input diode to V_{DD} is deleted here so that level shifting can be achieved where inputs are higher than V_{DD}.



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FIGURE 2. Protective Network for CD4049/50 and MM74C901/2

Figure 3 shows a transmission gate with the intrinsic diode protection. No additional series resistors are used so the on resistance of the transmission gate is not affected.

All CMOS circuits from National's CD4000 Series and 74C Series meet MIL-STD-38510 zap test requirements of 400V from a 100 pF charging capacitor and 1.5 kΩ series resistance. This human body simulated model of 100 pF capaci-

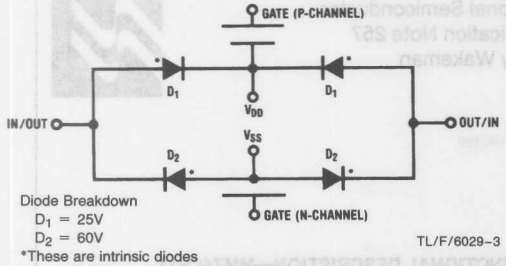


FIGURE 3. Transmission Gate with Intrinsic Diodes to Protect Against Static Discharge

tance in series with 1.5 kΩ series resistance was proposed by Lenzlinger[2] and has been widely accepted by the industry. The set-up used to perform the zap test is shown in *Figure 4.*

V_{ZAP} is applied to DUT in the following modes by charging the 100 pF capacitor to V_{ZAP} with the switch S_1 in position 1 and then switching to position 2, thus discharging the charge through 1.5 kΩ series resistance into the device under test. Table II shows the various modes used for testing.

TABLE II. Modes of High-Voltage Test

Mode	+ Terminal	− Terminal
1	Input	V_{SS}
2	V_{DD}	Input
3	Input	Associated Output
4	Associated Output	Input

Pre- and post-zap performance is monitored on the input leakage parameter at V_{DD} = 18V. It has been found that all National's CMOS devices of CD4000 and 74C families can withstand 400V zap testing with above mentioned conditions and still be under the pre- and post-zap input leakage conditions of ±10 nA.

HANDLING GUIDE FOR CMOS DEVICES

From Table I, it is apparent that extremely high static voltages generated in a manufacturing environment can destroy even the optimally protected devices by reaching their threshold failure energy levels. For preventing such catastrophies, simple precautions taken could save thousands of dollars for both the manufacturer and the user.

In handling unmounted chips, care should be taken to avoid differences in voltage potential between pins. Conductive carriers such as conductive foams or conductive rails should be used in transporting devices. The following simple precautions should also be observed.

1. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
3. Table tops should be covered with grounded conductive tops. Also test areas should have conductive floor mats.

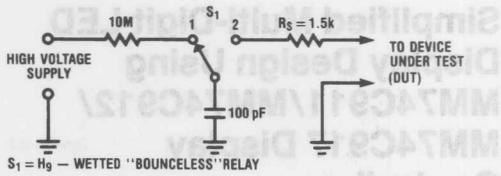


FIGURE 4. Equivalent RC Network to Simulate Human Body Static Discharge (after Lenzlinger[2])

Above all, there should be static awareness amongst all personnel involved who handle CMOS devices or the subassembly boards. Automated feed mechanisms for testing of devices, for example, must be insulated from the device under test at the point where devices are connected to the test set. This is necessary as the transport path of devices can generate very high levels of static electricity due to continuous sliding of devices. Proper grounding of equipment or presence of ionized-air blowers can eliminate all these problems.

At National all CMOS devices are handled using all the precautions described above. The devices are also transported in anti-static rails or conductive foams. Anti-static, by definition[3] means a container which resists generation of triboelectric charge (frictionally generated) as the device is inserted into, removed from, or allowed to slide around in it. It must be emphasized here that packaging problems will not be solved merely by using anti-static rails or containers as they do not necessarily shield devices from external static fields, such as those generated by a charged person. Commercially available static shielding bags, such as 3M company's low resistivity ($\leq 10^4\Omega$/sq.) metallic coated polyester bags, will help prevent damages due to external stray fields. These bags work on the well-known Faraday cage principle. Other commercially available materials are Legge company's conductive wrist straps, conductive floor coating, and various other grounding straps which help prevent against the electrostatic damage by providing conductive paths for the generated charge and equipotential surfaces.

It can be concluded that electrostatic discharge prevention is achievable with simple awareness and careful handling of CMOS devices. This will mean wide and useful applications of CMOS in system designs.

FOOTNOTES

1. T.S. Speakman, "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to ESD," 12th Annual Proc. of Reliability Physics, 1974.
2. M. Lenzlinger, "Gate Protection of MIS Devices," IEEE Transac. on Electron Devices, ED-18, No. 4, April 1971.
3. J.R. Huntsman, D.M. Yenni, G. Mueller, "Fundamental Requirements for Static Protective Containers." Presented at 1980 Nepcon/West Conference, Application Note—3M Static Control Systems.

Simplified Multi-Digit LED Display Design Using MM74C911/MM74C912/ MM74C917 Display Controllers

National Semiconductor
Application Note 257
Larry Wakeman

I. INTRODUCTION

The MM74C911, MM74C912 and MM74C917 are CMOS display controllers that control multiplexing of 8-segment LED displays. These devices each have an on-chip multiplex oscillator and associated logic to easily implement multi-digit displays with minimal additional hardware. These controllers were designed to be easily interfaced to a microprocessor as a small 4- or 6-byte area of write-only memory (WOM), but they are not limited to this environment.

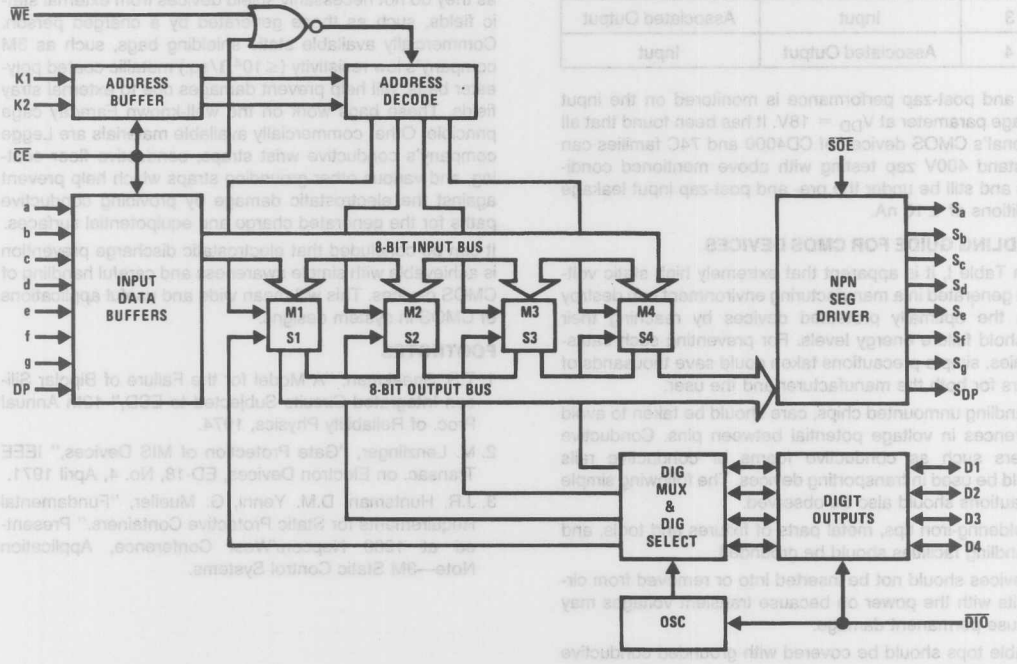
The MM74C911 is the simplest of these devices. It has one data input for each of its eight segment outputs, allowing direct control of any LED segment. Both the MM74C912 and MM74C917 have five data inputs which accept either BCD (MM74C912) or hexadecimal (MM74C917) data, plus decimal point. The MM74C911 can interface up to four 8-segment displays and the MM74C912/MM74C917 can control up to six 8-segment displays.

II. FUNCTIONAL DESCRIPTION—MM74C911

The functional block diagram for the MM74C911 is shown in *Figure 1*. The eight data inputs are buffered and bussed to the four dual-port latches. To write data into a particular latch, K1 and K2 address inputs are decoded and the proper latch is enabled when $\overline{CE}$ and $\overline{WE}$ are taken low.

The latch outputs are controlled by the multiplexer (MUX) logic. All four latch data outputs are commonly bussed, and are sequentially read by the MUX logic. The bussed 8-segment outputs are then buffered by bipolar segment driver transistors, which are enabled when $\overline{SOE}$ is low, and are in TRI-STATE® mode when Segment Output Enable ($\overline{SOE}$) is held high. This allows easy display blanking without loss of data.

The multiplexer logic controls all of the timing for the MM74C911 and also generates the digit output strobes. The timing diagram is shown in *Figure 2*.



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FIGURE 1. MM74C911 Block Diagram

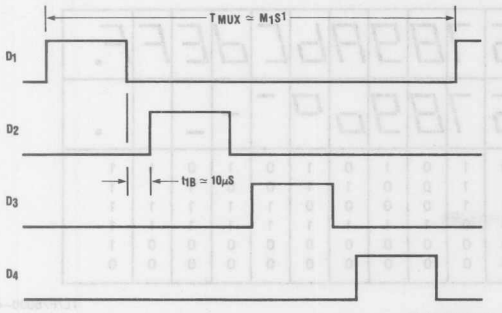


FIGURE 2. MUX Timing for MM74C911

By raising the Digit In-Out ($\overline{DIO}$) input high, the internal oscillator is disabled and the digit outputs become inputs which control reading of the 4-digit latches. This allows the MM74C911 to be slaved to other multiplex timing signals. If both $\overline{SOE}$ and $\overline{DIO}$ are held high, both the display and oscillator are disabled causing the MM74C911 to be in a low-power mode where it typically draws less than 1 μA. *Figure 3* shows the truth table for these control inputs.

$\overline{DIO}$/$\overline{OSE}$	$\overline{SOE}$	Mode
0	0	NORMAL DISPLAY MODE
0	1	DISPLAY BLANKED
1	0	WILL DISPLAY ONE DIGIT*
1	1	LOW POWER MODE

FIGURE 3. Operating Modes for the MM74C911/MM74C912/MM74C917 (*The 74C911 Digit Outputs become Inputs)

III. FUNCTIONAL DESCRIPTION— MM74C912/MM74C917

The functional block diagram for the MM74C912 and MM74C917 is shown in *Figure 4*. These devices are very similar to the MM74C911. There are only five data inputs on the MM74C912 and MM74C917 which are buffered, then bussed to six 5-bit dual-port latches. The address present on K1, K2, and K3 will dictate which of the six latches will be loaded when both $\overline{CE}$ and $\overline{WE}$ are low. The outputs of all of the latches are commonly bussed and fed into a decoder ROM which converts BCD (MM74C912) or hexadecimal (MM74C917) code to seven segment. The fifth bit is the decimal point, which bypasses the ROM. The 8-segment bits are then buffered by eight NPN-segment drivers. Like the MM74C911, these outputs are TRI-STATE and will blank the display when $\overline{SOE}$ is held high.

All of the multiplexing is controlled by an internal oscillator and control logic. The logic sequentially reads each latch and activates the digit outputs. The oscillator can be disabled by raising the Oscillator Enable ($\overline{OSE}$) input high, but the digit outputs do not become inputs and thus the MM74C912, and MM74C917 can not be slaved. However, by raising both $\overline{SOE}$ and $\overline{OSE}$ high, these parts can be put into a low-power mode similar to the MM74C911. *Figure 3* shows the controller operating modes.

The MM74C912 and the MM74C917 are identical except for the last seven ROM locations. The ROM outputs are shown in *Figure 5* for both parts.

IV. DISPLAY INTERFACE DESIGN

A. Common Cathode LED's

Since the MM74C911/MM74C912/MM74C917 contain all the multiplex circuitry necessary to operate a 4- or 6-digit display, all the designer must do is choose appropriate segment resistors and digit drivers to properly illuminate the LEDs. A typical LED connection is shown in *Figure 6*. Based on the selected display, a certain segment current will be required. This current will determine the value of the segment resistor and the type of digit driver necessary. The design for the MM74C911 is nearly the same as for the MM74C912/MM74C917 except that due to multiplexing the 6-digit controllers must be designed to a higher peak current value.

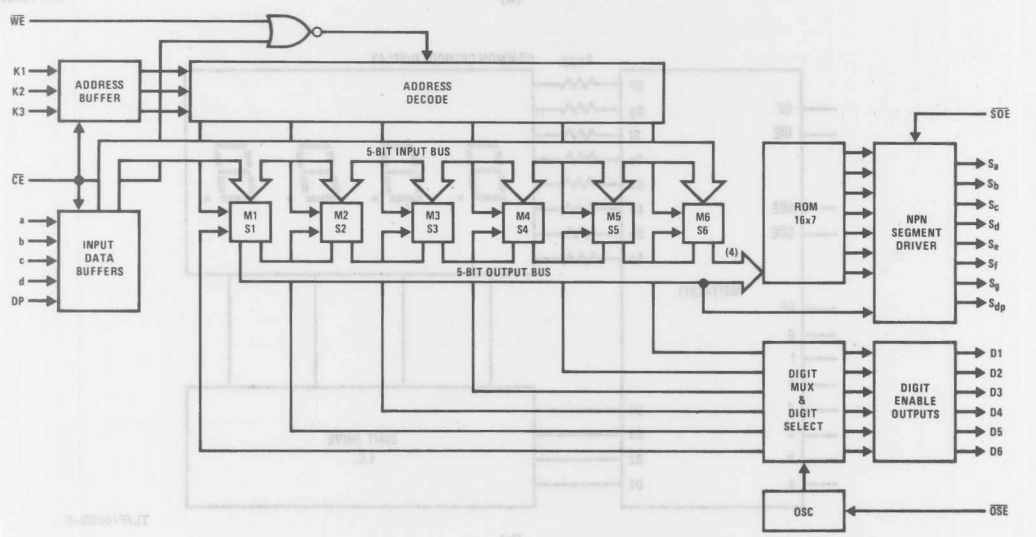
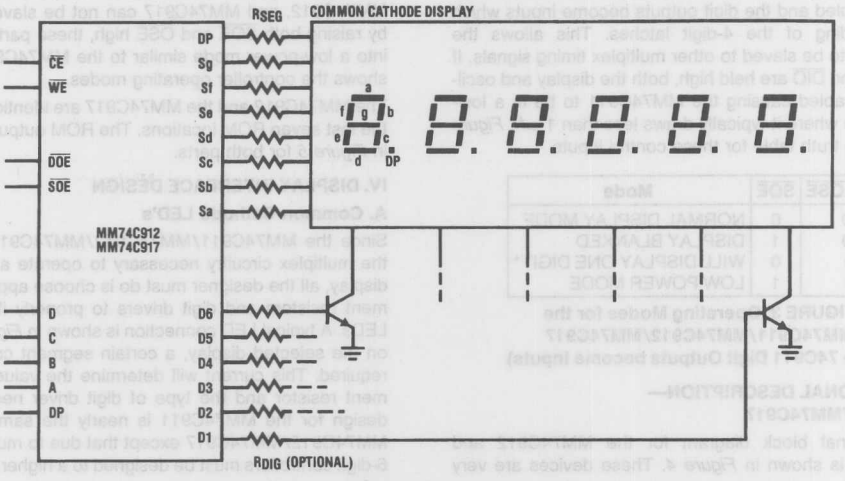


FIGURE 4. MM74C912 and MM74C917 Display Controller

MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	F.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	o	°	¯	-	_		.
Input A 2^0	X	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Output Enable $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

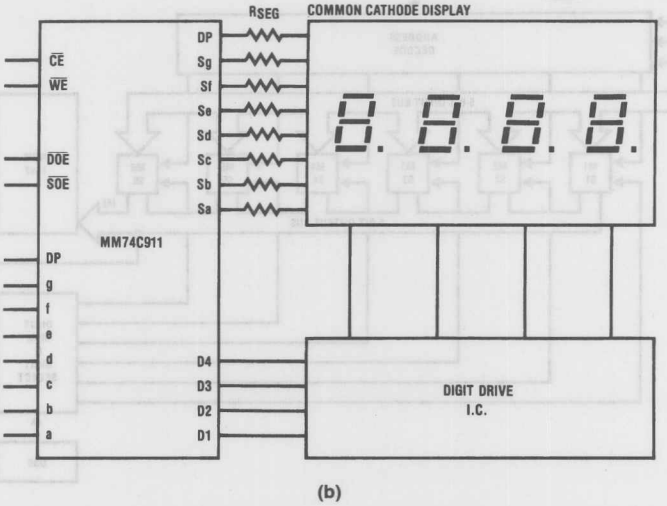
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FIGURE 5. MM74C912/MM74C917 Character Fonts



(a)

TL/F/6030–5



TL/F/6030–6

(b)

FIGURE 6. Typical LED Connections for (a) MM74C912/MM74C917 (b) MM74C911

As an example, suppose the NSN781 (2-digit, 0.7″ common catholde LED display) has been selected. These displays require an average current of 8 mA per segment for good illumination. The MM74C911 multiplexes four digits; thus, any one digit is on ¼ of the time. Each digit must have a peak current four times its average current to achieve the same brightness. The MM74C911 must supply about 32 mA per segment, and the MM74C912/MM74C917 would have to supply a current six times the average current or about 48 mA.

The maximum digit driver current is the maximum number of "on" segments multiplied by the segment current. For the MM74C911 design, the digit current is ~260 mA, and is ~380 mA for the MM74C912/MM74C917. Using this digit current value, the digit driver can be selected. *Figure 7* shows possible digit driver ICs, but discrete transistors or Darlingtons may also be used, and may be desirable in some higher current applications. It is also important to keep in mind that the output voltage of the driver at the designed current, as this voltage can affect the display controllers current drive. For most designs, an output voltage of < 2V is reasonable.

Once the digit driver has been chosen and the output voltage at the desired current is known, the segment resistor, R_{SEG} can be calculated using:

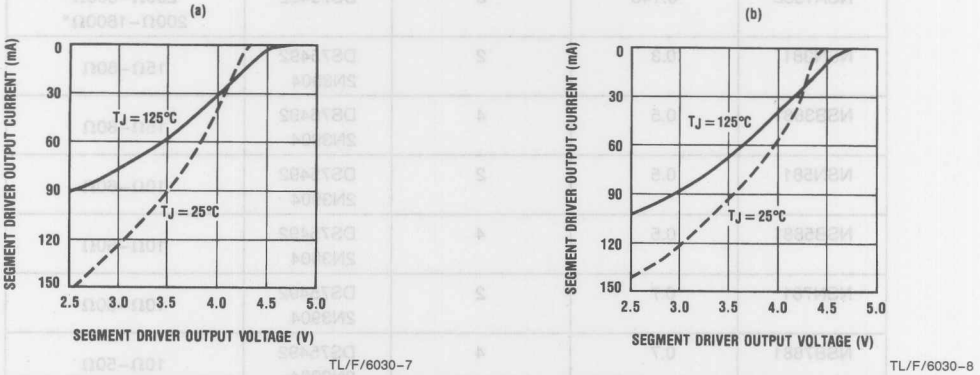
$$R_{SEG} = \frac{V_{SEG} - V_{LED} - V_{DO}}{I_{SEG}}$$

where V_{LED} is the voltage across the LED, 1.8V; V_{DO} is the digit driver output voltage at the chosen current; I_{SEG} is the peak segment current; and V_{SEG} is the MM74C911 or MM74C912 segment driver output voltage at the peak segment current, which can be determined from the curves in *Figure 8*.

In most cases, R_{SEG} can be more quickly determined from *Figure 9* which plots R_{SEG} vs. average segment current. These curves are plotted for various digit driver output voltages using current values from *Figure 8*. Thus, for the above example, if a DS75492 driver I.C. is used with the MM74C911 to interface to the NSB781 LEDs $R_{SEG} = 38\Omega$ assuming the drivers output voltage is 1.0V. Note that *Figure 7* tabulates minimum output drive where the above V_{DO} is an approximation of the DS75492s typical V_{DO} at 260 mA.

Part Number	Driver Type	Number of Drivers	Minimum Output Drive
DS75492	Darlington Driver	6	250 mA @ 1.5V
DS75494	Multiple Transistor Driver	6	150 mA @ 0.35V
DS8646	Transistor Driver	6	84 mA @ 0.55V
DS8658	Transistor Driver	4	84 mA @ 0.55V
DS8870	Darlington Driver	6	350 mA @ 1.4V
DS8871/2	Transistor Driver	8/9	40 mA @ 0.5V
DS8877	Transistor Driver	6	35 mA @ 0.5V
DS8920	Transistor Driver	9	40 mA @ 0.5V
DS8963	Darlington Driver	8	500 mA @ 1.5V
DS8978	Transistor Driver	9	100 mA @ 0.7V
DS8692	Transistor Driver	8	350 mA @ 1.0V

FIGURE 7. Typical LED Digit Drivers and Their Characteristics



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FIGURE 8. Typical Segment Driver Current vs. Output Voltage for (a) MM74C911 (b) MM74C912/MM74C917

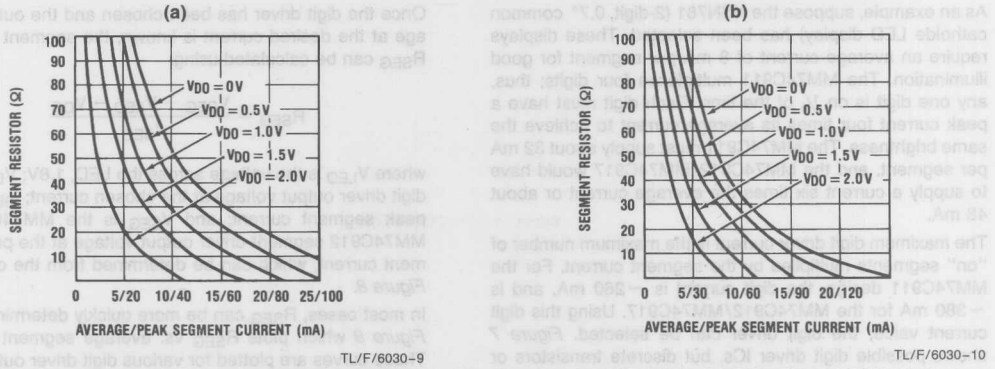


FIGURE 9. Average LED Segment Current vs. Segment Resistor for (a) MM74C911 (b) MM74C912/MM74C917

Figures 10 and *11* tabulate some typical segment resistor values for various National LED displays. (See Optoelectronics Databook for detailed specifications.) This table was compiled for a well lit room, but variation in ambient lighting may require some slight modification in the typical segment resistor values.

If a transistor digit driver is being used, it is sometimes desirable to use a base current limiting resistor between the controller's output and the transistor's base. This will help limit the power dissipation of the display controller in critical situations. The digit resistor, R_{DIG}, can be calculated using:

$$R_{DIG} = \frac{V_{DIG} - V_{DI}}{I_{DI}}$$

where V_{DI} is the digit driver input voltage, 0.7V for a transistor, I_{DI} is the desired digit driver current and V_{DIG} is the controller's digit output voltage for the chosen current which can be found from *Figure 12*.

When the MM74C911 is to be used as a "master" to drive another MM74C911 or other logic, the digit outputs must have a high output voltage of 3.0V to drive another MM74C911 or 3.5V to drive standard CMOS logic. The digit resistor should be $> 300\Omega$ for $V_{OH} \geq 3.0V$ and $R_{DIG} > 350$ for $V_{OH} \geq 3.5V$.

A final design consideration is power dissipation. When designing a low-power system where the total current is to be minimized, the total system power consumption is simply:

$$P_T \cong V_{CC}(I_{DO} + I_{DI})$$

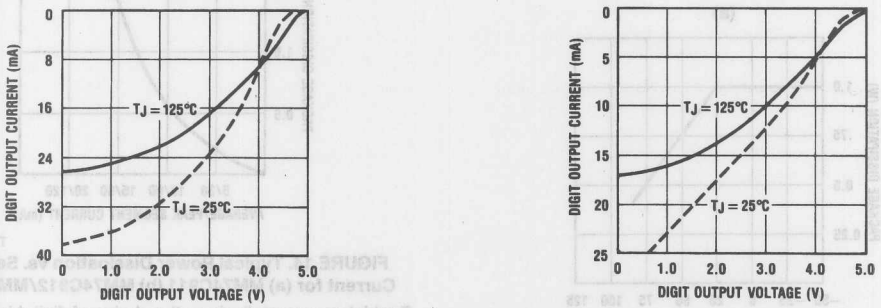
where I_{DO} is the maximum digit driver output current, V_{CC} is the power supply voltage, and I_{DI} is the digit driver input current.

Display			Driver	Typical Range of Segment Resistors
Part No.	Height (In.)	No. of Digits		
NSA1298	0.110	9	DS75492	300Ω–1000Ω 300Ω–2000Ω*
NSA1558	0.140	8	DS75492	200Ω–800Ω 200Ω–1800Ω*
NSN381	0.3	2	DS75492 2N3904	15Ω–80Ω
NSB3881	0.5	4	DS75492 2N3904	15Ω–80Ω
NSN581	0.5	2	DS75492 2N3904	10Ω–60Ω
NSB5881	0.5	4	DS75492 2N3904	10Ω–60Ω
NSN781	0.7	2	DS75492 2N3904	10Ω–50Ω
NSB7881	0.7	4	DS75492 2N3904	10Ω–50Ω

FIGURE 10. MM74C911 Segment Resistor Values for Various Displays (V_{CC} = 5V)
(*Using Red LED Filter over Display)

Display			Driver	Typical Range of Segment Resistors
Part No.	Height (In.)	No. of Digits		
NSA1298	0.110	9	DS75494	200Ω–800Ω 300Ω–1500Ω*
NSA1558	0.140	8	DS75494	150Ω–700Ω 150Ω–1000Ω*
NSN381	0.3	2	DS75492	5Ω–50Ω
NSB581	0.5	2	DS75492	5Ω–50Ω
NS5931	0.5	6	DS75492 2N3904	5Ω–40Ω
NSN781	0.7	2	DS75492 2N3904	5Ω–30Ω

FIGURE 11. MM74C912/MM74C917 Segment Resistor for Average Intensity for Various Displays (*Using Red LED Filter over Display)



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FIGURE 12. Typical Digit Driver Current vs. Output Voltage for (a) MM74C911 (b) MM74C912/MM74C917

When a circuit design employs large segment currents, the maximum dissipation should be calculated to ensure that the power consumption of the controller or digit driver is within the maximum limits. The display controller power dissipation:

$$P_C = S(I_{SEG})(V_{CC} - V_{SEG})$$

where I_{SEG} and V_{SEG} are the peak segment current and segment voltage, as previously determined; and S is the maximum number of segments lit per digit. The maximum package dissipation for the controllers vs. temperature is shown in *Figure 13*.

To gain an understanding of how segment current affects the controllers power dissipation, *Figure 14* plots average and peak LED segment current vs. package dissipation for both the MM74C911 and the MM74C912/MM74C917. These typical curves are plotted using the typical segment driver output currents and voltages from *Figure 8*.

As the digit driver output voltage V_{DO} becomes larger, the driver dissipates more power, thus the designer should also ensure that the driver's dissipation is not exceeded. Generally, the standard digit driver IC will dissipate around ½W. (See specific data sheets.) Driver power dissipation can be calculated by:

$$P_D = (V_{DO})(I_{DIG})$$

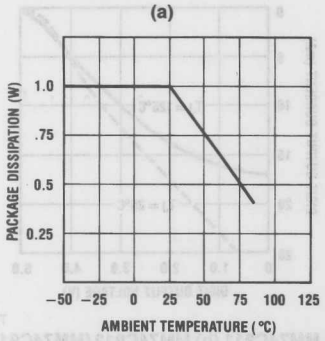
where V_{DO} and I_{DIG} are the digit driver output voltage and current. In a standard digit driver, one output will be active

all the time, but if discrete transistors are used, each transistor is turned on 25% of the tiime. The average power dissipation for each discrete transistor digit driver is ¼ of the above equation.

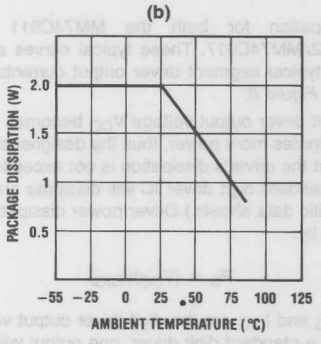
B. Common Anode LED Display

Although connecting the MM74C911/MM74C912/MM74C917 to common anode displays is somewhat more difficult than to common cathode displays, it can be done. These controllers still provide all the necessary timing signals, but some extra buffering must be added to ensure the correct logic levels and drive capability.

To drive common anode displays, the display controller's segment outputs must be inverted and the digit outputs must be current buffered. *Figure 15* shows a simple circuit to interface to most common anode displays. An 8-digit calculator digit driver IC, DS8871, is used to drive the display segments. Segment resistors on the controller's segment outputs are not necessary but may be necessary on the outputs of the DS8871 driver.

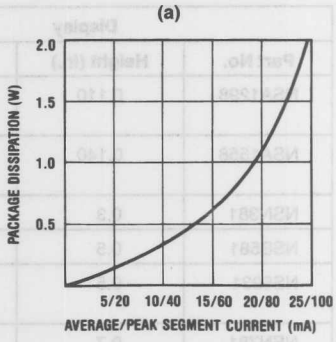


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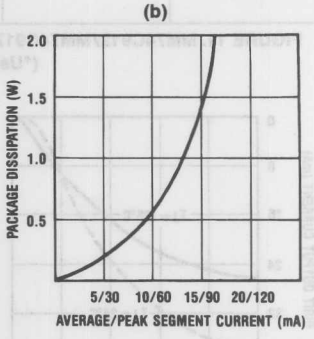


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FIGURE 13. MM74C911/MM74C912/MM74C917 Maximum Power Dissipation for (a) Plastic "N" Package (b) Ceramic "J" Package (Note $T_{J(MAX)}$ = 125°C Maximum Junction Temperature)



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TL/F/6030–16

FIGURE 14. Typical Power Dissipation vs. Segment Current for (a) MM74C911 (b) MM74C912/MM74C917

For higher current displays, the choice of digit driver transistor is important as the digit current will depend on how high the digit driver output of the display controller can pull up due to the emitter follower configuration. For good display brightness, a high gain medium power transistor should be used.

C. Vacuum Fluorescent (VF) Displays

The MM74C911/MM74C912/MM74C917 are not directly capable of driving VF displays, but serve as a major functional block to ease driving 4- or 6-digit displays. The controllers provide the multiplex timing for this display, but the segment and digit outputs must be level shifted, and a filament voltage must be applied.

In *Figure 16*, a DS8654 or similar device is used to translate the segment and digit voltages to 30V to drive the segment plates and digit grids. The AC filament voltage is derived from a separate low-voltage transformer which is biased by a zener. Since there is no pull-down in the DS8654, pull-down resistors must be added. The exact anode and cathode voltages and the bias zener will depend on the display used, but the basic circuit is the same.

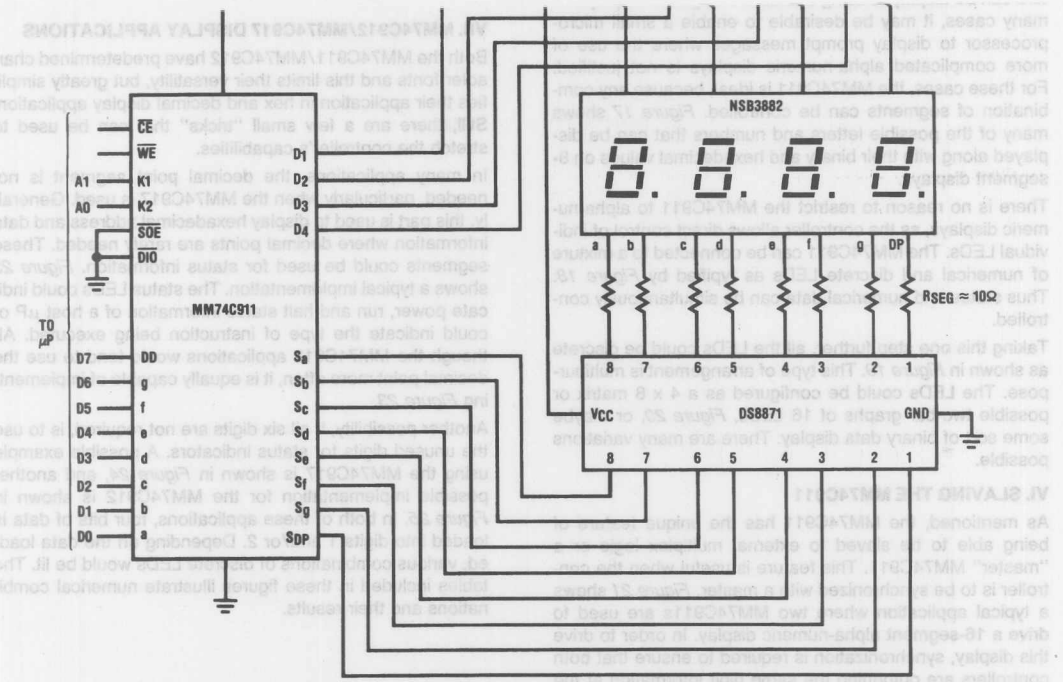


FIGURE 15. MM74C911 to Common Anode LED Interface Using 9 Digit Driver

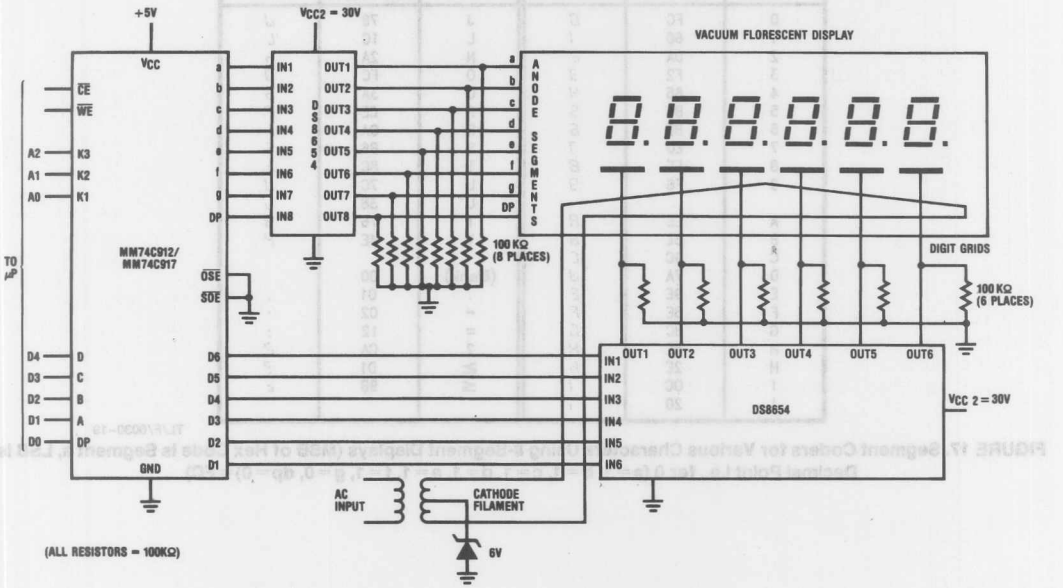


FIGURE 16. MM74C912/MM74C917 to Vacuum Fluorescent Display Interface

V. MM74C911 DISPLAY APPLICATIONS

Of the three CMOS display controllers, the MM74C911 is the simplest, but also the most versatile. Since the character font is not predetermined, many non-numerical characters can be displayed using standard 8-segment displays. In many cases, it may be desirable to enable a small microprocessor to display prompt messages where the use of more complicated alpha-numeric displays is not justified. For these cases, the MM74C911 is ideal, because any combination of segments can be controlled. *Figure 17* shows many of the possible letters and numbers that can be displayed along with their binary and hexadecimal values on 8-segment displays.

There is no reason to restrict the MM74C911 to alpha-numeric displays, as the controller allows direct control of individual LEDs. The MM74C911 can be connected to a mixture of numerical and discrete LEDs as typified by *Figure 18*. Thus status and numerical data can be simultaneously controlled.

Taking this one step further, all the LEDs could be discrete as shown in *Figure 19*. This type of arrangement is multipurpose. The LEDs could be configured as a 4 x 8 matrix or possible two-bar graphs of 16 LEDs, *Figure 20*, or maybe some sort of binary data display. There are many variations possible.

VI. SLAVING THE MM74C911

As mentioned, the MM74C911 has the unique feature of being able to be slaved to external multiplex logic or a "master" MM74C911. This feature is useful when the controller is to be synchronized with a master. *Figure 21* shows a typical application where two MM74C911s are used to drive a 16-segment alpha-numeric display. In order to drive this display, synchronization is required to ensure that both controllers are outputting the same digit information at the same time.

A more subtle advantage to slaving MM74C911s occurs when trying to use multi-controllers to drive more digits. This case, illustrated in *Figure 22*, allows fewer, more powerful digit drivers to be used. This can be advantageous when using smaller displays that require little power to begin with.

VII. MM74C912/MM74C917 DISPLAY APPLICATIONS

Both the MM74C911/MM74C912 have predetermined character fonts and this limits their versatility, but greatly simplifies their application in hex and decimal display application. Still, there are a few small "tricks" that can be used to stretch the controller's capabilities.

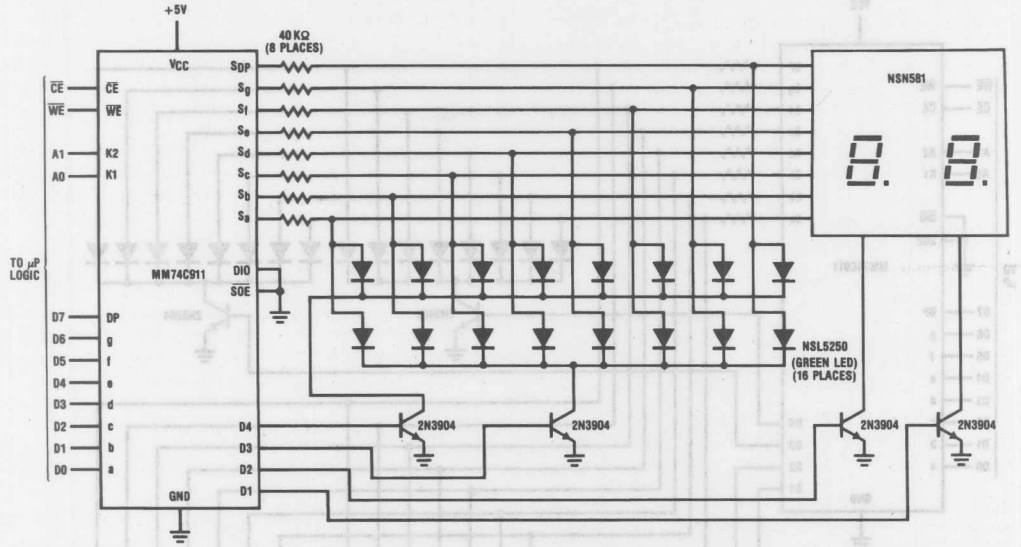
In many applications, the decimal point segment is not needed, particularly when the MM74C917 is used. Generally, this part is used to display hexadecimal address and data information where decimal points are rarely needed. These segments could be used for status information. *Figure 23* shows a typical implementation. The status LEDs could indicate power, run and halt status information of a host μP or could indicate the type of instruction being executed. Although the MM74C912 applications would tend to use the decimal point more often, it is equally capable of implementing *Figure 23*.

Another possibility, if all six digits are not required, is to use the unused digits for status indicators. A possible example using the MM74C917 is shown in *Figure 24*, and another possible implementation for the MM74C912 is shown in *Figure 25*. In both of these applications, four bits of data is loaded into digits 1 and/or 2. Depending on the data loaded, various combinations of discrete LEDs would be lit. The tables included in these figures illustrate numerical combinations and their results.

CHARACTER	HEX CODE FOR 74C911	DISPLAY	CHARACTER	HEX CODE FOR 74C911	DISPLAY
0	FC	0	J	78	J
1	60	1	L	1C	L
2	DA	2	N	2A	n
3	F2	3	O	FC	O
4	66	4	o	3A	o
5	B6	5	P	CE	P
6	BE	6	R	OA	r
7	EO	7	S	B6	S
8	FF	8	T	8C	t
9	F6	9	U	7C	U
			U	38	u
A	EE	A	Y	76	y
B	3E	b	Y	4E	Y
C	9C	C			
D	7A	d	(Blank)	00	
E	9E	E	.	01	.
F	8E	F	-	02	-
G	BC	G	=	12	=
H	6E	H	?	CA	?
H	2E	h	≧	D1	≥
I	OC	I	≦	9B	≤
I	20	i			

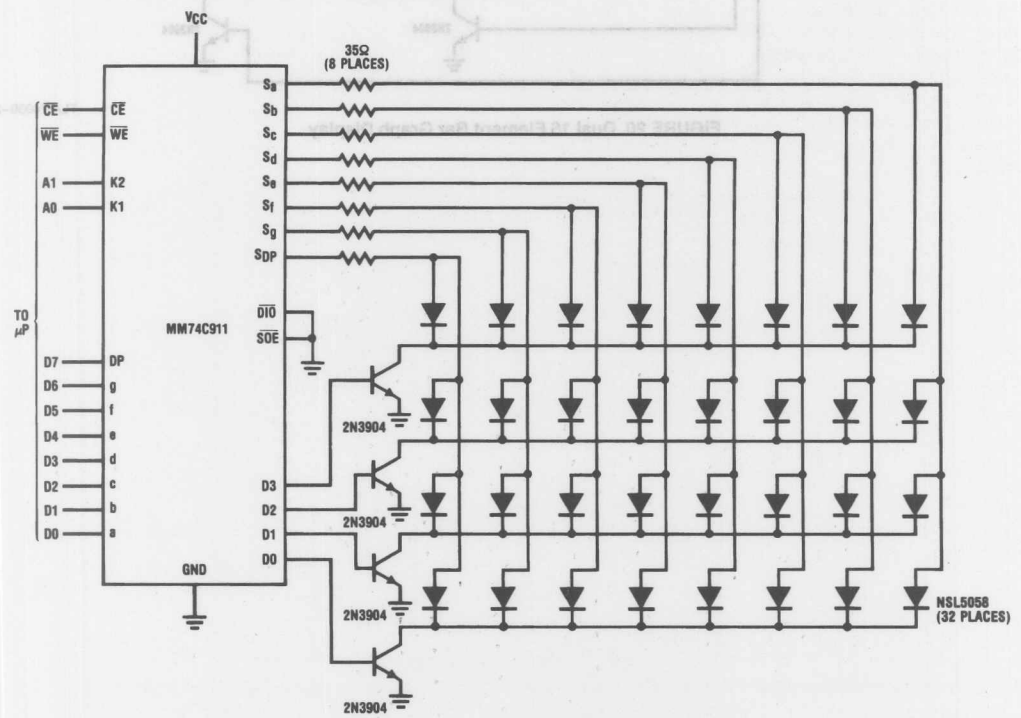
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FIGURE 17. Segment Coders for Various Characters Using 8-Segment Displays (MSB of Hex Code is Segment a, LSB is Decimal Point i.e., for 0 (a = 1, b = 1, c = 1, d = 1, e = 1, f = 1, g = 0, dp = 0) = FC)



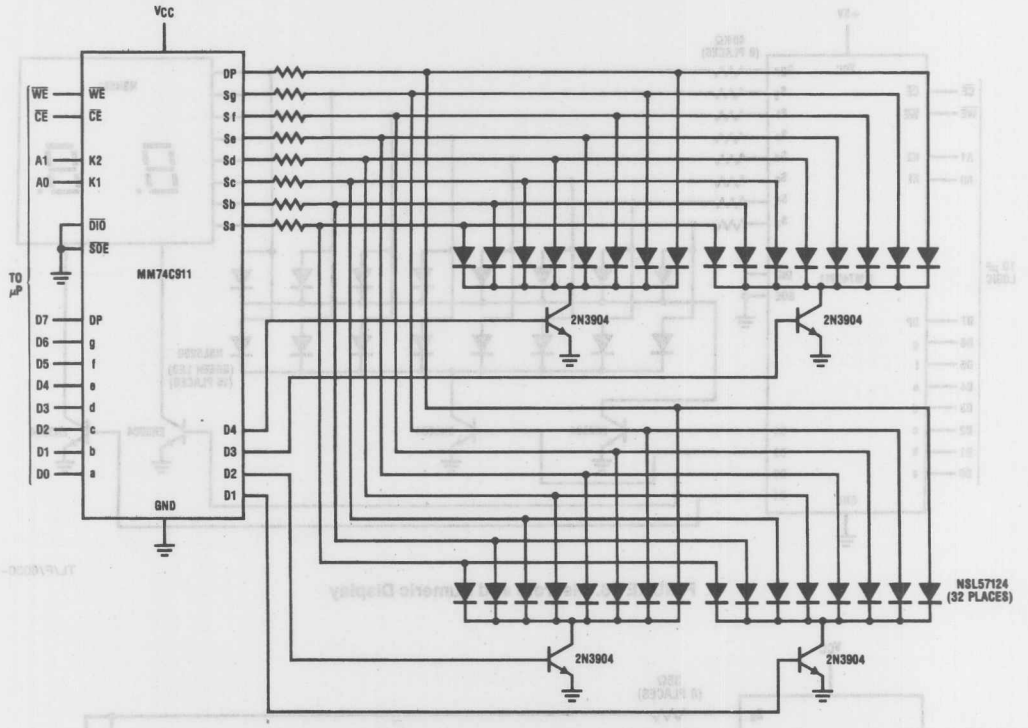
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FIGURE 18. Discrete and Numeric Display



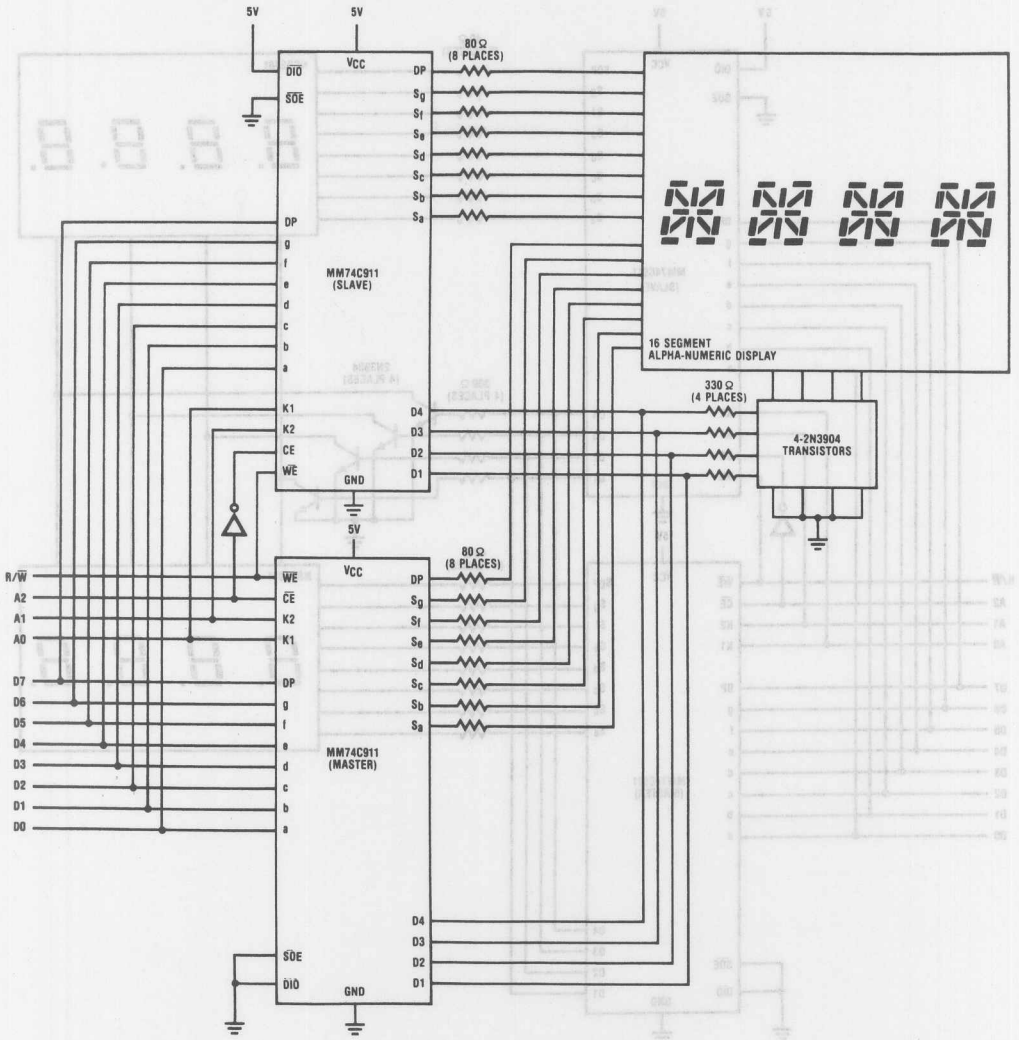
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FIGURE 19. Discrete LED Matrix Display



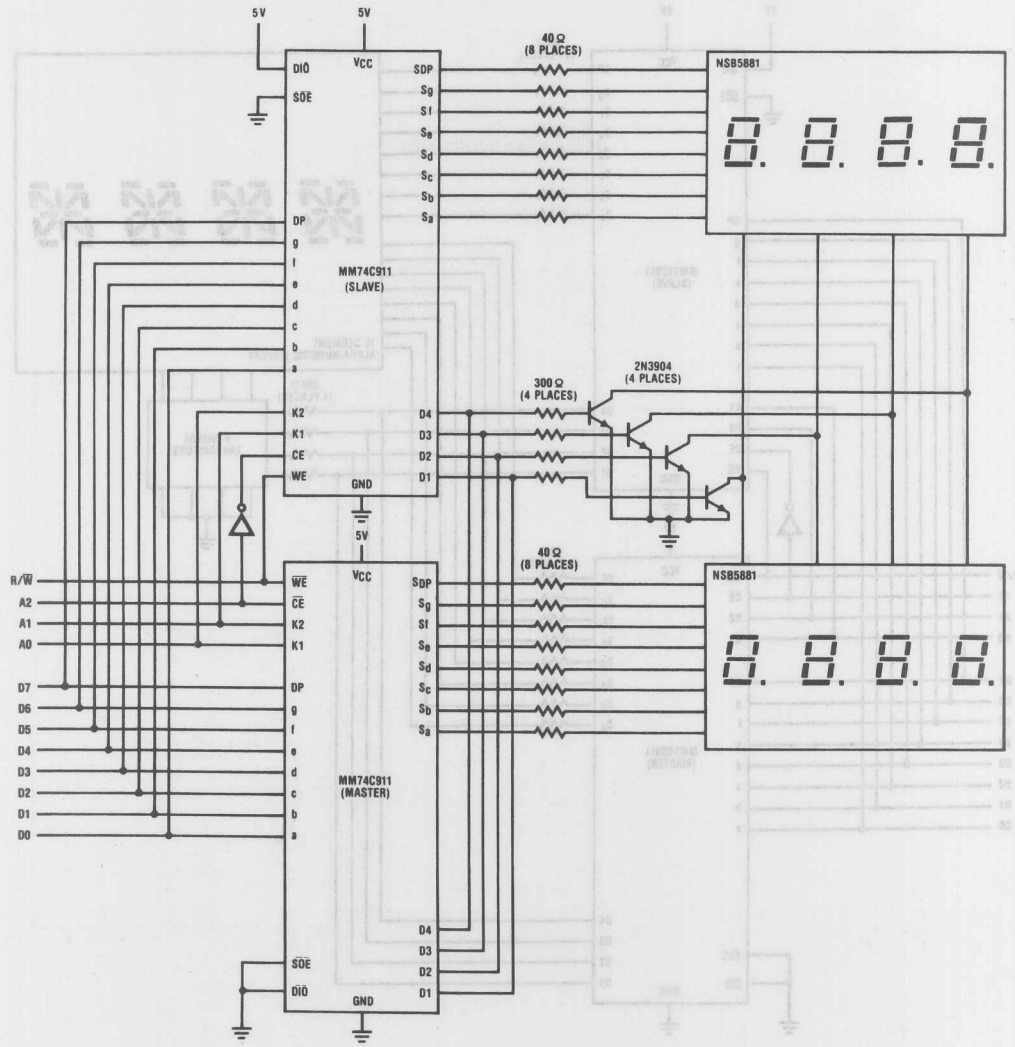
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FIGURE 20. Dual 16 Element Bar Graph Display



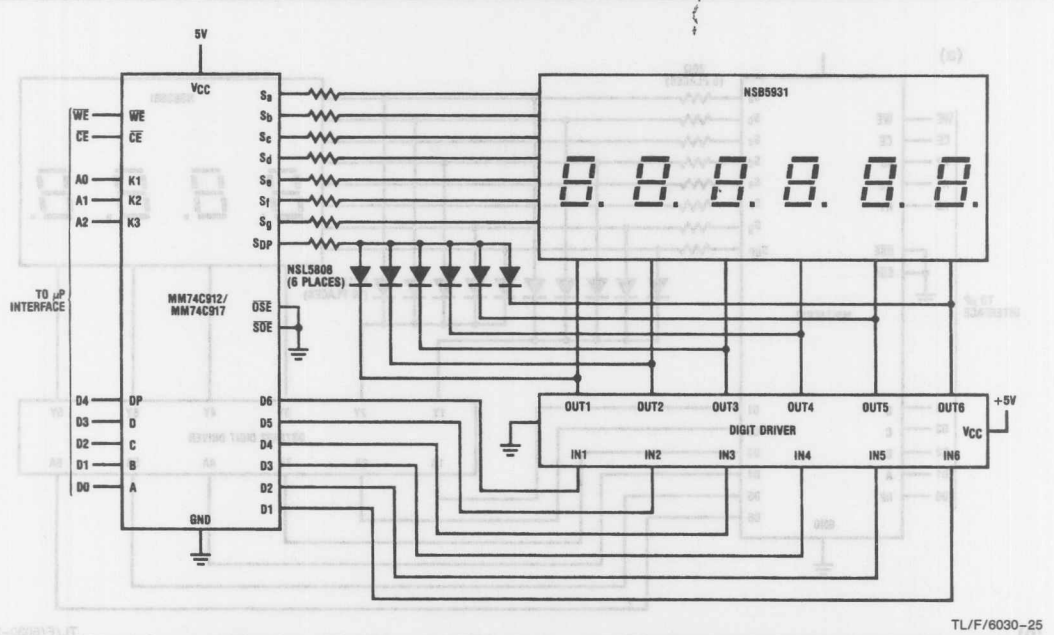
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FIGURE 21. Interfacing to Alphanumeric Displays



TL/F/6030–24

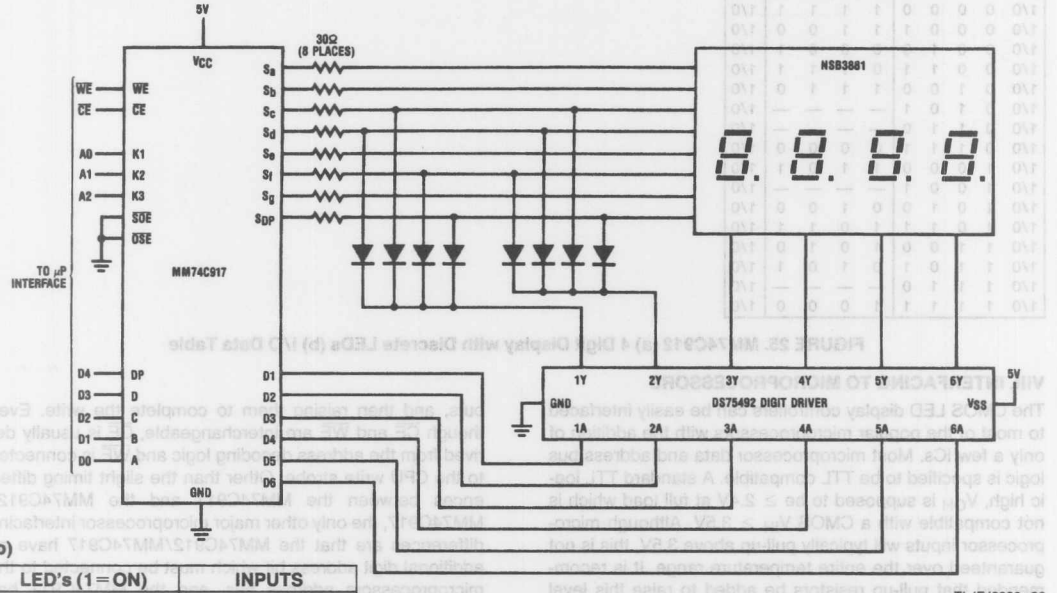
FIGURE 22. Multi-Digit Displays



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FIGURE 23. 7-Segment Displays with 6-Discrete LED Indicators for MM74C912/MM74C917 Using "DP" Segment

(a)

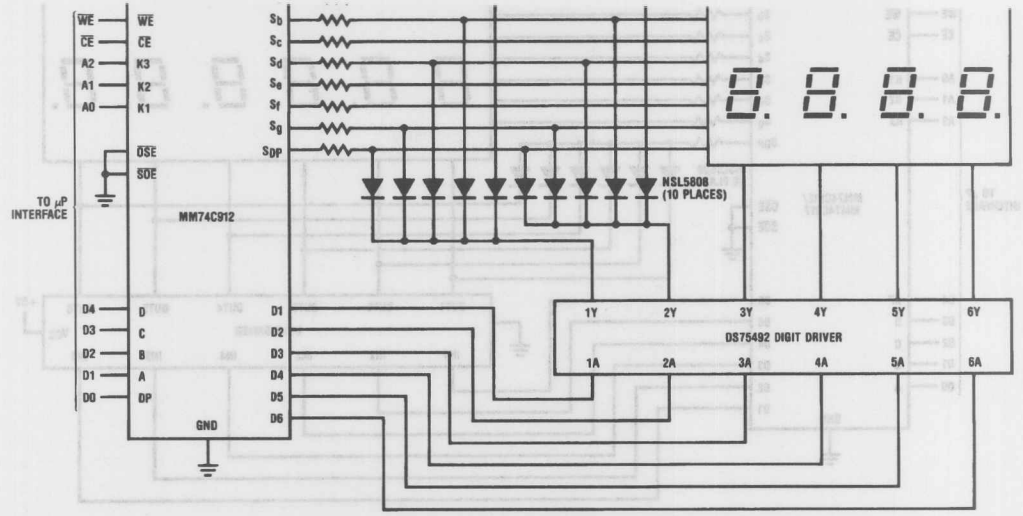


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(b)

LED's (1 = ON)				INPUTS				
DP	f	d	c	A	B	C	D	DP
1/0	0	0	0	—	—	—	—	1/0
1/0	0	0	1	0	0	0	1	1/0
1/0	0	1	0	0	0	1	0	1/0
1/0	0	1	1	0	0	1	1	1/0
1/0	1	0	0	1	1	1	1	1/0
1/0	1	0	1	0	1	0	0	1/0
1/0	1	1	0	1	1	0	0	1/0
1/0	1	1	1	1	0	0	0	1/0

FIGURE 24. MM74C917 (a) Display with 8 Discrete LED's (b) Inputs for LED Output Table



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(b)

"ON" SEGMENTS					BCD INPUTS				
DP	G	D	B	A	D	C	B	A	DP
1/0	0	0	0	0	1	1	1	1	1/0
1/0	0	0	0	1	1	1	0	0	1/0
1/0	0	0	1	0	0	0	0	1	1/0
1/0	0	0	1	1	0	1	1	1	1/0
1/0	0	1	0	0	1	1	1	0	1/0
1/0	0	1	0	1	—	—	—	—	1/0
1/0	0	1	1	0	—	—	—	—	1/0
1/0	0	1	1	1	0	0	0	0	1/0
1/0	1	0	0	0	1	1	0	1	1/0
1/0	1	0	0	1	—	—	—	—	1/0
1/0	1	0	1	0	0	1	0	0	1/0
1/0	1	0	1	1	1	0	1	1	1/0
1/0	1	1	0	0	1	0	1	0	1/0
1/0	1	1	0	1	0	1	0	1	1/0
1/0	1	1	1	0	—	—	—	—	1/0
1/0	1	1	1	1	1	0	0	0	1/0

FIGURE 25. MM74C912 (a) 4 Digit Display with Discrete LEDs (b) I/O Data Table

VIII. INTERFACING TO MICROPROCESSORS

The CMOS LED display controllers can be easily interfaced to most of the popular microprocessors with the addition of only a few ICs. Most microprocessor data and address bus logic is specified to be TTL compatible. A standard TTL logic high, V_{OH} is supposed to be $\geq$ 2.4V at full load which is not compatible with a CMOS $V_{IH} \geq$ 3.5V. Although microprocessor inputs will typically pull-up above 3.5V, this is not guaranteed over the entire temperature range. It is recommended that pull-up resistors be added to raise this level above 3.5V. Under most conditions, a 5k–10k resistor should suffice.

The write timing of the display controllers is illustated in *Figure 26*. The minimum write access time is 430 ns for the MM74C912/MM74C917 and 450 ns for the MM74C911. A write to the controller is accomplished by placing the desired data on the data inputs, lowering the $\overline{CE}$ and $\overline{WE}$ inputs, and then raising them to complete the write. Even though $\overline{CE}$ and $\overline{WE}$ are interchangeable, $\overline{CE}$ is usually derived from the address decoding logic and $\overline{WE}$ is connected to the CPU write strobe. Other than the slight timing differences between the MM74C911 and the MM74C912/MM74C917, the only other major microprocessor interfacing differences are that the MM74C912/MM74C917 have an additional digit address bit which must be connected to the microprocessors address bus, and the MM74C911 has eight data inputs whereas the MM74C912/MM74C917 have only five.

A. Interfacing to the INS8080

These controllers can be connected to the INS8080/INS8224/INS8238 CPU group with no external logic if no more than a minimal amount of address decoding is required. Since the INS8080 has a separate memory and I/O

port address spaces, one of the I/O port address bits could be directly connected to the $\overline{CE}$ input. *Figure 27* illustrates this using an MM74C911. Whenever an OUT instruction is executed causing the $\overline{I/OW}$ (INS8080 write enable signal) to go low and the address is such that A7 is low, A0 A1 will select the digit to be written. If more decoding is required, some external gating logic may be added to the $\overline{CE}$ input.

The MM74C912/MM74C917 would be interfaced by connecting the A, B, C, D and DP to bit D0–D4 of the data bus and connecting K1–K3 to A_0–A_2. Writing data to these controllers would be the same as writing to the MM74C911.

B. Interfacing to the Z80®

To connect these display controllers to the Z80 microprocessor, only a minor modification to the INS8080 need be made. The Z80 control signals are slightly different from the INS8080. Instead of the INS8080 I/O write strobe, the Z80 has an I/O request line ($\overline{IOREQ}$), which goes low to indicate an I/O port is to be accessed, and a write ($\overline{WR}$) strobe which indicates that a memory or I/O write is to be done. By OR-ing, these together an equivalent $\overline{I/OW}$ signal is generated as shown in *Figure 28*.

C. Interfacing to the NSC800™

The NSC800 has very different timing because the lower eight address bits and the data bus are multiplexed. But when connecting the display controllers as I/O ports, the interface is only slightly different from the INS8080 design. When an I/O instruction is executed, the port address that appears on A0–A7 is duplicated on A8–A15, and this address can be used directly. The controller $\overline{WE}$ input must be decoded from a $\overline{WR}$ (write enable) and IO/$\overline{M}$ (I/O or memory enable) as shown in *Figure 29*. Note that since the NSC800 is a CMOS microprocessor, no pull-up resistors are needed.

Figure 29 uses address bit A15 which is equivalent to bit A7 on the previous examples. As with the previous examples, if more address decoding is required, either gates or decoders could be connected to the $\overline{CE}$ input.

D. Interfacing to the 6800

When using the INS8080, Z80, or NSC800, these processors have separate I/O and memory address spaces. This usually allows simpler interfaces to be designed. The 6800 has no separate I/O addressing so I/O ports are usually mapped into a small block of memory. This requires more address decoding to ensure that memory and I/O don't overlap.

Figure 30 shows a DM8131 6-bit address bus comparator whose B_n inputs are a combination of A15–A12 address bits, the Φ_2 (6800 system clock) and the VMA (Valid Memory Access) control signal. When these inputs equal the corresponding T_n inputs, the output goes low. The 6800 R/$\overline{W}$ signal is connected to the $\overline{WE}$.

E. Interfacing to the INS8060/INS8070

Like the 6800, the INS8060/8070 series of microprocessors don't have any separate I/O addressing, so the MM74C911/MM74C912/MM74C917 must be memory addressed, but unlike the 6800 both the INS8070 series and the INS8060 have separate read/write strobes, which can simplify interfacing the display controllers. *Figure 31* illustrates a typical INS8060 interface. The $\overline{NWDS}$ (write enable) is directly connected to the MM74C912s $\overline{WE}$ input and the DM8131 provides the address decoding for the controller. The INS8060 has only 12 address bits (unless using paged addressing) so bits A_6–A_{11} are decoded by the comparator.

The INS8070 series microprocessor has the identical $\overline{NWDS}$ signal but has 16 address bits. Thus *Figure 31* would connect the A10–A15 address bits to the DM8131.

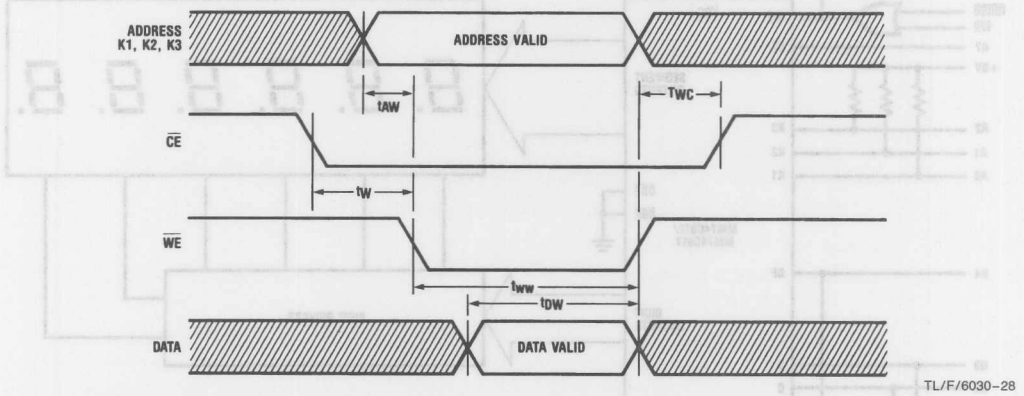
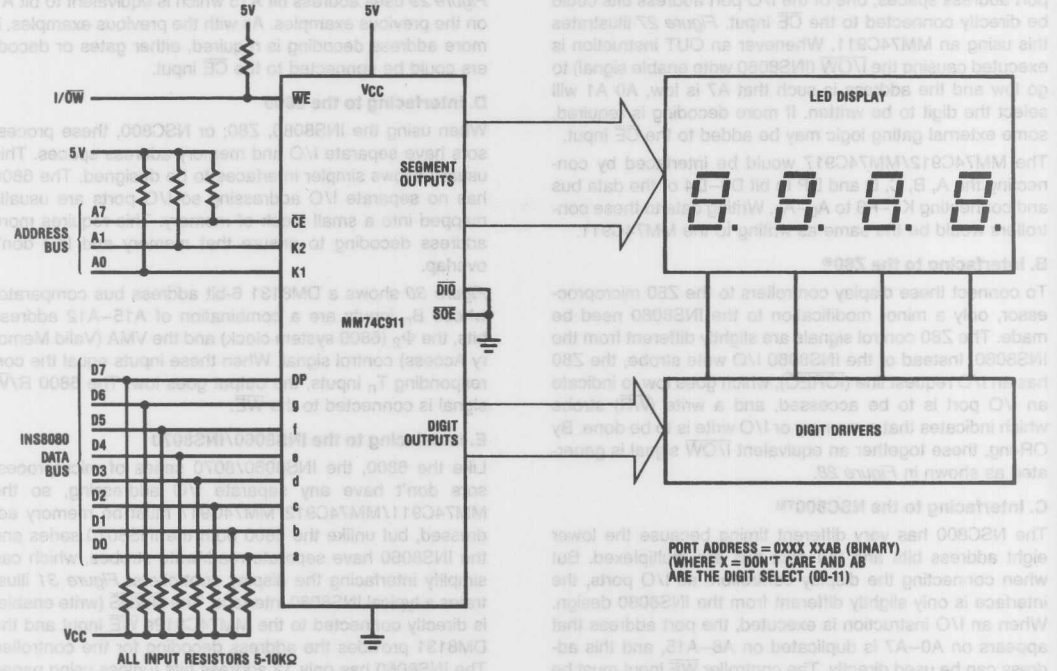
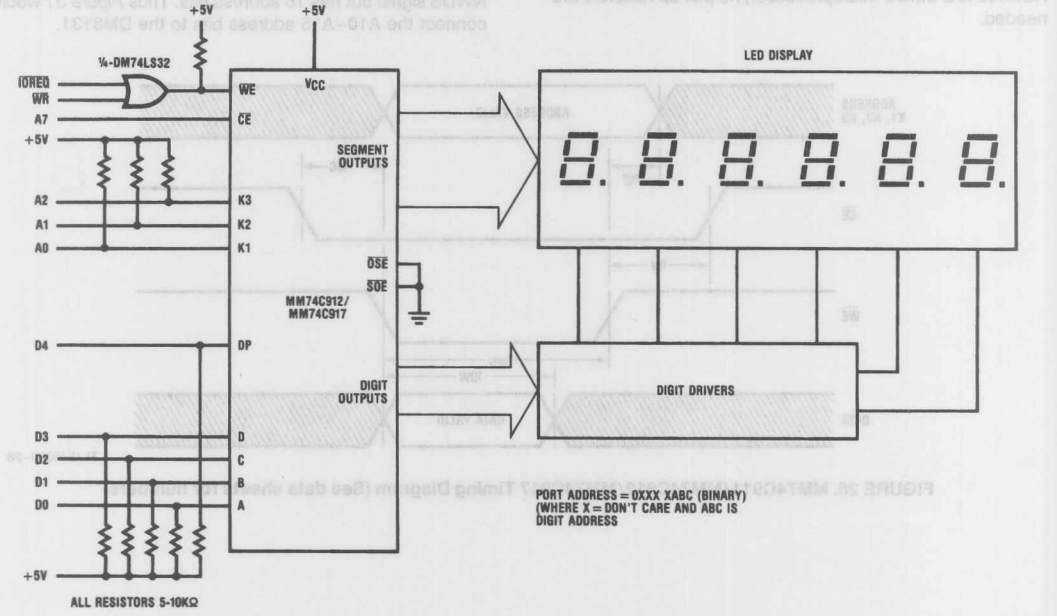


FIGURE 26. MM74C911/MM74C912/MM74C917 Timing Diagram (See data sheets for numbers)



TL/F/6030–29

FIGURE 27. INS8080/INS8224/INS8238 Interface to MM74C911



TL/F/6030–30

FIGURE 28. Z80 Interface to MM74C912/MM74C917

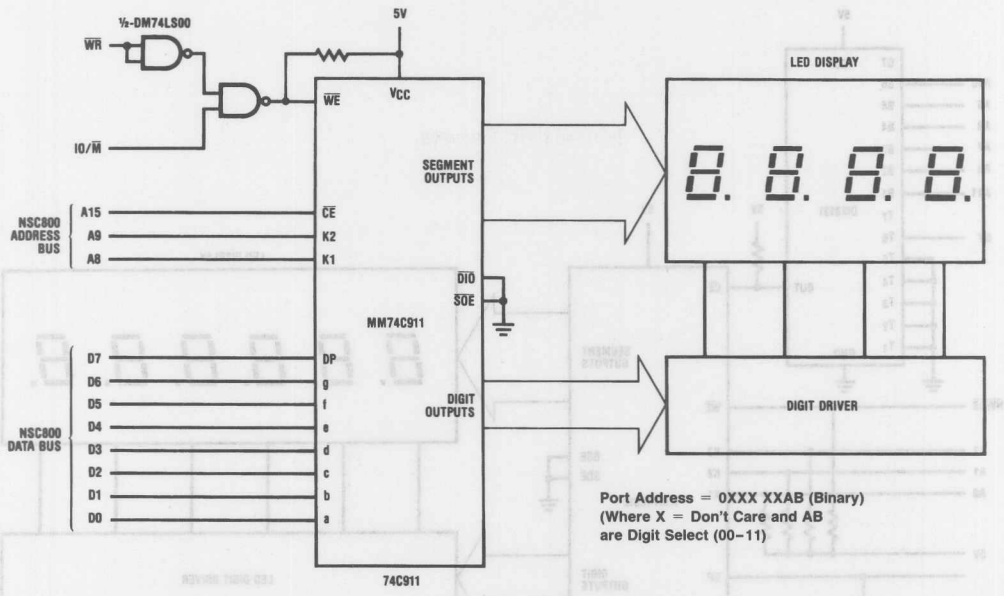


FIGURE 29. NSC800 Interface to MM74C911

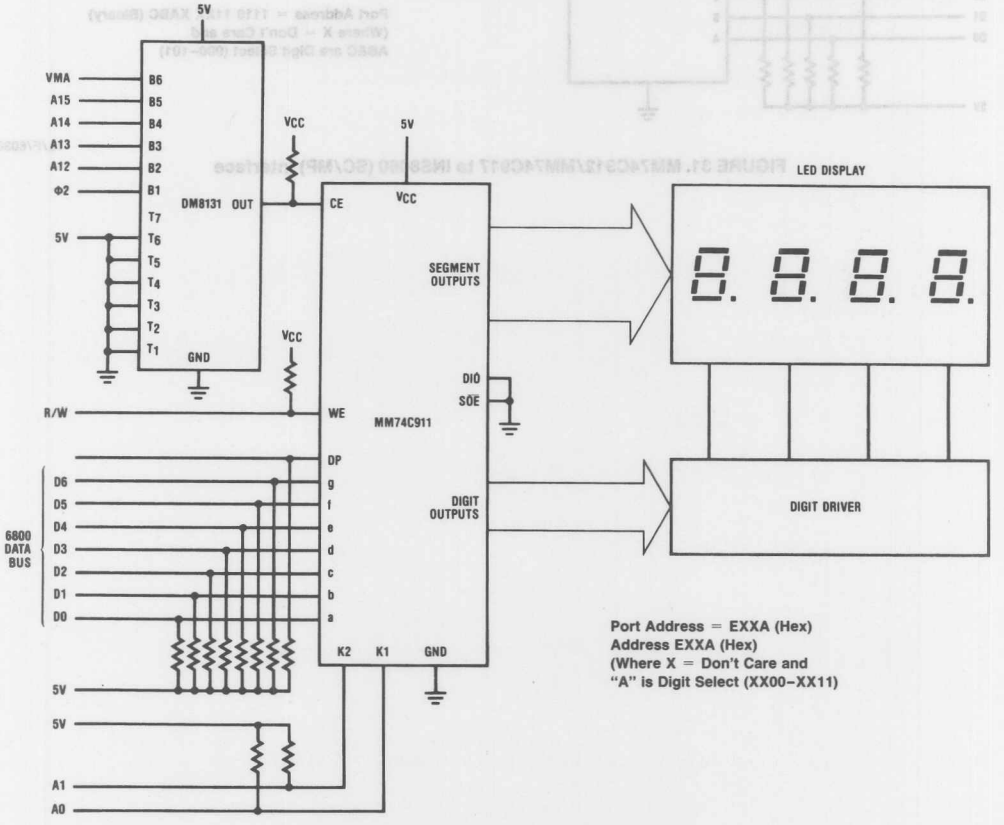
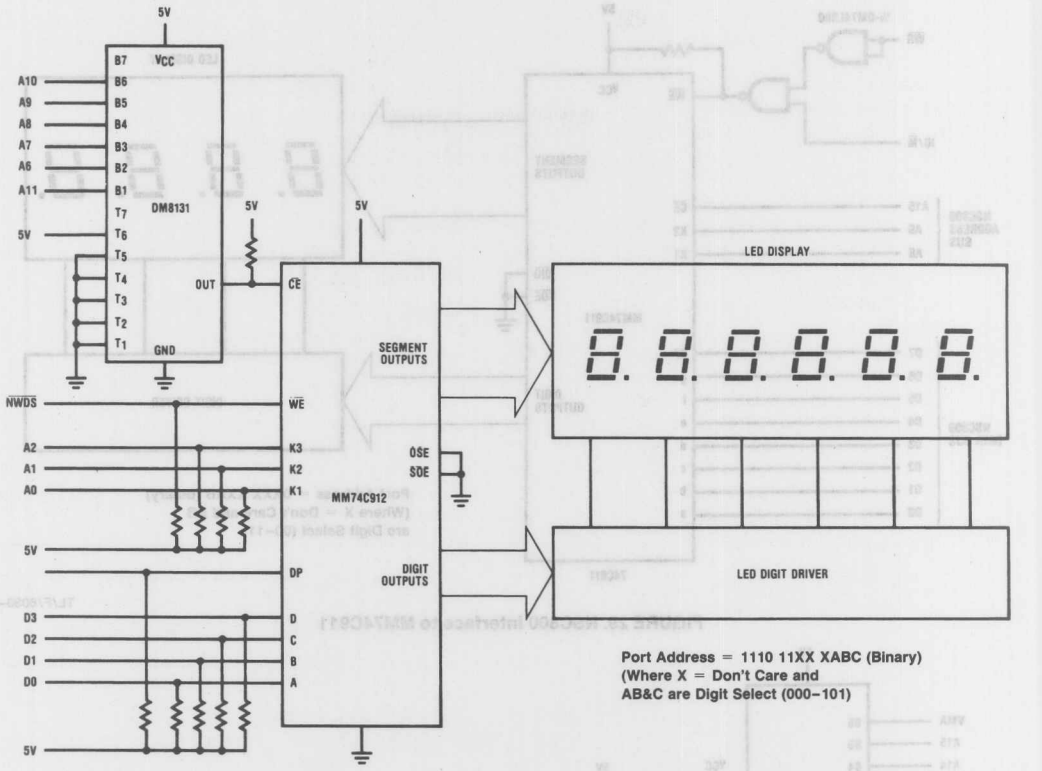


FIGURE 30. MM74C911 to 6800 Microprocessor Interface



TL/F/6030–33

FIGURE 31. MM74C912/MM74C917 to INS8060 (SC/MP) Interface

F. Multiple Display Controllers

In systems where multiple display controllers are to be used, the simple addressing schemes of the previous examples may prove to be too costly in I/O capabilities, so some extra decoding is necessary to derive the $\overline{CE}$ signals. A typical method uses a 2–4 line decoder or a 3–8 line decoder. Where the total time from a stable address to the write pulse goes inactive is $\geq 1\ \mu s$, a CMOS decoder such as the MM74C42 or MM74C154 can be used, but if faster accessing is required, their LS equivalents should be employed.

Figure 32 shows a typical implementation of a 16-digit display using half of a DM74LS139 decoder to provide the $\overline{CE}$ signals for each controller.

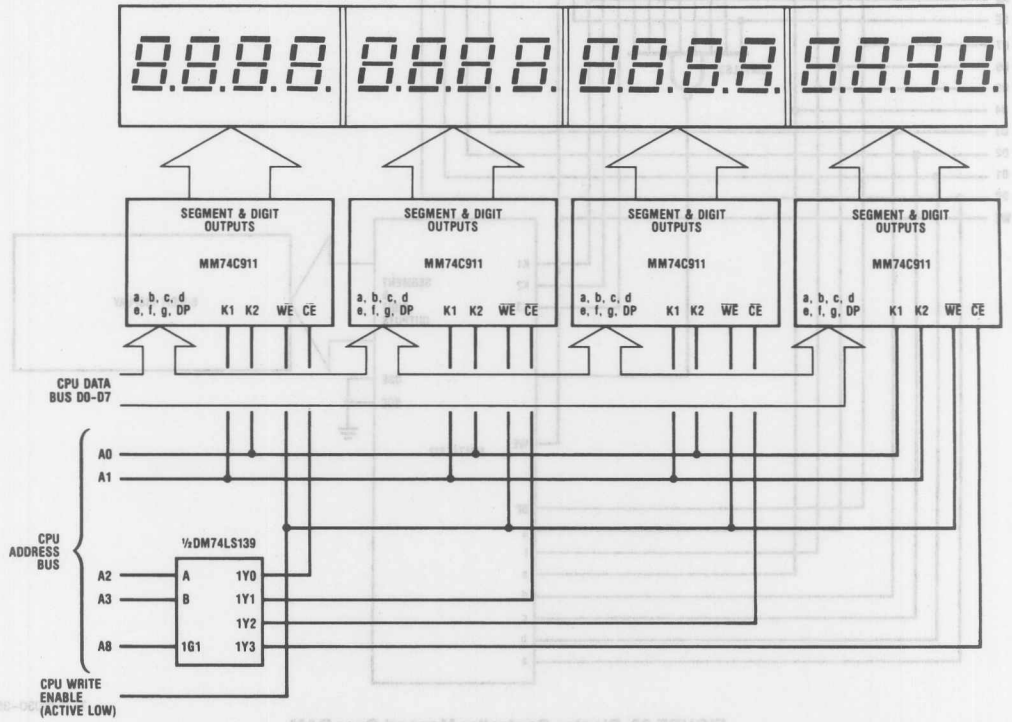
G. Making the MM74C911/MM74C912/MM74C917 Look Like RAM

So far, the discussion of addressing the controllers has been to separate the devices from memory, but there are certain advantages to not doing this. In many instances, microprocessor software requirements are such that data outputted to the controller also must be remembered by the microprocessor for later use. Since data cannot be read from the display controllers, the processor must also write the data in a spare register or a memory location. This extra writing and "bookkeeping" software can be eliminated by addressing the MM74C911/MM74C912/MM74C917 over existing RAM. When data is written to the controller, it could also be stored in RAM simultaneously and can be read later by the CPU.

Figure 31 shows a simple example of this using an MM74C912 controller and two MM2114 1k x 4 memory chips. A DM74LS30 is used to detect when the last eight bytes of this memory is being accessed and enables the controller display. Thus, the last eight bytes of the RAM contains a duplicate copy of what the display controller is displaying.

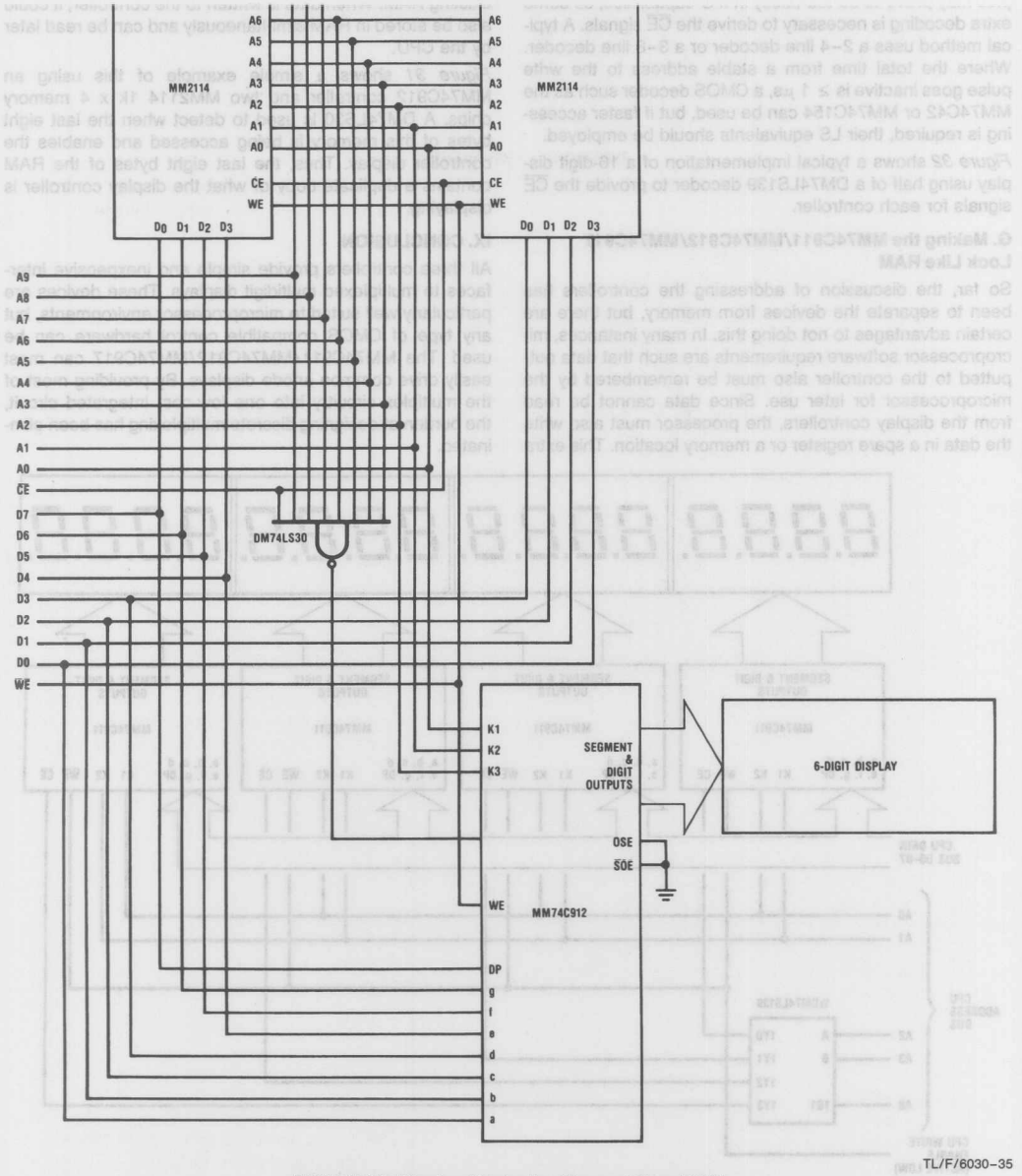
IX. CONCLUSION

All three controllers provide simple and inexpensive interfaces to multiplexed multidigit displays. These devices are particularly well suited to microprocessor environments, but any type of CMOS compatible control hardware can be used. The MM74C911/MM74C912/MM74C917 can most easily drive common anode displays. By providing most of the multiplex circuitry into one low-cost integrated circuit, the burden of designing discrete multiplexing has been eliminated.



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FIGURE 32. Multi-Digit Array



TL/F/6030–35

FIGURE 33. Display Controller Mapped Over RAM
(5 kΩ–10 kΩ Pull-Up Resistors may be needed on MM74C912 Inputs)

HC-MOS Power Dissipation

National Semiconductor
Application Note 303
Kenneth Karakotsios

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, high-speed CMOS draws five to seven orders of magnitude less power than the equivalent LSTTL function. When switching, the amount of power dissipated by both metal gate and high-speed silicon gate CMOS is directly proportional to the operating frequency of the device. This is because the higher the operating frequency, the more often the device is being switched. Since each transition requires power, power consumption increases with frequency.

First, one will find a description of the causes of power consumption in HC-CMOS and LSTTL applications. Next will follow a comparison of MM54HC/MM74HC to LSTTL power dissipation. Finally, the maximum ratings for power dissipation imposed by the device package will be discussed.

Quiescent Power Consumption

Ideally, when a CMOS integrated circuit is not switching, there should be no DC current paths from V_{CC} to ground, and the device should not draw any supply current at all. However, due to the inherent nature of semiconductors, a small amount of leakage current flows across all reverse-biased diode junctions on the integrated circuit. These leakages are caused by thermally-generated charge carriers in the diode area. As the temperature of the diode increases, so do the number of these unwanted charge carriers, hence leakage current increases.

Leakage current is specified for all CMOS devices as I_{CC}. This is the DC current that flows from V_{CC} to ground when all inputs are held at either V_{CC} or ground, and all outputs are open. This is known as the quiescent state.

For the MM54HC/MM74HC family, I_{CC} is specified at ambient temperatures (T_A) of 25°C, 85°C, and 125°C. There are three different specifications at each temperature, depending on the complexity of the device. The number of diode junctions grows with circuit complexity, thereby increasing the leakage current. The worst case I_{CC} specifications for the MM54HC/MM74HC family are summarized in Table I. In addition, it should be noted that the maximum I_{CC} current will decrease as the temperature goes below 25°C.

TABLE I. Supply Current (I_{CC}) for MM54HC/MM74HC Specified at $V_{CC}=6V$

T_A	Gate	Buffer	MSI	Unit
25°C	2.0	4.0	8.0	μA
85°C	20	40	80	μA
125°C	40	80	160	μA

To obtain the quiescent power consumption for any CMOS device, simply multiply I_{CC} by the supply voltage:

$$P_{DC}=I_{CC}V_{CC}$$

Sample calculations show that at room temperature the maximum power dissipation of gate, buffer, and MSI circuits at $V_{CC}=6V$ are 10 μW, 20 μW, and 40 μW, respectively.

Dynamic Power Consumption

Dynamic power consumption is basically the result of charging and discharging capacitances. It can be broken down into three fundamental components, which are:

1. Load capacitance transient dissipation
2. Internal capacitance transient dissipation
3. Current spiking during switching.

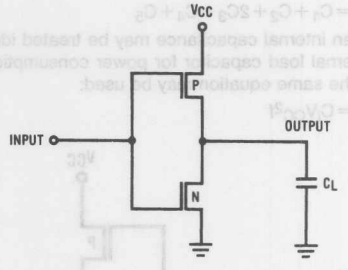
Load Capacitance Transient Dissipation

The first contributor to power consumption is the charging and discharging of external load capacitances. *Figure 1* is a schematic diagram of a simple CMOS inverter driving a capacitive load. A simple expression for power dissipation as a function of load capacitance can be derived starting with:

$$Q_L=C_LV_{CC}$$

where C_L is the load capacitance, and Q_L is the charge on the capacitor. If both sides of the equation are divided by the time required to charge and discharge the capacitor (one period, T, of the input signal), we obtain:

$$\frac{Q_L}{T}=C_LV_{CC}\left(\frac{1}{T}\right)$$



TL/F/5021–1

FIGURE 1. Simple CMOS Inverter Driving a Capacitive External Load

Since charge per unit time is current ($Q_L/T=I$) and the inverse of the period of a waveform is frequency ($1/T=f$):

$$I_L=C_LV_{CC}f$$

To find the power dissipation, both sides of the equation must be multiplied by the supply voltage ($P=VI$), yielding:

$$P_L=C_L\,V_{CC}{}^2f$$

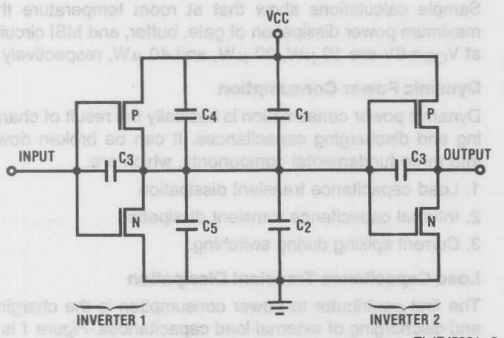
One note of caution is in order. If all the outputs of a device are not switching at the same frequency, then the power consumption must be calculated at the proper frequency for each output:

$$P_L = V_{CC}^2(C_{L1}f_1 + C_{L2}f_2 + \ldots + C_{Ln}f_n)$$

Examples of devices for which this may apply are: counters, dual flip-flops with independent clocks, and other integrated circuits containing dual, triple, etc., independent circuits.

Internal Capacitance Transient Dissipation

Internal capacitance transient dissipation is similar to load capacitance dissipation, except that the internal parasitic "on-chip" capacitance is being charged and discharged. *Figure 2* is a diagram of the parasitic nodal capacitances associated with two CMOS inverters.



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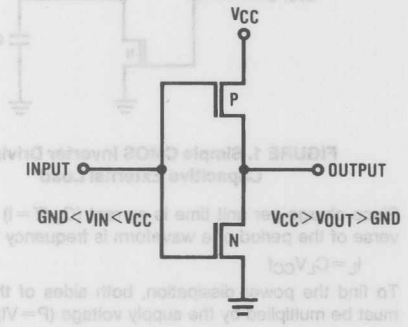
FIGURE 2. Parasitic Internal Capacitances Associated with Two Inverters

C_1 and C_2 are capacitances associated with the overlap of the gate area and the source and channel regions of the P- and N-channel transistors, respectively. C_3 is due to the overlap of the gate and source (output), and is known as the Miller capacitance. C_4 and C_5 are capacitances of the parasitic diodes from the output to V_{CC} and ground, respectively. Thus the total internal capacitance seen by inverter 1 driving inverter 2 is:

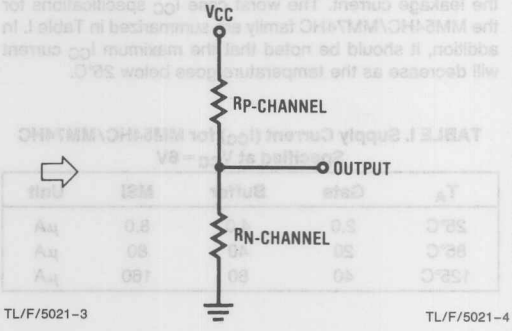
$$C_I = C_1 + C_2 + 2C_3 + C_4 + C_5$$

Since an internal capacitance may be treated identically to an external load capacitor for power consumption calculations, the same equation may be used:

$$P_I = C_I V_{CC}^2 f$$



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TL/F/5021–4

FIGURE 3. Equivalent schematic of a CMOS inverter whose input is between logic levels

At this point, it may be assumed that different parts of the internal circuitry are operating at different frequencies. Although this is true, each part of the circuit has a fixed frequency relationship between it and the rest of the device. Thus, one value of an effective C_I can be used to compute the internal power dissipation at any frequency. More will be said about this shortly.

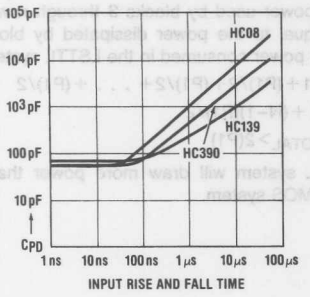
Current Spiking During Switching

The final contributor to power consumption is current spiking during switching. While the input to a gate is making a transition between logic levels, both the P- and N-channel transistors are turned partially on. This creates a low impedance path for supply current to flow from V_{CC} to ground, as illustrated in *Figure 3*.

For fast input rise and fall times (shorter than 50 ns for the MM54HC/MM74HC family), the resulting power consumption is frequency dependent. This is due to the fact that the more often a device is switched, the more often the input is situated between logic levels, causing both transistors to be partially turned on. Since this power consumption is proportional to input frequency and specific to a given device in any application, as is C_I, it can be combined with C_I. The resulting term is called "C_{PD}," the no-load power dissipation capacitance. It is specified for every MM54HC/MM74HC device in the AC Electrical Characteristic section of each data sheet.

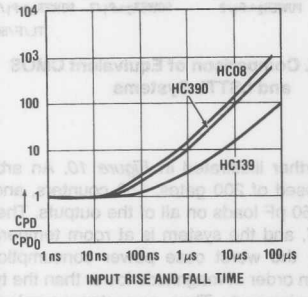
It should be noted that as input rise and fall times become longer, the switching current power dissipation becomes more dependent on the amount of time that both the P- and N-channel transistors are turned on, and less related to C_{PD} as specified in the data sheets. *Figure 4* is a representation of the effective value of C_{PD} as input rise and fall times increase for the MM54HC/MM74HC08, MM54HC/MM74HC139, and MM54HC/MM74HC390. To get a fair comparison between the three curves, each is divided by the value of C_{PD} for the particular device with fast input rise and fall times. This is represented by "C_{PD0}," the value of C_{PD} specified in the data sheets for each part. This comparison appears in *Figure 5*. C_{PD} remains constant for input rise and fall times up to about 20 ns, after which it rises, approaching a linear slope of 1. The graphs do not all reach a slope of 1 at the same time because of necessary differences in circuit design for each part. The MM54HC/MM74HC08 exhibits the greatest change in C_{PD}, while the MM54HC/MM74HC139 shows less of an increase in C_{PD} at

any given frequency. Thus, the power dissipation for most of the parts in the MM54HC/MM74HC family will fall within these two curves. One notable exception is the MM54HC/MM74HCU04.



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FIGURE 4. Comparison of Typical C_{PD} for MM54HC/MM74HC08, MM54HC/MM74HC139 MM54HC/MM74HC390 as a Function of Input Rise and Fall Time. $t_{rise} = t_{fall}$, $V_{CC} = 5V$, $T_A = 25°C$



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FIGURE 5. Normalized Effective C_{PD} (Typical) for Slow Input Rise and Fall Times. $t_{rise} = t_{fall}$, $V_{CC} = 5V$, $T_A = 25°C$

Inputs that do not pull all the way to V_{CC} or ground can also cause an increase in power consumption, for the same reason given for slow rise and fall times. If the input voltage is between the minimum input high voltage and V_{CC}, then the input N-channel transistor will have a low impedance (i.e., be "turned on") as expected, but the P-channel transistor will not be completely turned off. Similarly, if the input is between ground and the maximum input low voltage, the P-channel transistor will be fully on and the N-channel transistor will be partially on. In either case, a resistive path from V_{CC} to ground will occur, resulting in an increase in power consumption.

Combining all the derived equations, we arrive at the following:

$$P_{TOTAL} = (C_L + C_{PD})V_{CC}^2 f + I_{CC}V_{CC}$$

This equation can be used to compute the total power consumption of any MM54HC/MM74HC device, as well as any other CMOS device, at any operating frequency. It includes both DC and AC contributions to power usage. C_{PD} and I_{CC} are supplied in each data sheet for the particular device, and V_{CC} and f are determined by the particular application.

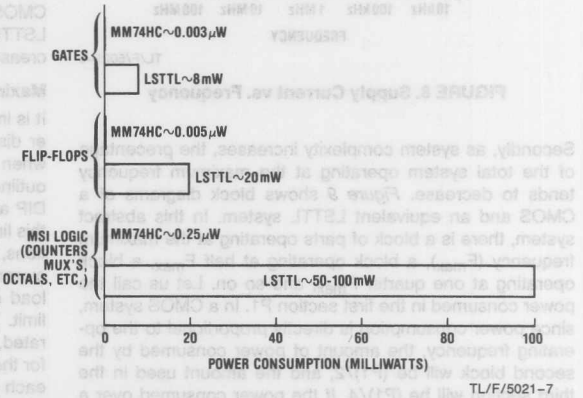
Comparing HC-CMOS to LSTTL

Although power consumption is somewhat dependent on frequency in LSTTL devices, the majority of power dissipated below 1 MHz is due to quiescent supply current. LSTTL contains many resistive paths from V_{CC} to ground, and even when it is not switching, it draws several orders of magnitude greater supply current than HC-CMOS. *Figure 6* is a bar graph comparison of quiescent power requirements $(V_{CC}) \times (I_{CC})$ between LSTTL and HC-CMOS devices.

The reduction in CMOS power consumption as compared to LSTTL devices is illustrated in *Figures 7* and *8*. These graphs are comparisons of the typical supply current (I_{CC}) required for equivalent functions in MM54HC/MM74HC, MM54HC/MM74C, CD4000, and 54LS/74LS logic families. The currents were measured at room temperature (25°C) with a supply voltage of 5V.

Figure 7 represents the supply current required for a quad NAND gate with one gate in the package switching. The MM54HC/MM74HC family draws slightly more supply current than the 54C/74C and CD4000 series. This is mainly due to the large size of the output buffers necessary to source and sink currents characteristic of the LSTTL family. Other reasons include processing differences and the larger internal circuitry required to drive the output buffers at high frequencies. The frequency at which the CMOS device draws as much power as the LSTTL device, known as the power cross-over-frequency, is about 20 MHz.

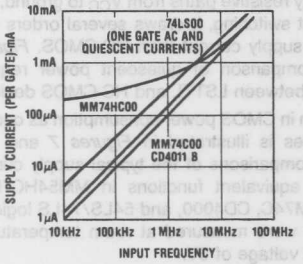
In *Figure 8*, which is a comparison of equivalent flip-flops (174) and shift registers (164) from the different logic families, the power cross-over frequency again occurs at about 20 MHz.



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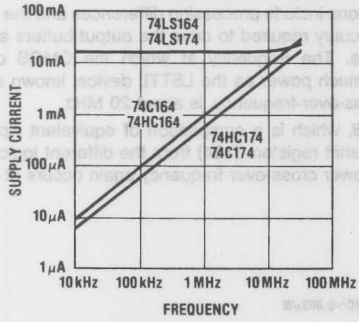
FIGURE 6. High Speed CMOS (HC-CMOS) vs. LSTTL Quiescent Power Consumption

The power cross-over frequency increases as circuit complexity increases. There are two major reasons for this. First, having more devices on an LSTTL integrated circuit means that more resistive paths between V_{CC} and ground will occur, and more quiescent current will be required. In a CMOS integrated circuit, although the supply leakage current will increase, it is of such a small magnitude (nanoAmps per device) that there will be very little increase in total power consumption.



TL/F/5021–8

FIGURE 7. Supply Current vs. Input Frequency for Equivalent NAND Gates



TL/F/5021–9

FIGURE 8. Supply Current vs. Frequency

Secondly, as system complexity increases, the precentage of the total system operating at the maximum frequency tends to decrease. *Figure 9* shows block diagrams of a CMOS and an equivalent LSTTL system. In this abstract system, there is a block of parts operating at the maximum frequency (F_{max}), a block operating at half F_{max}, a block operating at one quarter F_{max}, and so on. Let us call the power consumed in the first section P1. In a CMOS system, since power consumption is directly proportional to the operating frequency, the amount of power consumed by the second block will be (P1)/2, and the amount used in the third section will be (P1)/4. If the power consumed over a large number of blocks is summed up, we obtain:

$$P_{TOTAL} = P1 + (P1)/2 + (P1)/4 + \ldots + (P1)/(2^{n-1})$$

and $P_{TOTAL} \leq 2(P1)$

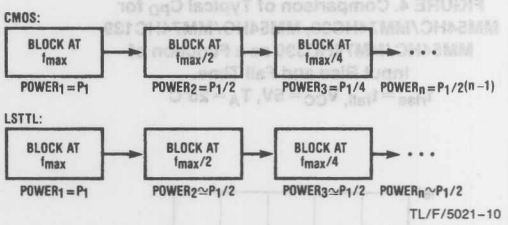
Now consider the LSTTL system. Again, the power consumed in the first block is P1. The amount of power dissipated in the second block is something less than P1, but greater than (P1)/2. For simplicity, we can assume the best case, that P2 = (P1)/2. The power consumption for all system blocks operating at frequencies $F_{max}/2$ and below will be dominated by quiescent current, which will not change with frequency. The power used by blocks 3 through n will be approximately equal to the power dissipated by block 2, (P1)/2. The total power consumed in the LSTTL system is:

$$P_{TOTAL} = (P1 + (P1)/2 + (P1)/2 + \ldots + (P1)/2$$

$$P_{TOTAL} = P1 + (N-1)(P1)/2$$

and for $n > 2$, $P_{TOTAL} > 2(P1)$

Thus, an LSTTL system will draw more power than an equivalent HC-CMOS system.



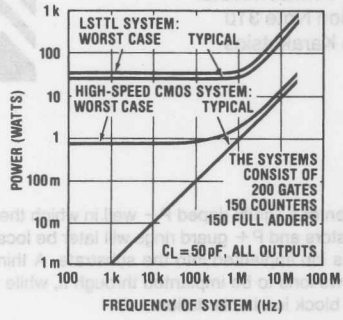
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FIGURE 9. Comparison of Equivalent CMOS and LSTTL Systems

This effect is further illustrated in *Figure 10*. An arbitrary system is composed of 200 gates, 150 counters, and 150 full adders, with 50 pF loads on all of the outputs. The supply voltage is 5V, and the system is at room temperature. For this system, the worst case power consumption for CMOS is about an order of magnitude lower than the typical LSTTL power requirements. Thus, as system complexity increases, CMOS will save more power.

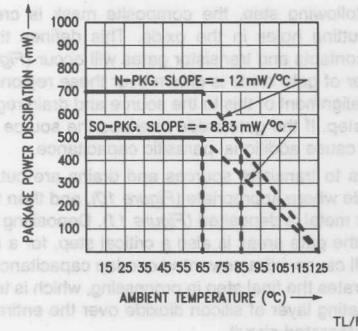
Maximum Power Dissipation Limits

It is important to take into consideration the maximum power dissipation limits imposed on a device by the package when designing with high-speed CMOS. The plastic small-outline (SO) can dissipate up to 500 mW, and the ceramic DIP and plastic DIP can dissipate up to 700 mW. Although this limit will rarely be reached in typical high-speed applications, the MM54HC/MM74HC family has such large output current source and sink capabilities that driving a resistive load could possibly take a device to the 500 or 700 mW limit. This maximum power dissipation rating should be derated, starting at 65°C for the plastic packages and 100°C for the ceramic packages. The derating factor is different for each package. The factor for the plastic small-outline is −8.83 mW/°C; the plastic DIP, −12 mW/°C; and the ceramic DIP, −14 mW/°C. This is illustrated in *Figures 11* and *12*. Thus, if a device in a plastic DIP package is operating at 70°C, then the maximum power dissipation rating would be 700 mW − (70°C − 65°C) (12 mW/°C) = 640 mW. Note that the maximum ambient temperature is 85°C for plastic packages and 125°C for ceramic packages.



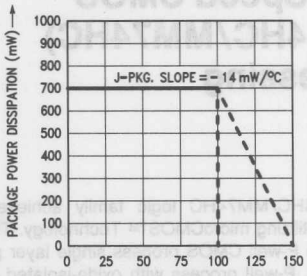
TL/F/5021–11

FIGURE 10. System Power vs. Frequency MMHC74HC vs. LSTTL



TL/F/5021–12

FIGURE 11. Plastic Package (MM74HC) High Temperature Power Derating for MM54HC/MM74HC Family



TL/F/5021–13

FIGURE 12. Ceramic Package (MM54HC) High Temperature Power Derating for MM54HC/MM74HC Family

Summary

The MM54HC/MM74HC high-speed silicon gate CMOS family has quiescent (standby) power consumption five to seven orders of magnitude lower than the equivalent LSTTL function. At high frequencies (30 MHz and above), both families consume a similar amount of power for very simple systems. However, as system complexity increases, HC-CMOS uses much less power than LSTTL. To keep power consumption low, input rise and fall times should be fast (less than 50 to 100 ns) and inputs should swing all the way to V_{CC} and ground.

There is an easy-to-use equation to compute the power consumption of any HC-CMOS device in any application:

$$P_{TOTAL} = (C_L + C_{PD})V_{CC}^2 f + I_{CC}V_{CC}$$

The maximum power dissipation rating is 500 mW per package at room temperature, and must be derated as temperature increases.

High-Speed CMOS (MM54HC/MM74HC) Processing

National Semiconductor
Application Note 310
Kenneth Karakotsios

The MM54HC/MM74HC logic family achieves its high speed by utilizing microCMOS™ Technology. This is a 3.5 silicon gate P-well CMOS process single layer poly, single layer metal, P-well process with oxide-isolated transistors. Why do silicon-gate transistors (polycrystalline) switch faster than metal-gate transistors? The reason is related both to the parasitic capacitances inherent in integrated circuits and the gain of the transistors. The speed at which an MOS transistor can switch depends on how fast its internal parasitic capacitance, as well as its external load capacitance, can be charged and discharged. Capacitance takes time to be charged and discharged, and hence degrades a transistor's performance. The gain of a transistor is a measure of how well a transistor can charge and discharge a capacitor. Therefore, to increase speed, it is desirable to both decrease parasitic capacitance and increase transistor gain. These advantages are achieved with National's silicon-gate CMOS process. To understand exactly how these improvements occur in silicon-gate CMOS, it is helpful to compare the process to the metal-gate CMOS process.

Metal-Gate CMOS Processing

Figure 1 through *12* are cross sections of a metal-gate CMOS pair of P- and N-channel transistors with associated guard rings. Guard rings are necessary in metal-gate processing to prevent leakage currents between the sources and drains of separate transistors. The starting material is an N− type silicon substrate covered by a thin layer of thermally grown silicon dioxide (SiO_2) (*Figure 1*). Silicon dioxide, also called oxide acts as both a mask for certain processing steps and a dielectric insulator. *Figure 2* shows the addition of a lightly doped P− well in which the N-channel transistors and P+ guard rings will later be located. The P− well is ion implanted into the substrate. A thin layer of oxide allows ions to be implanted through it, while a thicker oxide will block ion implantation.

Next, the oxide over the P− well is stripped, and a new layer of oxide is grown. Following this, holes are etched into the oxide where the P+ source, drain, and guard ring diffusions shall occur. The P+ regions are diffused, and then additional oxide is grown to fill the holes created for diffusion (*Figures 3, 4,* and *5*). The following step is to cut holes in the oxide to diffuse the N-channel sources, drains and guard bands. Then oxide is again thermally grown (*Figures 6* and *7*).

In the following step, the composite mask is created by again cutting holes in the oxide. This defines the areas where contacts and transistor gates will occur (*Figure 8*). A thin layer of gate oxide is grown over these regions (*Figure 9*), and alignment of this to the source and drain regions is a critical step. If the gate oxide overlaps the source or drain, this will cause additional parasitic capacitance.

Contacts to transistor sources and drains are cut into the thin oxide where appropriate (*Figure 10*), and then the interconnect metal is deposited (*Figure 11*). Depositing the metal over the gate areas is also a critical step, for a misalignment will cause extra unwanted overlap capacitance. *Figure 12* illustrates the final step in processing, which is to deposit an insulating layer of silicon dioxide over the entire surface of the integrated circuit.

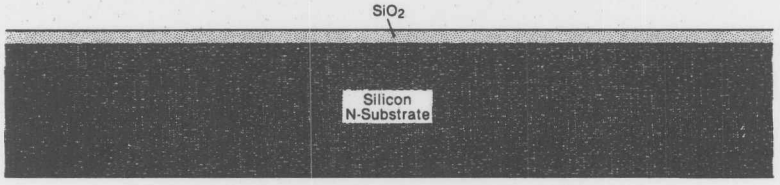
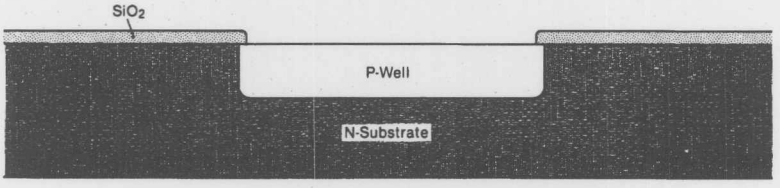


FIGURE 1. Initial Oxidation, Thermally Grown Silicon Dioxide Layer on Silicon Substrate Surface



TL/L/5044–1

FIGURE 2. P− Mask and Formation of P− Well Tub in Which N-Channel Devices Will Be Located

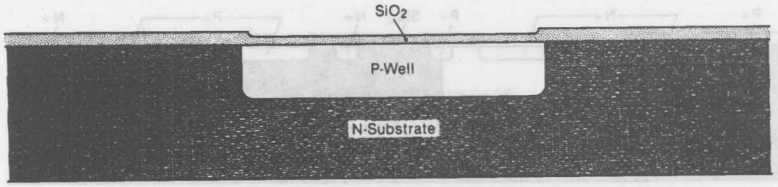


FIGURE 3. P− Well Oxidation, Thermally Grown Silicon Dioxide Layer Over P− Well Area

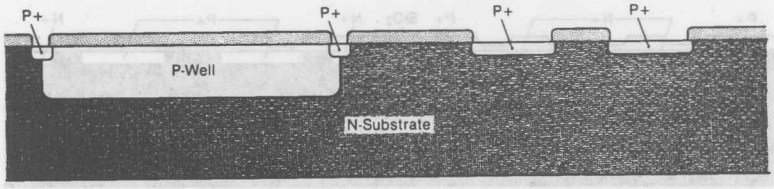
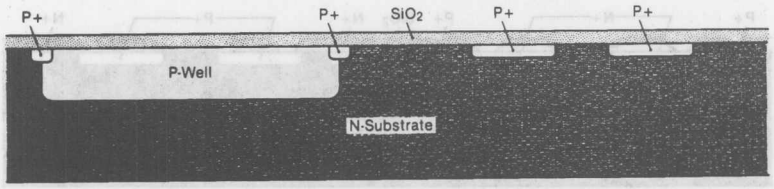


FIGURE 4. P + Mask and Formation of Low Resistance P + Type Pockets in − Well and N-Substrate



TL/L/5044–2

FIGURE 5. P + Oxidation, Thermally Grown Silicon Dioxide Layer Over P+ Type Pockets

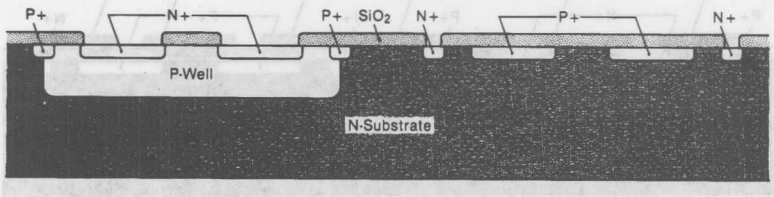
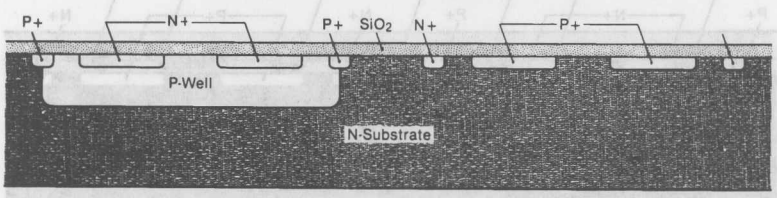


FIGURE 6. N + Mask and Formation of Low Resistance N + Type Pockets in P− Well and N-Substrate



TL/L/5044–3

FIGURE 7. N + Oxidation, Thermally Grown Silicon Dioxide Layer Over N + Type Pockets

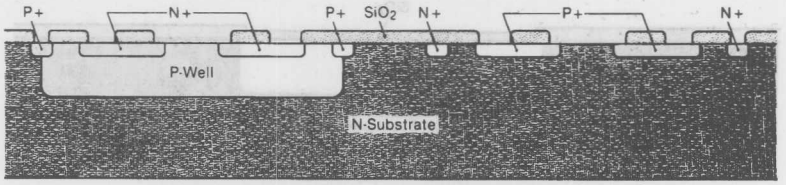


FIGURE 8. Composite Mask and Openings to N- and P-Channel Devices

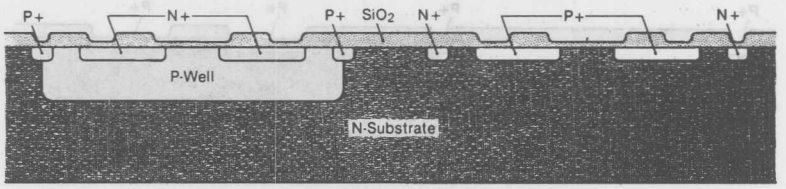
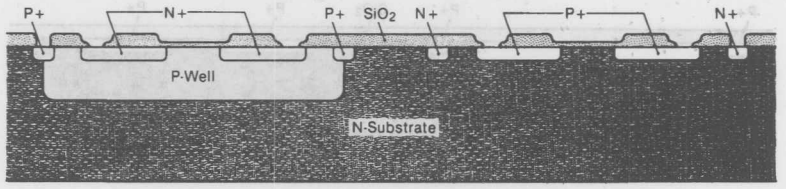


FIGURE 9. Gate Oxidation, Thermally Grown Silicon Dioxide Layer Over N- and P-Channel Devices



TL/L/5044–4

FIGURE 10. Contact Mask and Openings to N- and P-Channel Devices

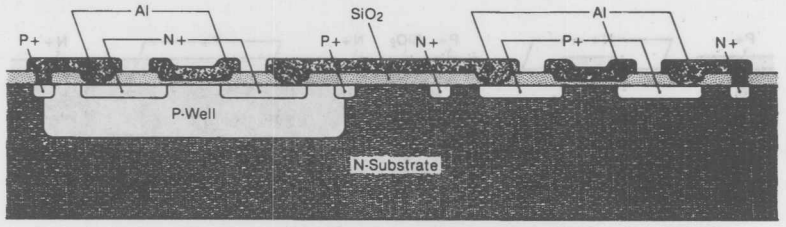
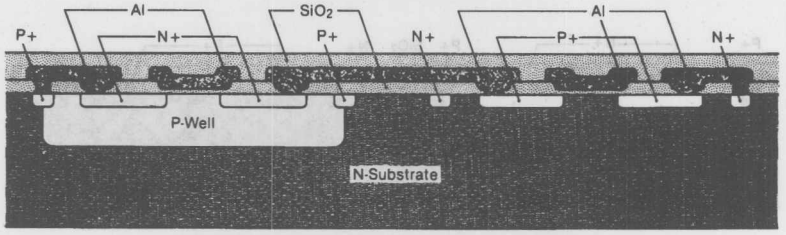


FIGURE 11. Metallization, Metal Mask, Resulting in Gate Metal and Metal Interconnects



TL/L/5044–5

FIGURE 12. Passivation Oxide, Deposited Silicon Dioxide Over Entire Die Surface

Silicon-Gate CMOS Processing

The silicon-gate CMOS process starts with the same two steps as the metal-gate process, yielding an N− substrate with an ion-implanted P− well (*Figures 13* and *14*). That, however, is where the similarity ends. Next, the initial oxide is stripped, and another layer of oxide, called pad oxide, is thermally grown. Also, a layer of silicon nitride is deposited across the surface of the wafer (*Figure 15*). The nitride prevents oxide growth on the areas it covers. Thus, in *Figure 16*, the nitride is etched away wherever field oxide is to be grown. The field oxide is a very thick layer of oxide, and it is grown everywhere except in the transistor regions (*Figure 17*). As an oxide grows in silicon, it consumes the silicon substrate beneath it and combines it with ambient oxygen to produce silicon dioxide. Growth of this very thick oxide causes the oxide to be recessed below the surface of the silicon substrate by a significant amount. A recessed field oxide eliminates the need for guard ring diffusions, because current cannot flow through the field oxide, which completely isolates each transistor from every other transistor.

The next step is to deposit a layer of polycrystalline silicon, also called poly, which will form both the gate areas and a second layer of interconnect (*Figure 18*). The poly is then etched, and any poly remaining becomes a gate if it is over gate oxide, and interconnect if it is over field oxide. A new layer of oxide is grown over the poly, which will act as an insulator between the poly and the metal interconnect (*Figure 19*). The poly over the transistor areas is not as wide as the gate oxide. This allows the source and drain diffusions to be ion implanted through the gate oxide. The poly gate itself, along with the field oxide, is used as a mask for implantation. Therefore, the source and drain implants will automatically be aligned to the gate poly, which is what makes this process a self-aligned gate process (*Figure 20*).

Figure 21 illustrates the steps of cutting contacts into the insulating layer of oxide, so the metal may be connected to gate and field poly, as well as to source and drain implants. A layer of metal is deposited across the entire wafer, and is etched to produce the desired interconnection. Finally, as in metal-gate processing, an insulating layer of oxide is deposited onto the wafer (*Figure 22*).

Advantages of Silicon-Gate Processing

There are three major ways in which silicon-gate processing reduces parasitic capacitance: recessed field oxide, lower gate overlap capacitance, and shallower junction depths. *Figures 23* and *24* are cross sections of metal gate and silicon gate CMOS circuits, respectively. These figures show the parasitic on-chip capacitances (C_1 through C_4) for each type of process.

The N+ and P+ source and drain regions, as well as guard ring regions, in the metal-gate process, have two capacitances associated with them: periphery and area capacitances (C_2 and C_1). These capacitances are associated with the diode junctions between the P+ regions and the N− substrate, as well as the N+ regions and P− well. The finer line widths of silicon-gate CMOS, coupled with the shallower junction depths, act to decrease the size of these parasitic diodes. Capacitance is proportional to diode area, hence the diode area reduction results in a significantly reduced parasitic capacitance in silicon-gate CMOS.

Another origin of unwanted capacitance is the area where the gate overlaps the source and drain regions (C_4). The overlap is much larger in metal-gate processing than in silicon-gate CMOS. This is due to the fact that the metal-gate must be made wider than the channel width to allow for alignment tolerances. In silicon-gate processing, since the gate acts as the mask for the ion implantation of the source and drain regions, there is no alignment error, which results in greatly reduced overlap.

How does the use of polysilicon gates increase the gain of a MOSFET? Polysilicon may be etched to finer line widths than metal, permitting the fabrication of transistors with shorter gate lengths. The equation that describes the gain of a MOSFET is shown below:

$$I = \frac{(\text{Beta})(\text{Width})}{2(\text{Length}}[(\text{Gate Voltage}) - (\text{Threshold Voltage})]^2$$

Thus, a decrease in gate length will cause an increase in current drive capability. This, in turn, will allow the transistor to charge a capacitance more rapidly, therefore increasing the gain of the transistor. Also, the gate oxide is thinner for the silicon-gate CMOS process. A thinner gate oxide increases the Beta term in the equation, which further increases gain. Finally, although it is not apparent from the processing cross sections, the transistor threshold (turn on) voltage is lower. This is accomplished by the use of ion implants to adjust the threshold.

There is one more advantage of silicon-gate processing that should be noted: the polysilicon provides for an additional layer of interconnect. This allows three levels of interconnect, which are metal, polysilicon, and the N+ and P+ ion-implanted regions. Having these three levels helps to keep the die area down, since much die area is usually taken up by interconnection.

When all these advantages are summed up, the result is a CMOS technology that produces devices as fast as the equivalent LSTTL device. *Figure 25* illustrates a comparison between the MM74HC00 buffered NAND gate and the MM74C00, CD4011B, and DM74LS00 NAND gates. The MM74HC00 is about an order of magnitude faster than the CD4011B buffered NAND gate, and about 5 times faster than the unbuffered MM74C00, at 15 pF. As load capacitance increases, the speed differential between metal-gate and silicon-gate CMOS increases, with the MM74HC00 operating as fast as the DM74S00 at any load capacitance.

Summary

Polycrystalline silicon-gate CMOS has many advantages over metal-gate CMOS. It is faster because on-chip parasitic capacitances are reduced and transistor gains are increased. This is due mainly to a recessed field oxide and a self-aligned gate process. Transistor gains are increased by decreasing transistor lengths and threshold voltages, and increasing beta. Polysilicon also allows for an extra layer of interconnect, which helps to keep die area down.

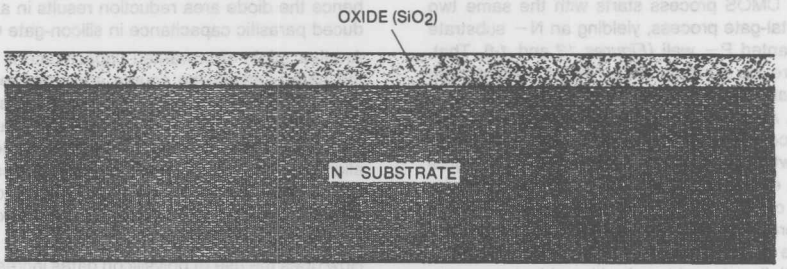
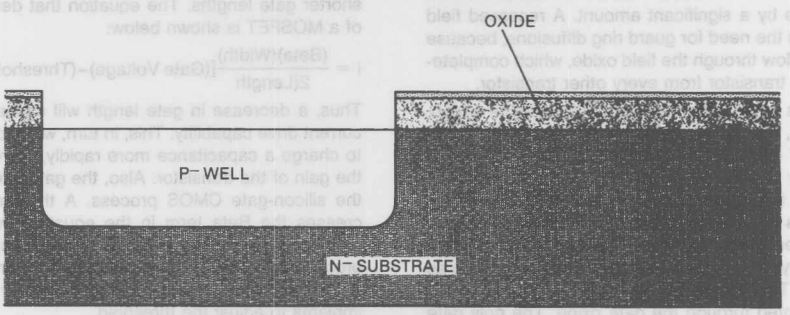
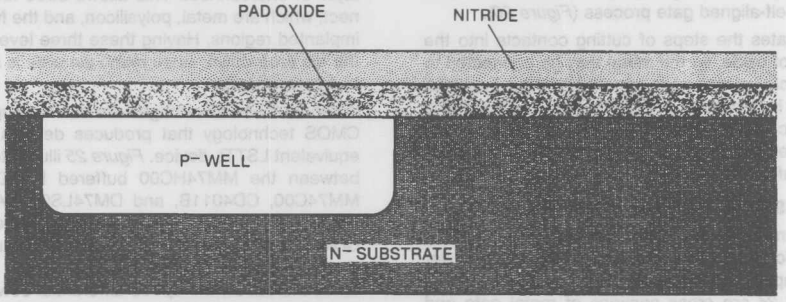


FIGURE 13. Initial Oxidation, Thermally Grown Silicon Dioxide on N − Silicon Substrate



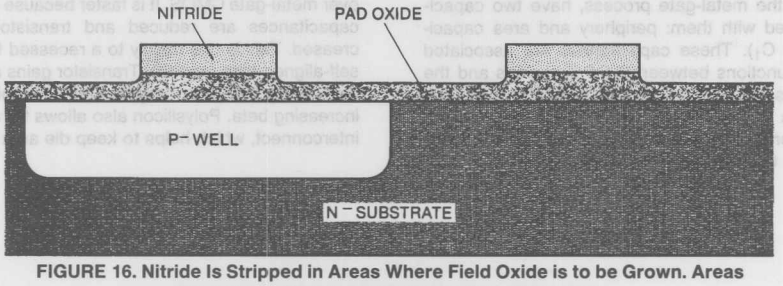
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FIGURE 14. Ion-Implanted P − Tub in Which N-Channel Devices Will Be Located



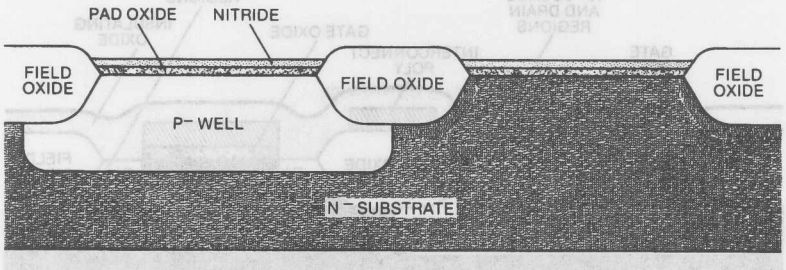
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FIGURE 15. Initial Oxide Is Stripped, Pad Oxide Is Thermally Grown, and a Layer of Silicon Nitride Is Deposited Across the Surface of the Wafer



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FIGURE 16. Nitride Is Stripped in Areas Where Field Oxide is to be Grown. Areas Covered by Nitride Will Become Transistor Area



TL/L/5044–8

FIGURE 17. Field Oxide Is Thermally Grown. The Nitride Acts as a Barrier to Oxide Growth

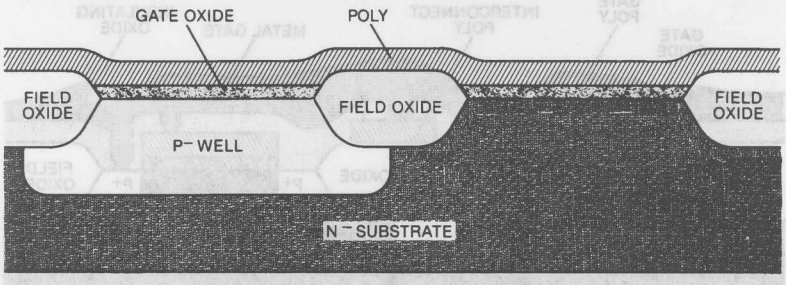
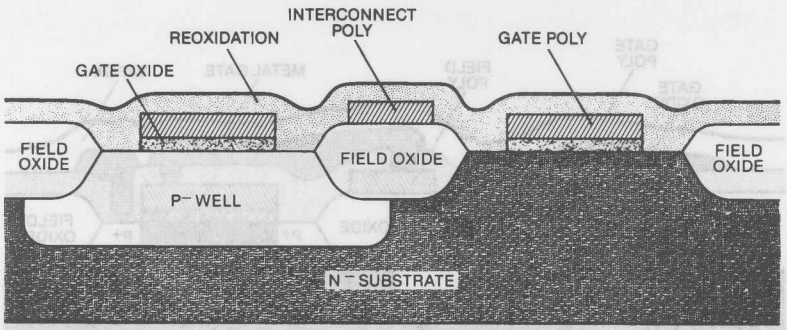


FIGURE 18. Nitride is Stripped, Pad Oxide Is Stripped Over Transistor Areas and a Thin Gate Oxide Is Grown Polycrystalline Silicon Is Deposited



TL/L/5044–9

FIGURE 19. Polysilicon Layer Is Etched to Provide Gate and Interconnect Poly Areas. New Layer of Oxidation is Grown

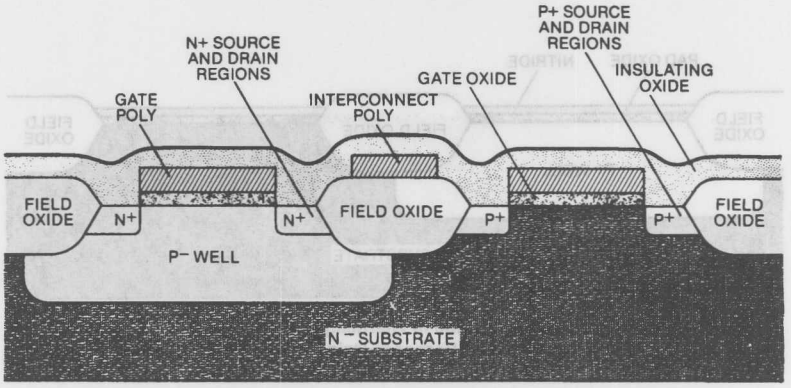
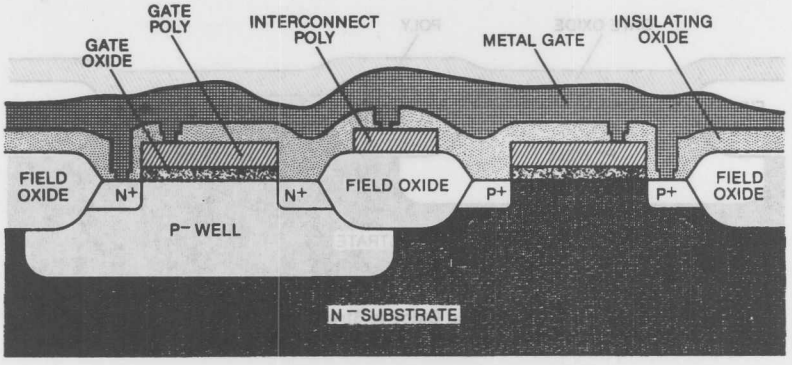
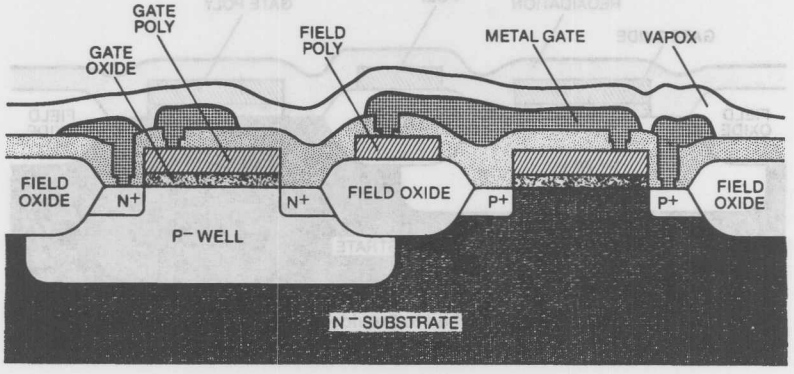


FIGURE 20. N+ and P+ Source and Drain Regions Are Ion Implanted, and the Reoxidation Is Grown Thicker to Form an Insulating Layer



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FIGURE 21. Contact Openings Are Cut in the Insulating Oxide, and a Layer of Metalization Is Deposited Across the Entire Wafer



TL/L/5044–11

FIGURE 22. Metal Mask Is Etched to Provide Interconnect. Vapox (SiO_2) Is Deposited Over Entire Surface of Wafer

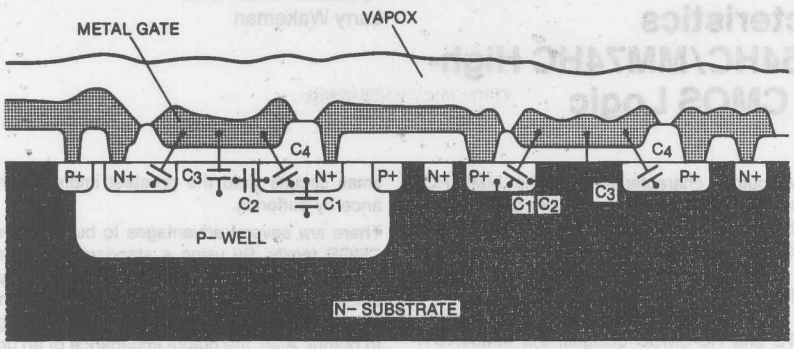
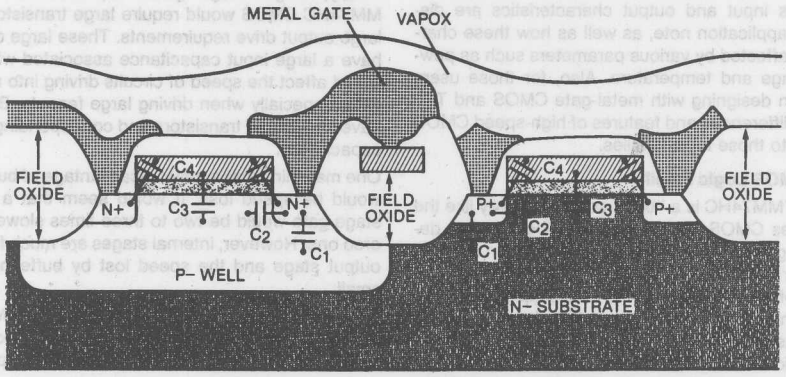
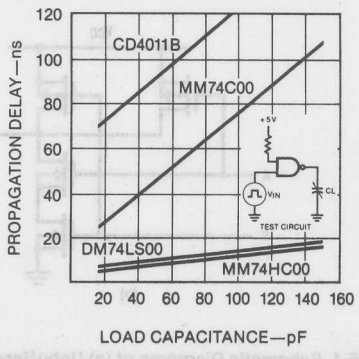


FIGURE 23. Cross Section of Metal Gate CMOS Process Showing Parasitic On-Chip Capacitances



TL/L/5044–12

FIGURE 24. Cross Section of Silicon Gate CMOS Process Showing Parasitic On-Chip Capacitances



TL/L/5044–13

FIGURE 25. Propagation Delay vs. Load Capacitance for 2-Input NAND Gate

2

of MM54HC/MM74HC High-Speed CMOS Logic

The input and output characteristics of the MM54HC/MM74HC high-speed CMOS logic family were conceived to meet several basic goals. These goals are to provide input current and voltage requirements, noise immunity and quiescent power dissipation similar to CD4000 and MM54C/MM74C metal-gate CMOS logic and output current drives similar to low power Schottky TTL. In addition, to enable merging of TTL and HC-CMOS designs, the MM54HCT/MM74HCT sub family differs only in their input voltage requirements, which are the same as TTL, to ease interfacing between logic families.

In order to familiarize the user with the MM54HC/MM74HC logic family, its input and output characteristics are discussed in this application note, as well as how these characteristics are affected by various parameters such as power supply voltage and temperature. Also, for those users who have been designing with metal-gate CMOS and TTL logic, notable differences and features of high-speed CMOS are compared to those logic families.

A Buffered CMOS Logic Family

The MM54HC/MM74HC is a "buffered" logic family like the CD4000B series CMOS. Buffering CMOS logic merely denotes designing the IC so that the output is taken from an inverting buffer stage. For example, the internal circuit implementation of a NAND gate would be a simple NAND followed by two inverting stages. An unbuffered gate would be implemented as a single stage. Both are shown in *Figure 1*. Most MSI logic devices are inherently buffered because they are inherently multi-stage circuits. Gates and similar small circuits yield the greatest improvement in performance by buffering.

There are several advantages to buffering this high-speed CMOS family. By using a standardized buffer, the output characteristics for all devices are more easily made identical. Multi-stage gates will have better noise immunity due to the higher gain caused by having several stages from input to output. Also, the output impedance of an unbuffered gate may change with input logic level voltage and input logic combination, whereas buffered outputs are unaffected by input conditions.

Finally, single stage gates implemented in MM54HC/MM74HC CMOS would require large transistors due to the large output drive requirements. These large devices would have a large input capacitance associated with them. This would affect the speed of circuits driving into an unbuffered gate, especially when driving large fanouts. Buffered gates have small input transistors and correspondingly small input capacitance.

One may think that a major disadvantage of buffered circuits would be speed loss. It would seem that a two or three stage gate would be two to three times slower than a buffered one. However, internal stages are much faster than the output stage and the speed lost by buffering is relatively small.

The one exception to buffering is the MM54HCU04/MM74HCU04 hex inverter which is unbuffered to enable its use in various linear and crystal oscillator applications.

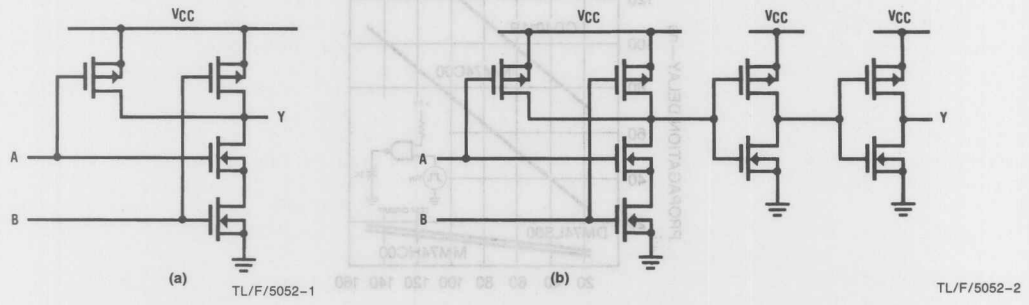


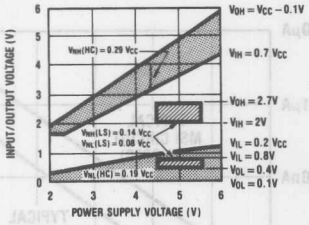
FIGURE 1. Schematic Diagrams of (a) Unbuffered and (b) Buffered NAND Gate

CMOS Input Voltage Characteristics

As mentioned before, MM54HC/MM74HC standard input levels are similar to metal-gate CMOS. This enables the high-speed logic family to enjoy the same wide noise margin of CD4000 and MM54C/MM74C logic. With $V_{CC}=5V$ these input levels are 3.5V for minimum logic "1" (V_{IH}) and 1.0V for a logic "0" (V_{IL}). The output levels when operated at $V_{CC}=5V\pm10\%$ and worst case input levels, are specified to be $V_{CC}-0.1$ or 0.1V. The output levels will actually be within a few millivolts of either V_{CC} or ground.

When operated over the entire supply voltage range, the input logic levels are: $V_{IH}=0.7V_{CC}$ and $V_{IL}=0.2V_{CC}$. *Figure 2* illustrates the input voltage levels and the noise margin of these circuits over the power supply range. The shaded area indicates the noise margin which is the difference between the input and output logic levels. The logic "1" noise margin is 29% of V_{CC} and the logic "0" noise margin is 19% of V_{CC}. Also shown for comparison are the 54LS/74LS input levels and noise margins over their supply range.

These input levels are specified on individual data sheets at $V_{CC}=2.0V$, 4.5V, 6.0V. At 2.0V the input levels are not quite $0.7(V_{CC})$ and $0.2(V_{CC})$ as at low voltages transistor turn on thresholds become significant. This is shown in *Figure 2*.

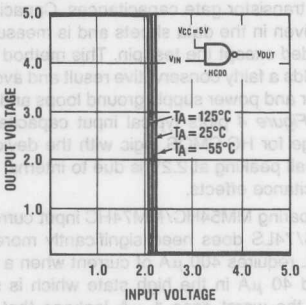


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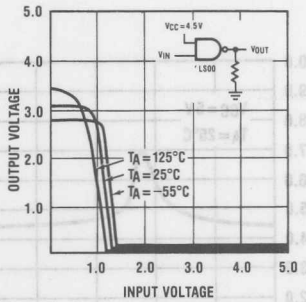
FIGURE 2. Worst Case Input and Output Voltages Over Operating Supply Range for "HC" and "LS" Logic

The input and output logic voltages and their behavior with temperature variation is determined by the input to output transfer function of the logic circuit. *Figure 3a* shows the transfer function of the MM54HC00/MM74HC00 NAND gate. As can be seen, the NAND gate has V_{CC} and ground output levels and a very sharp transition at about 2.25V. Thus, good noise immunity is achieved, since input noise of a volt or two will not appear on the output. The transition point is also very stable with temperature, drifting typically 50 or so millivolts over the entire temperature range. As a comparison, the transfer function for a 54LS00/74LS00 is plotted in *Figure 3b*. LSTTL output transitions at about 1.1V and the transition region varies several hundred millivolts over the temperature range. Also, since the transition region is closer to the low logic level, less ground noise can be tolerated on the input.

In typical systems, noise can be capacitively coupled to the signal lines. The amount of voltage coupled by capacitively induced currents is dependent on the impedance of the output driving the signal line. Thus, the lower the output impedance the lower the induced voltage. High-speed CMOS offers improved noise immunity over CD4000 in this respect because its output impedance is one tenth that of CD4000 and so it is about 7 times less susceptible to capacitively induced current noise.



TL/F/5052–4



TL/F/5052–5

FIGURE 3. Input/Output Transfer Characteristics for (a) 'HC00 and (b) 'LS00 Nand Gate

The MM54HCT/MM74HCT sub-family of MM54HC/MM74HC logic provides TTL compatible input logic voltage levels. This will enable TTL outputs to be guaranteed to correctly drive CMOS inputs. An incompatibility results because TTL outputs are only guaranteed to pull to a 2.7V logic high level, which is not high enough to guarantee a valid CMOS logic high input. To design the entire family to be TTL compatible would compromise speed, input noise immunity and circuit size. This sub-family can be used to interface sub-systems implemented using TTL logic to CMOS sub-systems. The input level specifications of MM54HCT/MM74HCT circuits are the same as LSTTL. Minimum input high level is 2.0V and the maximum low level is 0.8V using a $5V\pm10\%$ supply.

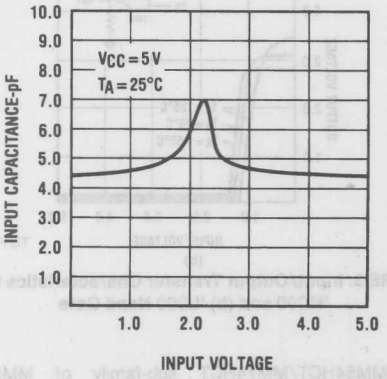
A fairly simple alternative to interfacing from LSTTL is to tie a pull-up resistor from the TTL output to V_{CC}, usually 4–10 kΩ. This resistor will ensure that TTL will pull up to V_{CC}. (See Interfacing MM54HC/MM74HC High-Speed CMOS Logic application note.)

High-Speed CMOS Input Current and Capacitance

Both standard "HC" and TTL compatible "HCT" circuits maintain the ultra low input currents inherent in CMOS circuits when CMOS levels are applied. This current is typically less than a nanoamp and is due to reverse leakages of the input protection diodes. Input currents are so small that they can usually be neglected. Since CMOS inputs present essentially no load, their fanout is nearly infinite.

Each CMOS input has some capacitance associated with it, as do TTL inputs. This capacitance is typically 3–5 pF for MM54HC/MM74HC, and is due to package, input protection diode, and transistor gate capacitances. Capacitance information is given in the data sheets and is measured with all pins grounded except the test pin. This method is used because it yields a fairly conservative result and avoids capacitance meter and power supply ground loops and decoupling problems. *Figure 4* plots typical input capacitance versus input voltage for HC-CMOS logic with the device powered on. The small peaking at 2.2V is due to internal Miller feedback capacitance effects.

When comparing MM54HC/MM74HC input currents to TTL logic, 54LS/74LS does need significantly more input current. LSTTL requires 400 μA of current when a logic low is applied and 40 μA in the high state which is significantly more than the worst case 1 μA leakage that MM54HC/MM74HC has.



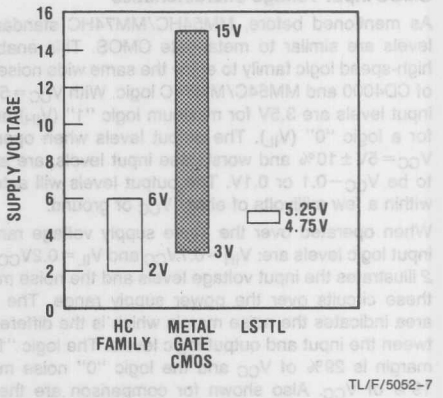
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FIGURE 4. Input Capacitance vs. Input Voltage for a Typical Device

MM54HC/MM74HC Power Supply Voltage and Quiescent Current

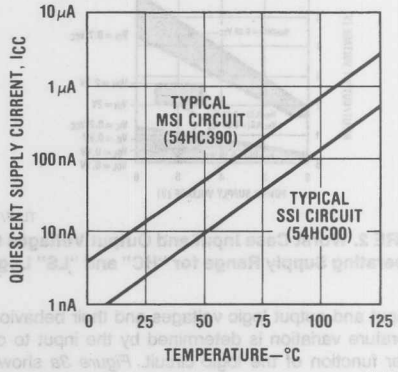
Figure 5 compares the operating power supply range of high-speed CMOS to TTL and metal-gate CMOS. As can be seen, MM54HC/MM74HC can operate at power supply voltages from 2–6V. This range is narrower than the 3–15V range of CD4000 and MM54C/MM74C CMOS. The narrower range is due to the silicon-gate CMOS process employed which has been optimized to attain high operating frequencies at V_{CC} = 5V. The 2–6V range is however much wider than the 4.5V to 5.5V range specified for TTL circuits, and guaranteeing operation down to 2V is useful when operating CMOS off batteries in portable or battery backup applications.

The quiescent power supply current of the high-speed CMOS family is very similar to CD4000 and MM54C/MM74C CMOS. When CMOS circuits are not switching there is no current path between V_{CC} and ground, except for leakage currents which are typically much less than 1 μA. These are due to diode and transistor leakages.



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FIGURE 5. Comparison of Supply Range for "HC", "LS" and Metal-Gate



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FIGURE 6. Typical Quiescent Supply Current Variation with Temperature

Figure 6 illustrates how this leakage increases with temperature by plotting typical leakage current versus temperature for an MSI and SSI device. As a result of this temperature dependence, there is a set of standardized I_{CC} specifications which specify higher current at elevated temperatures. A summary of these specifications are shown in Table I.

TABLE I. Standardized I_{CC} Specifications for MM54HC/MM74HC Logic at 25°C, 85°C and 125°C at V_{CC} = 6.0V

Temperature	Gates	Flip-Flops	MSI
25°C	2 μA	4 μA	8 μA
85°C	20 μA	40 μA	80 μA
125°C	40 μA	80 μA	160 μA

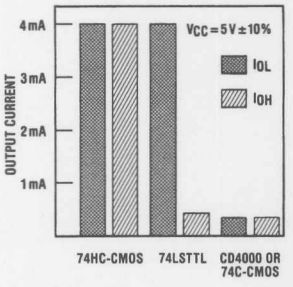
Output Characteristics

One of the prime advantages of MM54HC/MM74HC over metal-gate CMOS (besides speed) is the output drive current, which is about ten times CD4000 or MM54C/MM74C logic. The larger output current enables high-speed CMOS to directly drive large fanouts of 54LS/74LS devices, and also enables HC-CMOS to more easily drive large capacitive loads. This improvement in output drive is due to a variety of enhancements provided by the silicon-gate process used. The basic current equation for a MOSFET is:

$$I = (\text{Beta})(\text{Width}/\text{Length})((V_g - V_t)V_d - 0.5(V_d^2))$$

Where V_g is the transistor gate voltage, V_t is the transistor threshold voltage, and V_d is the transistor drain voltage which is equivalent to the circuit output voltage. This CMOS process, when compared to metal-gate CMOS, has increased transistor gains, Beta, and lower threshold voltages, V_t. Also, improved photolithography has reduced the transistor lengths, and wider transistors are also possible because of tighter geometries.

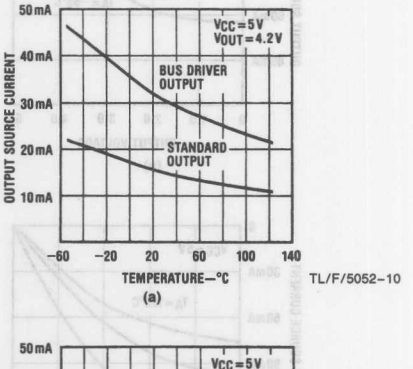
Figure 7 compares the output high and low current specifications of MM74HC, 74LS and metal-gate CMOS for standard device outputs. High-speed CMOS has worst case output low current of 4 mA which is similar to low power Schottky TTL circuits, and offers symmetrical logic high and low currents as well. In addition, CMOS circuits whose functions make them ideal for use driving large capacitive loads have a larger output current of 6 mA. For example, these bus driver outputs are used on the octal flip-flops, latches, buffers, and bidirectional circuits.



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FIGURE 7. Comparison of 74HC, 74LS and CD4000/ 74C Output Drive Currents, I_{OH} and I_{OL}

Table II summarizes the various output current specifications for MM54HC/MM74HC CMOS along with their equivalent LSTTL fanouts. As Table II shows, the output currents of the MM54HC/MM74HC devices are derated from the MM74HC devices. The derating is caused by the decrease in current drive of the output transistors as temperature is increased. To show this, *Figure 8* plots typical output source and sink currents against temperature for both standard and bus driver circuits. This variation is similar to that found in metal-gate CMOS, and so the same −0.3% per °C derating that is used to approximate temperature derating of CD4000 and MM54C/MM74C can be applied to 54HC/74HC. As an example, the approximate worst case 25°C current drive one would expect by using the 4 mA 85°C data sheet number would be about 4 mA at $V_{OUT} = 0.26V$, and this is what is specified in the device data sheets.



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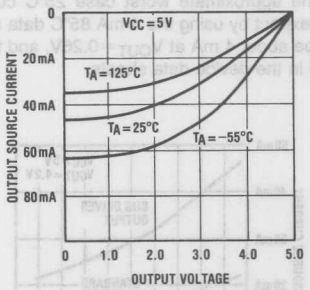
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FIGURE 8. Typical Output (a) Source and (b) Sink Current Temperature for Standard and Bus Outputs

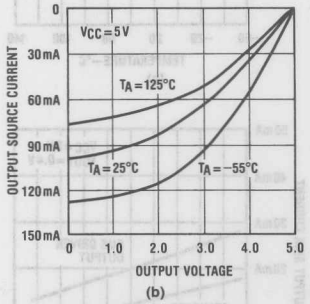
TABLE II. Data Sheet Output Current Specifications for MM54HC/MM74HC Logic

Device $V_{CC} = 4.5V$	Output High Current	Output Low Current	LSTTL Fanout
Standard 54HC	4.0 mA ($V_{OUT} = 3.7V$)	4.0 mA ($V_{OUT} = 0.4V$)	10
Bus Driver 54HC	6.0 mA ($V_{OUT} = 3.7V$)	6.0 mA ($V_{OUT} = 0.4V$)	15
Standard 74HC	4.0 mA ($V_{OUT} = 3.94$)	4.0 mA ($V_{OUT} = 0.33V$)	10
Bus 74HC	6.0 mA ($V_{OUT} = 3.94$)	6.0 mA ($V_{OUT} = 0.33V$)	15

current for each of three temperature ranges, room, commercial, and military. The outputs can supply much larger currents if larger output voltages are allowed. This is shown in *Figures 9* and *10*, which plot output current versus output voltage for both N-channel sink current and P-channel source current. Both standard and bus driver outputs are shown. For example, a standard output would typically sink 20 mA with $V_{OL} = 1V$, and typically capable of a short circuit current of 50 mA.

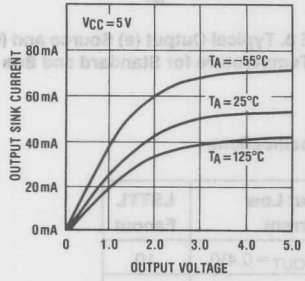


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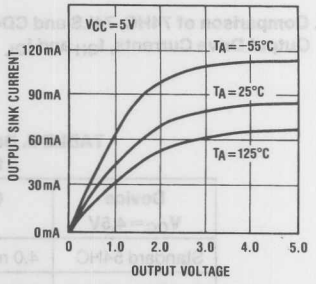


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FIGURE 9. Typical P-Channel Output Source Current vs. Output Voltage for (a) Standard and (b) Bus Outputs



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TL/F/5052–15

FIGURE 10. Typical N-Channel Output Sink Current vs. Output Voltage for (a) Standard and (b) Bus Outputs

more current available, the faster the load can be switched. In order for HC-CMOS to achieve LSTTL performance, the outputs should have characteristics similar to LSTTL. This similarity is illustrated in *Figure 11* by plotted typical LSTTL and HC-CMOS output characteristics together.

As the supply voltage is decreased, the output currents will decrease. *Figure 12a* plots the output sink current versus power supply voltage with a 0.4V output voltage, and *Figure 12b* plots output source current against power supply with an output voltage of $V_{CC} - 0.8V$. It is interesting to note that MM54HC/MM74HC powered at $V_{CC} = 3V$, typically, will still drive 10 LSTTL inputs ($T = 25°C$).

Absolute Maximum Ratings

Absolute maximum ratings are a set of guidelines that define the limits of operation for the MM54HC/MM74HC logic devices. To exceed these ratings could cause a device to malfunction and permanently damage itself. These limits are tabulated in Table III, and their reasons for existing are discussed below.

The largest power supply voltage that should be applied to a device is 7V. If larger voltages are applied, the transistors will breakdown, or "punch through". The smallest voltage that should be applied to a MM54HC/MM74HC circuit is −0.5V. If more negative voltages are applied, a substrate diode would become forward biased. In both cases large currents could flow, damaging the device.

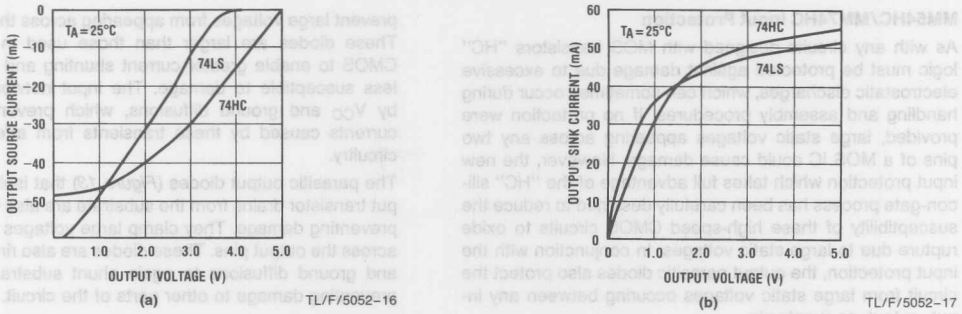


FIGURE 11. Comparison of Standard LSTTL and HC-CMOS Output (a) Source and (b) Sink Currents

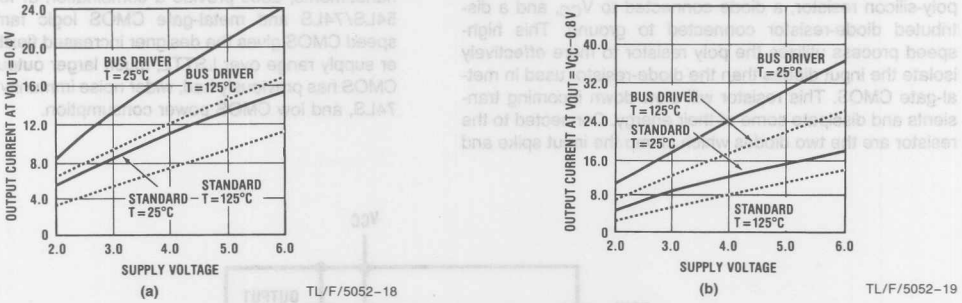


FIGURE 12. Output (a) Sink and (b) Source Current Variation with Power Supply

High-speed CMOS inputs should not have DC voltages applied to them that exceed V_{CC} or go below ground by more than 1.5V. To do so would forward bias input protection diodes excessive currents which may damage them. In actuality the diodes are specified to withstand 20 mA current. Thus the input voltage can exceed 1.5V if the designer limits his input current to less than 20 mA. The output voltages should be restricted to no less than −0.5V and no greater than $V_{CC}+0.5V$, or the current must be limited to 20 mA. The same limitations on the input diodes apply to the outputs as well. This includes both standard and TRI-STATE® outputs. These are DC current restrictions. In normal high speed systems, line ringing and power supply spiking unavoidably cause the inputs or outputs to glitch above these limits. This will not damage these diodes or internal circuitry. The diodes have been specifically designed to withstand momentary transient currents that would normally occur in high speed systems.

Additionally, there is a maximum rating on the DC output or supply currents as shown in Table 3. This is a restriction dictated by the current capability of the integrated circuit metal traces. Again this is a DC specification and it is expected that during switching transients the output and supply currents could exceed these specifications by several times these numbers.

For most CD4000 and MM54C/MM74C CMOS operating at $V_{CC}=5V$, the designer does not need to worry about excessive output currents, since the output transistors usually cannot source or sink enough current to stress the metal or dissipate excessive amounts of power. The high-speed CMOS devices do have much improved output characteristics, so care should be exercised to ensure that they do not draw excessive currents for long durations, i.e., greater than 0.1 seconds. It is also important to ensure that internal dissipation of a circuit does not exceed the package power dissipation. This will usually only occur when driving large currents into small resistive loads.

TABLE III. Absolute Maximum Ratings for MM54HC/MM74HC CMOS Logic

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to 7.0	V
V_{IN}	DC Input Voltage		−1.5 to $V_{CC}+1.5$	V
V_{OUT}	DC Output Voltage		−0.5 to $V_{CC}+0.5$	V
I_{OUT}	DC Current, Per Output Pin	Standard	±25	mA
		Bus Driver	±35	mA
I_{CC}	DC V_{CC} or Ground Current	Standard	±50	mA
		Bus Driver	±70	mA
I_{IK}, I_{OK}	Input or Output Diode Current		±20	mA

MM54HC/MM74HC Input Protection

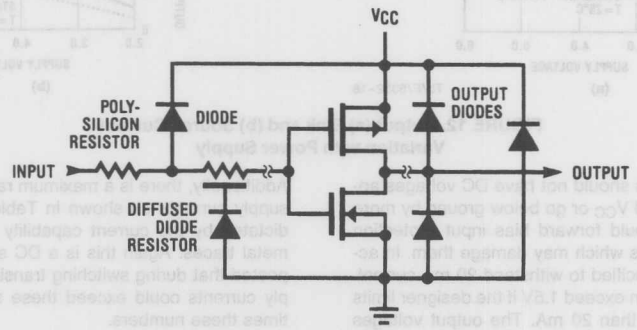
As with any circuits designed with MOS transistors "HC" logic must be protected against damage due to excessive electrostatic discharges, which can sometimes occur during handling and assembly procedures. If no protection were provided, large static voltages appearing across any two pins of a MOS IC could cause damage. However, the new input protection which takes full advantage of the "HC" silicon-gate process has been carefully designed to reduce the susceptibility of these high-speed CMOS circuits to oxide rupture due to large static voltages. In conjunction with the input protection, the output parasitic diodes also protect the circuit from large static voltages occuring between any input, output, or supply pin.

Figure 13 shows a schematic of the input protection network employed. The network consists of three elements: a poly-silicon resistor, a diode connected to V_{CC}, and a distributed diode-resistor connected to ground. This high-speed process utilizes the poly resistor to more effectively isolate the input diodes than the diode-resistor used in metal-gate CMOS. This resistor will slow down incoming transients and dissipate some of their energy. Connected to the resistor are the two diodes which clamp the input spike and prevent large voltages from appearing across the transistor. These diodes are larger than those used in metal-gate CMOS to enable greater current shunting and make them less susceptible to damage. The input network is ringed by V_{CC} and ground diffusions, which prevent substrate currents caused by these transients from affecting other circuitry.

The parasitic output diodes (*Figure 13*) that isolate the output transistor drains from the substrate are also important in preventing damage. They clamp large voltages that appear across the output pins. These diodes are also ringed by V_{CC} and ground diffusions to again shunt substrate currents, preventing damage to other parts of the circuit.

Summary

The MM54HC/MM74HC, because of many process enhancements, does provide a combination of features from 54LS/74LS and metal-gate CMOS logic families. High-speed CMOS gives the designer increased flexibility in power supply range over LSTTL, much larger output drive than CMOS has previously had, wider noise immunity than 54LS/74LS, and low CMOS power consumption.



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FIGURE 13. Schematic Diagram of Input and Output Protection Structures

Logic

On many occasions it might be necessary to interface MM54HC/MM74HC logic to other types of logic or to some other control circuitry. HC-CMOS can easily be interfaced to any other logic family including 54LS/74LS TTL, MM54C/MM74C, CD4000 CMOS and 10,000 ECL logic. Logic interfacing can be sub-divided into two basic categories: interfacing circuitry operating at the same supply voltage and interfacing to circuitry operating on a different voltage. In the latter case, some logic level translation is usually required, but many easily available circuits simplify this task. Usually, both instances require little or no external circuitry.

Interfacing Between TTL and MM54HC/MM74HC Logic

This high-speed CMOS family can operate from 2–6V, however, in most applications which interface to TTL, both logic families will probably operate off the same 5V TTL supply. The interconnection can be broken down into two categories: TTL outputs driving CMOS inputs, and CMOS outputs driving TTL inputs. In both cases the interface is very simple.

In the first case, TTL driving HC, there are some minor differences in TTL specifications for totem-pole outputs and high-speed CMOS input specifications. The TTL output low level is completely compatible with the MM54HC/MM74HC input low, but TTL outputs are specified to have an output high level of 2.4V (2.7V for LSTTL). High-speed CMOS's logic "1" input level is 3.5V (V_{CC} = 5.0V), so TTL is not guaranteed to pull a valid CMOS logic "1" level. If the TTL circuit is only driving CMOS, its output voltage is usually about 3.5V. HC-CMOS typically recognizes levels greater than 3V as a logic high, so in most instances TTL can drive MM74HC/MM54HC.

To see why TTL does not pull up further, *Figure 1a* shows a typical standard TTL gate's output schematic. As the output pulls up, it can go no higher than two diode voltage drops below V_{CC} due to Q2 and D2. So when operating with a 5V supply, the TTL output cannot go much higher than about 3.5V. *Figure 1b* shows an LSTTL gate, which has an output structure formed by Q2 and Q4. As the LSTTL output goes high, these two transistors cannot pull higher than two base-emitter voltage drops below V_{CC}, and, as above, the output cannot go much higher than 3.5V. If the output of either the LSTTL or TTL gate is loaded or the off sink transistor has some collector leakages, the output voltage will be lower.

Many LSTTL and ALSTTL circuits take R2 of *Figure 2b* and instead of connecting it to ground, it is connected to the output. This enables the TTL output to go to 4.3V (V_{CC} = 5.0V) which is more than adequate to drive CMOS. A simple measurement of open circuit V_{OH} can verify this circuit configuration.

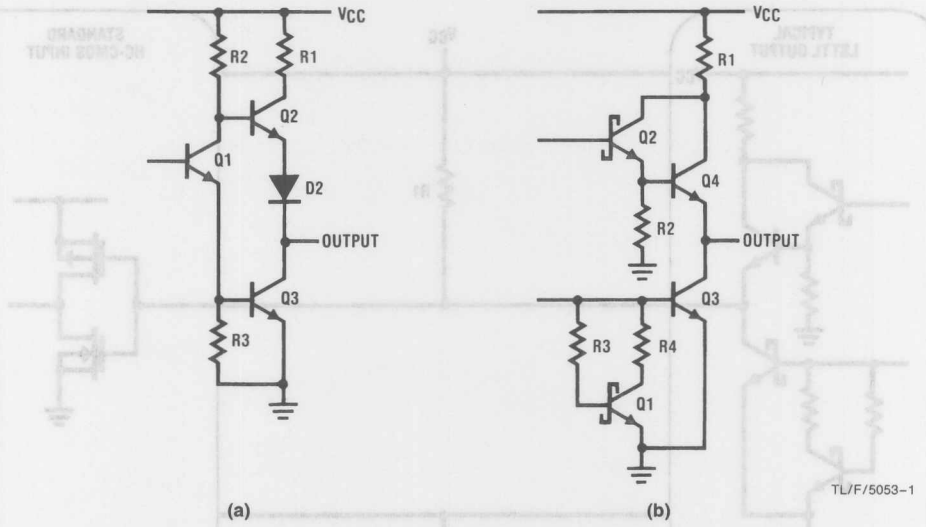
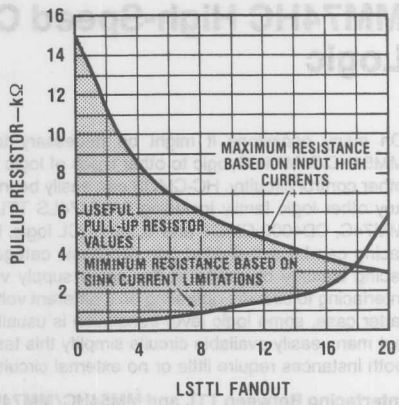


FIGURE 1. Schematic Diagrams for Typical (a) Standard and (b) Low Power Schottky TTL Outputs

Since LSTTL specifications guarantee a 2.7V output high level instead of a 3.5V output high, when designing to the worst case characteristics greater compatibility is sometimes desired. One solution to increase compatibility is to raise the output high level on the TTL output by placing a pull-up resistor from the TTL output to V_{CC}, as shown in *Figure 2*. When the output pulls up, the resistor pulls the voltage very close to V_{CC}. The value of the resistor should be chosen based on the LSTTL and CMOS fanout of the LS gate. *Figure 3* shows the range of pull-up resistors values versus LS fanout that can be used. For example, if an LSTTL device is driving only CMOS circuits, the resistor value is chosen from the left axis which corresponds to a zero LSTTL fanout.

A second solution is to use one of the many MM54HCT/MM74HCT TTL input compatible devices. These circuits have a specially designed input circuit that is compatible with TTL logic levels. Their input high level is specified at 2.0V and their input low is 0.8V with $V_{CC} = 5.0V \pm 10\%$. Thus LS can be directly connected to HC logic and the extra pull-up resistors can be eliminated. The direct interconnection of the TTL to CMOS translators is shown in *Figure 4*.

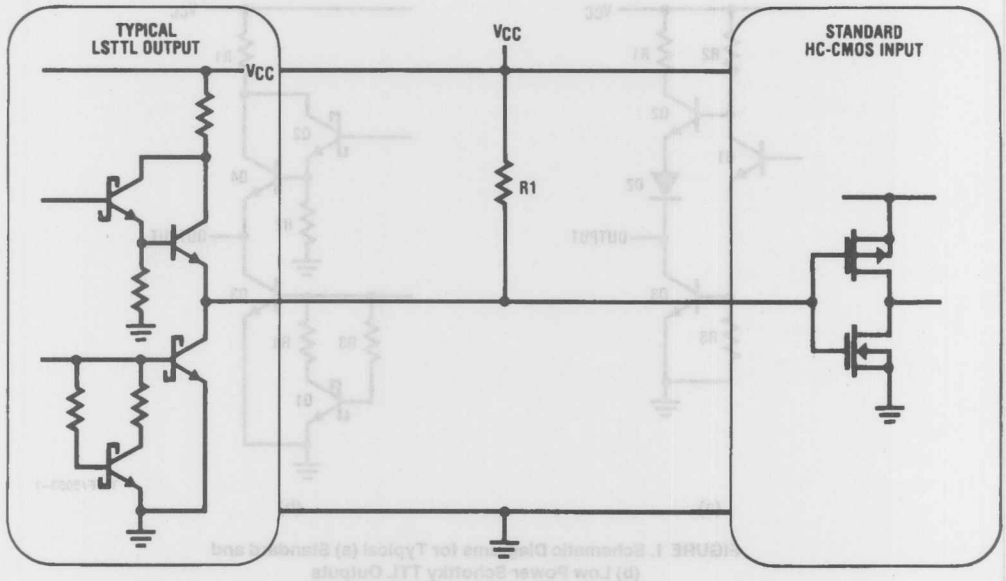
If TTL open collector outputs with a pull-up resistor are driving MM54HC/MM74HC logic, there is no interface circuitry needed as the external pull-up will pull the output to a high level very close to V_{CC}. The value of this pull-up for LS gates has the same constraints as the totem-pole outputs and its value can be chosen from *Figure 2* as well. The special TTL to CMOS buffers may also be used in this case, but they are not necessary.



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FIGURE 3. Range of Pull-Up Resistors for Low Power Schottkey TTL to CMOS Interface

When MM54HC/MM74HC outputs are driving TTL inputs, as shown in *Figure 5*, there is no incompatibility. Both the high and low output voltages are compatible with TTL. The only restriction in high-speed CMOS driving TTL is the same fanout restrictions that apply when TTL is driving TTL.



TL/F/5053–3

FIGURE 2. Interfacing LSTTL Outputs to Standard CMOS Inputs Using a Pull-Up Resistor

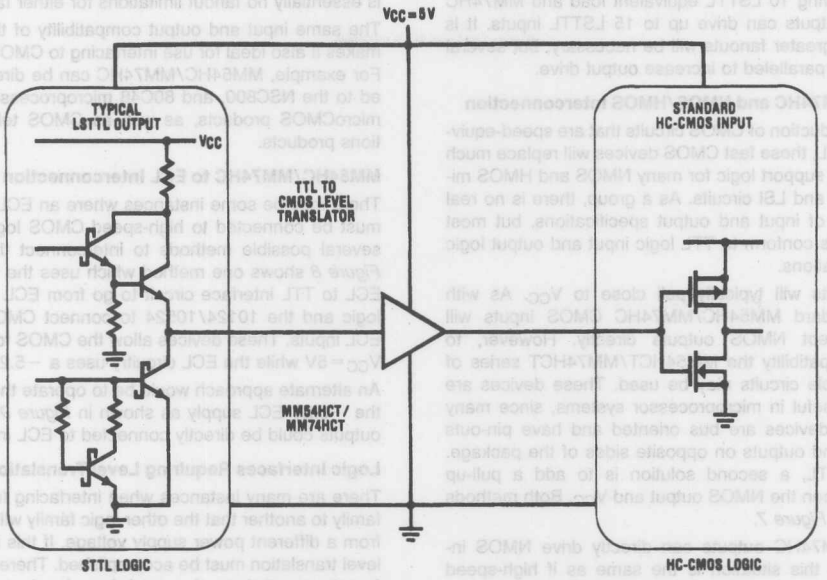


FIGURE 4. LSTTL Outputs Directly Drives MM54HCT/MM74HCT Logic Directly Which Can Interface to MM54HC/MM74HC

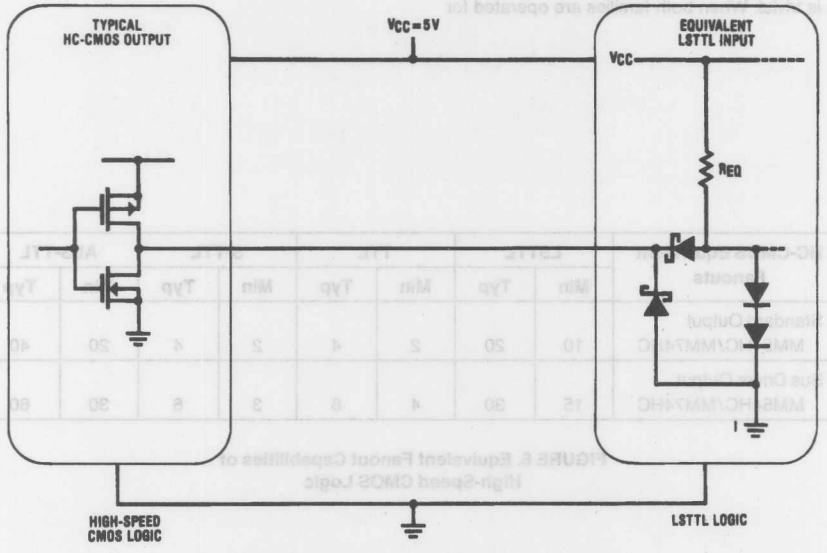


FIGURE 5. High-Speed CMOS Can Directly Connect Up to LSTTL Within its Fanout Restrictions

High-speed CMOS has much improved output drive compared to CD4000 and MM54C/MM74C metal-gate CMOS logic. *Figure 6* tabulates the fanout capabilities for this family. MM54HC/MM74HC standard outputs have a fanout capability of driving 10 LSTTL equivalent load and MM74HC bus driver outputs can drive up to 15 LSTTL inputs. It is unlikely that greater fanouts will be necessary, but several gates can be paralleled to increase output drive.

MM54HC/MM74HC and NMOS/HMOS Interconnection

With the introduction of CMOS circuits that are speed-equivalent to LSTTL, these fast CMOS devices will replace much of the bipolar support logic for many NMOS and HMOS microprocessor and LSI circuits. As a group, there is no real standard set of input and output specifications, but most NMOS circuits conform to TTL logic input and output logic level specifications.

NMOS outputs will typically pull close to V_{CC}. As with LSTTL, standard MM54HC/MM74HC CMOS inputs will typically accept NMOS outputs directly. However, to improve compatibility the MM54HCT/MM74HCT series of TTL compatible circuits may be used. These devices are particularly useful in microprocessor systems, since many of the octal devices are bus oriented and have pin-outs with inputs and outputs on opposite sides of the package. As with LSTTL, a second solution is to add a pull-up resistor between the NMOS output and V_{CC}. Both methods are shown in *Figure 7*.

MM54HC/MM74HC outputs can directly drive NMOS inputs. In fact, this situation is the same as if high-speed CMOS was driving itself. NMOS circuits have near zero input current and usually have input voltage levels that are TTL compatible. Thus MM54HC/MM74HC needs no additional circuitry to drive NMOS and there is also virtually no DC fanout restriction.

Interfacing High-Speed CMOS to MM54C/MM74C, CD4000 and CMOS-LSI

MM54HC/MM74HC CMOS and metal-gate CMOS logic interconnection is trivial. When both families are operated for the same power supply, no interface circuitry is needed. MM54HC/MM74HC, CD4000 and MM54C/MM74C logic families are completely input and output logic level compatible. Since both families have very low input currents, there is essentially no fanout limitations for either family.

The same input and output compatibility of the HC-CMOS makes it also ideal for use interfacing to CMOS-LSI circuits. For example, MM54HC/MM74HC can be directly connected to the NSC800, and 80C48 microprocessors and other microCMOS products, as well as CMOS telecommunications products.

MM54HC/MM74HC to ECL Interconnection

There may be some instances where an ECL logic system must be connected to high-speed CMOS logic. There are several possible methods to interconnect these families. *Figure 8* shows one method which uses the 10125/10525 ECL to TTL interface circuit to go from ECL to HC-CMOS logic and the 10124/10524 to connect CMOS outputs to ECL inputs. These devices allow the CMOS to operate with $V_{CC} = 5V$ while the ECL circuitry uses a $-5.2V$ supply.

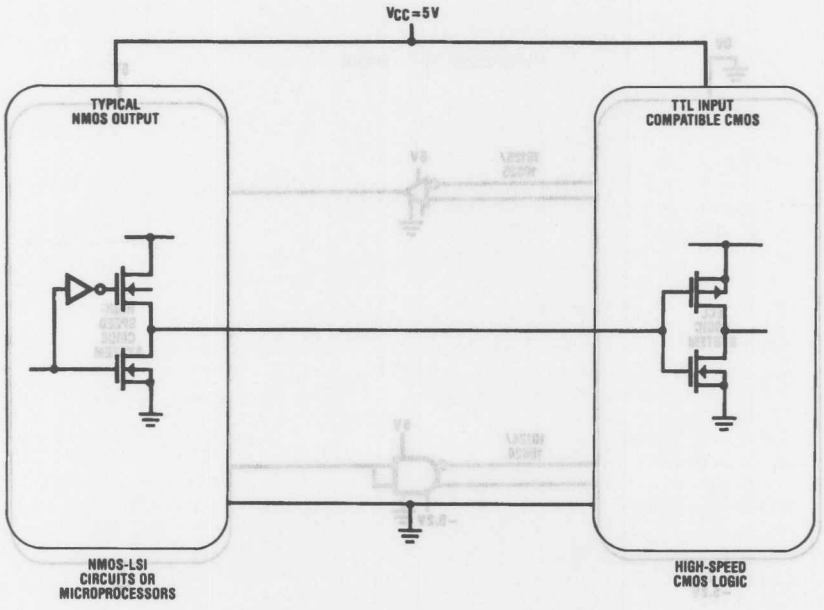
An alternate approach would be to operate the CMOS from the $-5.2V$ ECL supply as shown in *Figure 9*. Thus CMOS outputs could be directly connected to ECL inputs.

Logic Interfaces Requiring Level Translation

There are many instances when interfacing from one logic family to another that the other logic family will be operating from a different power supply voltage. If this is the case, a level translation must be accomplished. There are many different permutations of up and down level conversions that may be required. A few of the more likely ones are discussed here.

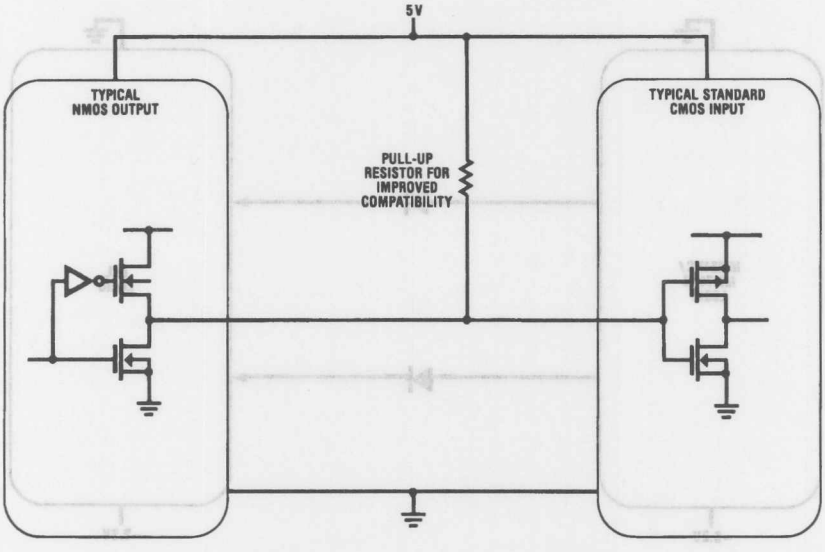
HC-CMOS Equivalent Fanouts	LSTTL		TTL		S-TTL		ALS-TTL	
	Min	Typ	Min	Typ	Min	Typ	Min	Typ
Standard Output MM54HC/MM74HC	10	20	2	4	2	4	20	40
Bus Driver Output MM54HC/MM74HC	15	30	4	8	3	6	30	60

FIGURE 6. Equivalent Fanout Capabilities of High-Speed CMOS Logic



TL/F/5053–6

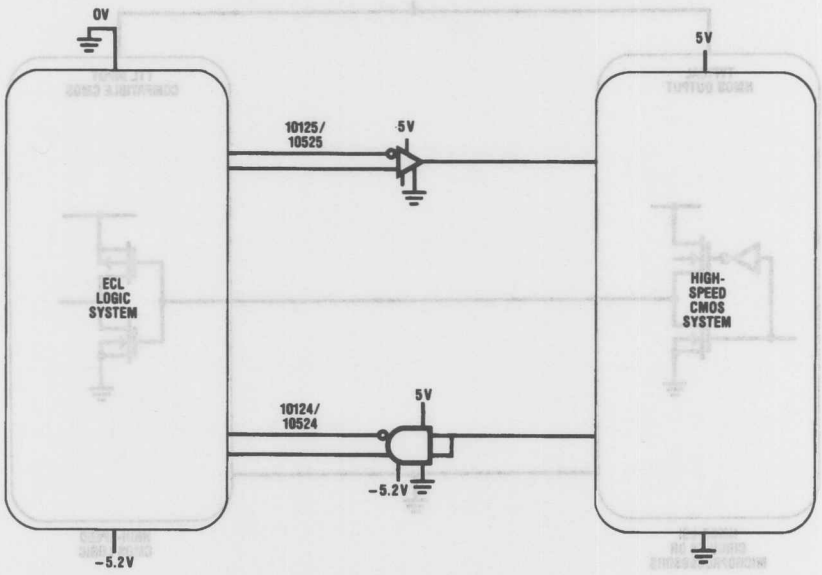
(a)



TL/F/5053–7

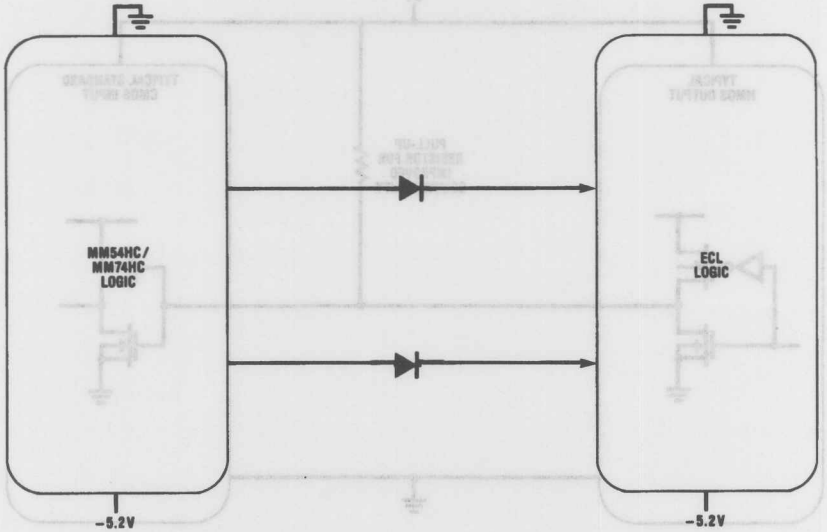
(b)

FIGURE 7. Improved Compatibility NMOS to CMOS Connection Using (a) TTL Input Compatible Devices or (b) External Pull-Up Resistors



TL/F/5053–8

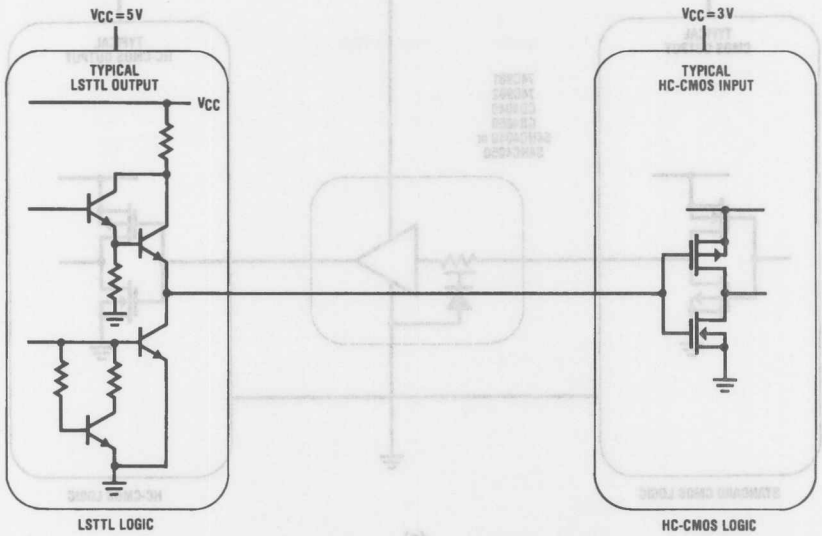
FIGURE 8. MM54HC/MM74HC to ECL and ECL to HC-CMOS Interface



TL/F/5053–9

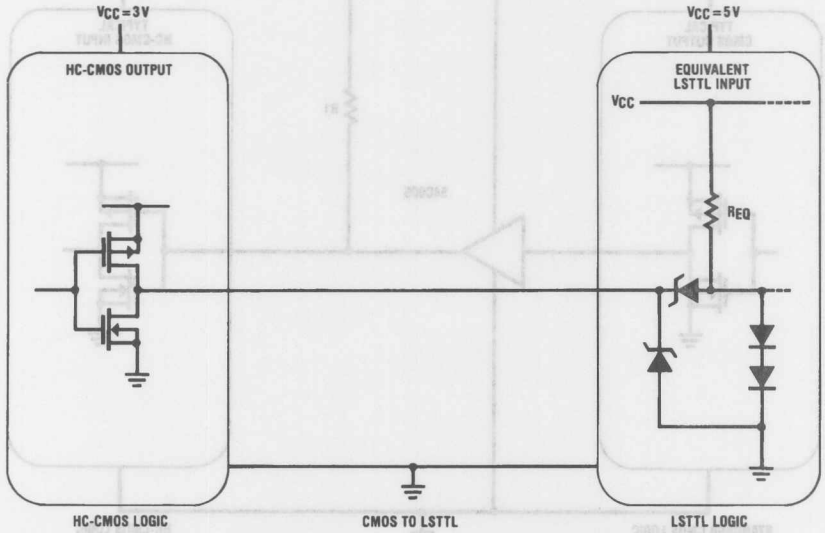
FIGURE 9. HC-CMOS Driving ECL Logic from Same Power Supply

If MM54HC/MM74HC is operated in a battery back up application for a TTL system, high-speed CMOS may be operated at $V_{CC} = 2-3V$ and can be connected to 5V TTL. CMOS operating at 3V can be directly connected to TTL since its input and output levels are compatible with TTL, and the TTL output levels are compatible with CMOS inputs, as shown in *Figure 10*. When high-speed CMOS is operated at 2V, the TTL outputs will exceed the CMOS power supply and the CMOS outputs will just barely pull high enough to drive TTL, so some level translation will be necessary.



TL/F/5053–10

(a)

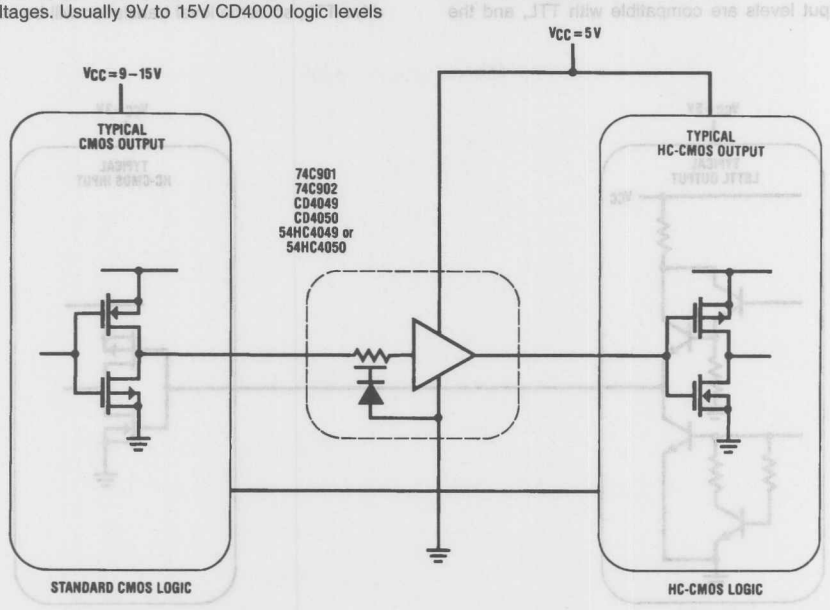


TL/F/5053–11

(b)

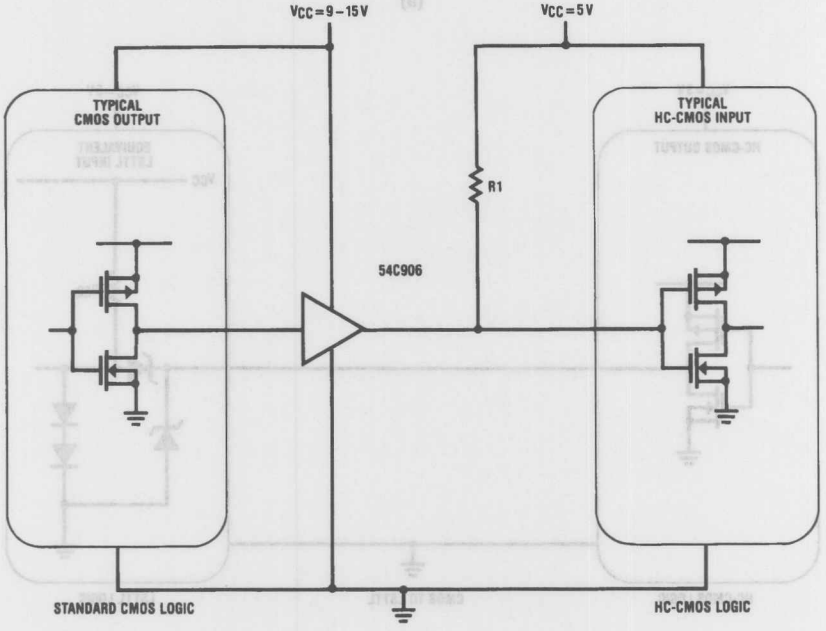
FIGURE 10. When HC-CMOS Is Operating At $V_{CC} = 3V$ No Logic Level Conversion Circuitry Is Needed

CD4000 and MM54C/MM74C metal-gate CMOS logic can be operated over a wider supply range that MM54HC/MM74HC, and because of this there will be instances when metal-gate CMOS and HC-CMOS will be operated off different supply voltages. Usually 9V to 15V CD4000 logic levels will have to be down converted to 5V high-speed CMOS levels. *Figure 11* shows several possible down conversion techniques using either a CD4049, CD4050, MM54HC4049, MM54HC4050, or MM54C906.



TL/F/5053–12

(a)



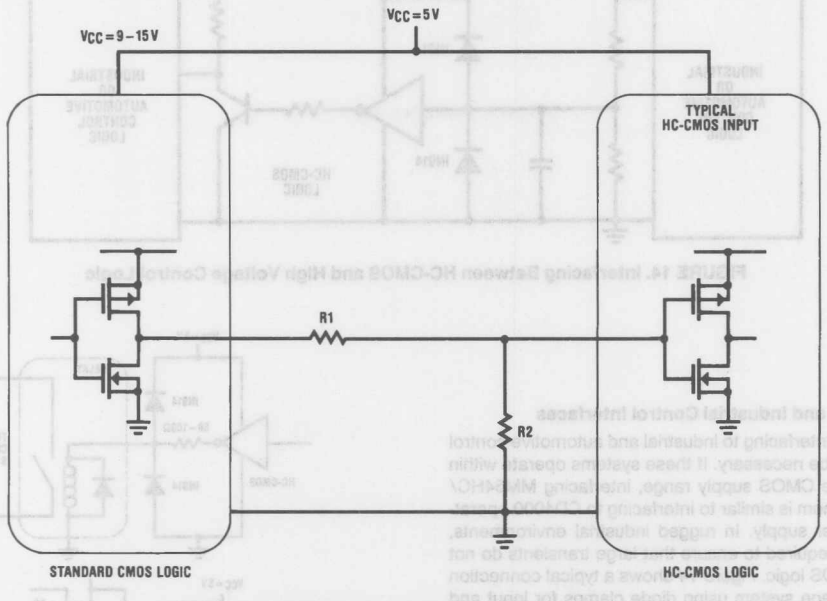
TL/F/5053–13

(b)

FIGURE 11. CD4000 or 74C Series CMOS to HC-CMOS Connection with Logic Level Conversion Using (a) Special Down Converters or (b) Open Drain CMOS

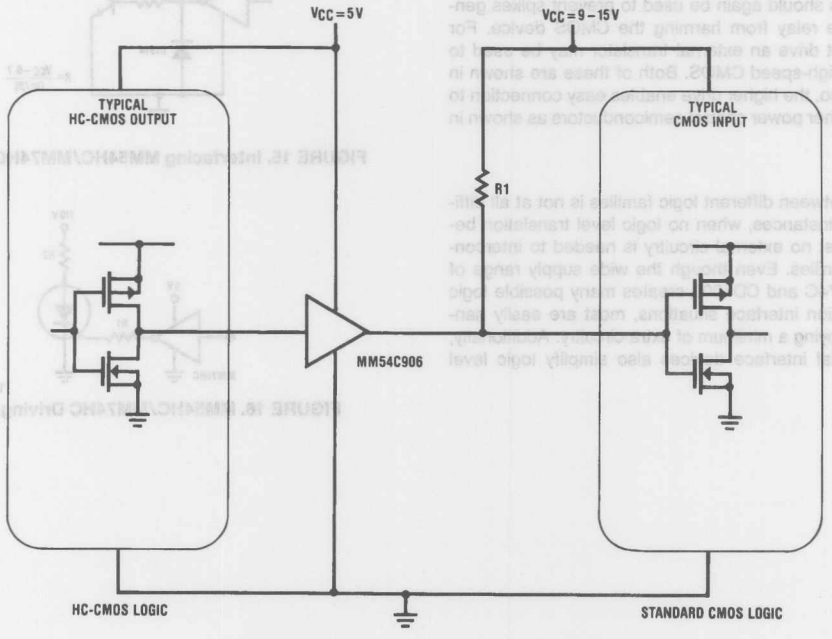
Since CMOS has a high input impedance, another possibility is to use a resistor voltage divider for down level conversion as shown in *Figure 12*. Voltage dividers will, however, dissipate some power.

Up conversion from MM54HC/MM74HC to metal-gate CMOS can be accomplished as shown in *Figure 13*. Here an MM54C906 open drain buffer with a pull-up resistor tied to the larger power supply is used.



TL/F/5053–14

FIGURE 12. CMOS to "HC" CMOS Logic Level Translation Using Resistor Divider



TL/F/5053–15

FIGURE 13. HC-CMOS to CD4000 or 74C Series CMOS Connection with Logic Level Conversion Using an Open Drain CMOS Circuit

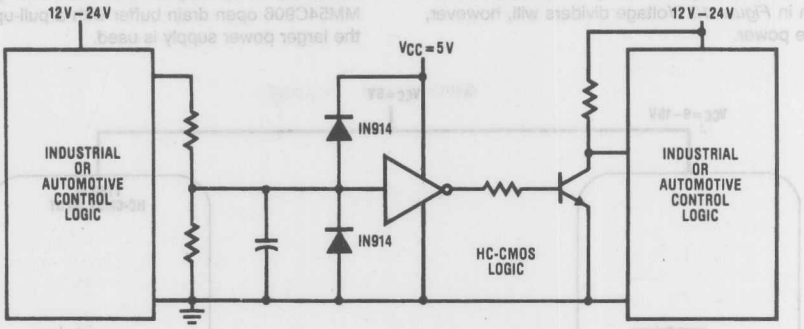


FIGURE 14. Interfacing Between HC-CMOS and High Voltage Control Logic

High Voltage and Industrial Control Interfaces

On occasion, interfacing to industrial and automotive control systems may be necessary. If these systems operate within the metal-gate CMOS supply range, interfacing MM54HC/MM74HC to them is similar to interfacing to CD4000 operating at a higher supply. In rugged industrial environments, care may be required to ensure that large transients do not harm the CMOS logic. *Figure 14* shows a typical connection to a high voltage system using diode clamps for input and output protection.

The higher drive of HC-CMOS can enable direct connection to relay circuits, but additional isolation is recommended. Clamp diodes should again be used to prevent spikes generated by the relay from harming the CMOS device. For higher current drive an external transistor may be used to interface to high-speed CMOS. Both of these are shown in *Figure 15*. Also, the higher drive enables easy connection to SCR's and other power control semiconductors as shown in *Figure 16*.

Conclusion

Interfacing between different logic families is not at all difficult. In most instances, when no logic level translation between is done, no external circuitry is needed to interconnect logic families. Even though the wide supply range of MM54C/MM74C and CD4000 creates many possible logic level conversion interface situations, most are easily handled by employing a minimum of extra circuitry. Additionally, several special interface devices also simplify logic level conversion.

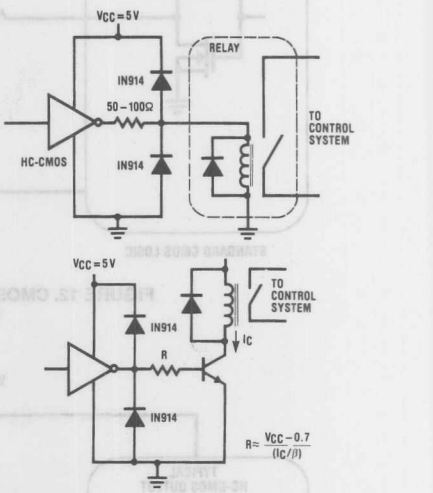


FIGURE 15. Interfacing MM54HC/MM74HC to Relays

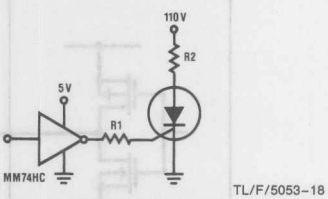


FIGURE 16. MM54HC/MM74HC Driving an SCR

AC Characteristics of MM54HC/MM74HC High-Speed CMOS

National Semiconductor
Application Note 317
Larry Wakeman

When deciding what circuits to use for a design, speed is most often a very important criteria. MM54HC/MM74HC is intended to offer the same basic speed performance as low power Schottky TTL while giving the designer the low power and high noise immunity characteristics of CMOS. In other words, HC-CMOS is about ten times faster than CD4000 and MM54C/MM74C metal-gate CMOS logic. Even though HC-CMOS logic does have speeds similar to LSTTL, there are some differences in how this family's speeds are specified, and how various parameters affect circuit performance.

To give the designer an idea of the expected performance, this discussion will include how the AC characteristics of high-speed CMOS are specified. This logic family has been specified so that in the majority of applications, the specifications can be directly applied to the design. Since it is impossible to specify a device under all possible situations, performance variations with power supply, loading and temperature are discussed, and several easy methods for determining propagation delays in nearly any situation are also described. Finally, it is useful to compare the performance of HC-CMOS to 54LS/74LS and to CD4000.

Data Sheet Specifications

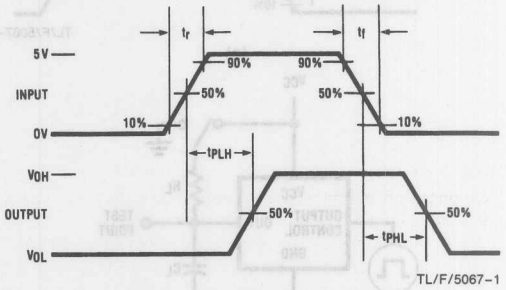
Even though the speeds achieved by this high-speed CMOS family are similar to LSTTL, the input, output and power supply characteristics are very similar to metal-gate CMOS. Because of this, the actual measurements for various timing parameters are not done the same way as TTL. The MM54HCT/MM74HCT TTL input compatible circuits are an exception.

Standard HC-CMOS AC specifications are measured at V_{CC} = 2.0V, 4.5V, 6.0V for room, military and commercial temperature ranges. Also HC is specified with LS equivalent supply (5.0V) and load conditions to enable proper comparison to low power Schottkey TTL. Input signal levels are ground to V_{CC} with rise and fall times of 6 ns (10% to 90%). Since standard CMOS logic has a logic trip point at about mid-supply, and the outputs will transition from ground to V_{CC}, timing measurements are made from the 50% points on input and output waveforms. This is shown in *Figure 1*. Using the mid-supply point gives a more accurate representation of how high-speed CMOS will perform in a CMOS system. This is different from the 1.3V measurement point and ground to 3V input waveforms that are used to measure TTL timing.

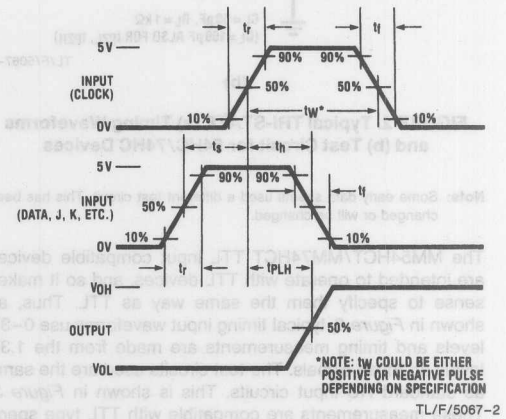
This output loading used for data sheet specifications fall into two categories, depending on the output drive capability of the specific device. The output drive categories are standard outputs (I_{OL} = 4 mA) and bus driver outputs (I_{OL} = 6 mA). Timing measurements for standard outputs are made using a 50 pF load. Bus driver circuits are measured using both a 50 pF and 150 pF load. In all AC tests, the test load capacitance includes all stray and test jig capacitances.

TRI-STATE® measurements where the outputs go from an active output level to a high impedance state, are made using the same input waveforms described above, but the timing is measured to the 10% or 90% points on the output waveforms. The test circuit load is composed of a 50 pF capacitor and a 1 kΩ resistor. To test t_{PHZ}, the resistor is swiched to ground, and for t_{PLZ} it is switched to V_{CC}. The TRI-STATE test circuit and typical timing waveforms are shown in *Figure 2*.

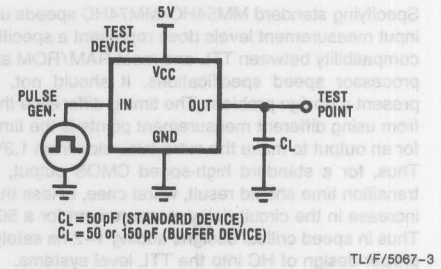
Measurements, where the output goes from the high impedance state to active output, are the same except that measurements are made to the 50% points and for bus driver devices both 50 pF and 150 pF capacitors are used.



(a)



(b)



(c)

FIGURE 1. Typical Timing Waveform for (a) Propagation Delays, and (b) Clocked Delays. Also Test Circuit (c) for These Waveforms ($t_r = t_f$ = 6 ns)

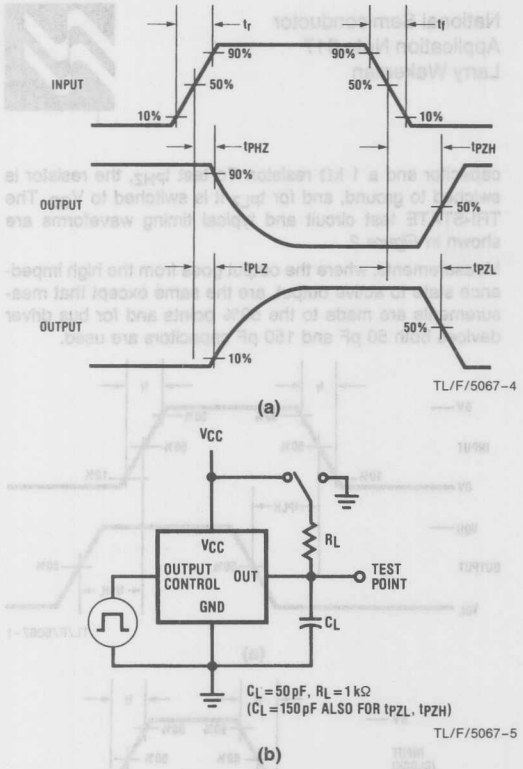


FIGURE 2. Typical TRI-STATE (a) Timing Waveforms and (b) Test Circuit for 54HC/74HC Devices

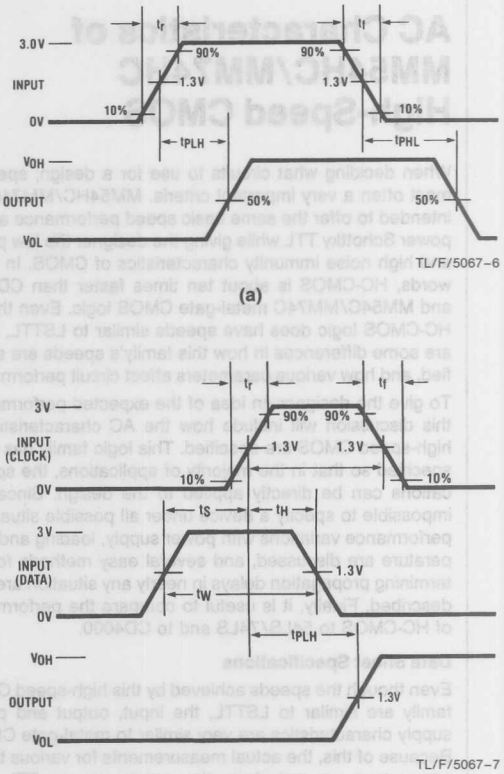


FIGURE 3. Typical Timing Waveforms for (a) Propagation Delays, and (b) Clocked Delays for 54HCT/74HCT Devices ($t_r = t_f = 6$ ns)

Note: Some early data sheets used a different test circuit. This has been changed or will be changed.

The MM54HCT/MM74HCT TTL input compatible devices are intended to operate with TTL devices, and so it makes sense to specify them the same way as TTL. Thus, as shown in *Figure 3*, typical timing input waveforms use 0–3V levels and timing measurements are made from the 1.3V levels on these signals. The test circuits used are the same as standard HC input circuits. This is shown in *Figure 3*. These measurements are compatible with TTL type specified devices.

Specifying standard MM54HC/MM74HC speeds using 2.5V input measurement levels does represent a specification incompatibility between TTL and most RAM/ROM and microprocessor speed specifications. It should not, however, present a design problem. The timing difference that results from using different measurement points is the time it takes for an output to make the extra excursion from 1.3V to 2.5V. Thus, for a standard high-speed CMOS output, the extra transition time should result, worst case, in less than a 2 ns increase in the circuit delay measurement for a 50 pF load. Thus in speed critical designs adding 1–2 ns safely enables proper design of HC into the TTL level systems.

Power Supply Affect on AC Performance

The overall power supply range of MM54HC/MM74HC logic is not as wide as CD4000 series CMOS due to performance optimization for 5V operation; however, this family can operate over a 2–6V range which does enable some versatility, especially when battery operated. Like metal-gate CMOS, lowering the power supply voltage will result in increased circuit delays. Some typical delays are shown in *Figure 4*. As the supply voltage is decreased from 5V to 2V, propagation delays increase by about two to three times, and when the voltage is increased to 6V, the delays decrease by 10–15%.

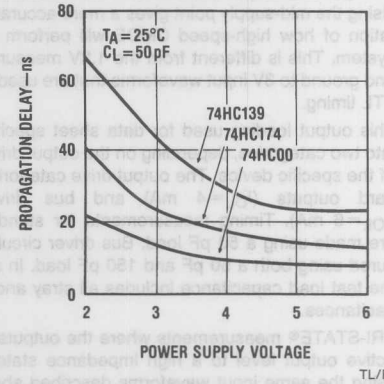


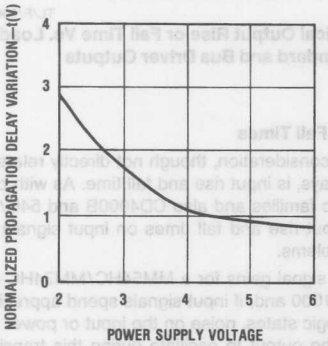
FIGURE 4. Typical Propagation Delay Variations of 74HC00, 74HC139, 74HC174 with Power Supply

In some designs it may be important to calculate the expected propagation delays for a specific situation not covered in the data sheet. This can easily be accomplished by using the normalized curve of *Figure 5* which plots propagation delay variation constant, t(V), versus power supply voltage normalized to 4.5V and 5V operation. This constant, when used with the following equation and the data sheet 5.0V specifications, yields the required delay at any power supply.

$$t_{PD}(V) = [t(V)]\,[t_{PD}(5V)] \qquad 1.0$$

Where $t_{PD}(5V)$ is the data sheet delay and $t_{PD}(V)$ is the resultant delay at the desired supply voltage. This curve can also be used for the $V_{CC}=4.5V$ specifications.

For example, to calculate the typical delay of the 74HC00 at $V_{CC}=6V$, the data sheet typical of 9 ns (15 pF load) is used. From *Figure 5* t(V) is 0.9, so the 6V delay would be 8 ns.



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FIGURE 5. MM54HCMM74HC Propagation Delay Variation Vs. Power Supply Normalized to $V_{CC}=4.5V$, and $V_{CC}=5.0V$

Speed Variation with Capacitive Loading

When high-speed CMOS is designed into a CMOS system, the load on a given output is essentially capacitive, and is the sum of the individual input capacitances, TRI-STATE output capacitances, and parasitic wiring capacitances. As the load is increased, the propagation delay increases. The rate of increase in delay for a particular device is due to the increased charge/discharge time of the output and the load. The rate at which the delay changes is dependent on the output impedance of the MM54HC/MM74HC circuit. As mentioned, for high-speed CMOS, there are two output structures: bus driver and standard.

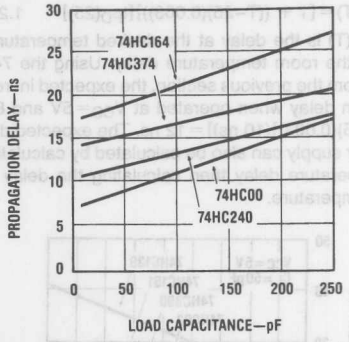
Figure 6 plots some typical propagation delay variations against load capacitance. To calculate under a particular load condition what the propagation delay of a circuit is, one need only know what the rate of change of the propagation delay with the load capacitance and use this number to extrapolate the delay from the data sheet vaue to the desired value. *Figure 7* plots this constant, t(C), against power supply voltage variation. Thus, by expanding on equation 1.0, the propagation delay at any load and power supply can be calculated using:

$$t_{PD}(C,V) = [t(C)\,(C_L - 15\text{ pF})] + [t_{PD}(5V)\,t(V)] \qquad 1.1$$

Where t(V) is the propagation delay variation with power supply constant, $t_{PD}(5V)$ is the data sheet 4.5V (use (C_L – = 50 pF) in equation) or 5V delay, C_L is the load capacitance and $t_{PD}(C,V)$ is the resultant propagation delay at the desired load and supply. This equation's first term is the difference in propagation delay from the desired load and the data sheet specification load. The second term is essentially equation 1.0. If the delay is to be calculated at $V_{CC}=5V$, then t(V) = 1 and t(C) = 0.042 ns/pF (standard output), 0.028 ns/pF (bus output).

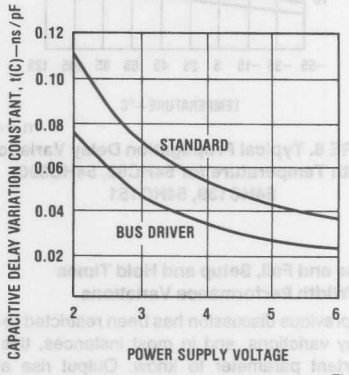
Using the previous 74HC00 example, the delay at $V_{CC}=6V$ and a 100 pF load is:

$$t_{PD}(100\text{ pF},6V) = (0.042)(100—15) + (0.9 \times 9) = 11\text{ ns}$$



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FIGURE 6. Typical Propagation Delay Variation With Load Capacitance for 74HC04, 74HC164, 74HC240, 74HC374



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FIGURE 7. Propagation Delay Capacitance Variation Constant Vs. Power Supply

Speed Variations with Change in Temperature

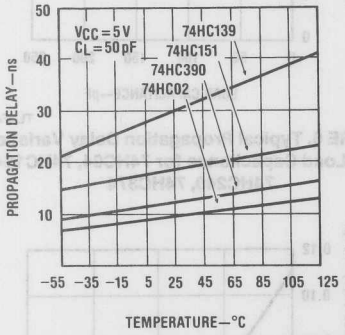
Changes in temperature will cause some change in speed. As with CD4000 and other metal-gate CMOS logic parts, MM54HC/MM74HC operates slightly slower at elevated temperatures, and somewhat faster at lower temperatures. The mechanism which causes this variation is the same as that which causes variations in metal-gate CMOS. This

Figure 8 shows some typical temperature-delay variations for some high-speed CMOS circuits. As can be seen, speeds derate fairly linearly from 25°C at about −0.3%/C. Thus, 125°C propagation delays will be increased about 30% from 25°C. 54HC/74HC speeds are specified at room temperature, −40 to 85°C (commercial temperature range), and −55 to 125°C (military range). In virtually all cases the numbers given are for the highest temperature.

To calculate the expected device speeds at any temperature, not specified in the device data sheet, the following equation can be used:

$$t_{PD}(T) = [1 + ((T-25)(0.003))][t_{PD}(25)] \qquad 1.2$$

Where $t_{PD}(T)$ is the delay at the desired temperature, and $t_{PD}(25)$ is the room temperature delay. Using the 74HC00 example from the previous section, the expected increase in propagation delay when operated at $V_{CC}=5V$ and 85°C is $[1+(85-25)(0.003)](10\ ns)]=12$ ns. The expected delay at some other supply can also be calculated by calculating the room temperature delay then calculating the delay at the desired temperature.



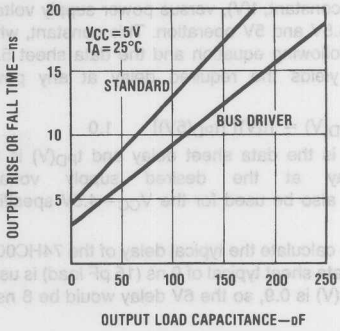
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FIGURE 8. Typical Propagation Delay Variation With Temperature for 54HC02, 54HC390, 54HC139, 54HC151

Output Rise and Fall, Setup and Hold Times and Pulse Width Performance Variations

So far, the previous discussion has been restricted to propagation delay variations, and in most instances, this is the most important parameter to know. Output rise and fall times may also be important. Unlike TTL type logic families HC specifies these in the data sheet. High-speed CMOS outputs were designed to have typically symmetrical rise and fall times. Output rise and fall time variations track very closely the propagation delay variations over temperature and supply. *Figure 9* plots rise and fall time against output load at $V_{CC}=5V$ and at room temperature. Load variation of the transition time is twice the delay variation because delays are measured at halfway points on the waveform transition.

Setup times and pulse width performance under different conditions may be necessary when using clocked logic circuits. These parameters are indirect measurements of in-



TL/F/5067–13

FIGURE 9. Typical Output Rise or Fall Time Vs. Load For Standard and Bus Driver Outputs

Input Rise and Fall Times

Another speed consideration, though not directly related to propagation delays, is input rise and fall time. As with other high-speed logic families and also CD4000B and 54C/74C CMOS, slow input rise and fall times on input signals can cause logic problems.

Typically, small signal gains for a MM54HC/MM74HC gate is greater than 1000 and, if input signals spend appreciable time between logic states, noise on the input or power supply will cause the output to oscillate during this transition. This oscillation could cause logic errors in the user's circuit as well as dissipate extra power unnecessarily. For this reason MM54HC/MM74HC data sheets recommend that input rise and fall times be shorter than 500 ns at $V_{CC}=4.5V$.

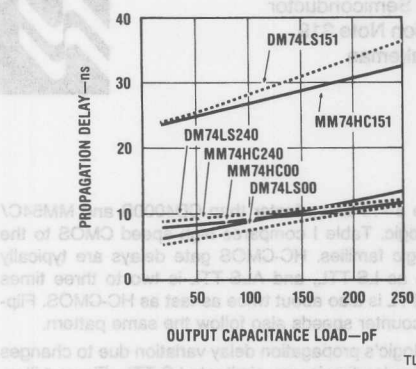
Flip-flops and other clocked circuits also should have their input rise and fall times faster than 500 ns at $V_{CC}=4.5V$. If clock input rise and fall times become too long, system noise can generate internal oscillations, causing the internal flip-flops to toggle on the wrong external clock edge. Even if no noise were present, internal clock skew caused by slow rise times could cause the logic to malfunction.

If long rise and fall times are unavoidable, Schmitt triggers ('HC14/'HC132) or other special devices that employ Schmitt trigger circuits should be used to speed up these input signals.

Logic Family Performance Comparison

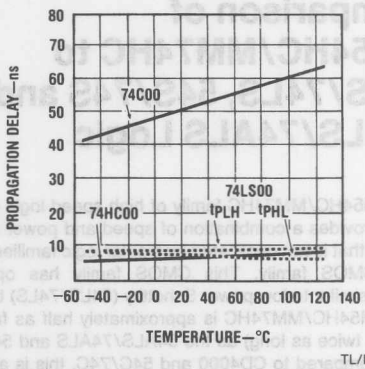
To obtain a better feeling of how high-speed CMOS compares to bipolar and other CMOS logic families, *Figure 10* plots MM54HC/MM74HC, 54LS/74LS and CD4000B logic device speeds versus output loading. HC-CMOS propagation delay and delay variation with load is nearly the same as LSTTL and about ten times faster than metal-gate CMOS. Utilizing a silicon-gate process enables achievement of LSTTL speeds, and the large output drive of this family enables the variation with loading to be nearly the same as LSTTL as well.

When comparing to CD4000 operating at 5V, HC-CMOS is typically ten times faster, and about three times faster than CD4000 logic operating at 15V. This is shown in *Figure 11*.



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FIGURE 10. Comparison of LSTTL and High-Speed CMOS Delays



TL/F/5067–16

FIGURE 12. Comparison of HC-CMOS, Metal-Gate CMOS, and LSTTL Propagation Delay Vs. Temperature

At 5V CD4000 has about a tenth the output drive of MM54HC/MM74HC and as seen in *Figure 10*, the capacitive delay variation is much larger.

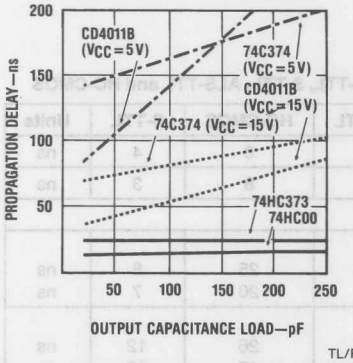
As shown in *Figure 12*, the temperature variation of HC-CMOS is similar to CD4000. This is due to the same physical phenomenon in both families. The 54LS/74LS logic family has a very different temperature variation, which is due to different circuit parameter variations. One advantage to CMOS is that its temperature variation is predictable, but with LSTTL, sometimes the speed increases and other times speed decreases with temperature.

The inherent symmetry of MM54HC/MM74HC's logic levels and rise and fall times tends to make high to low and low to high propagation delay very similar, thus making these parts easy to use.

Conclusion

High-speed CMOS circuits are speed compatible with 54LS/74LS circuits, not only on the data sheets, but even driving different loads. In general, HC-CMOS provides a large improvement in performance over older metal-gate CMOS.

By using some of the equations and curves detailed here, along with data sheet specifications, the designer can very closely estimate the performance of any MM54HC/MM74HC device. Even though the above examples illustrate typical performance calculations, a more conservative design can be implemented by more conservatively estimating various constants and using worst case data sheet limits. It is also possible to estimate the fastest propagation delays by using speeds about 0.4–0.7 times the data sheet typicals and aggressively estimating the various constants.



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FIGURE 11. Comparison of Metal-Gate CMOS and High-Speed CMOS Delays

Comparison of MM54HC/MM74HC to 54LS/74LS, 54S/74S and 54ALS/74ALS Logic

National Semiconductor
Application Note 319
Larry Wakeman

The MM54HC/MM74HC family of high speed logic components provides a combination of speed and power characteristics that is not duplicated by bipolar logic families or any other CMOS family. This CMOS family has operating speeds similar to low power Schottky (54LS/74LS) technology. MM54HC/MM74HC is approximately half as fast (delays are twice as long) as the 54ALS/74ALS and 54S/74S logic. Compared to CD4000 and 54C/74C, this is an order of magnitude improvement in speed, which is achieved by utilizing an advanced 3.5 micron silicon gate-recessed oxide CMOS process. The MM54HC/MM74HC components are designed to retain all the advantages of older metal gate CMOS, plus provide the speeds required by today's high speed systems.

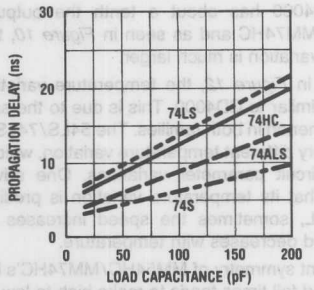
Another key advantage of the MM54HC/MM74HC family is that it provides the functions and pin outs of the popular 54LS/74LS series logic components. Many functions which are unique to the CD4000 metal gate CMOS family have also been implemented in this high speed technology. In addition, the MM54HC/MM74HC family contains several special functions not previously implemented in CD4000 or 54LS/74LS.

Although the functions and the speeds are the same as 54LS/74LS, some of the electrical characteristics are different from either LS-TTL, S-TTL or ALS-TTL. The following discusses these differences and highlights the advantages and disadvantages of high speed CMOS.

AC PERFORMANCE

As mentioned previously, the MM54HC/MM74HC logic family has been designed to have speeds equivalent to LS-TTL, and to be 8–10 times faster than CD4000B and MM54C/MM74C logic. Table I compares high speed CMOS to the bipolar logic families. HC-CMOS gate delays are typically the same as LS-TTL, and ALS-TTL is two to three times faster. S-TTL is also about twice as fast as HC-CMOS. Flip-flop and counter speeds also follow the same pattern.

Also, HC logic's propagation delay variation due to changes in capacitive loading is very similar to LS-TTL. *Figure 1* illustrates this by plotting delay versus loading for the various bipolar logic families and MM54HC/MM74HC. HC-CMOS has virtually the same speed and load-delay variation as



TL/F/5101–1

FIGURE 1. HC, LS, ALS, S Comparison of Propagation Delay vs Load for a NAND Gate

TABLE I. Comparison of Typical AC Performance of LS-TTL, S-TTL, ALS-TTL and HC-CMOS

Gates		LS-TTL	ALS-TTL	HC-CMOS	S-TTL	Units
74XX00	Propagation Delay	8	5	8	4	ns
74XX04	Propagation Delay	8	4	8	3	ns
Combinational MSI						
74XX139	Propagation Delay					
	Select	25	8	25	8	ns
	Enable	21	8	20	7	ns
74XX151	Propagation Delay					
	Address	27	8	26	12	ns
	Strobe	26	7	17	12	ns
74XX240	Propagation Delay	12	3	10	5	ns
	Enable/Disable Time	20	7	17	10	ns
Clocked MSI						
74XX174	Propagation Delay	20	7	18	13	ns
	Operating Frequency	40	50	50	100	MHz
74XX374	Propagation Delay	19	7	16	11	ns
	Enable/Disable Time	21	9	17	11	ns
	Operating Frequency	50	50	50	100	MHz

LS-TTL and, as is expected, is slower than ALS and S-TTL logic. The slopes of these lines indicate the amount of variation in speed with loading, and are dependent on the output impedance of the particular logic gate. The delay variation of LS-TTL and HC-CMOS is similar whereas ALS-TTL and S-TTL have slightly less variation.

POWER DISSIPATION

CD4000B and MM54C/MM74C CMOS devices are well known for extremely low quiescent power dissipation, and high speed CMOS retains this feature. Table II compares typical HC static power consumption with LS, ALS and S-TTL. Even CMOS MSI dissipation is well below 1 μW while LS-TTL dissipation is many milliwatts. This makes MM54HC/MM74HC ideal for battery operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

TABLE II. Comparison of Typical Quiescent Supply Current for Various Logic Families

	HC-CMOS	LS-TTL	ALS-TTL	S-TTL
SSI	0.0025 μW	5.0 mW	2.0 mW	75 mW
Flip-Flop	0.005 μW	20.0 mW	10 mW	150 mW
MSI	0.25 μW	90 mW	40 mW	470 mW

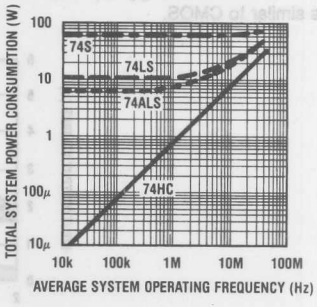
CMOS dissipation increases proportionately with operating frequency. Doubling the operating frequency doubles the current consumption. This is due to currents generated by charging internal and load capacitances. *Figure 2* shows power dissipation versus frequency for a completely unloaded NAND gate, flip-flop and counter implemented in all 4 technologies.

The LS, S and ALS curves are essentially flat because the quiescent currents mask out capacitive effects, except at very high frequencies. Capacitive effects are slightly lower for the TTL families, so that, at high frequencies, CMOS dissipation may actually be more than ALS and LS. However, the power crossover frequency is usually well above the maximum operating frequency of MM54HC/MM74HC.

The previously mentioned curves plot unloaded circuits. When considering typical system power consumption, capacitive loading should also be considered. Table III lists components to implement all the support logic for a small microprocessor based system. By assuming a typical load capacitance of 50 pF, the power dissipation for these devices can be calculated at various average system clock frequencies. *Figure 3* plots power consumption for 74HC, 74LS, 74ALS and 74S logic implementations. Above 1 MHz, capacitive currents now also tend to dominate bipolar power dissipation as well.

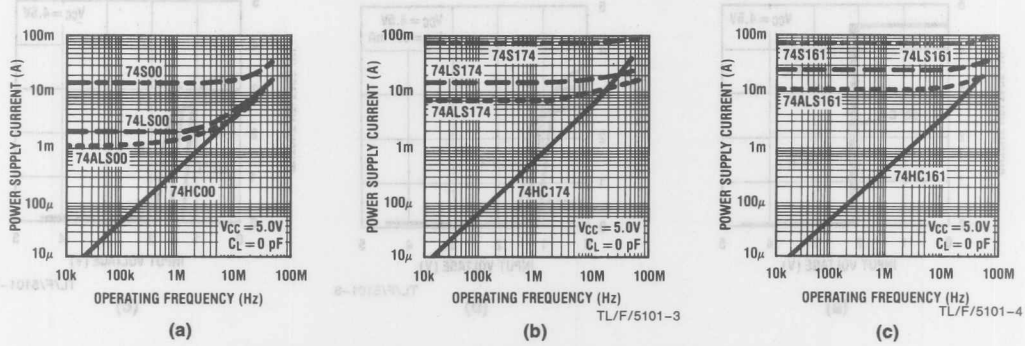
TABLE III. Hypothetical "Glue" Logic for a Typical Microprocessor System

System Components	# of ICs
Address Decoders ('138)	10
Address Comparators ('688)	5
Address/Data Buffers ('240/4)	10
Address/Data Latches ('373/4)	20
MSI Control/Gating ('00, '10)	30
Misc. Counter/Shift Reg ('161, '164)	20
Flip-Flops ('73/4)	10



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FIGURE 3. Power Consumption for Hypothetical Microprocessor System Support Logic



TL/F/5101–3

TL/F/5101–4

FIGURE 2. Supply Current Consumption Comparison for (a) 74XX00 (b) 74XX714 (c) 74XX161 Circuits

Since, in a typical system, some sections will operate at a high frequency and other parts at lower frequencies, the average system clock frequency is a simplification. For example, a 10 MHz microprocessor will have a bus cycle frequency of 2 to 5 MHz. Most system and memory components will be accessed a small amount of the time, resulting in effective clock frequencies on the order of 100 kHz for these sections. Thus, the average system clock frequency would be around 1 to 2 MHz, and an 8 to 1 power savings would be realized by using CMOS.

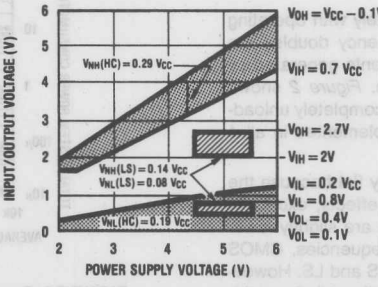
Another simplification was made to calculate system power. CMOS circuits will dissipate much less power when TRI-STATE®, which would save much power since, in a given bus cycle, only a few buffers will be enabled. LS, ALS and S, however, actually dissipate more power when their outputs are disabled.

Several interesting conclusions can be drawn from *Figure 3*. First, notice that, at higher frequencies, the bipolar logic families start to dissipate more power. This is a result of current consumption due to switching the load. As the operating frequency approaches infinity, this will be the dominant effect. So, for extremely fast low power systems, minimizing load capacitance and overall operating frequency becomes more important. As lower power TTL logic is introduced, system power will be increasingly dependent on capacitive load effects similar to CMOS.

Second, TTL logic has a slightly smaller logic voltage swing than CMOS. Thus, for a given load, TTL will actually have a lower average load current. So, similar to the unloaded example, at very high frequencies, CMOS could consume more power than TTL. As *Figure 5* indicates, these frequencies are usually far above the 30 MHz limit of HC-CMOS or LS-TTL.

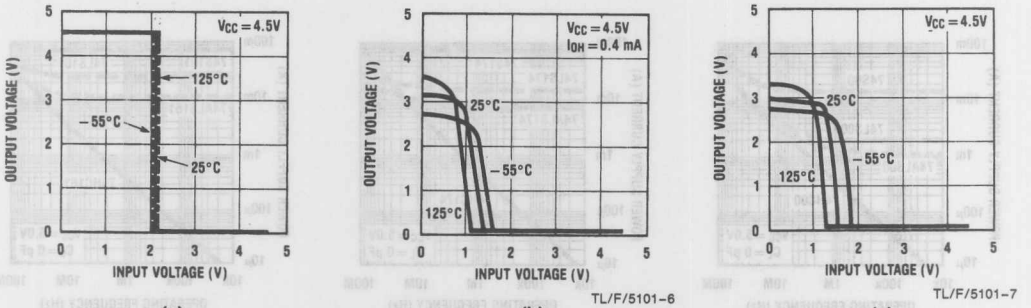
INPUT VOLTAGE CHARACTERISTICS AND NOISE IMMUNITY

To maintain the advantage CMOS has in noise immunity, the input logic levels are defined to be similar to metal gate CMOS. At $V_{CC}=5V$, MM54HC/MM74HC is designed to have input voltages of $V_{IH}=3.5V$ and $V_{IL}=1.0V$. Additionally, input voltage over the operating supply voltage range is: $V_{IH}=0.7V_{CC}$ and $V_{IL}=0.2V_{CC}$. This compares to $V_{IH}=2.0V$ and $V_{IL}=0.8V$ specified for LS-TTL over its supply range. *Figure 4* illustrates the input voltage differences, and the greater noise immunity HC logic has over its supply range. Maintaining wide noise immunity gives HC-CMOS an advantage in many industrial, automotive, and computer applications where high noise levels exist.



TL/F/5101–5

FIGURE 4. Worst-Case Input and Output Voltages Over Operating Supply Range for HC and LS Logic



TL/F/5101–6

TL/F/5101–7

FIGURE 5. Input-Output Transfer Characteristics for 74XX00 NAND Gate Implemented in (a) HC-CMOS (b) LS-TTL (c) ALS-TTL

Another indication of DC noise immunity is the typical transfer characteristics for the logic families. *Figure 5* shows the transfer function of the 74XX00 NAND gate for HC-CMOS, LS-TTL and ALS-TTL. High speed CMOS has a very sharp transition typically at 2.25V, and this transition point is very stable over temperature. The bipolar logic transfer functions are not as sharp and vary several hundred millivolts over temperature. This sharp transition is due to the large circuit gains provided by triple buffering the HC-CMOS gate compared to the single bipolar gain stage. *Figure 6* compares the transfer function of the 'HC08 and the 'ALS08, both of which are double buffered. The 'ALS08 has a sharper transition, but the CMOS gate still has less temperature variation and a more centered trip point. However, the TTL trip point is not dependent on V_{CC} variation as CMOS is.

The high speed CMOS input levels are not totally compatible with TTL output voltage specifications. To make them compatible would compromise noise immunity, die size, and significant speed. The designer may improve compatibility by adding a pull-up resistor to the TTL output. He may also utilize a series of TTL-to-CMOS level converters which are being provided to ease design of mixed HC/LS/ALS/S systems. These buffers have 0.8V and 2.0V TTL input voltage specifications, and provide CMOS compatible outputs. When mixing logic, the noise immunity at the TTL to CMOS interface is no better than LS-TTL, but a substantial savings in power will occur when using MM54HC/MM74HC logic.

INPUT CURRENT

The HC family maintains the ultra-low input currents typical of CMOS circuits. This current is less than 1 μA and is caused by input protection diode leakages. This compares to the much larger LS-TTL input currents of 0.4 mA for a low input and 40 μA for a high input. ALS-TTL input currents are 0.2 mA and 20 μA and S-TTL input currents are 3.2 mA and 100 μA. *Figure 7* tabulates these values. The near zero input current of CMOS eases designing, since a typical input can be viewed as an open circuit. This eliminates the need for fanout restrictions which are necessary in TTL logic designs.

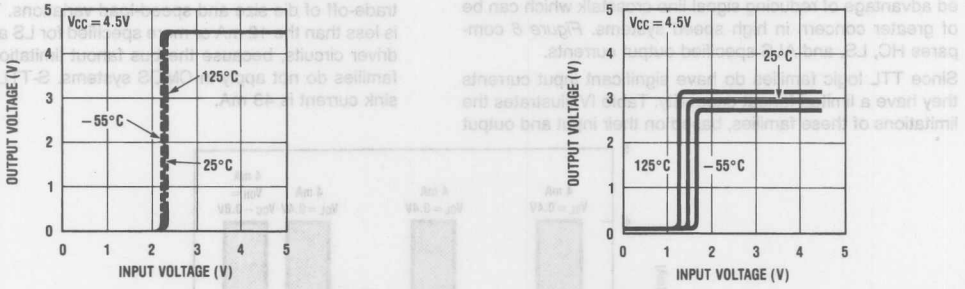


FIGURE 6. Input-Output Transfer Characteristics for 74XX08 AND Gate Implemented in (a) HC-CMOS (b) ALS-TTL

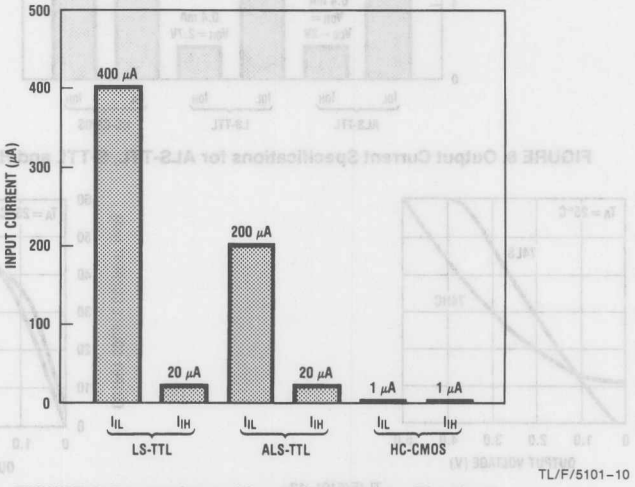


FIGURE 7. Comparison of Input Current Specifications for Various Logic Families

POWER SUPPLY RANGE

Figure 4 also compares the supply range of MM54HC/MM74HC logic and LS-TTL. The high speed CMOS family is specified to operate at voltages from 2V to 6V. 54LS, 54S and 54ALS logic is specified to operate from 4.5V to 5.5V, and 74LS and 74S will operate from 4.75V to 5.25V. 74ALS is specified over a 4.5V to 5.5V supply range. This wider operating range for the HC family eases power supply design by eliminating costly regulators and enhances battery operation capabilities.

OUTPUT DRIVE

Since there was no speed, noise immunity, or power tradeoff, standard HC-CMOS was designed to have similar high current output drive that is characteristic of LS-TTL and ALS-TTL. Schottky TTL has about 5 times the output drive of MM54HC/MM74HC. Thus HC-CMOS has an output low current specification of 4 mA at an output voltage of 0.4V. In keeping with CD4000B series and 54C/74C series logic, the source and sink currents are symmetrical. Thus HC logic can source 4 mA as well. This large increase in output current for high speed CMOS over CD4000B also has the added advantage of reducing signal line crosstalk which can be of greater concern in high speed systems. *Figure 8* compares HC, LS, and ALS specified output currents.

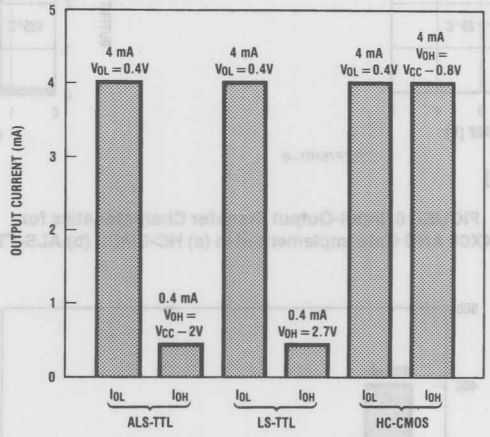
Since TTL logic families do have significant input currents they have a limited fanout capability. Table IV illustrates the limitations of these families, based on their input and output currents. High speed CMOS is also included. MM54HC/MM74HC has the same CMOS-to-CMOS fanout characteristics as CD4000B, virtually infinite.

TABLE IV. Fanout of HC-CMOS, LS-TTL, ALS-TTL, S-TTL

From, To	74HC	74LS	74ALS	74S
74HC	4000	10	20	2
74LS	*	20	40	4
74ALS	*	20	40	4
74S	*	50	100	10

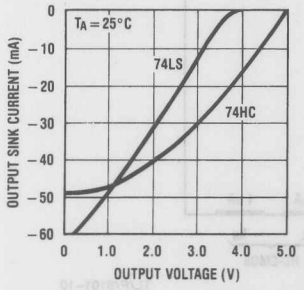
As another indication of the similarity of HC-CMOS to LS-TTL, *Figure 9* plots typical output currents versus output voltage for LS and HC. The output sink current curves are very similar, but LS source current is somewhat different, due to its emitter-follower output circuitry.

MM54HC/MM74HC bus driving circuits, namely the TRI-STATE buffers and latches, have half again as much output current drive as standard outputs. These components have a 6 mA output drive. The 6 mA was chosen based on a trade-off of die size and speed-load variations. This current is less than the 12 mA or more specified for LS and ALS bus driver circuits, because the bus fanout limitations of these families do not apply in CMOS systems. S-TTL bus output sink current is 48 mA.



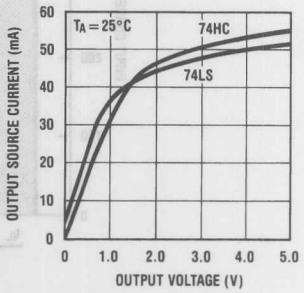
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FIGURE 8. Output Current Specifications for ALS-TTL, S-TTL and HC-CMOS



TL/F/5101–12

(a)



TL/F/5101–13

(b)

FIGURE 9. Comparison of Standard LS-TTL and HC-CMOS Output (a) Source (b) Sink Currents

OPERATING TEMPERATURE RANGE

The operating temperature range and temperature effects on various HC-CMOS operating parameters differ from bipolar logic. The recommended temperature range for 74LS, 74S, and 74ALS is 0°C to 70°C, compared to −40°C to 85°C for the 74HC family. 54 series logic is specified from −55°C to 125°C for all four families.

Temperature variation of operating parameters for the MM54HC/MM74HC family behaves very predictably and is due to the gain decreasing of MOSFET transistors as temperature is increased. Thus the output currents decrease and propagation delays increase at about 0.3% per degree centigrade.

Figure 10 shows typical propagation delays for the 74XX00 over the −55°C to +125°C temperature range. The 'HC00's speed increases almost linearly with temperature, whereas the LS and ALS behave differently.

A WORD ABOUT PLUG-IN REPLACEMENT OF TTL

MM54HC/MM74HC logic implements TTL equivalent functions with the same pin outs as TTL. HC is not designed to be directly plug-in replaceable, but, with some care, some TTL systems can be converted to MM54HC/MM74HC with little or no modification. The replaceability of HC is determined by several factors.

One factor is the difference in input levels. In systems where all TTL is not being replaced and TTL outputs feed CMOS inputs, the input high voltages, as specified, are not totally compatible. Although TTL outputs will typically drive HC inputs correctly, an external pull-up resistor should be added to the TTL outputs, or an MM54HCT/MM74HCT TTL compatible circuit should be used. This incompatibility tends to limit the designer's ability to intermingle TTL and HC-CMOS. Note, though, that HC outputs are completely compatible with the various TTL family's input specifications; therefore, there is no problem when HC is driving TTL.

Another source of possible problems can occur when the LS design floats device inputs. This practice is not recommended when using LS-TTL, but it is sometimes done. Usually, TTL inputs float high; however, CMOS inputs may float either high or low depending on the static charge on the input. It is therefore important to always tie unused CMOS inputs to either V_{CC} or ground to avoid incorrect logic functioning.

A third factor to consider when replacing any TTL logic is AC performance. The logic functions provided by 54HC/74HC are equivalent to LS-TTL, and the propagation delay, set-up and hold times are similar to LS. However, there are some differences in the way CMOS circuits are implemented which will cause differences in speed. For the most part, these differences are minor, but it is important to verify that they do not affect the design.

CONCLUSION

The MM54HC/MM74HC family represents a major step forward in CMOS performance. It is a full line family capable of being designed into virtually any application which now uses LS-TTL with substantial improvement in power consumption. ALS and S-TTL primarily offer faster speeds than HC-CMOS, but still do not have the input and output advantages or the lower power consumption of CMOS. Because of its high input impedance and large output drive, HC logic is actually easier to use. This, coupled with continued expansion of the 54HC/74HC, will make it an increasingly popular logic family.

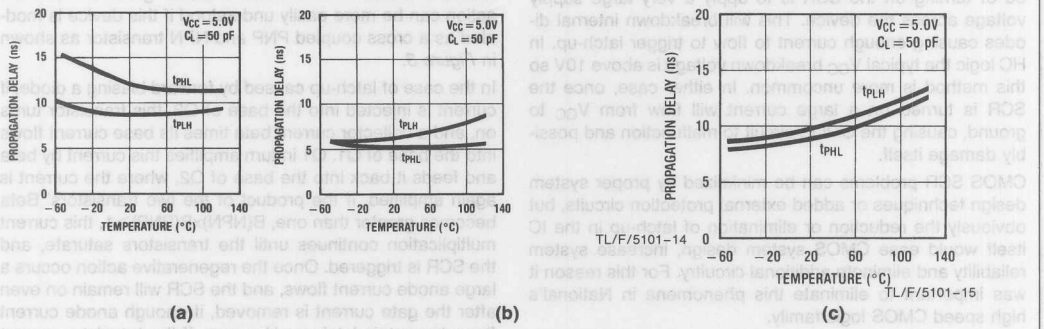


FIGURE 10. Propagation Delay Variation Across Temperature for (a) 74LS00 (b) 74ALS00 and (c) 74HC00

Latch-Up Problem In 54HC/74HC Logic

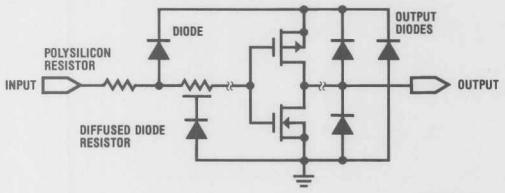
INTRODUCTION

SCR latch-up is a parasitic phenomena that has existed in circuits fabricated using bulk silicon CMOS technologies. The latch-up mechanism, once triggered, turns on a parasitic SCR internal to CMOS circuits which essentially shorts V_{CC} to ground. This generally destroys the CMOS IC or at the very least causes the system to malfunction. In order to make MM54HC/MM74HC high speed CMOS logic easy to use and reliable it is very important to eliminate latch-up. This has been accomplished through several layout and process enhancements. It is primarily several proprietary innovations in CMOS processing that eliminates the SCR.

First, what is "SCR latch-up?" It is a phenomena common to most monolithic CMOS processes, which involves "turning on" a four layer thyristor structure (P-N-P-N) that appears from V_{CC} to ground. This structure is formed by the parasitic substrate interconnections of various circuit diffusions. It most commonly can be turned on by applying a voltage greater than V_{CC} or less than ground any input or output, which forward biases the input or output protection diodes. *Figure 1* schematically illustrates these diodes found in the MM54HC/MM74HC family. Standard CD4000 and MM54C/MM74C logic also has a very similar structure. These diodes can act as the gate to the parasitic SCR, and if enough current flows the SCR will trigger. A second method of turning on the SCR is to apply a very large supply voltage across the device. This will breakdown internal diodes causing enough current to flow to trigger latch-up. In HC logic the typical V_{CC} breakdown voltage is above 10V so this method is more uncommon. In either case, once the SCR is turned on a large current will flow from V_{CC} to ground, causing the CMOS circuit to malfunction and possibly damage itself.

CMOS SCR problems can be minimized by proper system design techniques or added external protection circuits, but obviously the reduction or elimination of latch-up in the IC itself would ease CMOS system design, increase system reliability and eliminate additional circuitry. For this reason it was important to eliminate this phenomena in National's high speed CMOS logic family.

Characterization of this proprietary high speed CMOS process for latch up has verified the elimination of this parasitic mechanism. In tests conducted under worst case conditions ($V_{CC}=7V$ and $T_A=125°C$) it has been impossible to latch-up these devices on the inputs or on the outputs.



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FIGURE 1. Schematic Diagram of Input and Output Protection Structures

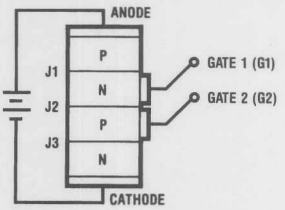
In testing for latch-up, caution must be exercised when trying to force large currents into an IC. As with any integrated circuit there are maximum limitations to the current handling capabilities of the internal metalization, and diodes, and thus they can be damaged by excessive currents. This is discussed later in the test section.

To enable the user to understand what latch-up is and how it has been eliminated, it is useful to review the operating of a simple discrete SCR, and then apply this to the CMOS SCR. Since most latch-up problems historically have been caused by extraneous noise and system transients, the AC characteristics of CMOS latch are presented. Also various methods of external and internal protection against latch-up is discussed as well as example test methods for determining the latch up susceptibility of CMOS IC's.

SIMPLE DISCRETE SCR OPERATION

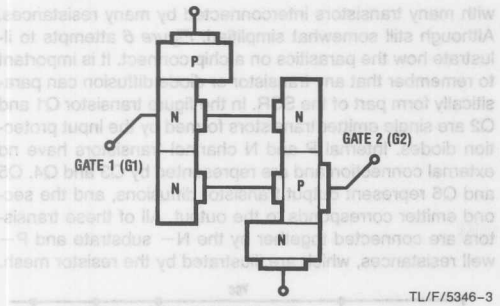
To understand the behavior of the SCR structure parasitic to CMOS IC's, it is first useful to review the basic static operation of the discrete SCR, and then apply it to the CMOS SCR. There are two basic trigger methods for this SCR. One is turning on the SCR by forcing current into its gate, and the second is by placing a large voltage across its anode and cathode. *Figure 2* shows the basic four layer structure biased into its forward blocking state. The SCR action can be more easily understood if this device is modeled as a cross coupled PNP and NPN transistor as shown in *Figure 3*.

In the case of latch-up caused by forward biasing a diode, if current is injected into the base of Q2, this transistor turns on, and a collector current beta times its base current flows into the base of Q1. Q1 in turn amplifies this current by beta and feeds it back into the base of Q2, where the current is again amplified. If the product of the two transistors' Beta becomes greater than one, $B(NPN)xB(PNP)>1$, this current multiplication continues until the transistors saturate, and the SCR is triggered. Once the regenerative action occurs a large anode current flows, and the SCR will remain on even after the gate current is removed, if enough anode current flows to sustain latch-up. However, if the transistor current gains are small no self sustaining positive feedback will occur, and when the base current is removed the collector current will stop. In a similar manner the SCR can be triggered by drawing current by forward biasing the base of Q1.



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FIGURE 2. Simplified SCR Structure



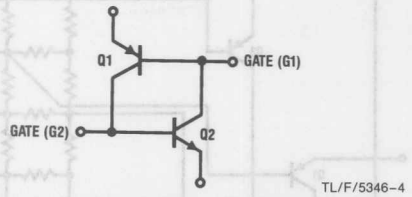


FIGURE 3. Cross-Coupled Transistor Model of SCR

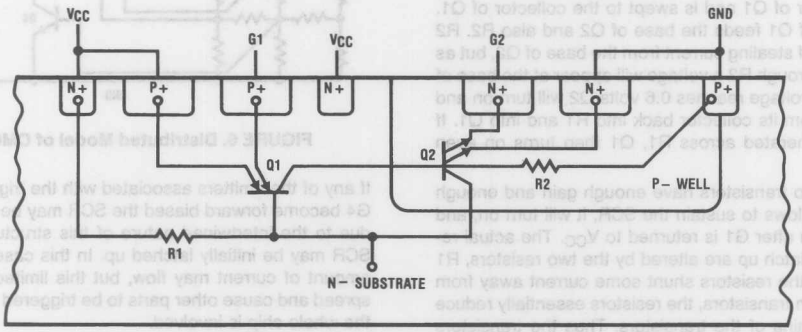
The second case, the SCR may also be triggered without injecting any gate current. In the forward blocking state the small leakage current that is present does not trigger the SCR, but if the voltage is increased to a point where significant leakage currents start conducting, these currents could also trigger the SCR, again forming a low impedance path through the device. The same requirement that the Beta product of the PNP and NPN be greater than one in order for the SCR to trigger applies here as well. This leakage current trigger is characteristic of Schottky diode operation.

THE CMOS SCR: STATIC DC OPERATION

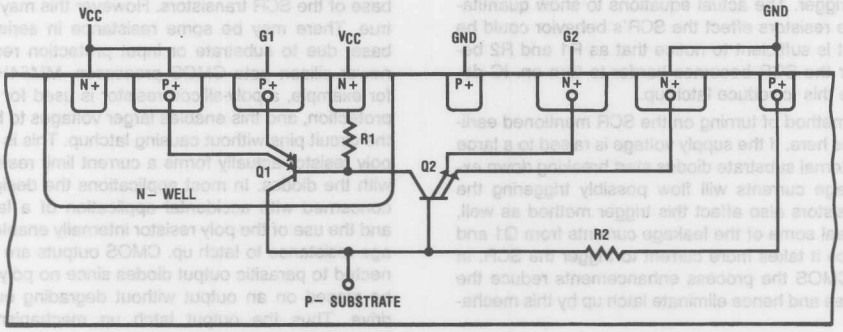
For discussion purposes CMOS SCR latch up characteristics can be divided into two areas. One is the basic operation of the SCR when static DC voltages are applied, and the second is the behavior when transients or pulses are applied.

First looking at the device statically, the parasitic SCR in CMOS integrated circuits is much more complex and its triggering is somewhat different than the simple SCR already discussed. However, the regenerative feedback effect is basically the same. *Figure 4a* shows a simplified P− well CMOS structure illustrating only the diffusions and the resultant parasitic transistors. The NPN transistor is a vertical device whose emitter is formed by n+ diffusions. The P− well forms the base and the N− substrate forms the collector of the NPN. The PNP transistor is a lateral device. Its emitter is formed by p+ diffusions, its base is the N− substrate, and its collector is the P− well.

Figure 4b illustrates a cross section of a simplified N− well process and its corresponding parasitic bipolar transistors. In this process the NPN is a lateral device and the PNP is vertical. Essentially the description of the P− well SCR is the same as the N− well version except the NPN is a low gain lateral device and the PNP is a high gain vertical transistor. Thus the following discussion for the P− well also applies to the N− well with this exception.



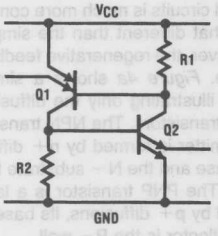
(a)



(b)

FIGURE 4. Simplified Cross Section of CMOS Processes a) P− well and b) N− well

The transistors for the P− well CMOS process are drawn schematically in *Figure 5*, so that their cross coupled interconnection is more easily seen. The SCR structure in *Figure 5* differs from that of *Figure 3* in two ways. First, the transistors of *Figure 5* have multiple emitters, due to the many diffusions on a typical die. One emitter of each transistor could function as the trigger input to the SCR. Secondly, R1 and R2 have been added and are due to P− and N− substrate resistances between the base of each transistor and the substrate power supply contacts.



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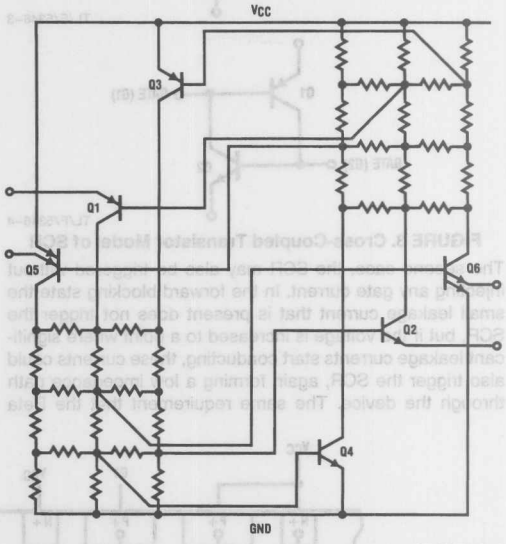
FIGURE 5. Schematic of Simple SCR Model

Like the discrete SCR there are two basic methods of turning the CMOS SCR on. The first method is however slightly different. In the CMOS parasitic SCR current cannot be directly injected into the base of one of its transistors. Instead either node G1 must be raised above V_{CC} enough to turn on Q1, or node G2 must be lowered below ground enough to turn on Q2. If G1 is brought above V_{CC}, current is injected from the emitter of Q1 and is swept to the collector of Q1. The collector of Q1 feeds the base of Q2 and also R2. R2 has the effect of stealing current from the base of Q2, but as current flows through R2 a voltage will appear at the base of Q2. Once this voltage reaches 0.6 volts Q2 will turn on and feed current from its collector back into R1 and into Q1. If 0.6 volts is generated across R1, Q1 then turns on even more.

Again, if the two transistors have enough gain and enough anode current flows to sustain the SCR, it will turn on, and remain on even after G1 is returned to V_{CC}. The actual requirements for latch up are altered by the two resistors, R1 and R2. Since the resistors shunt some current away from the base of both transistors, the resistors essentially reduce the effective gains of the transistors. Thus the transistors must actually have much higher gains in order to achieve an overall SCR loop gain greater than one, and hence enable the SCR to trigger. The actual equations to show quantitatively how the resistors effect the SCR's behavior could be derived, but it is sufficient to notice that as R1 and R2 become smaller the SCR becomes harder to turn on. IC designers utilize this to reduce latch up.

The second method of turning on the SCR mentioned earlier also applies here. If the supply voltage is raised to a large value, and internal substrate diodes start breaking down excessive leakage currents will flow possibly triggering the SCR. The resistors also affect this trigger method as well, since they steal some of the leakage currents from Q1 and Q2, and hence it takes more current to trigger the SCR. In high speed CMOS the process enhancements reduce the transistor betas and hence eliminate latch up by this mechanism as well.

While useful, the SCR model of *Figures 4 and 5* is very simplified, since in actuality the CMOS SCR is a structure with many transistors interconnected by many resistances. Although still somewhat simplified, *Figure 6* attempts to illustrate how the parasitics on a chip connect. It is important to remember that any transistor or diode diffusion can parasitically form part of the SCR. In the figure transistor Q1 and Q2 are single emitter transistors formed by the input protection diodes. Internal P and N channel transistors have no external connection and are represented by Q3 and Q4. Q5 and Q6 represent output transistor diffusions, and the second emitter corresponds to the output. All of these transistors are connected together by the N− substrate and P− well resistances, which are illustrated by the resistor mesh.



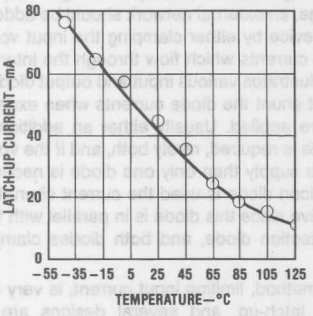
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FIGURE 6. Distributed Model of CMOS SCR

If any of the emitters associated with the trigger inputs G1–G4 become forward biased the SCR may be triggered. Also due to the intertwined nature of this structure, part of the SCR may be initially latched up. In this case only a limited amount of current may flow, but this limited latch up may spread and cause other parts to be triggered until eventually the whole chip is involved.

In general the trigger to the SCR has been conceptualized as a current, since ideally the CMOS input looks into the base of the SCR transistors. However this may not be quite true. There may be some resistance in series with each base, due to substrate or input protection resistances. In newer silicon gate CMOS processes, MM54HC/MM74HC for example, a poly-silicon resistor is used for electrostatic protection, and this enables larger voltages to be applied to the circuit pins without causing latchup. This is because the poly resistor actually forms a current limit resistor in series with the diodes. In most applications the designer is more concerned with accidental application of a large voltage, and the use of the poly resistor internally enables good voltage resistance to latch up. CMOS outputs are directly connected to parasitic output diodes since no poly resistor can be placed on an output without degrading output current drive. Thus the output latch up mechanism is usually thought of as a current.

Temperature variations will affect the amount of current required to trigger the SCR. This is readily understandable since temperature effects the bipolar transistor's gain and the resistance of the base-emitter resistors. Generally, as the temperature is increased less current is needed to cause latch-up. This is because as temperature increases the bipolar transistor's base-emitter voltage decreases and the base-emitter resistor value increases. *Figure 7* plots trigger current versus temperature for a sensitive CMOS input. This data was taken on a CMOS device without any layout or process enhancements to eliminate latch up. Increasing temperature from room to 125°C will reduce the trigger current by about a factor of three. Once the circuit is latched up, heating of the device die caused by SCR currents will actually increase the susceptibility to repeated latch up.



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FIGURE 7. Temperature versus SCR Trigger Current for Special CMOS Test Structure

OTHER LATCH UP TRIGGER METHODS

There are some other methods of latching up CMOS circuits, they are not as circuit design related and shall only be briefly mentioned. The first is latch up due to radiation bombardment. In hostile environments energetic atomic particals can bombard a CMOS die freeing carriers in the substrate. These carriers then can cause the SCR to trigger. This can be of concern in high radiation environments which call for some sort of radiation hardened CMOS logic.

Another latch up mechanism is the application of a fast rise or fall spike to the supply inputs of a CMOS device. Even if insufficient current is injected into the circuit the fast voltage change could trigger latch up. This occurs because the voltage change across the part changes the junction depletion capacitances, and this change in capacitance theoretically could cause a current that would trigger the SCR latch. In actual practice this is very difficult to do because the response time of the SCR (discussed shortly) is very poor. This is hardly a problem since power supplies must be adequately decoupled anyway.

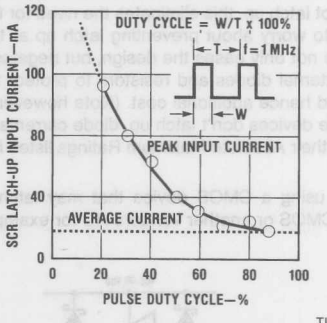
A third latch up cause which is completely internal to the IC itself and is out of the control of the system designer is internally triggered latch up. Any internal switching node connects to a diode diffusion, and as these diffusions switch the junction depletion capacitance associated with these nodes changes causing a current to be generated. This current could trigger the SCR. The poor frequency response of the SCR tends to make this difficult, but as chip geometries are shrunk packing densities will increase and the gain of the lateral PNP transistor increase. This may increase the latch up susceptibility. It is up to the IC designer to ensure that this doesn't happen, and care in the layout and circuit design of 54HC/74HC logic has ensured that this will be avoided.

THE CMOS SCR: TRANSIENT BEHAVIOR

With the introduction of fast CMOS logic the transient nature of the CMOS SCR phenomena becomes more important because signal line ringing and power supply transients are more prevalent in these systems. Older metal gate CMOS (CD4000 & 74HC) circuits have slow rise and fall times which do not cause a large amount of line ringing. Power supply spiking is also somewhat less, again due to slow switching times associated with these circuits.

The previous discussion assumed that the trigger to the CMOS SCR was essentially static and was a fixed current. Under these conditions a certain value current will cause the SCR to trigger, but if the trigger is a short pulse the peak value of the pulse current that will trigger the SCR can be much larger than the static DC trigger current. This is due to the poor frequency characteristics of the SCR.

For short noise pulses, $<5\ \mu s$, the peak current required to latch up a device is dependent on the duty cycle of the pulses. At these speeds it is the average current that causes latch-up. For example, if a 1 MHz 50% duty cycle over voltage pulse train is applied to a device that latched with 20 mA DC current, then typically the peak current required will be about 40 mA. For a 25% duty cycle the peak current would be 80 mA. An example of this is shown in *Figure 8* which plots latch up current against over-voltage pulse width at 1 MHz.

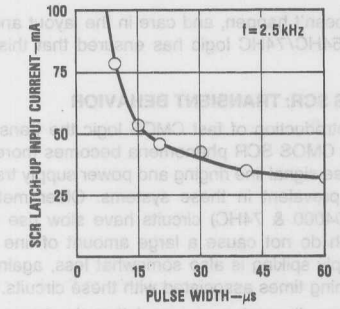


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FIGURE 8. Trigger Current of SCR of Input Overvoltage Pulses at High Repetition Rate on Special Test Unit

If the pulse widths become long, many microseconds, the latch up current will approach the DC value even for low duty cycles. This is shown in *Figure 9* which plots peak trigger current vs pulse width for the same test device used in *Figure 8*. The repetition rate in this case is a slow 2.5 kHz (period = 400 μs). These long pulse widths approach the trigger time of the SCR, and thus pulses lasting several microseconds are long enough to appear as DC voltages to the SCR. This indirectly indicates the trigger speed of the SCR to be on the order of ten to fifteen microseconds. This is however dependent on the way the IC was designed and the processing used.

In normal high speed systems noise spikes will typically be only a few nanoseconds in duration, and the average duty cycle will be small. So even a device that is not designed to



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FIGURE 9. Trigger Current of Pulse on Special Test Unit SCR for Single Transient Overvoltage

be latch up resistant, will probably not latch up even with significant line ringing on its inputs or outputs (Then again . . .). However, in some systems where inductive or other loads are used transients of several microseconds can be easily generated. For example, some possible applications are automotive and relay drivers. In other CMOS logic families spikes of this nature are much more likely to cause the SCR to trigger, but here again MM54HC/MM74HC high speed CMOS is immune.

PREVENTING SCR LATCH UP: USER SYSTEM DESIGN SOLUTIONS

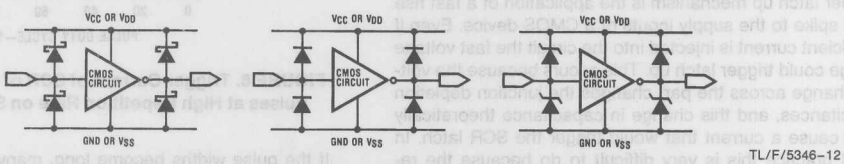
SCR latch-up can be prevented either on the system level or on the IC level. Since National's MM54HC/MM74HC series will not latch up, this eliminates the need for the system designer to worry about preventing latch up at the system level. This not only eases the design, but negates the need to add external diodes and resistors to protect the CMOS circuit, and hence additional cost. (Note however that even though the devices don't latch up, diode currents should be limited to their Absolute Maximum Ratings listed in the Data Sheets).

If one is using a CMOS device that may latch up, older CD4000 CMOS or another vendors HC for example, and its input or output voltages may forward bias the input or output diodes then some external circuitry may need to be added to eliminate possible SCR triggering. As with the previous discussions of latch-up preventing SCR latch-up falls into two categories: the static case, and the transient condition. Each is related but has some unique solutions.

In the static condition to ensure SCR latch up does not occur, the simplest solution is to design CMOS systems so that their input/output diodes don't become forward biased. To ease this requirement some special circuits that have some of their input protection diodes removed are provided, and this enables input voltages to exceed the supply range. These devices are MM54HC4049/50, CD4049/50, and MM54C901/2/3/4.

If standard logic is used and input voltages will exceed the supply range, an external network should be added that protects the device by either clamping the input voltage or by limiting the currents which flow through the internal diodes. *Figure 10* illustrates various input and output diode clamping circuits that shunt the diode currents when excessive input voltages are applied. Usually either an additional input or output diode is required, rarely both, and if the voltages only exceed one supply then only one diode is necessary. If an external silicon diode is used the current shunt is only partially effective since this diode is in parallel with the internal silicon protection diode, and both diodes clamp to about 0.7V.

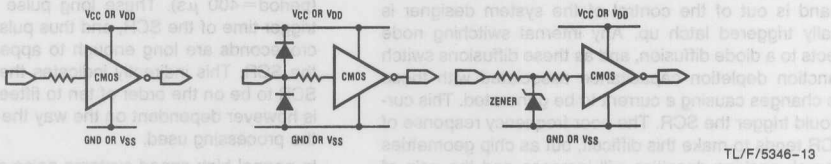
A second method, limiting input current, is very effective in preventing latch-up, and several designs are shown in *Figure 11*. The simplest approach is a series input resistor. It is recommended that this resistor should be as large as possible without causing excessive speed degradation yet ensure the input current is limited to a safe value. If speed is critical, it is better to use a combination diode-resistor network as shown in *Figures 11b* and *11c*. These input networks effectively limit input currents while using lower input resistors. The series resistor may not be an ideal solution for protecting outputs because it will reduce the effective drive of the output. In most cases this is only a problem when the output must drive a lot of current or must switch large capacitances quickly.



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Schottky Diodes (a) Germanium Diodes (b) Zener Diodes (c)

FIGURE 10. External Input and Output Protection Diodes Circuits for Eliminating SCR Latch-up

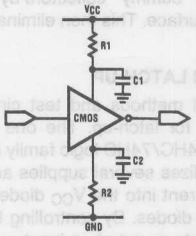


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(a) (b) (c)

FIGURE 11. Input Resistor and Resistor-Diode Protection Circuits for Eliminating Latch-up

A third approach is instead of placing resistors in series with the inputs to place them in series with the power supply lines as shown in *Figure 12*. The resistors must be bypassed by capacitors so that momentary switching currents don't produce large voltage transients across R1 and R2. These resistors can limit input currents but primarily they should be chosen to ensure that the supply current that can flow is less than the holding current of the SCR. Thus even though the input current can cause latch up it cannot be sustained and the IC will not be damaged.



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FIGURE 12. Supply Resistor-Capacitor Circuits for Eliminating Latch-up

This last solution has the advantage of fewer added components, but also has some disadvantages. This method may not prevent latch up unless the resistors are fairly large, but this will greatly degrade the output current drive and switching characteristics of the device. Secondly, this circuit protects the IC from damage but if diodes currents are applied causing large supply currents, the circuits will logically malfunction where as with other schemes logic malfunction can be prevented as well.

PREVENTING LATCH UP: IC DESIGN SOLUTIONS

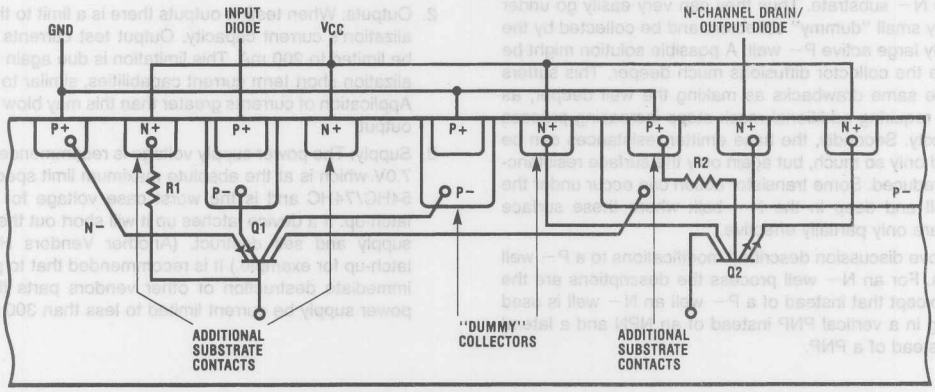
The previous latch up solutions involve adding extra components and hence extra cost and board space. One can imagine that in a microprocessor bus system if for some reason the designer had to protect each output of several CMOS devices that are driving a 16-bit address bus that up to 32 diodes and possibly 16 resistors may need to be added. Thus for the system designer the preferable solution is to use logic that won't latch up.

Most methods previously employed to eliminate latch up are either not effective, increase the die size significantly, and/or degrade MOS transistor performance. The process enhancements employed on 54HC/74HC logic circumvent these problems. Primarily it is effective without degrading MOS performance.

When designing CMOS integrated circuits, there are many ways that the SCR action of these circuits can be reduced. One of the several methods of eliminating the SCR is to reduce the effective gain of at least one of the transistors, thus eliminating the regenerative feedback. This can be accomplished either by modifying the process and/or by inserting other parasitic structures to shunt the transistor action. Also the substrate resistances modeled as R1 and R2 in *Figures 4* and *5* can be reduced. As these resistances approach zero more and more current is required to develop enough voltage across them to turn on the transistors.

As mentioned, the current gains of the NPN and PNP parasitic transistors directly affect the current required to trigger the latch. Thus some layout and process enhancements can be implemented to reduce the NPN and PNP Betas. In a P−well process the gain of the vertical NPN is determined by the specific CMOS process, and is dependent on junction depths and doping concentrations. These parameters also control the performance of the N-MOS transistors as well and so process modification must be done without degrading CMOS performance. To reduce the gain of the vertical PNP the doping levels of the P− well can be increased. This will decrease minority carrier lifetimes. It will also reduce the substrate resistance lowering the NPN base-emitter resistance. However this will increase parasitic junction capacitances, and may affect NMOS threshold voltages and carrier mobility. The depth of the well may be increased as well. This will reduce layout density due to increased lateral diffusion, and increase processing time as it will take longer to drive the well deeper into the substrate.

The lateral PNP's gain is determined by the spacing of input and output diode diffusions to active circuitry and minority carrier life times in the N− substrate. The carrier life times are a function of process doping levels as well, and care must be exercised to ensure no MOS transistor performance degradation. Again the doping levels of the substrate can be increased, but this will increase parasitic junction capacitances, and may alter the PMOS threshold characteristics. The spacing between input/output diodes and other



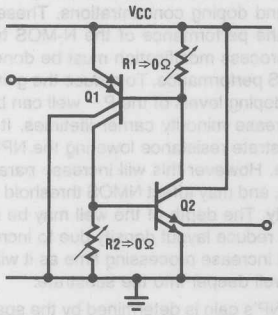
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FIGURE 13. Simplified CMOS Cross Section Showing Added Latch-up Reduction Structures

diffusions can be increased. This will increase the PNP's base width, lowering its beta. This may be done only a limited amount without significantly impacting die size and cost.

Another method for enhancing the latch-up immunity of MM54HC/MM74HC is to short out the SCR by creating additional parasitic transistors and reducing the effective substrate resistances. These techniques employ the use of ringing structures (termed guard rings) to surround inputs and outputs with diffusions that are shorted to V_{CC} or ground. These diffusions act to lower the substrate resistances, making it harder to turn on the bipolar transistors. They also act "dummy" collectors that shunt transistor action by collecting charges directly to either V_{CC} or ground, rather than through active circuitry. *Figure 13* shows a cross section of how this might look and *Figure 14* schematically illustrates how these techniques ideally modify the SCR structure.

Ideally, in *Figure 14* if the inputs are forward biased any transistor action is immediately shunted to V_{CC} or ground through the "dummy" collectors. Any current not collected will flow through the resistors, which are now much lower in value and will not allow the opposite transistor to turn on.



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FIGURE 14. Schematic Representation of SCR with Improvements to Reduce Turn On.

Unfortunately in order to reduce latch up these techniques add quite significantly to the die size, and still may not be completely effective.

The ineffectiveness of the ringing structures at completely eliminating latch up is for one because the collectors are only surface devices and carriers can be injected very deep into the N− substrate. Thus they can very easily go under the fairly small "dummy" collectors and be collected by the relatively large active P− well. A possible solution might be to make the collector diffusions much deeper. This suffers from the same drawbacks as making the well deeper, as well as requiring additional mask steps increasing process complexity. Secondly, the base emitter resistances can be reduced only so much, but again only the surface resistances are reduced. Some transistor action can occur under the P− well and deep in the N− bulk where these surface shorts are only partially effective.

The above discussion described modifications to a P− well process. For an N− well process the descriptions are the same except that instead of a P− well an N− well is used resulting in a vertical PNP instead of an NPN and a lateral NPN instead of a PNP.

These methods are employed in 54HC/74HC CMOS logic, but in addition processing enhancements were made that effectively eliminate the PNP transistor. The primary enhancement is a modification to the doping profile of the N− substrate (P− well process). This lowers the conductivity of the substrate material while maintaining a lightly dope surface concentration. This allows optimum performance NMOS and PMOS transistors while dramatically reducing the gain of the PNP and its base-emitter resistance. The gain of the PNP is reduced because the minority carrier lifetimes are reduced. This modification also increases the effectiveness of the "dummy" collectors by maintaining carriers closer to the surface. This then eliminates the SCR latch up mechanism.

5.0 TESTING SCR LATCH-UP

There are several methods and test circuits that can be employed to test for latch-up. The one primarily used to characterize the 54HC/74HC logic family is shown in *Figure 15*. This circuit utilizes several supplies and various meters to either force current into the V_{CC} diodes or force current out of the ground diodes. By controlling the input supply a current is forced into or out of an input or output of the test device. As the input supply voltage is increased the current into the diode increases. Internal transistor action may cause some supply current to flow, but this should not be considered latch up. When latch-up occurs the power supply current will jump, and if the input supply is reduced to zero the power supply current should remain. The input trigger current is the input current seen just prior to the supply current jumping.

Testing latch-up is a destructive test, but in order to test 54HC/74HC devices without causing immediate damage, test limits for the amount of input or output currents and supply voltages should be observed. Even though immediate damage is avoided, SCR latch-up test is a destructive test and the IC performance may be degraded when testing to these limits. Therefore parts tested to these limits should not be used for design or production purposes. In the case of National's high speed CMOS logic the definition of "latch-up proof" requires the following test limits when using the standard DC power supply test as is shown in *Figure 15*.

1. Inputs: When testing latch-up on CMOS inputs the current into these inputs should be limited to less than 70 mA. Application of currents greater than this may damage the input protection poly resistor or input metalization, and prevent further testing of the IC.
2. Outputs: When testing outputs there is a limit to the metalization's current capacity. Output test currents should be limited to 200 mA. This limitation is due again to metalization short term current capabilities, similar to inputs. Application of currents greater than this may blow out the output.
3. Supply: The power supply voltage is recommended to be 7.0V which is at the absolute maximum limit specified in 54HC/74HC and is the worst case voltage for testing latch-up. If a device latches up it will short out the power supply and self destruct. (Another Vendors HC may latch-up for example.) It is recommended that to prevent immediate destruction of other vendors parts that the power supply be current limited to less than 300 mA.

In almost all instances at high temperature, if it is going to occur, latch-up will occur at current values between 0–50 mA.

There are a few special considerations when trying to measure worst case latch-up current. Measuring input latch-up current is straight forward, just force the inputs above or below the power supply, but to measure an output it must first be set to a high level when forcing it above V_{CC}, or to a low level when forcing it below ground. When measuring Tri-State outputs, the outputs should be disabled, and when measuring analog switches they should be either left open or turned off.

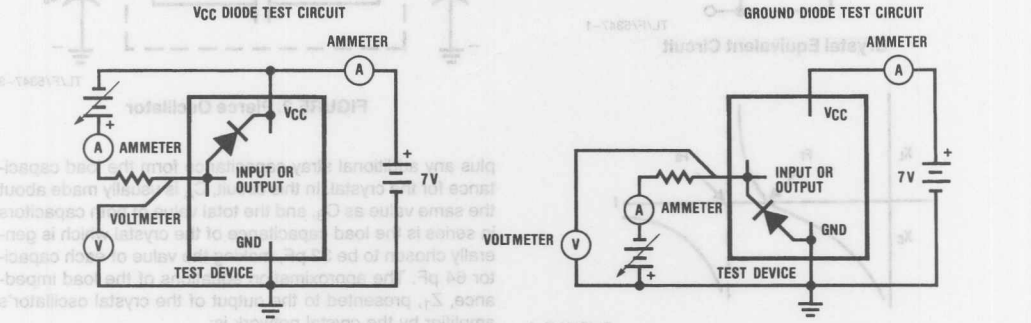
To measure the transient behavior of the test device or to reduce IC heating effects a pulse generator can be used in place of the input supply and an oscilloscope with a current probe should then replace the current meter. Care should be exercised to avoid ground loops in the test hardware as this may short out the supplies.

Although there are several methods of testing latch-up, this method is very simple and easy to understand. It also yields conservative data since manually controlling the supplies is a slow process which causes localized heating on the chip prior to latch-up, and lowers the latch-up current.

6.0 CONCLUSION

SCR latch-up in CMOS circuits is a phenomena which when understood can be effectively controlled both from the integrated circuit and system level. National's proprietary CMOS process and layout considerations have eliminated CMOS latch-up in the MM54HC/MM74HC family. This will increase the ease of use and design of this family by negating the need for extra SCR protection circuitry as well as very favorable impact system integrity and reliability.

Testing SCR Latch-Up of HCMOS

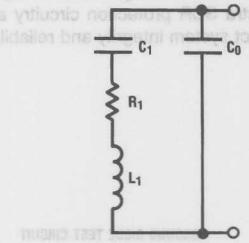


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$T_A = 125°C$

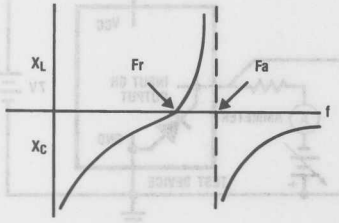
FIGURE 15. Bench Test Setup for Measuring Latch-up

With the advent of high speed HCMOS circuits, it is possible to build systems with clock rates of greater than 30 MHz. The familiar gate oscillator circuits used at low frequencies work well at higher frequencies and either L–C or crystal resonators maybe used depending on the stability required. Above 20 MHz, it becomes expensive to fabricate fundamental mode crystals, so overtone modes are used.



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Crystal Equivalent Circuit



TL/F/5347–2

Reactance of Crystal Resonator
FIGURE 1

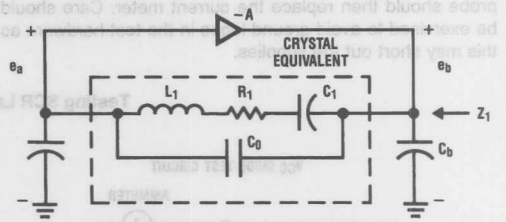
Basic Oscillator Theory

The equivalent circuit of a quartz crystal, and its reactance characteristics with frequency are shown in *Figure 1*. F_R is called the resonant frequency and is where L_1 and C_1 are in series resonance and the crystal looks like a small resistor R1. The frequency F_A is the antiresonant frequency and is the point where L_1–C_1 look inductive and resonate with C_O to form the parallel resonant frequency F_A, F_R and F_A are usually less than 0.1% apart. In specifying crystals, the frequency F_R is the oscillation frequency to the crystal in a series mode circuit, and F_R is the parallel resonant frequency. In a parallel mode circuit, the oscillation frequency will be slightly below F_A where the inductive component of the $L_1 - C_1$ arm resonates with C_O and the external circuit capacitance. The exact frequency is often corrected by the crystal manufacture to a specified load capacitance, usually 20 or 32 picofarads.

TABLE I. Typical Crystal Parameters

Parameter	32 kHz fundamental	200 kHz fundamental	2 MHz fundamental	30 MHz overtone
R_1	200 kΩ	2 kΩ	100 Ω	20 Ω
L_1	7000H	27H	529 mH	11 mH
C_1	0.003 pF	0.024 pF	0.012 pF	0.0026 pF
C_0	1.7 pF	9 pF	4 pF	6 pF
Q	100k	18k	54k	100k

The Pierce oscillator is one of the more popular circuits, and is the foundation for almost all single gate oscillators in use today. In this circuit, *Figure 2*, the signal from the input to the output of the amplifier is phase shifted 180 degrees. The crystal appears as a large inductor since it is operating in the parallel mode, and in conjunction with C_A and C_B, forms a pi network that provides an additional 180 degrees of phase shift from output to the input. C_A in series with C_B



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FIGURE 2. Pierce Oscillator

plus any additional stray capacitance form the load capacitance for the crystal. In this circuit, C_A is usually made about the same value as C_B, and the total value of both capacitors in series is the load capacitance of the crystal which is generally chosen to be 32 pF, making the value of each capacitor 64 pF. The approximation equations of the load impedance, Z_1, presented to the output of the crystal oscillator's amplifier by the crystal network is:

$$Z_L = \frac{X_C^2}{R_L}$$

Where $X_C = -j/\omega C_B$ and R_L is the series resistance of the crystal as shown in Table I. Also $\omega = 2\pi f$ where f is the frequency of oscillation.

The ratio of the crystal network's input voltage to it's output voltage is given by:

$$\frac{e_A}{e_B} = \frac{\omega C_B}{\omega C_A} = \frac{C_B}{C_A}$$

C_A and C_B are chosen such that their series combination capacitance equals the load capacitance specified by the manufacturer, ie 20 pF or 32 pF as mentioned. In order to oscillate the phase shift at the desired frequency around the oscillator loop must be 360° and the gain of the oscillator loop must be greater or equal to one, or:

$$(A_A)(A_F) \geq 1$$

Where A_A is amplifier gain and A_F is crystal network voltage gain of the crystal π network: e_A/e_B. Thus not only should the series combination of C_B and C_A be chosen. The ratio of the two can be set to adjust the loop gain of the oscillator.

For example if a 2 MHz oscillator is required. Then $R_L = 100\Omega$ (Table I). If $e_A/e_B = 1$ and the crystal requires a 32 pF load so $C_B = 64$ pF and then C_A becomes 64 pF also. The load presented by the crystal network is $Z_L = (1/2\pi\ (2\ \text{MHz})\ (64\ \text{pF})^2)/100 = 16\ \text{k}\Omega$.

The CMOS Gate Oscillator

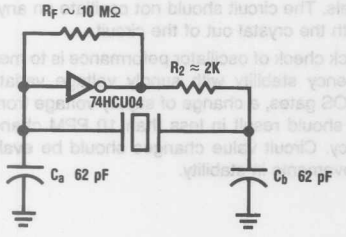
A CMOS gate sufficiently approaches the ideal amplifier shown above that it can be used in almost the same circuit. A review of manufacturers data sheets will reveal there are two types of inverting CMOS gates:

a) Unbuffered: gates composed of a single inverting stage. Voltage gain in the hundreds.

b) Buffered: gates composed of three inverting stages in series. Voltage gains are greater than ten thousand.

CMOS gates must be designed to drive relatively large loads and must supply a fairly large amount of current. In a single gate structure that is biased in its linear region so both devices are on, supply current will be high. Buffered gates are designed with the first and second gates to be much smaller than the output gate and will dissipate little power. Since the gain is so high, even a small signal will drive the output high or low and little power is dissipated. In this manner, unbuffered gates will dissipate more power than buffered gates.

Both buffered and unbuffered gates maybe used as crystal oscillators, with only slight design changes in the circuits.



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FIGURE 3. Typical Gate Oscillator

In this circuit, R_F serves to bias the gate in its linear region, insuring oscillation, while R_2 provides an impedance to add some additional phase shift in conjunction with C_B. It also serves to prevent spurious high frequency oscillations and isolates the output of the gate from the crystal network so a clean square wave can be obtained from the output of the gate. Its value is chosen to be roughly equal to the capacitive reactance of C_B at the frequency of oscillation, or the value of load impedance Z_L calculated above. In this case, there will be a two to one loss in voltage from the output of the gate to the input of the crystal network due to the voltage divider effect of R_2 and Z_L. If C_A and C_B are chosen equal, the voltage at the input to the gate will be the same as that at the input to the crystal network or one half of the voltage at the output of the gate. In this case, the gate must have a voltage gain of 2 or greater to oscillate. Except at very high frequencies, all CMOS gates have voltage gains well in excess of 10 and satisfactory operation should result.

Theory and experiment show that unbuffered gates are more stable as oscillators by as much as 5 to 1. However, unbuffered gates draw more operating power if used in the same circuit as a buffered gate. Power consumption can be minimized by increasing feedback which forces the gate to operate for less time in its linear region.

When designing with buffered gates, the value of R_2 or C_B may be increased by a factor of 10 or more. This will increase the voltage loss around the feedback loop which is desirable since the gain of the gate is considerably higher than that of an unbuffered gate.

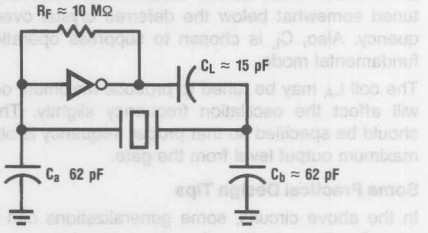
C_A and C_B form the load capacitance for the crystal. Many crystals are cut for either 20 to 32 picofarad load capacitance. This is the capacitance that will cause the crystal to oscillate at its nominal frequency. Varying this capacitance will vary the frequency of oscillation. Generally designers work with crystal manufacturers to select the best value of load capacitance for their application, unless an off the shelf crystal is selected.

High Frequency Effects

The phase shift thru the gate may be estimated by considering it's delay time:

Phase Shift = Frequency X Time delay X 360°

The "typical gate oscillator" works well at lower frequencies where phase shift thru the gate is not excessive. However, above 4 MHz, where 10 nsec of time delay represents 14.4° of excess phase shift, R_2 should be changed to a small capacitor to avoid the additional phase shift of R_2. The value of this capacitor is approximately $1/\omega C$ where $\omega = 2\pi f$, but not less than about 20 pF.

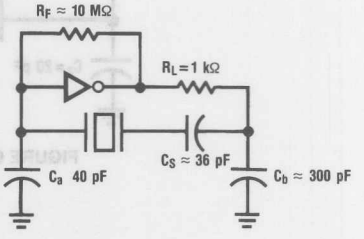


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FIGURE 4. Gate Oscillator for Higher Frequencies

Improving Oscillator Stability

The CMOS gate makes a mediocre oscillator when compared to a transistor or FET: It draws more power and is generally less stable. However, extra gates are often available and are often pressed into service as oscillators. If improved stability is required, especially from buffered gate oscillators, an approach shown in *Figure 5* can be used.



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FIGURE 5. Gate oscillator with improved stability

In this circuit, C_A and C_B are made large to swamp out the effects of temperature and supply voltage change on the gate input and output impedances. A small capacitor in series with the crystal acts as the crystal load and further isolates the crystal from the rest of the circuit.

Overtone Crystal Oscillators

At frequencies above 20 MHz, it becomes increasingly difficult to cut or work with crystal blanks and so generally a crystal is used in it's overtone mode. Also, fundamental mode crystals above this frequency have less stability and greater aging rates. All crystals will exhibit the same reactance vs. frequency characteristics at odd overtone frequencies that they do at the fundamental frequency. However, the overtone resonances are not exact multiples of the fundamental, so an overtone crystal must be specified as such.

In the design of an overtone crystal oscillator, it is very important to suppress the fundamental mode, or the circuit will try to oscillate there, or worse, at both the fundamental and the overtone with little predictability as to which. Basically, this requires that the crystal feedback network have more gain at the overtone frequency than the fundamental. This is usually done with a frequency selective network such as a tuned circuit.

The circuit in *Figure 6* operates in the parallel mode just as the Pierce oscillator above. The resonant circuit L_A—C_B is an effective short at the fundamental frequency, and is tuned somewhat below the deferred crystal overtone frequency. Also, C_L is chosen to suppress operation in the fundamental mode.

The coil L_A may be tuned to produce maximum output and will affect the oscillation frequency slightly. The crystal should be specified so that proper frequency is obtained at maximum output level from the gate.

Some Practical Design Tips

In the above circuits, some generalizations can be made regarding the selection of component values.

R_F: Sets the bias point, should be as large as practical.

R1: Isolates the crystal network from the gate output and provides excess phaseshift decreasing the probability of spurious oscillation at high frequencies. Value should be approximately equal to input impedance of the crystal network or reactance of C_B at the oscillator frequency. Increasing value will decrease the amount of feedback and improve stability.

C_B: Part of load for crystal network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

C_A: Part of crystal load network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

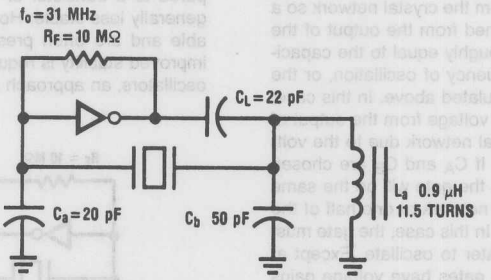
C_L: Used in place of R1 in high frequency applications. Reactance should be approximately equal to crystal network input impedance.

Oscillator design is an imperfect art at best. Combinations of theoretical and experimental design techniques should be used.

A. Do not design for an excessive amount of gain around the feedback loop. Excessive gain will lead to instability and may result in the oscillator not being crystal controlled.

B. Be sure to worst case the design. A resistor may be added in series with the crystal to simulate worst case crystals. The circuit should not oscillate on any frequency with the crystal out of the circuit.

C. A quick check of oscillator peformance is to measure the frequency stability with supply voltage variations. For HCMOS gates, a change of supply voltage from 2.5 to 6 volts should result in less than 10 PPM change in frequency. Circuit value changes should be evaluated for improvements in stability.



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FIGURE 6. Parallel Mode Overtone Circuit

MM74HC942 and MM74HC943 Design Guide

National Semiconductor
Application Note 347
Peter Single
Steve Munich

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1) TIMING AND CONTROL

a) Input and Output Thresholds

The MM74HC942/943 may be used in a CMOS or TTL environment. In a CMOS environment, no interfacing is required. If the MM74HC942/943 is interfaced to NMOS or bipolar logic circuits, standard interface techniques may be used. These are discussed in detail in National Semiconductor Application Note AN-314. This note is included in the National Semiconductor MM54HC/74HC High Speed micro-CMOS Logic Family Databook.

b) Logic States and Control Pin Function

Transmitted Data

TXD (pin 11) in conjunction with O/A selects the frequency of the transmitted tone and thus controls the transmitted data.

TXD = V_{CC} selects a "mark" and thus the high tone of the tone pair. This is discussed further in the following section.

Originate and Answer Mode

This is controlled by O/A (pin 13). O/A = V_{CC} selects originate mode. O/A = GND selects answer mode. These modes refer to the tone allocation used by the modem. When two modems are communicating with each other one will be in originate mode and one will be in answer mode. This assures that each modem is receiving the tone pair that the other modem is transmitting. The modem on the phone that originated the phone call is called the originate modem. The other modem is the answer modem.

The other pin controlling the transmitted tone is TXD (pin 11).

Bell 103 Tone Allocation				
Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz

Squelch Transmitter

Transmitter squelch is achieved by putting SQT = V_{CC} (SQT is pin 14). The line driver remains active in this state (assuming ALB = GND).

This state is commonly used during the protocol of establishing a call. The originate user initiates a phone call with its transmitter squelched, and waits for a tone to be received before beginning transmission. During the wait time, the modem is active to allow tone detection, but no tone may be transmitted.

The state SQT = V_{CC} may also be used if the line driver is required but a signal other than modem tones (e.g., DTMF tones or voice) is to be transmitted. This is discussed further in Transmission of Externally Generated Tones (section 3d).

Analog Loop Back

ALB = V_{CC}, SQT = GND selects the state "analog loop back". (The state ALB = SQT = V_{CC} is discussed in the following section.)

In analog loop back mode, the modulator output (at the line driver) is connected to the demodulator input (at the hybrid), and the demodulator is tuned to the transmitted frequency tone set. Thus the data on the TXD pin will, after some

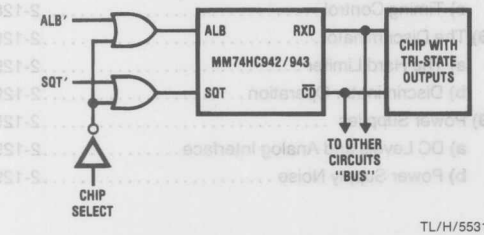
back is sufficient to cause the carrier detect output CD to go low indicating receipt of carrier.

In analog loop back mode, the modulator and transmitter are active, so the transmitted tone is not squelched.

Power-Down Mode

The state SQT = ALB = V_{CC} puts the MM74HC942/943 in power-down mode. In this state, the entire circuit except the oscillator is disabled. (The oscillator is left running in case it is required for a system clock). In power-down mode the supply current falls from 8 mA (typ) to 180 μA (typ), and all outputs, both analog and digital, TRI-STATE (become Hi-Z).

Using TRI-STATE Capability



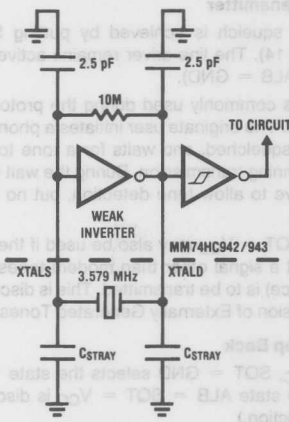
TL/H/5531–1

The ability of the outputs to TRI-STATE allows the modem to be connected to other circuitry in a bus-like configuration with the state SQT or ALB = GND being the modem chip select.

c) The Oscillator

The oscillator is a Pierce crystal oscillator. The crystal used in such an oscillator is a parallel resonant crystal.

The Oscillator



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The capacitors used on each end of the crystal are a combination of on-chip and stray capacitances. This generally means the crystal is operating with less than the specified parallel capacitance. This causes the oscillator to run faster than the frequency of the crystal. This is not a problem as the frequency shift is small (approximately 0.1%).

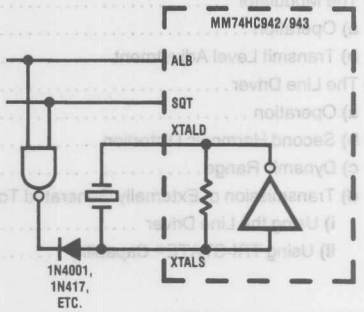
The oscillator is designed to run with equal capacitive loading on each side of the crystal. This should be taken into consideration when designing PC layouts. This need not be exact.

The Oscillator and Power-Down Mode

When the chip powers down, all circuits except the oscillator are switched off. The oscillator is left running so it may be used as a clock to drive other circuits within the system.

It is possible to shut the oscillator down by clamping the XTALS pin to V_{CC} or GND. This will cause the total chip current to fall to less than 5 μA. This may be useful in battery powered systems where minimizing supply current is important.

Powering Down the Oscillator



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2) MODULATOR SECTION

a) Operation

The modulator receives data from the transmit data (TXD) pin and synthesizes a frequency shift keyed, phase coherent sine wave to be transmitted by the line driver through the transmit analog (TXA) pin. Four different sine wave frequencies are generated, depending on whether the modem is set to the originate or answer mode and whether the data input to TXD is a logical high or low. See Timing and Control (section 1) for more information.

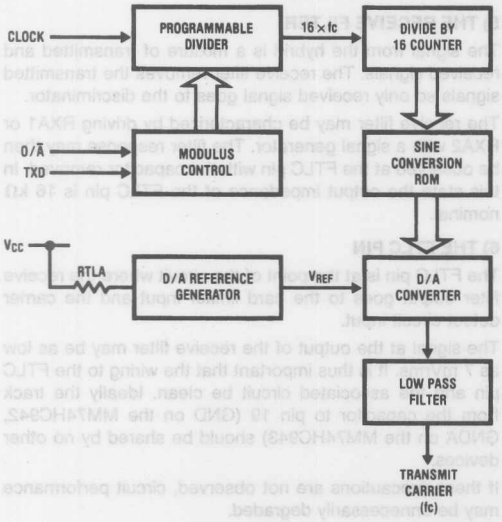
The TXD and O/A pins set the divisor of a dual modulus programmable divider. This produces a clock frequency which is sixteen times the frequency of the carrier to be transmitted. The clock signal is then fed to a four bit counter whose outputs go to the sine ROM. The ROM acts like a four-to-sixteen decoder that selects the appropriate tap on the D/A converter to synthesize a staircase-approximated sine wave. A switched capacitor filter and a low pass filter smooth the sine wave, removing high frequency components and insuring that noise levels are below FCC regulations.

b) Transmit Level Adjustment

The maximum transmit level of the MM74HC943 is −9dBm. Since most phone lines attenuate the signal by 3 dB, the maximum level that will be received at the exchange is −12 dBm. This level is also the maximum allowed by most phone companies. The MM74HC942 has a maximum transmit level of 0 dBm, making possible adjustments for line losses up to −12 dB. The resistor values required to adjust the transmit level for both the MM74HC942 and the MM74HC943 follow the Universal Service Order Code and can be found in the data sheets.

phone company. This resistor is usually wired into the phone jack at the installation as the resistor value is specific to the particular phone line. This is called the Universal Registered Jack Arrangement. This arrangement is possible only with the MM74HC942 because of the dynamic range constraints of the MM74HC943.

The Modulator



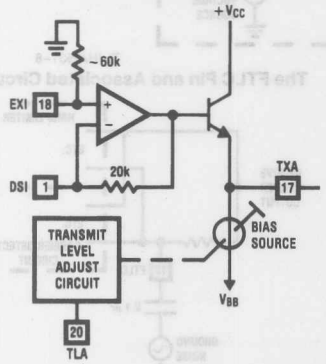
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3) THE LINE DRIVER

a) Operation

The line driver is a class A power amplifier for transmitting the carrier signals from the modulator. It can also be used to transmit externally generated tones such as DTMF signals, as discussed in section 3d. When used for transmitting modem-produced tones, the external input (EXI) pin should be grounded to pin 19 for both the MM74HC942 and the MM74HC943. The line driver output is the transmit analog (TXA) pin.

The Line Driver Equivalent Schematic



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receive frequency band from 2025 Hz to 2225 Hz. While the modulator produces very little second harmonic energy, the amplifier has been designed not to degrade the analog output any further. The result is that the second harmonic is below −56 dBm. Thus it is well below the minimum carrier amplitude recognized by the demodulator.

c) Dynamic Range

The decision to use the MM74HC942 or the MM74HC943 is a tradeoff between output dynamic range and power supply constraints. The power supply is discussed in another section. The MM74HC942 will transmit at 0 dBm while the maximum transmit level of the MM74HC943 is −9 dBm. This level applies to externally generated tones as well as the standard modem tone set.

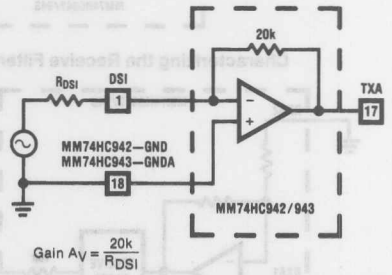
It is important to realize that the signal levels referred to above, and in the data sheet's specifications, are the levels referred to a 600Ω load resistor (representing the phone line) when driven from the external 600Ω source resistor. Also, the transmit levels discussed previously are maximum values. Typical values are 1 dB to 2 dB below these.

d) Transmission of Externally Generated Tones

Since a phone line connection is usually made on the TXA pin, it may be useful to use the line driver to transmit DTMF, voice or other externally generated tones. Both the inverting and non-inverting inputs to the line driver are available for this purpose. A DTMF tone generator with a TRI-STATE output may instead be directly connected to the same node as the TXA pin rather than the line driver. The choice of which method to use depends on whether the MM74HC942 or MM74HC943 is being used and the signal level of the transmission. Most phone companies allow DTMF tone generation at 0 dBm. This level is the maximum that the MM74HC942 can produce and is beyond the range of the MM74HC943.

If the line driver is to be used for external tone generation, the modem must be powered up and the transmission must be squelched by the SQT pin being held high. This will disable the output of the modulator section. The choice between the EXI pin and DSI pin is up to the user. The EXI pin gives a fixed gain of about 2. The DSI input allows for adjustable gain as a series resistor is necessary.

Using the DSI Input

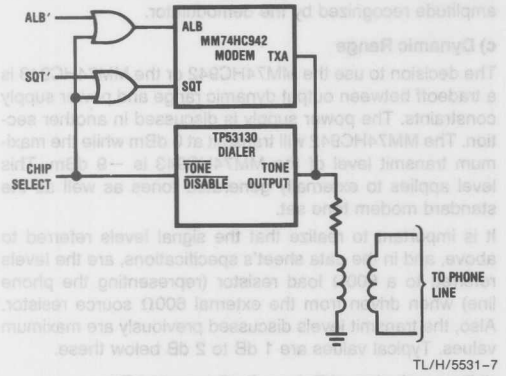


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A better solution may be to use the power-down mode of the MM74HC942/943 with a DTMF tone generator that has a TRI-STATE output. Such a device is a TP53130 and is

shown in the diagram following. When the tone generator is not in use and the modem is not squelched, the DTMF generator's output is in TRI-STATE. Rather than using the line driver, the tone generator's output is instead connected to the same node as the TXA pin. The tone generator is active when the modem is in power-down. Power-down TRI-STATEs the TXA output.

Interfacing to DTMF Generator Using TRI-STATE Feature



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4) THE HYBRID

The MM74HC942/943 has an on-chip hybrid. (A hybrid in this context refers to a circuit which performs two-to-four wire conversion.)

Under ideal conditions the phone line and isolation network have an equivalent input impedance of 600Ω. Under these conditions the gain from the transmitter to the op amp output is zero, while the gain from the phone line to the op amp output is unity. Thus the hybrid, by subtracting the transmitted signal from the total signal on the phone line, has removed the transmitted component.

Unfortunately, these ideal conditions rarely exist and filtering is used to remove the remaining transmitted signal component. This is discussed further in the next section.

Note that the signals into the hybrid must be referred to GND in the MM74HC942 and GNDA in the case of the MM74HC943. Thus blocking capacitors are required in the latter case. This is discussed further in DC Levels and Analog Interface (section 9a).

5) THE RECEIVE FILTER

The signal from the hybrid is a mixture of transmitted and received signals. The receive filter removes the transmitted signals so only received signal goes to the discriminator.

The receive filter may be characterized by driving RXA1 or RXA2 with a signal generator. The filter response may then be observed at the FTLC pin with the capacitor removed. In this state the output impedance of the FTLC pin is 16 kΩ nominal.

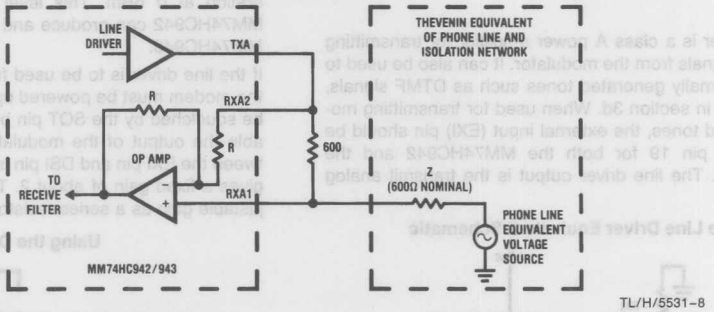
6) THE FTLC PIN

The FTLC pin is at the point of the circuit where the receive filter output goes to the hard limiter input and the carrier detect circuit input.

The signal at the output of the receive filter may be as low as 7 mVrms. It is thus important that the wiring to the FTLC pin and the associated circuit be clean. Ideally the track from the capacitor to pin 19 (GND on the MM74HC942, GNDA on the MM74HC943) should be shared by no other devices.

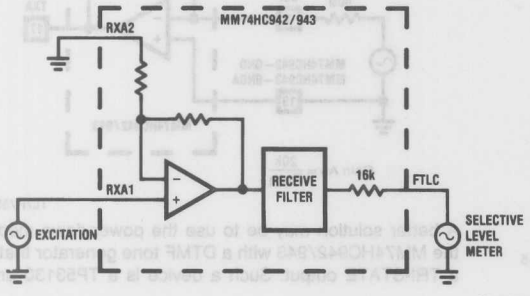
If these precautions are not observed, circuit performance may be unnecessarily degraded.

The Hybrid



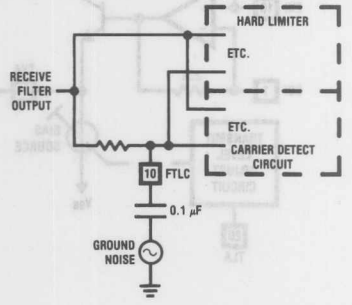
TL/H/5531–8

Characterizing the Receive Filter



TL/H/5531–9

The FTLC Pin and Associated Circuitry



TL/H/5531–10

7) THE CARRIER DETECT CIRCUIT

a) Operation

The carrier detect circuit senses if there is carrier present on the line. If carrier is not present, the data output is clamped high.

The RC circuit filters the DC from the output of the receive filter. The comparator inputs are thus the filter output, and the DC level of the receive filter minus the controlled offset. The controlled offset sets the amount that the AC signal must exceed the DC level (and thus the AC amplitude) before the comparator switches. When this happens, the comparator output sets a resettable one-shot which converts the periodic comparator output to a continuous signal. This signal then controls the time delay set by the CDT pin. After the preset time delay the CD bar output goes low. This shifts the comparator offset providing hysteresis to the overall circuit.

b) Threshold Control

The carrier detect threshold may be adjusted by adjusting the voltage on the CDA pin.

The carrier detect trip points are nominally set at −43 dBm and −46 dBm. The CDA pin sits at a nominal 1.2V. The carrier detect trip points are directly proportional to the voltage on this pin, so doubling the voltage causes a 6 dB increase in the carrier detect trip points. Similarly, halving the voltage causes a 6 dB decrease in carrier detect trip points.

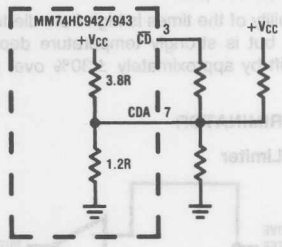
Note that as the carrier detect trip point is reduced, the system noise will approach the carrier level, and the accuracy and predictability of the carrier detect trip points will decrease.

The output impedance of the CDA pin is high. It is constant (±10%) from die to die but has a very high temperature coefficient. It is thus advisable, if the CDA pin is driven, to drive from a low source impedance.

Because the output impedance of the CDA pin is high, capacitive coupling from the adjacent XTALD pin can present a problem. For this reason a 0.1 μF capacitor is usually connected from the CDA pin to ground. If the CDA pin is driven from a low impedance source, this capacitor may be omitted.

If a resistor is connected from the CD bar pin to the CDA pin, the CDA voltage will vary depending on whether carrier is detected. This will effectively increase the carrier detect hysteresis.

Increased Carrier Detect Hysteresis



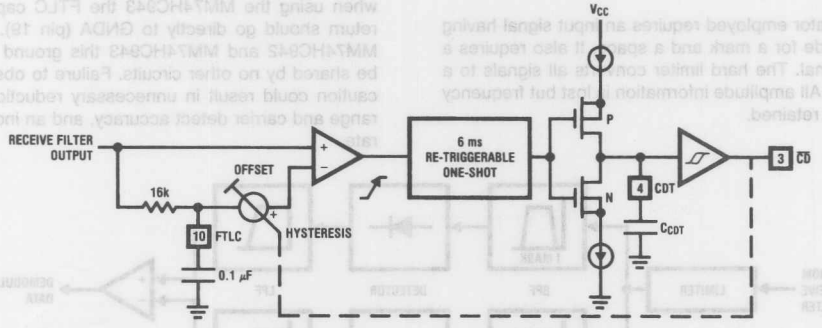
TL/H/5531–11

Similarly an inverter and a resistor from the CD bar pin to the CDA pin will reduce the hysteresis. This is not recommended as the 3 dB nominal figure chosen is close to the minimum value useable for stable operation.

c) Timing Control

The capacitor on the CDT pin adjusts the amount of time that carrier must be present before the carrier is recognized as valid.

Carrier Detect Block Diagram



TL/H/5531–12

$T_{on\text{-}to\text{-}off} = C \times 0.54$ seconds

and

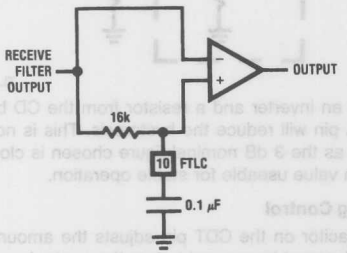
$T_{off\text{-}to\text{-}on} = C \times 6.4$ seconds.

The ratio of on-to-off and off-to-on times may be adjusted over a narrow range by the addition of pull-up or pull-down resistors on the CDT pin.

The repeatability of the times is high from die to die at fixed temperature, but is strongly temperature dependent. The times will shift by approximately ±30% over process and temperature.

8) THE DISCRIMINATOR

a) The Hard Limiter



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The signal to the inverting input of the comparator has the same DC component as the signal to the non-inverting input. The differential input to the comparator is thus the AC component of the filter output. The comparator has very low input offset and so the limiter will operate with very low input signal levels.

The demodulator employed requires an input signal having equal amplitude for a mark and a space. It also requires a high level signal. The hard limiter converts all signals to a square wave. All amplitude information is lost but frequency information is retained.

The discriminator separates the incoming energy into mark and space energy. This occurs in the band pass filters which are tuned to the mark and space frequencies. The outputs of the mark and space band pass filters are rectified to extract the output amplitudes. The rectifier outputs are filtered to remove ripple. The low pass filter outputs are compared to determine if the mark or space path is receiving greater energy, and thus if the incoming data is a mark or a space.

The output of the discriminator is only valid if carrier is being received. If carrier is not being received (as determined in the carrier detect circuit) the RXD output is clamped high. This stops the discriminator from attempting to demodulate a signal which is too low for reliable operation.

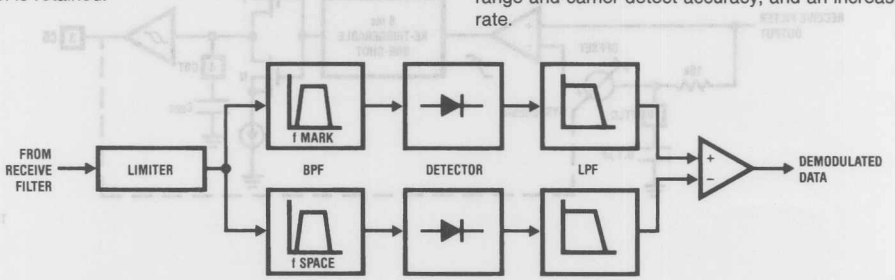
9) POWER SUPPLIES

a) DC Levels and Analog Interface

The MM74HC942 refers all analog inputs and outputs to GND (pin 19). The analog interface thus requires no DC blocking capacitors.

The MM74HC943 refers all analog inputs and outputs to GNDA (pin 19) which requires a nominal 2.5V supply. The current requirements of GNDA are low, so the GNDA supply may be derived with a simple resistive divider. The GNDA supply can then be referenced to GND using capacitors. This GNDA supply will have poor load regulation so the high current interface must be connected to GND and a DC blocking capacitor used.

As the FTLC capacitor is connected to the input of the hard limiter, any noise on the FTLC ground return will couple directly into this circuit. The signal on FTLC may be only millivolts, so it is important that the FTLC capacitor ground be at the same potential as the chip's ground reference. Thus when using the MM74HC943 the FTLC capacitor ground return should go directly to GNDA (pin 19). For both the MM74HC942 and MM74HC943 this ground return should be shared by no other circuits. Failure to observe this precaution could result in unnecessary reduction of dynamic range and carrier detect accuracy, and an increase in error rate.



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The MM74HC942/943 use switched capacitor techniques extensively. A feature of switched capacitor circuits is their ability to translate noise from high frequency bands to low frequency bands. At the same time it is difficult to design op amps with high power supply rejection at high frequencies. (The MM74HC942/943 has 19 op amps internally.) As a result the high frequency PSSR of the MM74HC942/943 is not high, so high frequency noise on the power supply can degrade circuit operation.

This should not cause a problem if the circuits are powered from a three terminal regulator, and no other circuitry shares the regulator. Power supply noise could be a problem if:

a) One or both of the power supplies are switching regulator circuits. Switching regulators can produce a lot of supply noise.

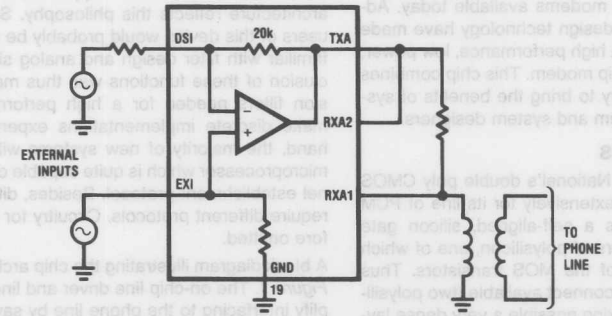
Ideally the modem could have its own supply. This may not be cost effective, so in some applications power supply filters may be necessary. These may just be RC filters but LC filters may be necessary depending on the extent of the supply noise. Miniature inductors in half watt resistor packages are cheap, lend themselves to automatic insertion, and are ideal for these filters.

It is difficult to set specifications for a "clean" supply because spectral density considerations are important. The following guidelines should be taken as "rule of thumb":

a) From 50 kHz to 20 MHz the ripple should not exceed −60 dBV.

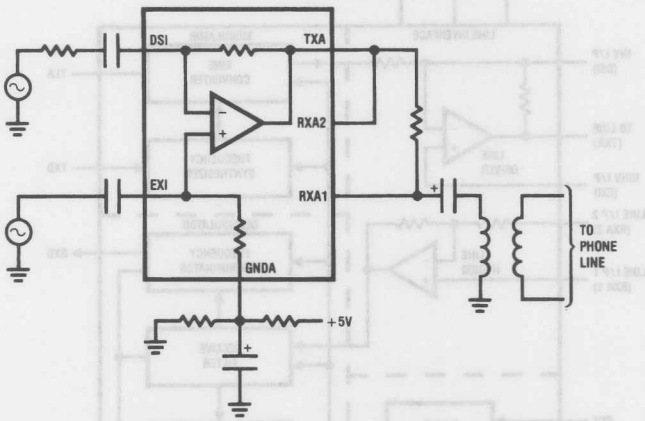
b) From DC to 50 kHz the ripple should not exceed −50 dBV.

MM74HC942 Analog Interface



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MM74HC943 Analog Interface



TL/H/5531–16

CMOS 300 Baud Modem

National Semiconductor
Application Note 349
Anthony Chan
Peter Single
Daniel Deschene

INTRODUCTION

The advent of low cost microprocessor based systems has created a strong demand for low cost, reliable means of data communication via the dial-up telephone network. The most widespread means for this task is the Bell 103 type modem, which has become the de facto standard of low speed modems. This type of modem uses frequency shift keying (FSK) to modulate binary data asynchronously at speeds up to 300 baud.

The success of this type of modem, despite its modest transmission speed, is largely due to its ability to provide full duplex data transmission at low error rates even with unconditioned telephone lines. It also has a significant cost advantage over the other types of modems available today. Advances in CMOS and circuit design technology have made possible the MM74HC942—a high performance, low power, Bell 103 compatible single chip modem. This chip combines both digital and linear circuitry to bring the benefits of system level integration to modem and system designers.

THE PROCESS—microCMOS

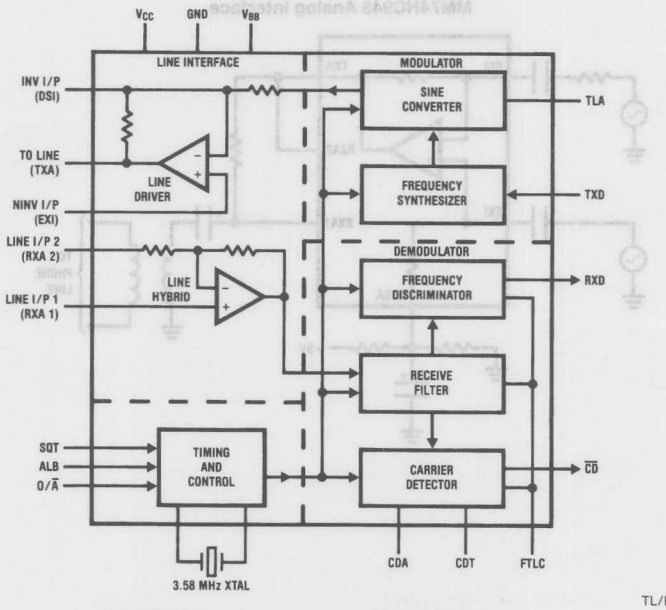
The chip was designed with National's double poly CMOS (microCMOS) process used extensively for its line of PCM CODECs and filters. This is a self-aligned, silicon gate CMOS process with two layers of polysilicon, one of which is primarily used for gates of the MOS transistors. Thus there are three layers of interconnect available (two polysilicon and one metal layer) making possible a very dense layout.

The two polysilicon layers also offer a near perfect capacitor structure which is used to advantage in the linear portions of the chip. The self-aligned silicon gate P and N-channel MOSFETs combine high gain with minimal parasitic gate-to-drain overlap capacitance, facilitating the design of operational amplifiers with high gain-bandwidth product and excellent dynamic range.

CHIP ARCHITECTURE

The chip architecture was arrived at after critically evaluating several trial system partitionings of the Bell 103 type data set. The overriding goal was to integrate as much of the function as possible without sacrificing versatility and cost effectiveness in new applications. The resulting chip architecture reflects this philosophy. Since the majority of users of this device would probably be digital designers unfamiliar with filter design and analog signal processing, inclusion of these functions was thus mandatory. The precision filters needed for a high performance modem also make discrete implementations expensive. On the other hand, the majority of new systems will typically include a microprocessor which is quite capable of handling the channel establishment protocol. Besides, different systems may require different protocols. Circuitry for this task was therefore omitted.

A block diagram illustrating the chip architecture is shown in *Figure 1*. The on-chip line driver and line hybrid greatly simplify interfacing to the phone line by saving two external op amps. The output of the line hybrid, which is used to reduce



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FIGURE 1. Chip Architecture of the MM74HC942

Reprinted from Midcon/82

the effect of the local transmit signal on the received signal, goes to a programmable receive bandpass filter. This filter improves the signal-to-noise ratio at the input of the frequency discriminator, which performs the actual FSK demodulation. The output of the receive filter is also monitored by a carrier detector which compares the amplitude of the received signal to an externally adjustable threshold level.

The modulator consists of a frequency synthesizer which generates a clock at a frequency determined by the TXD (transmit data) and O/$\overline{A}$ (originate/answer) inputs. This is subsequently shaped by the sine converter into the final modulated transmit carrier signal.

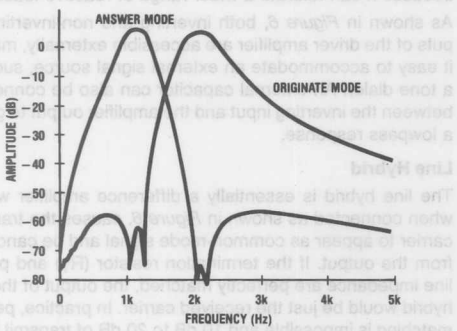
All internal clocks and control signals are derived from an on-chip oscillator operating from a common 3.58 MHz TV crystal. On-chip control logic allows the modem to be set to answer or originate mode operation, or to an analog loopback mode via the O/$\overline{A}$ and ALB inputs respectively. The line driver can be squelched via the SQT input, which typically occurs during the channel establishment sequence.

Another feature of this design not obvious from the block diagram of *Figure 1* is that the chip can be powered down by asserting the ALB and SQT inputs simultaneously, a condition that does not occur during normal operation. This cuts power consumption to typically under 50 μA, making it very suitable for battery operation.

DEMODULATOR

Receive Filter

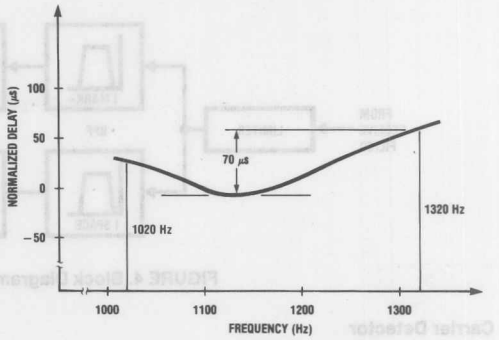
This is a nine pole, switched capacitor[1,2] bandpass filter. It is programmable by internal logic to one of two passbands, corresponding to originate or answer mode operation. The measured frequency response of the filter is shown in *Figure 2.* It shows that better than 60 dB of adjacent channel rejection has been achieved. Note also the deep notches at the frequencies of the locally transmitted tone pair.



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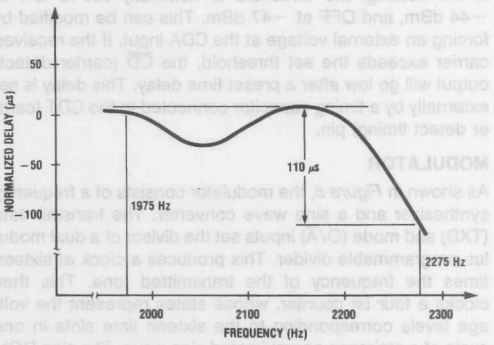
FIGURE 2. Measured Frequency Response of the Receive Filter

A key design goal was to minimize the delay distortion of the filter. This has also been met as evidenced by the delay response curves shown in *Figures 3a* and *3b.* These curves have been normalized to the delays at 1170 Hz and 2125 Hz respectively. They show that the delay distortion in the 1020 Hz to 1320 Hz band is approximately 70 μs, while that in the 1975 Hz to 2275 Hz band is approximately 110 μs. These bands contain all the significant sidebands of a 300 baud FSK signal. The low delay distortion of the receive filter translates directly into low jitter in the demodulated data.



TL/H/5532–3

FIGURE 3a. Normalized Delay Response of the Receive Filter in Answer Mode



TL/H/5532–4

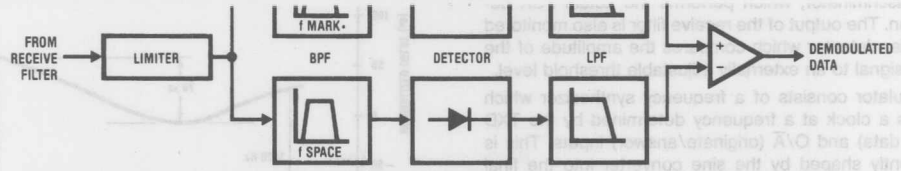
FIGURE 3b. Normalized Delay Response of the Receive Filter in Originate Mode

An on-chip, second order, real time anti-aliasing filter precedes the receive filter. This masks the sampled data nature of the switched capacitor design from the user, contributing to the ease of use of the chip.

Frequency Discriminator

Referring to *Figure 4*, the filtered receive carrier is first hard limited to remove any residual amplitude modulation. It is then split into two parallel, functionally indentical paths, each consisting of a second order bandpass filter (BPF), a full wave detector and a post detection lowpass filter (LPF).

The bandpass filter in the upper path is tuned to the 'mark' frequency, and that in the lower path to the 'space' frequency. The detectors are full wave rectifier circuits which, together with the post detection filters, measure the energy in the mark and space frequencies. These are compared by the trailing comparator to decide whether a mark or space has been received.



TL/H/5532–5

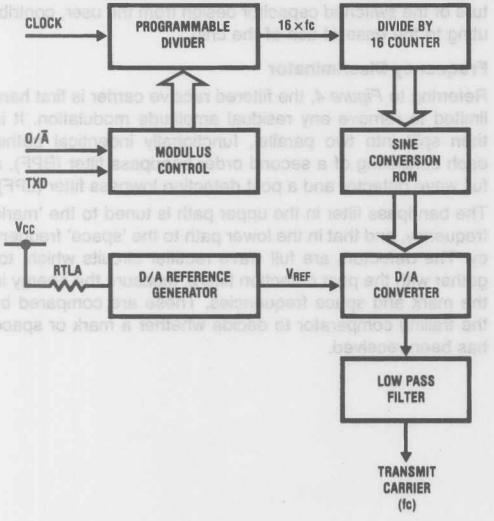
FIGURE 4. Block Diagram of the Frequency Discriminator

Carrier Detector

The carrier detector compares the output of the receive filter against an externally adjustable threshold voltage. Referring back to *Figure 1*, if the CDA (carrier detect adjust) pin is left floating, the threshold is nominally set to ON at −44 dBm, and OFF at −47 dBm. This can be modified by forcing an external voltage at the CDA input. If the received carrier exceeds the set threshold, the $\overline{CD}$ (carrier detect) output will go low after a preset time delay. This delay is set externally by a timing capacitor connected to the CDT (carrier detect timing) pin.

MODULATOR

As shown in *Figure 5*, the modulator consists of a frequency synthesizer and a sine wave converter. The transmit data (TXD) and mode (O/$\overline{A}$) inputs set the divisor of a dual modulus programmable divider. This produces a clock at sixteen times the frequency of the transmitted tone. This then clocks a four bit counter, whose states represent the voltage levels corresponding to the sixteen time slots in one cycle of a staircase approximated sine wave. The sine ROM decodes the state of the counter and drives a digital-to-analog converter to synthesize the frequency shift keyed sine wave. This modulator design also preserves phase coherence in the transmit carrier across frequency excursions.



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FIGURE 5. Modulator Block Diagram

The reference voltage for the digital-to-analog converter is derived from a reference generator controlled by an external resistor (RTLA). This allows the transmit signal level to be programmable in accordance with the Universal Service Order Code. This code specifies the programming resistances corresponding to various transmit levels. If no external resistor is connected, the transmit level defaults to −12 dBm.

The synthesized sine wave is filtered by a second order, real time low pass filter to remove spurious harmonics before being fed to the line driver amplifier.

LINE INTERFACE

Line Driver

This is a class A power amplifier designed to drive a 600Ω line through an external 600Ω terminating resistor. With the proper transmit level programming resistor installed, it will drive the line at 0 dBm when operated from ±5V supplies. The quiescent current of the output stage of the driver varies with the programmed transmit level to maximize the efficiency of the amplifier. A class A design was chosen mainly because it can tolerate a wider range of reactive loads.

As shown in *Figure 6*, both inverting and non-inverting inputs of the driver amplifier are accessible externally, making it easy to accommodate an external signal source, such as a tone dialer. An external capacitor can also be connected between the inverting input and the amplifier output to give it a lowpass response.

Line Hybrid

The line hybrid is essentially a difference amplifier which, when connected as shown in *Figure 6*, causes the transmit carrier to appear as common-mode signal and be cancelled from the output. If the termination resistor (R_T) and phone line impedance are perfectly matched, the output of the line hybrid would be just the received carrier. In practice, perfect matching is impossible and 10 dB to 20 dB of transmit carrier rejection is more realistic. The residual is more than adequately rejected by the receive filter of the demodulator.

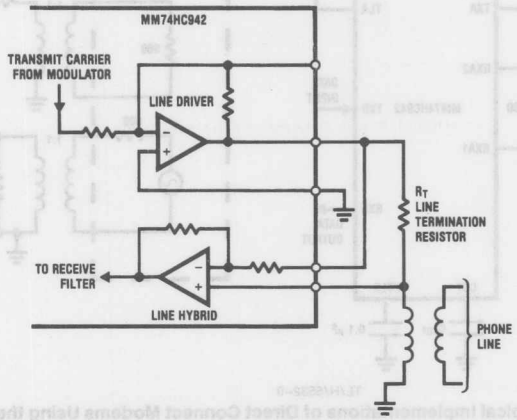
TIMING AND CONTROL

This includes an oscillator amplifier, divider chain and internal control logic. The oscillator, in conjunction with an external 3.58 MHz TV crystal and the divider chain, provides all the internal clocks for the switched capacitor circuits and the frequency synthesizer. The control logic orchestrates the various operating modes of the chip (e.g., originate, answer or analog loop-back modes).

APPLICATIONS

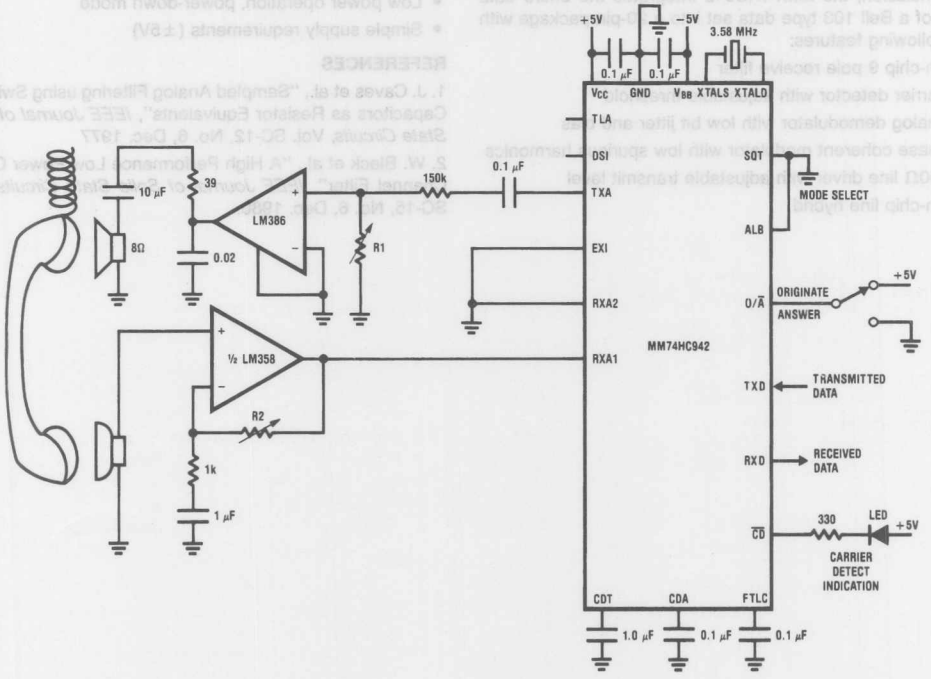
Figure 7 shows the MM74HC942 in an acoustically coupled modem application. It demonstrates the simplicity of the resulting design and a dramatic reduction in parts count. *Figure 8* shows two typical direct connect modem applications. The simplicity of these circuits is again evident.

The simple power supply requirement (±5V), low power (60 mW when transmitting at −9 dBm, 0.5 mW standby) and low external component count makes the MM74HC942 an efficient implementation of the 300 baud modem function.



TL/H/5532–7

FIGURE 6. Typical Interface Between the MM74HC942 and the Phone Line



TL/H/5532–8

FIGURE 7. Typical Implementation of an Acoustically Coupled Modem Using the MM74HC942

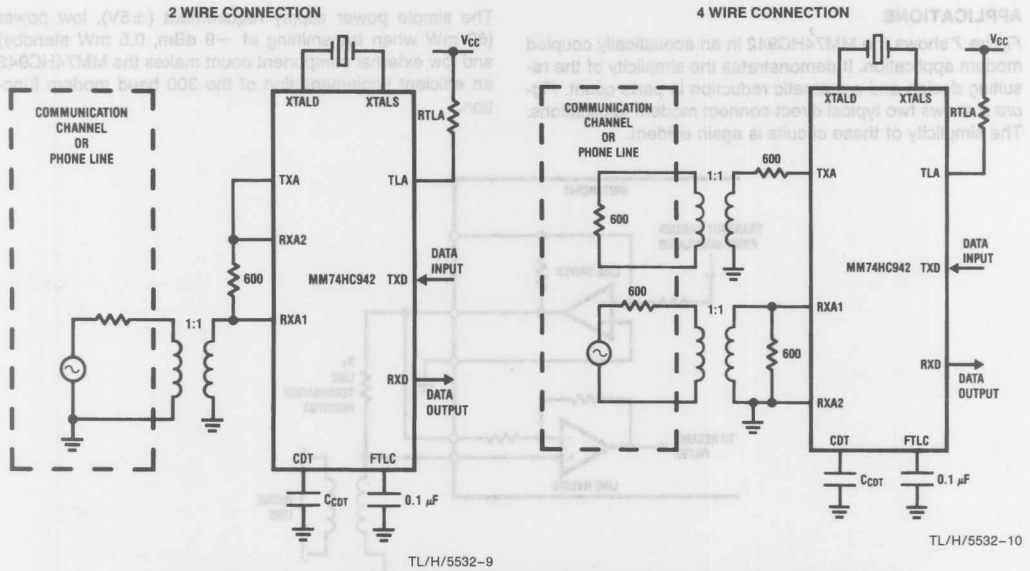


FIGURE 8. Typical Implementations of Direct Connect Modems Using the MM74HC942

SUMMARY

In conclusion, the MM74HC942 integrates the entire data path of a Bell 103 type data set into a 20-pin package with the following features:

- On-chip 9 pole receive filter
- Carrier detector with adjustable threshold
- Analog demodulator with low bit jitter and bias
- Phase coherent modulator with low spurious harmonics
- 600Ω line driver with adjustable transmit level
- On-chip line hybrid
- Full duplex originate or answer mode operation
- Low power operation, power-down mode
- Simple supply requirements (±5V)

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2. W. Black et al., "A High Performance Low Power CMOS Channel Filter", *IEEE Journal of Solid State Circuits,* Vol. SC-15, No. 6, Dec. 1980.

An Introduction to and Comparison of 54HCT/74HCT TTL Compatible CMOS Logic

National Semiconductor
Application Note 368
Larry Wakeman

The 54HC/74HC series of high speed CMOS logic is unique in that it has a sub-family of components, designated 54HCT/74HCT. Generally, when one encounters a 54/74 series number, the following letters designate some speed and power performance, usually determined by the technology used. Of course, the letters HC designate high speed CMOS with the same pinouts and functions as the 54LS/74LS series. The sub-family of HC, called HCT, is nearly identical to HC with the exception that its input levels are compatible with TTL logic levels.

This simple difference can, however, lead to some confusion as to why HCT is needed; how HCT should be used; how it is implemented; when it should be used; and how its performance compares to HC or LS. This paper will attempt to answer these questions.

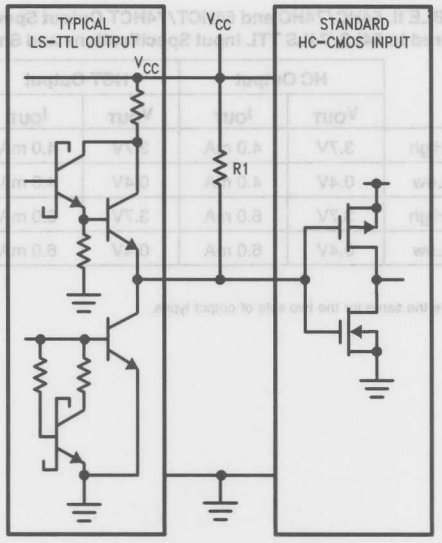
It should also be noted that not all HCTs are the same. That is, HCTs from other vendors may have some characteristics that are different. Thus, when discussing general characteristics this paper will directly address National Semiconductor's 54HCT/74HCT which is compatible with **JEDEC standard 7**. Other vendors' ICs which also meet this standard will probably have similar characteristics.

WHY DOES HCT EXIST?

Ideally, when a designer sits down to design a low power high speed system, he would like to use 54HC/74HC, and CMOS LSI components. Unfortunately, due to system requirements he may have to use NMOS microprocessors and their NMOS or bipolar peripherals or bipolar logic (54S/74S, 54F/74F, 54ALS/74ALS, or 54AS/74AS) because either the specific function does not exist in CMOS or the CMOS device may not have adequate performance. Since the system designer still desires to use HC where possible, he will mix HC with these products. If these devices are specified to be TTL compatible, incompatibilities may result at the interface between the TTL, NMOS, etc. and HC.

More specifically, in the case of where a TTL or NMOS output may drive an HC input, a specification incompatibility results. Table I lists the output drive specifications of TTL compatible outputs with the input specifications of 54HC/74HC. Notice that the output high level of a TTL specified device will not be guaranteed to have a logic high output voltage level that will be guaranteed to be recognized as a valid logic high input level by HC. A TTL output will be equal to or greater than 2.4V, but an HCMOS input needs at least 3.15V. It should be noted that in an actual application the TTL output will pull-up probably to about V_{CC} minus 2 diode voltages, and HC will accept voltages as low as 3V as a valid one level so that in almost all cases there is no problem driving HC with TTL.

Even with the specified incompatibility, it is possible to improve the TTL-CMOS interface without using HCT. *Figure 1* illustrates this solution. By merely tying a pull-up resistor from the TTL output to V_{CC}, this will force the output high voltage to go to V_{CC}. Thus, HC can be directly interfaced very easily to TTL. This works very well for systems with a few lines requiring pull-ups, but for many interfacing lines, HCT will be a better solution.



TL/F/6751–1

FIGURE 1. Interfacing LS-TTL Outputs to Standard CMOS Inputs Using a Pull-Up Resistor

The input high logic level of HC is the only source of incompatibility. 54HC/74HC can drive TTL easily and its input low level is TTL compatible. Again referring to Table I, the logic output of the TTL type device will be recognized to be a valid logic low (0) level, so there is no incompatibility here. Table II shows that the specified output drive of HC is capable of driving many LS-TTL inputs, so there is no incompatibility here either (although one should be aware of possible fanout restrictions similar to that encountered when designing with TTL).

The question then arises: since only the input high level must be altered, why not design CMOS logic to be TTL compatible? 54HC/74HC was designed to optimize performance in all areas, and making a completely TTL compatible logic family would sacrifice significant performance. Most importantly, there is a large loss of AC noise immunity, and there are speed and/or die size penalties when trying to design for TTL input levels.

Thus, since it is obvious that there is a need to interface with TTL and TTL compatible logic, yet optimum performance would be sacrificed, a limited sub-family of HCT devices was created. It is completely TTL input compatible, which enables guaranteed direct connection of TTL outputs to its inputs. In addition, HCT still provides many of the other advantages of 54HC/74HC.

WHEN TO USE 54HCT/74HCT LOGIC

The 54HCT/74HCT devices are primarily intended to be used to provide an easy method of interfacing between TTL compatible microprocessor and associated peripherals and bipolar TTL logic to 54HC/74HC. There are essentially two application areas where a designer will want to perform this interface.

1. The first case is illustrated in *Figure 2*. In this case the system is a TTL compatible microprocessor. This figure shows an NS16XXX (any NMOS μP may be substituted) that is in a typical system and therefore must be interfaced to 54HC/74HC. In this instance, the popular gate, buffer, decoder, and flip-flop functions provided in the 54HCT/74HCT sub-family can be used to interface the many lines that come from TTL compatible outputs. It is also easy to upgrade this configuration to an *all* CMOS system once the CMOS version of the microprocessor is available by replacing the HCT with HC.
2. A second application is, when in speed-critical situations a faster logic element than HC, probably ALS or AS, must be used in a predominantly 54HC/74HC system, or a specific logic function unique to TTL is placed into an HC design. This situation is illustrated in *Figure 3*. In this case, pull-up resistors on an HC input may be sufficient, but if not, then an HCT can be used to provide the guaranteed interface.

TABLE I. Output Specifications for LS-TTL and NMOS LSI Compared to the Input Specifications for HCT and HC

	LS Output		NMOS Output		HC Inputs		HCT Input		
	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{IN}	I_{IN}	V_{IN}	I_{IN}	
Output High	2.7V	400 μA	2.4V	400 μA	3.15V	1 μA	2.0V	1 μA	Input High
Output Low	0.5V	8.0 mA	0.4V	2.0 mA	0.9V	1 μA	0.8V	1 μA	Input Low

V_{CC} = 4.5V

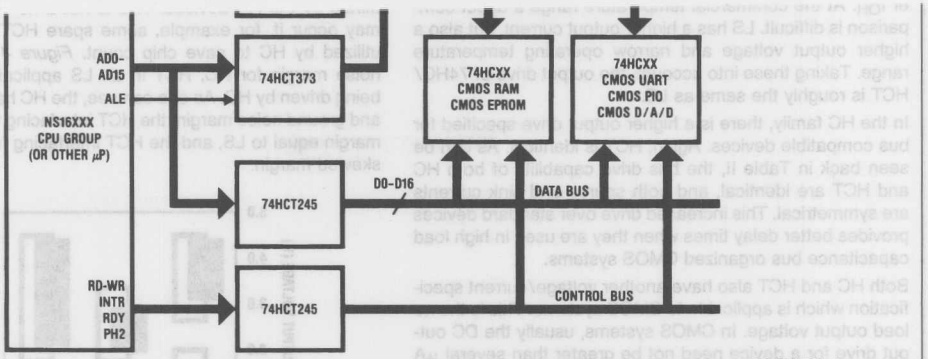
Note the specified incompatibility between the output levels and HC input levels.

TABLE II. 54HC/74HC and 54HCT/74HCT Output Specifications Compared to 54LS/74LS TTL Input Specifications and Showing Fanout

		HC Output		HCT Output		LS Inputs		
		V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{IN}	I_{IN}	Fanout
Standard Output	Output High	3.7V	4.0 mA	3.7V	4.0 mA	2.0V	40 μA	10
	Output Low	0.4V	4.0 mA	0.4V	4.0 mA	0.8V	400 μA	
Bus Output	Output High	3.7V	6.0 mA	3.7V	6.0 mA	2.0V	40 μA	15
	Output Low	0.4V	6.0 mA	0.4V	6.0 mA	0.8V	400 μA	

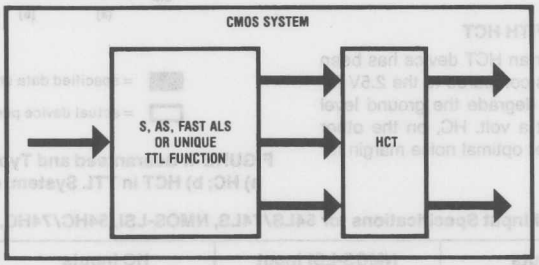
V_{CC} = 4.5V

Both HC and HCT output specifications are the same for the two sets of output types.



TL/F/6751–2

FIGURE 2. Applications Where a TTL Compatible NMOS Microprocessor is Interfaced to a CMOS System



TL/F/6751–3

FIGURE 3. A Conceptual Diagram Showing How HCT May Be Used to Interface a Faster ALS Part or Some Unique TTL Function in a CMOS System

The functions chosen for implementation in 54HCT/74HCT were chosen to avoid the undesirable situation where the designer is forced to add in an extra gate solely for the interface. A variety of HCT functions are provided to not only interface to HC, but to perform the desired logic function at the same time.

Although not the primary intention, a third use for 54HCT/74HCT is as a direct plug-in replacement for 54LS/74LS logic in already designed systems. If HCT is used to replace LS, power consumption can be greatly reduced, usually by a factor of 5 or so. This lower power consumption, and hence less heat dissipation, has the added advantage of increasing system reliability (in addition to the greater reliability of 54HC/74HC and 54HCT/74HCT). This is extremely useful in power-critical designs and may even offer the advantage of reduced power supply costs.

One note of caution: when plug-in replacing HCT for TTL, 54HCT/74HCT (as well as 54HC/74HC) does not have identical propagtion delays to LS. Minor differences will occur, as would between any two vendors' LS products. To be safe, it is recommended that the designer verify that the performance of HCT is acceptable.

PERFORMANCE COMPARISON: HCT vs HC LS-TTL

To enable intelligent use of HCT in a design, both for the interface to NMOS or TTL and for TTL replacement applications, it is useful to compare the various performance parameters of HCT to those of HC and LS-TTL.

Input/Output Voltages and Currents

Table III tabulates the input voltages for LS-TTL and LS-TTL compatible ICs, HCT, and HC. Since HCT was designed to have TTL compatible inputs, its input voltage levels are the same. However, the input currents for HCT are the same as HC. This is an advantage over LS-TTL, since there are no fanout restrictions when driving into HCT as there are when driving into LS.

Referring to Table II, the output voltage and current specifications for HC and HCT gates are shown. As can be seen, the output specifications of HCT are identical to HC. This was chosen since the primary purpose of HCT is to drive into HC as the interface from other logic.

There are some differences as to how LS-TTL, ALS-TTL and AS-TTL outputs are specified when compared to HCT (or HC), as shown in Table IV. The military parts are easy to compare. HC/HCT has the same I_{OL} as LS and much greater I_{OH}. At the commercial temperature range a direct comparison is difficult. LS has a higher output current, but also a higher output voltage and narrow operating temperature range. Taking these into account, the output drive of 74HC/HCT is roughly the same as LS.

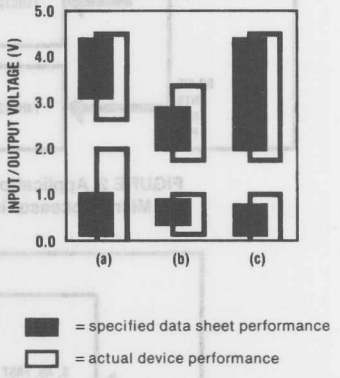
In the HC family, there is a higher output drive specified for bus compatible devices. Again, HCT is identical. As can be seen back in Table II, the bus drive capability of both HC and HCT are identical, and both source and sink currents are symmetrical. This increased drive over standard devices provides better delay times when they are used in high load capacitance bus organized CMOS systems.

Both HC and HCT also have another voltage/current specification which is applicable to CMOS systems. This is the no load output voltage. In CMOS systems, usually the DC output drive for a device need not be greater than several μA since all CMOS inputs are very high impedance. For this reason, there is a 20 μA output voltage specification which says that 54HC/74HC and 54HCT/74HCT will pull to within 100 mV of the supplies.

NOISE MARGIN TRADEOFFS WITH HCT

The nominal trip point voltage for an HCT device has been designated to be around 1.4V, as compared to the 2.5V for a standard HC device. This will degrade the ground level noise margin for HCT by almost a volt. HC, on the other hand, has its trip point set to offer optimal noise margin for both V_{CC} and ground.

This may be a minor point since normally HCT is mixed with TTL and in this case the worst-case system noise margin is defined by the TTL circuits. If the HCT is being driven only by HC and not LS, then the worst-case V_{CC} margin is determined by the HC devices. This is not a normal usage, but may occur if, for example, some spare HCT logic can be utilized by HC to save chip count. *Figure 4* graphs input noise margin for HC, HCT in an LS application and HCT being driven by HC. As one can see, the HC has a large V_{CC} and ground noise margin, the HCT interfacing from LS has a margin equal to LS, and the HCT interfacing from HC has a skewed margin.



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FIGURE 4. Guaranteed and Typical Noise Margins for a) HC; b) HCT in TTL System; c) HCT in HC System

TABLE III. A Comparison of Input Specifications for 54LS/74LS, NMOS-LSI, 54HC/74HC, and 54HCT/74HCT

	LS Inputs		NMOS-LSI Input		HC Inputs		HCT Input	
	V_{IN}	I_{IN}	V_{OUT}	I_{OUT}	V_{IN}	I_{IN}	V_{IN}	I_{IN}
Input High	2.0V	40 μA	2.0V	10 μA	3.15V	1 μA	2.0V	1 μA
Input Low	0.8V	400 μA	0.8V	10 μA	0.9V	1 μA	0.8V	1 μA

V_{CC} = 4.5V

The HCT specifications maintain the TTL compatible input voltage requirements and the HC input currents.

TABLE IV. This Compares the Output Drive of HC and HCT to LS for both the Military Temperature Range and the Commercial Temperature Range Devices at Rated Output Currents

	Military Temperature				Commercial Temperature*			
	HC/HCT Output		LS Output		HC/HCT Output		LS Output	
	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}
Input High	3.7V	4.0 mA	2.5V	400 μA	3.84V	4.0 mA	2.7V	400 μA
Input Low	0.4V	4.0 mA	0.4V	4.0 mA	0.33V	4.0 mA	0.5V	8.0 mA

V_{CC} = 4.5V

*The commercial temperature range for HC/HCT is −40°C to +85°C, but for LS is 0°C to +70°C.

POWER CONSUMPTION OF HCT

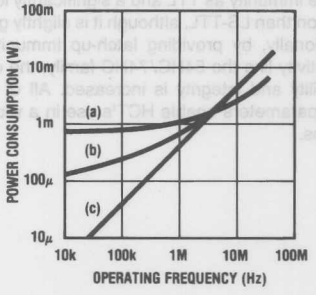
In normal HC applications, power consumption is essentially zero in the quiescent state but is proportional to operating frequency when operating. In LS, large quiescent currents flow which overshadow (except at very high frequencies) other dynamic components. 54HCT/74HCT is a combination of these, depending on the application. Both quiescent and frequency-dependent power can be significant.

Referring back to *Figure 1*, this figure shows an LS-TTL output driving an HCT input. To see how quiescent current is drawn, notice that it is possible to have valid TTL voltages of 2.7V and 0.4V (ignoring the pull-up resistor). With 0.4V on the HCT input, we find the input N-channel transistor OFF and the P-channel ON. Thus, the output of this stage is high. Also, since one of the P- or N-channel transistors is OFF, no quiescent current flows. However, when the HCT input is high, 2.7V, the N-channel is ON and the P-channel is slightly ON. This will cause some current to flow through both the transistors, even in the static state.

Thus in a TTL application, HCT has the unusual characteristic that it will draw static current only when its inputs are driven by TTL (and TTL-like) outputs, and only when those outputs are high. Thus, to calculate total power, this quiescent power must be summed with the frequency-dependent component.

When HCT is driven by HC, as it possibly might be, the HC outputs will have high and low levels of V_{CC} and ground; never statically turning on both transistors simultaneously. Thus in this application, HCT will only dissipate frequency-dependent power, and C_{PD} calculations can be made to determine power (see National Semiconductor Application Note, AN-303). In the latter application, HCT will dissipate the same amount of power as HC; in the first TTL application, the power dissipated will be more since there is also a DC component.

To show this, *Figure 5* plots power versus frequency for an HCT00 being driven by HC, typical LS and worst-case LS. Notice that at the lower frequencies, the DC component for the TTL input is much greater; at higher frequencies, the two converge as the dynamic component becomes dominant.



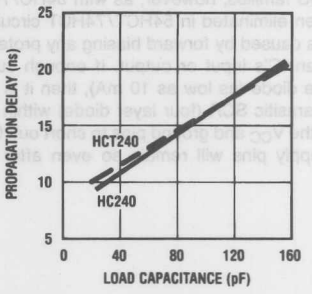
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FIGURE 5. Power Consumption of 74HCT00 Being Driven by a) Worst-Case TTL Levels; b) Typical TTL Levels; c) CMOS Levels

SPEED/PROPAGATION DELAY PERFORMANCE

Of primary importance is the speed at which the components operate in a system. HCT was designed to have the same basic speeds as HC. This was accomplished in spite of the fact that HCT requires the addition of a TTL input translator, which will add to internal propagation delays. A second concern in the design was to maintain the required speeds while minimizing the possible power consumption of the input stage when driven to TTL high levels.

These requirements dictated designing HCT on a slightly more advanced 3μ N-well process, as well as increasing the die to help compensate for speed loss. This process is slightly faster than the standard HC process, and this enables the HCT parts to have the same delays as their HC counterparts, while minimizing possible quiescent currents. *Figure 6* shows a comparison of 74HCT240 and 74HC240 propagation delays, and they are identical.



TL/F/6751–6

FIGURE 6. Typical propagation delay vs load for 74HC240 and 74HCT240 are virtually the same. Slight differences result from different design and processing.

sured using the 1.3V on both the input and the output waveforms.

The different test conditions for HCT result because HCT will be primarily used in LS-TTL applications. If HCT is used in HC systems, the actual speeds will be slightly different, but the differences will be small (< 1 ns–2 ns).

HC and HCT speeds are not identical to LS-TTL. Some delays will be faster and some slightly slower. This is due to inherent differences in designing with CMOS versus bipolar logic. For an average system implemented in HC or LS-TTL, the same overall performance will result. On an individual part basis, some speeds will differ, so the designer should not blindly assume that HC or HCT will duplicate whatever a TTL IC does.

CMOS LATCH-UP AND ELECTROSTATIC DISCHARGE OF 54HCT/74HCT

These two phenomena are not strictly performance related in the same sense that speed or noise immunity are. Instead, latch-up and electrostatic discharge (ESD) immunity impact the ease of design, insusceptibility to spurious or transient signals causing a failure, and general reliability of 54HCT/74HCT.

Latch-up is a phenomenon that is a traditional problem with older CMOS families; however, as with 54HC/74HC, latch-up has been eliminated in 54HCT/74HCT circuits. In older CMOS, it is caused by forward biasing any protection diode on either an IC's input or output. If enough current flows through the diode (as low as 10 mA), then it is possible to trigger a parasitic SCR (four layer diode) within the IC that will cause the V_{CC} and ground pins to short out. Once shorted, the supply pins will remain so even after the trigger occur in 54HC/74HC or 54HCT/74HCT. If one attempts to cause latch-up by forcing current into the protection diodes, the IC will be overstressed in the same manner as overstressing a TTL circuit.

ESD has also been a concern with CMOS ICs. Primarily for historical reasons, MOS devices have always been considered to be sensitive to damage due to static discharges. However, process enhancements and careful input protection network design have actually improved 54HC/74HC and 54HCT/74HCT immunity to where it is actually better than bipolar logic. This includes 74ALS, 74LS, 74S, 74AS and 74F. ESD is measured using a standard military 38510 ESD test circuit, which zaps the test device by discharging a 100 pF capacitor through a 1.5 kΩ resistor into the test circuit. ESD test data is shown in National Semiconductor Reliability Report, PR-11.

CONCLUSION

HCT is a unique sub-family designation of HC. It is intended primarily for TTL level to HC interfacing, although it is far from restricted only to this application. HCT can be used as a pin-for-pin socket replacement of TTL, or can be mixed with HC logic.

54HCT/74HCT has the same speeds as HC and LS, the same noise immunity as TTL and a significantly lower power consumption than LS-TTL, although it is slightly greater than HC. Additionally, by providing latch-up immunity and low ESD sensitivity like the 54HC/74HC family, the overall system reliability and integrity is increased. All of these performance parameters enable HCT's use in a wide range of applications.

High-Speed-CMOS designs address noise and I/O levels

National Semiconductor
Application Note 375
Larry Wakeman



To maximize the benefits of high-speed CMOS, you must cope with environmental interactions and component limitations. Especially important are system noise decoupling and both transient and steady-state level control.

Designs using high-speed-CMOS logic, such as the MM54HC/74HC Series, can attain characteristics that mark improvements over LS-TTL designs. To optimize these characteristics, however, you must adopt proper design procedures. This article deals with the ICs' input-output and noise-immunity considerations.

High-speed CMOS logic is essentially a digital-IC family that combines TTL (bipolar) and CD4000 (CMOS) characteristics. Because of the family's high speed, you must be more aware of the requirements of fast systems than in the case of CD4000B logic. Although the 54HC/74HC IC's CMOS construction results in noise immunity comparable to the CD4000 family, its high speed necessitates system-grounding and supply-decoding techniques normally used in LS-TTL system design.

The following sections discuss general usage guidelines, system noise susceptibility and immunity, and the 54HC/74HC logic's power-supply-noise characteristics. Note that, unless specific exceptions are stated, the considerations discussed apply also to 54HCT/74HCT, HC's TTL-compatible subset.

FOLLOW BASIC GUIDELINES

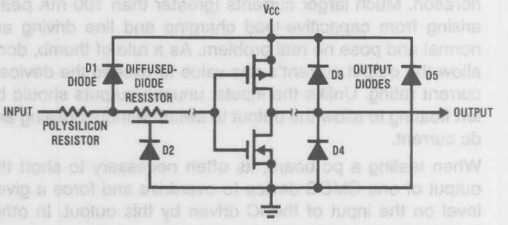
The basic rules for designing with 54HC/74HC circuits are similar to those that apply to 74LS, CD4000B and 54C/74C devices. First, under normal static operating conditions, the input should not exceed V_{CC} or go below ground. In normal high-speed systems, transients and line ringing can cause inputs to violate this rule momentarily, forcing the ICs to enter an SCR-latch-up mode.

Latch-up results if either the input- or output-protection diodes are forward biased because of voltages above V_{CC} or below ground. As a result, the IC's internal parasitic SCR shorts V_{CC} to ground *Figure 1* shows the diodes in a CMOS IC, schematically **(a)** and in a simplified die cross section **(b)**.

Thanks to some processing refinements, SCR latch-up isn't a problem with the MM54HC/74HC Series. There are, however, limitations on the currents that the internal metallization and protection diodes can handle, so for high-level transients (pulse widths less than 20 ms and inputs above V_{CC} or below ground), you must limit the current of the IC's internal diode to 20 mA rms, 100 mA peak. Usually, a simple resistor configured in series with the input suffices.

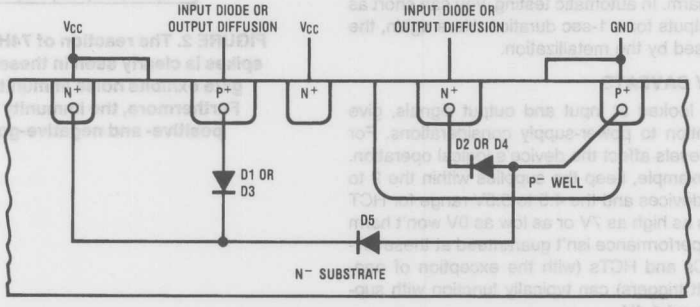
Powering the device is another important design concern. Don't power up inputs before both V_{CC} and ground are con-

(a)



TL/F/8127–1

(b)



TL/F/8127–2

FIGURE 1. Essential but sometimes evil, the diodes in CMOS-logic ICs can be easily damaged by excessive currents. Reversed supplies or large input or output currents can cause diode burnout.

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nected, and don't plug or unplug pc boards into or from powered connectors unless input currents are short lived or limited in the manner already described. Both conditions can forward bias input diodes, resulting in excessive diode currents. Again, *Figure 1* shows these diodes and the possible current paths. If these conditions are unavoidable, add external current limiting to prevent damage to 54HC/74HC circuits, or use special connectors that apply power before signals. Some family members (notably the HC4049/50) have modified input structures and can survive the application of power to the input before the supply.

Floating inputs are a frequently overlooked problem. CMOS inputs have extremely high impedance and, if left open, can float to any voltage. This situation can result in logic-function mishaps and unnecessary power consumption. Moreover, open inputs are susceptible to electrostatic damage. You should thus tie unused inputs to V_{CC} or ground, either through a resistor or directly.

Finally, for correct logic results you should use inputs with rise and fall times faster then 500 ns. Slower transition times can result in logic errors and oscillation.

OBSERVE OUTPUT RULES

You must observe certain usage rules for 54HC/74HC outputs as well as for inputs. Output voltages shouldn't exceed the supply voltage, and currents in the output diodes shouldn't exceed 20 mA. Moreover, output rms drive currents shouldn't exceed 25 mA for 4 mA standard-output devices or 35 mA for 6 mA devices. The die's metal lines dictate this limitation. Violations can result in long-term deterioration. Much larger currents (greater than 100 mA peak) arising from capacitive-load charging and line driving are normal and pose no real problem. As a rule of thumb, don't allow the output current's rms value to exceed the device's current rating. Unlike the inputs, unused outputs should be left floating to allow the output to switch without drawing any dc current.

When testing a pc board, its often necessary to short the output of one CMOS device to overdrive and force a given level on the input of the IC driven by this output. In other instances, you might need to short the outputs on a one-time basis. You can do so without degrading the IC's life if you follow a few rules. When bench testing 54HC/74HC devices, for example, you can short one output for several minutes without harm. In automatic testing, you can short as many as eight outputs for a 1-sec duration. Here again, the limitation is imposed by the metallization.

POWER-SUPPLY CAVEATS

Now that you've looked at input and output signals, give some extra attention to power-supply considerations. For instance, supply levels affect the device's logical operation. You should, for example, keep the supplies within the 2 to 6V range for HC devices and the 4.5 to 5.5V range for HCT devices. Voltages as high as 7V or as low as 0V won't harm the ICs, but their performance isn't guaranteed at these levels. However, HCs and HCTs (with the exception of one-shots and Schmitt triggers) can typically function with supplies as low as about 1.4V.

As with any IC, it's crucial that you *not* reverse the supply voltages. Doing so will forward bias a substrate diode between V_{CC} and ground (*Figure 1*), resulting in excessive currents and damage to the IC. As with inputs and outputs, don't let V_{CC} or ground rms currents exceed 50 mA for

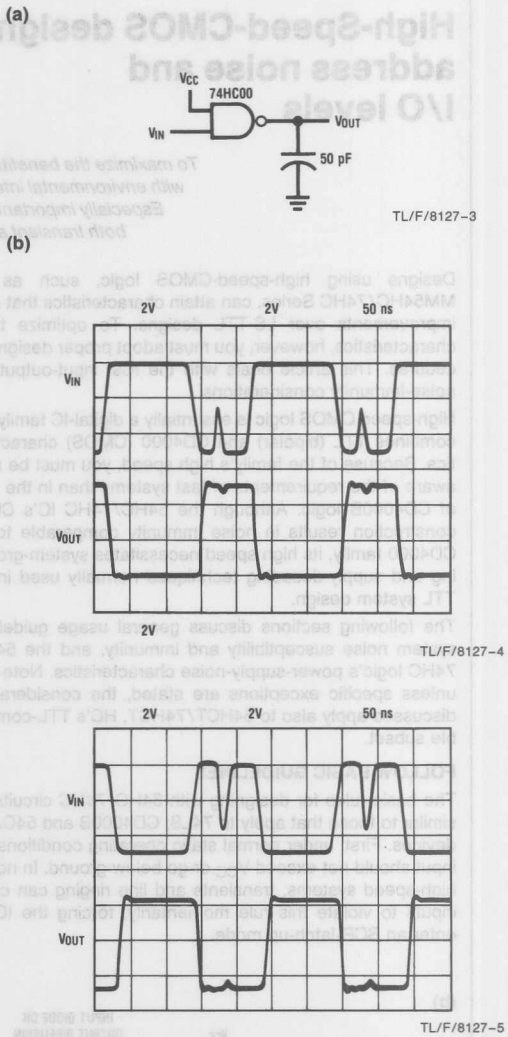


FIGURE 2. The reaction of 74HC00 gates (a) to noise spikes is clearly seen in these scope drawings. The gate exhibits noise immunity of 2V or more (b). Furthermore, the immunity is equally good for positive- and negative-going noise spikes.

4 mA devices or 70 mA for 6 mA units. Again, transients pose no real problem as long as their rms values stay within the devices' ratings.

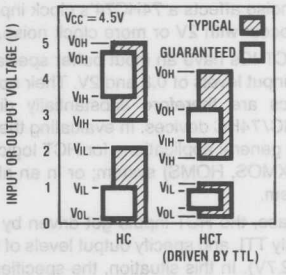
UNDERSTANDING NOISE

What happens if the signals just discussed aren't clean? In digital-logic systems, "noise" is defined as extraneous voltage in the signal or supply paths. For CMOS, ECL or TTL devices, system noise that's great enough can affect the logic's integrity. CMOS-logic families such as the CD4000 and 74C are highly immune to certain types of system noise. This immunity is due mainly to the nature of CMOS, but also to the fact that the devices' slowness reduces self-induced supply noise and crosstalk and prevents the logic from responding to short externally induced or radiated transients.

However, in high-speed CMOS (which is about 10 times faster than CD4000 logic), crosstalk, induced supply noise and noise transients become factors. Higher speeds allow the device to respond more quickly to externally induced noise transients and accentuate the parasitic interconnection inductances and capacitances that increase self-induced noise and crosstalk.

Because HC-CMOS specifies input levels similar to those of CD4000 logic, its dc noise rejection is also superior to LS-TTL. And because high-speed CMOS has an output impedance one-tenth that of CD4000 devices, it's less susceptible to noise currents coupled to its outputs. As a result, lower stray voltages are induced for a given amount of current coupling.

To quantify these noise parameters, first define "noise immunity": a device's ability to prevent noise on its input from being transferred to its output. More specifically, it's the amount of voltage that can be applied to an input without causing the output to change state. For HC-CMOS, this immunity is approximately 2V; in the worst case, it's the maximum input Low or High logic levels specified in the data sheet.



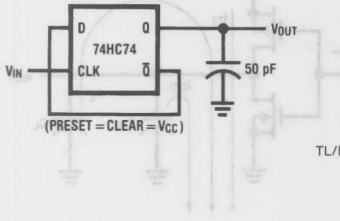
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FIGURE 4. Noise margins for HC-CMOS and an HCT-CMOS-TTL combination are illustrated by this graph. You can see that the all-CMOS system exhibits the higher noise immunity.

Noise immunity is an important attribute, but noise margin proves more useful because it defines the amount of noise that a system can tolerate and still maintain correct logic operation. It's defined as the difference between the output logic Low (or High) of one gate and the input logic Low (or High) of the gate the given device is driving.

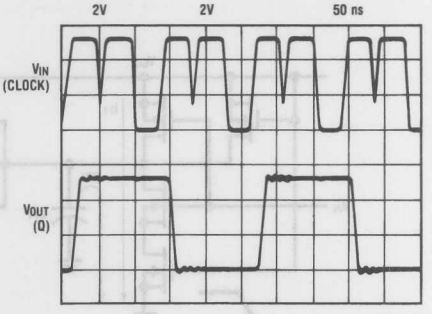
For example, in HC-CMOS using a 4.5V V_{CC}, typical output levels are ground and V_{CC}, and input thresholds are $V_{IH} = 3.15V$ and $V_{IL} = 0.9V$. These figures yield noise margins of approximately 1300 mV (logic One) and 850 mV (logic Zero). LS's noise immunity is 700 and 400 mV, respectively. Note that 54HC/74HC input levels are skewed slightly toward ground, so the ICs tolerate slightly more V_{CC} noise than ground noise.

(a)



TL/F/8127–7

(b)



TL/F/8127–8

FIGURE 3. Exhibiting high clock-noise immunity, this 74HC74 flip flop (a) shows no change in output for noise spikes greater than 2V (b)

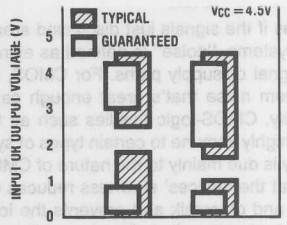
shows how noise affects a 74HC74's clock input. Again, no logic errors occur with 2V or more clock noise.

54HCT/74HCT ICs have an input buffer specially designed to yield TTL input levels of 0.8 and 2V. Their noise-immunity characteristics are therefore substantially different from those of 54HC/74HC devices. In evaluating these differences, note two general applications for HCT logic: in a TTL or NMOS (eg, XMOS, HOMS) system; or in an all-CMOS, HC or HCT system.

In the first case, the HCT inputs get driven by outputs that are essentially TTL and specify output levels of 0.4 and 2.4V (or 0.5 and 2.7V). In this situation, the specified noise margin is similar to the TTL margin: 400 mV for a logic Zero and either 400 or 700 mV for a logic One. These values, shown in *Figure 4*, are significantly less than those of an all-HC system.

Now examine the second case. When using HCT with HC, output logic levels are almost equal to power-supply levels. Therefore, HCT's specified noise margin is approximately 700 mV for a logic Zero and 2.4V for a logic One. At first glance, the high noise margin for Ones might seem strange, but this situation presents a tradeoff against the Zero-level margin. Compare the two gate-transfer functions in *Figure 5*; the HCT device has a logic trip point at 1.4V, while the HC gate trips at 2.4V. Thus, HC's typical performance is twice that of HCT for ground noise; for V_{CC} noise, HCT is about 50% better.

The conclusion? In a normal system (including all-CMOS systems), HC provides better noise immunity than HCT. The one case where HCT could prove more helpful is in systems that are designed with noiseless ground and dirty V_{CC}. Naturally, this design approach isn't good. A second fact highlighted by these transfer functions, HC is conservatively specified for its input and output logic levels, whereas HCT is specified more tightly. So even though data-sheet limits for HCT seem better, actual system performance indicates that HC provides better overall noise margins.



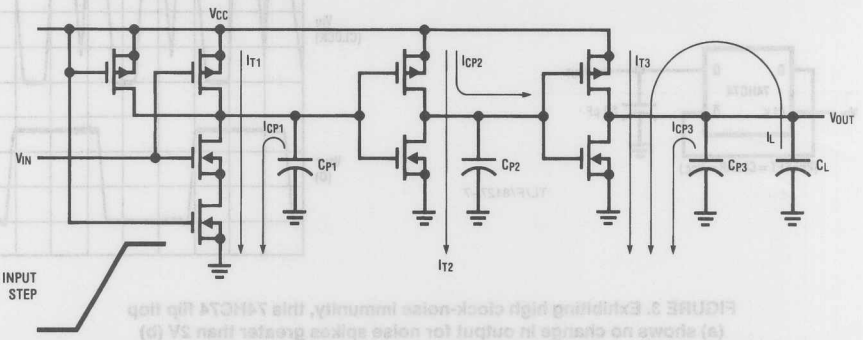
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FIGURE 5. Comparing HC and HCT logic, this graph shows noise immunity of the respective families. HC wins for ground noise, HCT for V_{CC} noise.

CONSIDER SYSTEM NOISE

Now take a closer look at system noise, which you can group into several categories, depending on the source. The type of noise dictates the appropriate noise-supression technique.

- Power-supply I_{CC} noise, generated in the power-supply line, comes from logic switching in CMOS circuits.
- Transmission-line reflections, unwanted ringing and overshoot phenomena arise from signals propagating down improperly terminated transmission and signal lines.
- Signal crosstalk is caused by capacitive or inductive coupling of extraneous voltages from one signal line to another or to the power-supply line.
- Radiated noise, an RF phenomenon that originates within a high-speed-logic system, emits to other systems. It arises from the high-frequency energy emitted when logic toggles. This noise, not a major problem with regard to logic integrity, can interfere with other systems.



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FIGURE 6. This schematic shows the currents in a 74HC00 gate that result when applying a positive input step. Also shown are the internal parasitic and external load capacitances.

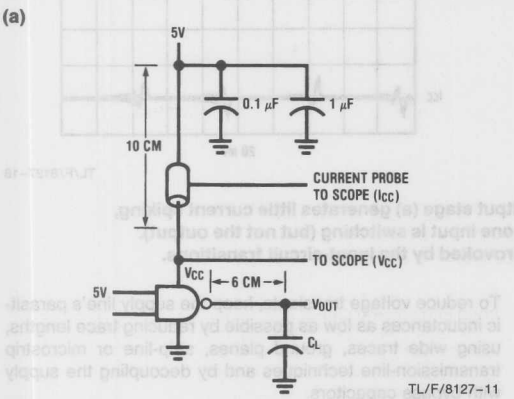
Power-supply spiking is perhaps the most important contributor to system noise. When any element switches logic states, it generates a current spike that produces a voltage transient. If these transients become too large, they can cause logic errors because the supply-voltage drop upsets internal logic, or because a supply spike on one circuit's output feeds an extraneous noise voltage into the next device's input.

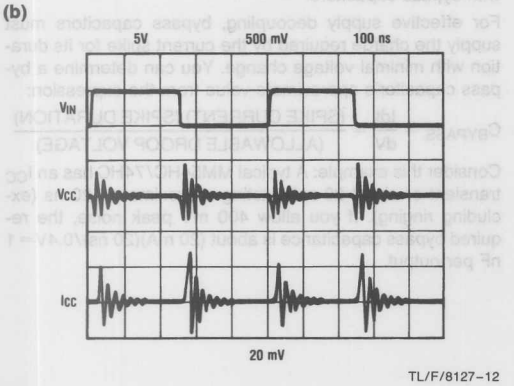
With CMOS logic in its quiescent state, essentially no current flows between V_{CC} and ground. But when an internal gate or an output buffer switches state, a momentary current flows from V_{CC} to ground. This current has two components: the current required to charge and discharge any stray or load capacitance, and the current that flows directly from V_{CC} to ground when the p- and n-channel transistors turn on momentarily during an input transition.

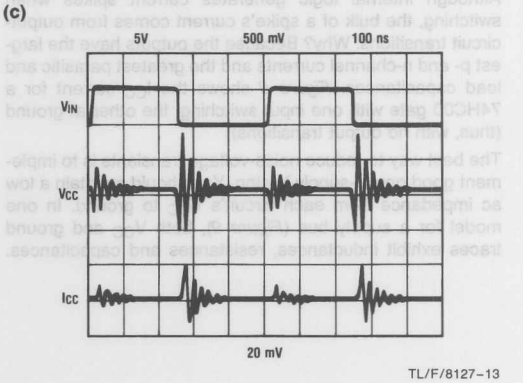
Figure 6 shows the paths for these current components within a 74HC00 upon application of a positive step to the device's input. C_{P1}, C_{P2}, and C_{P3} represent the internal parasitic capacitances; C_L is the external load capacitance. I_{T1}, I_{T2} and I_{T3} correspond to the currents that flow through both the n- and p-channel transistors during switching. I_{CP1}, I_{CP2} and I_{CP3} are the charging currents for the capacitances.

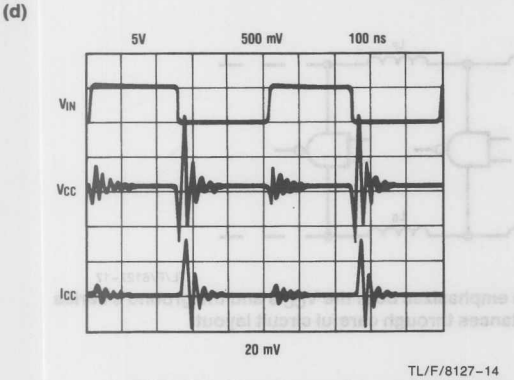
The switching transient caused by an unloaded output changing state typically equals 40 mA peak. *Figure 7b* shows the current and voltage spikes resulting from switching a single unloaded NAND gate. *Figures 7c* through *(e)* show the current spike's increase due to the addition of 15-, 50- and 100-pF loads. The large amount of ringing results from the test circuit's transmission-line effects.

This ringing occurs partly because the CMOS gate switches from a very high impedance to a very low one and back









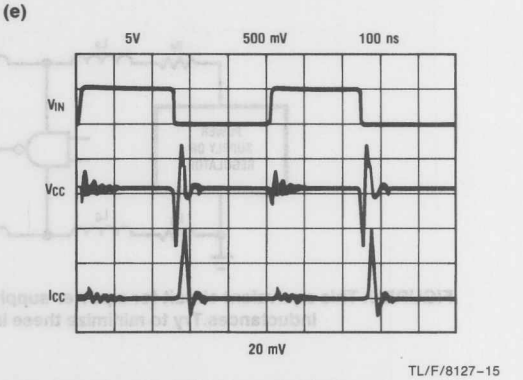


FIGURE 7. The effects of capacitive loads are seen in these drawings; (b) through (e) show the spikes resulting with no load and with 15-, 50- and 100-pF loads, respectively. The ringing arises from the test circuit's transmission-line effects.

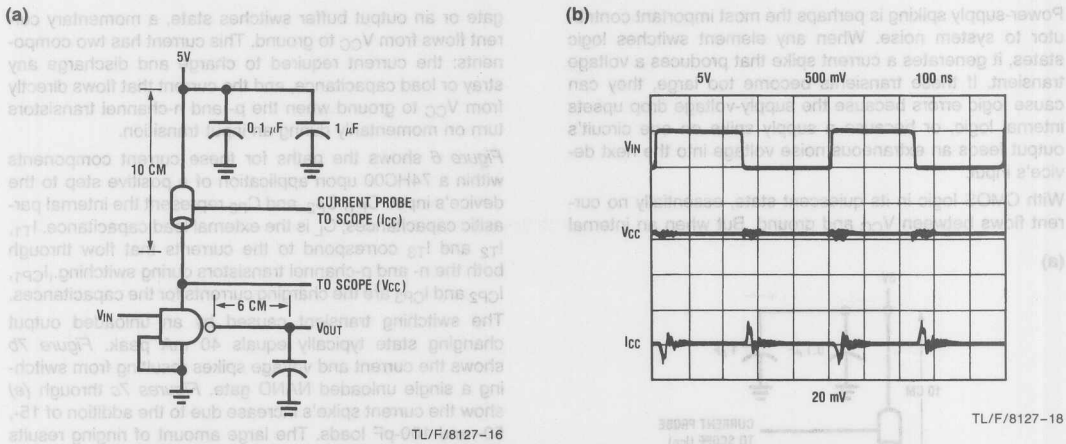


FIGURE 8. On-chip circuitry before a 74HC00's output stage (a) generates little current spiking, as shown in the drawing (b). In the test circuit, one input is switching (but not the output). Note the very small power-supply glitches provoked by the input-circuit transitions.

again. Note that, even for medium-size loads, load-capacitance current becomes a major current contributor, verified by the dramatic increase in current from the unloaded to the 100-pF-load case.

Although internal logic generates current spikes when switching, the bulk of a spike's current comes from output-circuit transitions. Why? Because the outputs have the largest p- and n-channel currents and the greatest parasitic and load capacitances. *Figure 8* shows the I_{CC} current for a 74HC00 gate with one input switching, the other at ground (thus, with no output transitions).

The best way to reduce noise-voltage transients is to implement good power-supply busing. You should maintain a low ac impedance from each circuit's V_{CC} to ground. In one model for a supply bus (*Figure 9*), both V_{CC} and ground traces exhibit inductances, resistances and capacitances.

To reduce voltage transients, keep the supply line's parasitic inductances as low as possible by reducing trace lengths, using wide traces, ground planes, strip-line or microstrip transmission-line techniques and by decoupling the supply with bypass capacitors.

For effective supply decoupling, bypass capacitors must supply the charge required by the current spike for its duration with minimal voltage change. You can determine a bypass capacitor's approximate value from the expression:

$$C_{BYPASS} = \frac{Idt}{dV} = \frac{(\text{SPIKE CURRENT})\,(\text{SPIKE DURATION})}{(\text{ALLOWABLE DROOP VOLTAGE})}$$

Consider this example: A typical MM54HC/74HC has an I_{CC} transient of about 20 mA, lasting approximately 20 ns (excluding ringing). If you allow 400 mV peak noise, the required bypass capacitance is about (20 mA)(20 ns)/0.4V = 1 nF per output.

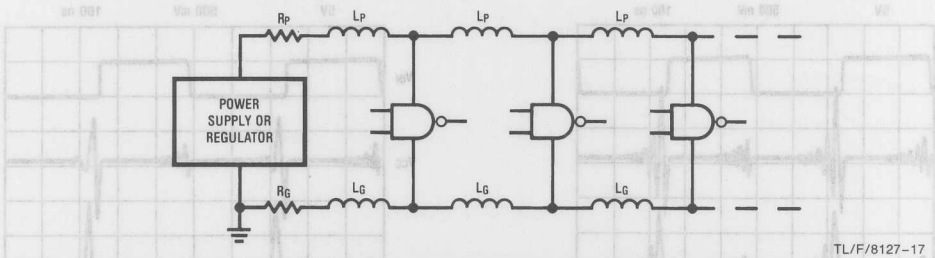
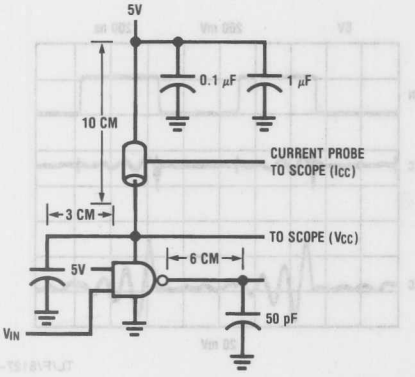


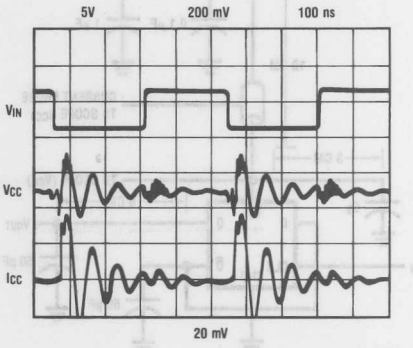
FIGURE 9. This equivalent circuit for a power-supply bus emphasizes both the V_{CC}'s and the ground's series inductances. Try to minimize these inductances through careful circuit layout.

(a)



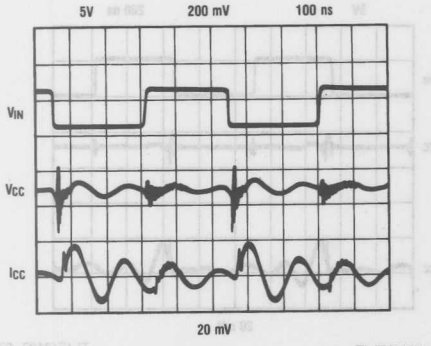
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(b)



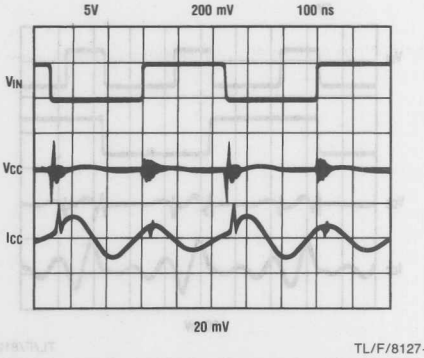
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(c)



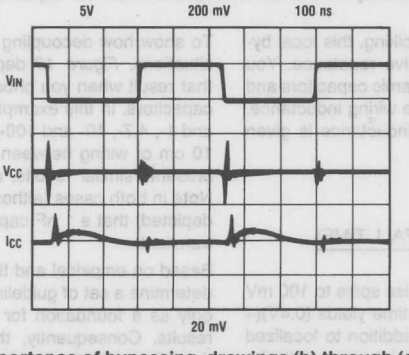
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(d)



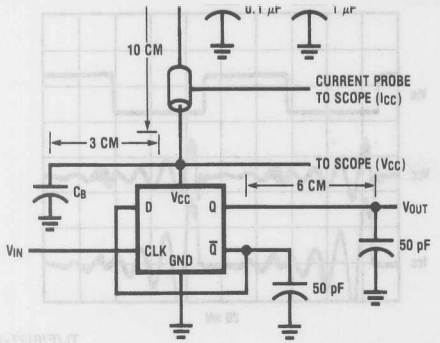
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(e)



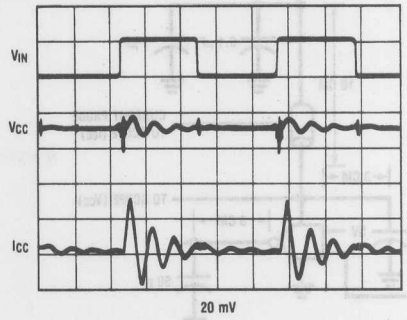
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FIGURE 10. Demonstrating the importance of bypassing, drawings (b) through (e) show power-supply transients that occur when a 74HC00 is decoupled with 1-, 4.7-, 10- and 100-nF capacitors, respectively.



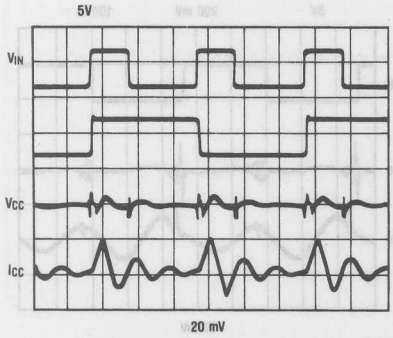
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(b)

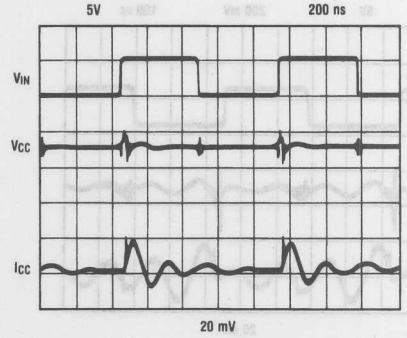


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(d)



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TL/F/8127–27

FIGURE 11. Showing results similar to those depicted in Figure 10, these drawings show the effects of bypassing a 74HC74 flip flop with capacitors of 1 (b) to 10 nF (d). You can see that the 10 nF bypass yields supply spiking approximately 40% lower than that of the 1-nF capacitor.

In order to prevent additional voltage spiking, this local bypass capacitor must exhibit low inductive reactance. You should therefore use high-frequency ceramic capacitors and place them very near the IC to minimize wiring inductance. The approximate amount of tolerable inductance is given by:

$$L_{SUPPLY} = \frac{Vdt}{di} =$$

$$\frac{\text{(SPIKE VOLTAGE) (SPIKE RISE OR FALL TIME)}}{\text{(SPIKE CURRENT)}}$$

For example, restricting the inductive noise spike to 100 mV peak with 20 mA current and 4 ns rise time yields (0.4V)(4 ns)/20 mA = 80 nH max. Note that, in addition to localized decoupling of very fast transients, you also need bulk decoupling of spikes generated by the board's ICs. To decouple, provide a high-value capacitor for smoothing long time periods.

To show how decoupling affects supply noise in real-world situations, *Figure 10* depicts the power-supply transients that result when you choose different values of decoupling capacitors. In this example, one gate of a 74HC00 toggles, and 1-, 4.7-, 10- and 100-nF capacitors have approximately 10 cm of wiring between them and the supply. *Figure 11* presents similar results, obtained with the 74HC74 circuit. Note in both cases (although the unbypassed situation isn't depicted) that a 1 nF capacitor greatly reduces the voltage transient.

Based on empirical and theoretical considerations, you can determine a set of guidelines. These practical maxims serve only as a foundation for a system that should yield good results. Consequently, there's some leeway in following them for particular designs. As a rule of thumb, it's generally good design practice to restrict both V_{CC} and ground noise to less than 250 mV.

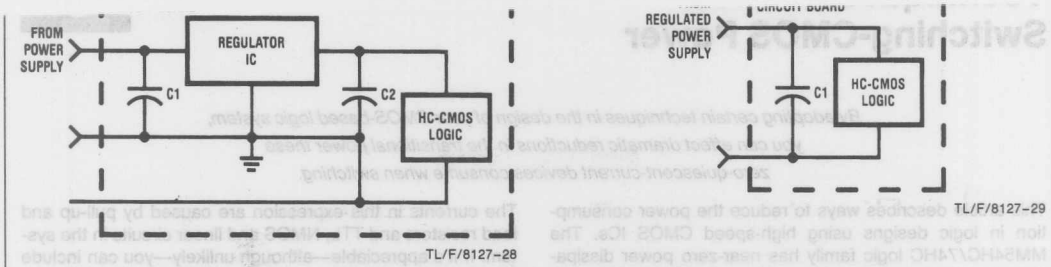


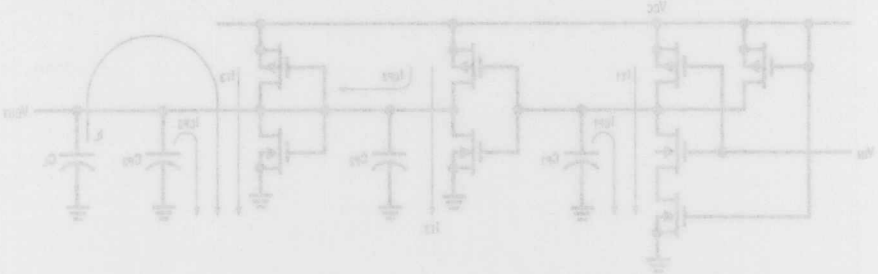
FIGURE 12. Tailor bypassing to the system's supply scheme. Circuit diagram (a) shows the method to use with local regulators; (b) shows the scheme to adopt with a centralized regulated supply. Use tantalum- or aluminum-electrolytic capacitors.

Before presenting the guidelines, examine some comparative attributes of earlier CMOS, HC, HCT and LS-TTL devices. First, because of higher speeds and larger output currents, the supply-bypassing requirements of HC devices are more rigorous than those of earlier metal-gate-CMOS ICs. Compared with those of LS-TTL, the requirements for HC/HCT are similar or a little more stringent, depending on the application.

Furthermore, for random logic, 54HC/74HC and 54LS/74LS are similar, but in bus-driving applications HC devices can produce larger spikes. Finally, HCT logic needs better grounding than HC logic. In fact, its design considerations closely follow those of LS-TTL. However, as with HC, HCT exhibits greater V_{CC} spiking in bus-driving applications.

Now you're ready for the guidelines:

- Keep V_{CC}-bus routing short. When using double-sided or multilayer circuit boards, use strip-line, transmission-line or ground-plane techniques.
- Keep ground lines short, and on pc boards make them as wide as possible, even if trace width varies. Use separate ground traces to supply high-current devices such as relay and transmission-line drivers.
- In systems mixing linear and logic functions and where supply noise is critical to the analog components' performance, provide separate supply buses or even separate supplies.
- If you use local regulators, bypass their inputs with a tantalum capacitor of at least 1 μF (*Figure 12a*), and bypass their outputs with a 10- to 50-μF tantalum- or alumium-electrolytic capacitor *(b)*.
- If the system uses a centralized regulated power supply, use a 10- to 20-μF tantalum-electrolytic capacitor or a 50- to 100-μF aluminum-electrolytic capacitor to decouple the V_{CC} bus connected to the circuit board (*Figure 12b*).
- Provide localized decoupling. For random logic, a rule of thumb dictates approximately 10 nF (spaced within 12 cm) per every two to five packages, and 100 nF for every 10 packages. You can group these capacitances, but it's more effective to distribute them among the ICs. If the design has a fair amount of synchronous logic with outputs that tend to switch simultaneously, additional decoupling might be advisable. Octal flip flops and buffers in bus-oriented circuits might also require more decoupling. Note that wire-wrapped circuits can require more decoupling than ground-plane or multilayer pc boards.
- For circuits that drive transmission lines or large capacitive loads (μP buses, for example), use a 10 nF ceramic capacitor close to the devices' supply pins.
- Finally, terminate transmission-line grounds near the drivers.



Logic-System Design Techniques Reduce Switching-CMOS Power

National Semiconductor
Application Note 376
Larry Wakeman

By adopting certain techniques in the design of your CMOS-based logic system, you can effect dramatic reductions in the transitional power these zero-quiescent-current devices consume when switching.

This article describes ways to reduce the power consumption in logic designs using high-speed CMOS ICs. The MM54HC/74HC logic family has near-zero power dissipation when in the quiescent mode. Its only substantial power drain arises from dynamic switching currents. Traditional TTL and NMOS systems do not share this low-power feature, requiring instead that you reduce power by selecting low-power ICs and external components.

The CMOS device is inherently efficient, but you can greatly enhance system efficiency by designing around the following guidelines:

- minimizing effective system operating frequency;
- minimizing static dc-current paths (eg, in pull-up or -down resistors);
- putting the logic to sleep (by removing the clock);
- capitalizing on power-down situations.

Total system power dissipation is the sum of two components: static (or quiescent) and dynamic power. LS TTL systems consume such a great amount of quiescent power that the dynamic component pales into insignificance. When using 54HC/74HC logic in power-critical applications, however, you must consider both components. The following sections describe how to determine system power by using HC devices' power-dissipation-capacitance (C_{PD}) specs. The text also discusses a few power-reduction philosophies and some of the differences in consumption for 54HCT/74HCT TTL-compatible CMOS logic. Because system power is simply total I_{CC} times the supply voltage, the calculations treat power and current interchangeably.

Calculating the quiescent power is just as easy—the sum of the dc currents times the supply voltage. Thus, total system quiescent power is

$$P_{SYSTEM} = (I_{CC1} + I_{CC2} + \ldots I_{CCn})\, V_{CC}. \qquad (1)$$

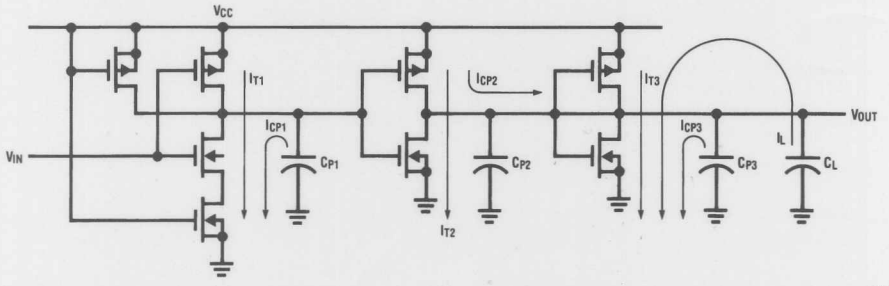
The currents in this expression are caused by pull-up and load resistors and TTL, NMOS and linear circuits in the system. If it's appreciable—although unlikely—you can include the very small quiescent I_{CC} of MM54HC/74HC devices. Generally, the worst-case I_{CC} values in the CMOS ICs' data sheets are very conservative. Typical values range from ten to 100 times less than the limits; moreover, it's almost statistically impossible for a system to contain all worst-case devices.

As pointed out earlier, the major contributors to CMOS ICs' power dissipation are dynamic switching currents. *Figure 1* is a schematic diagram of one 74HC00 NAND gate, and it shows the dynamic currents that result from switching one input Low to High. When the IC is not switching, there's no dc-current path from V_{CC} to ground except for leakage. This is because whenever an n-channel device is On, its complementary p-channel partner is Off.

CMOS power consumption is caused by the transient currents that charge and discharge internal and external capacitances during logic transitions. As frequency increases, these currents naturally increase. You can't measure these currents or their associated capacitances individually, but you can measure the total current. You can equate this total current to a power-dissipation capacitance (C_{PD}) as follows:

$$I_{CC} = (C_{PD} + C_L)(V_{CC})(f_{IC}), \qquad (2)$$

where I_{CC} is the supply current, V_{CC} is the supply voltage, f_{IC} is the input toggle rate and C_L is the toggled load capacitance. Referring again to *Figure 1*, the load current I_L results from switching the load capacitance. To obtain the internal equivalent capacitance, you must subtract the load current from I_{CC}.



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FIGURE 1. Principal contributors to CMOS power consumption, these transient currents are the result of transitional charging and discharging of internal and load capacitances. The average currents are naturally a function of the operating frequency.

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Using the C_{PD} figure spec'd in data sheets, you can estimate the current consumption of each device in your system if you know the toggling frequency. By multiplying both sides of **Equation 2** by V_{CC}, you can determine the dynamic power consumption.

$$P_{DYNAMIC} = (C_{PD} + C_L)(V_{CC}^2)(f). \quad (3)$$

As mentioned, C_{PD} is an indirect measure of the amount of switching current a circuit consumes. It depends on how much of the circuit's internal logic is switching and how many outputs are toggling. For example, a 74HC374 octal 3-state flip flop clocked at 1 MHz dissipates much more power if its data inputs change every clock period than it would if its outputs are disabled and its inputs are tied High or Low during clocking.

Figure 3 shows that when the flip flop's outputs are enabled and the data inputs are changing, virtually all internal nodes are toggling and all internal parasitic capacitances are charging. On the other hand, if the data is held High and the outputs are disabled, only the clock logic dissipates power (and very little at that). All other sections are static.

As you'll see, the method of testing C_{PD} (see "Test C_{PD} in realistic situations") can yield various values that might or might not be applicable to the particular way the part is being used. Fortunately, several generalizations allow reasonable approximations to C_{PD}'s value, as discussed in the following section.

TEST C_{PD} IN REALISTIC SITUATIONS

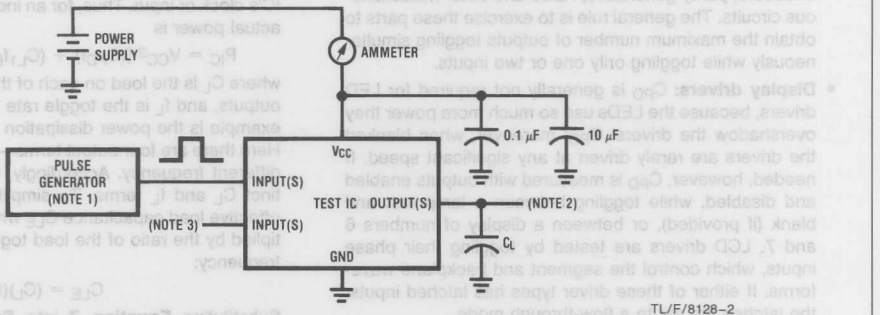
In 54HC/74HC data sheets, one or two C_{PD} values are specified. At best, the parameter is a simplification of the worst-case operating mode of a device under typical operating conditions. However, because most devices have several possible toggling modes (each having a different power consumption), you might do well to characterize C_{PD} for your particular application.

The nearby *Figure 2* shows a circuit for measuring C_{PD}. Normally, the IC is set up in a given toggling mode, with its output pins pulled out of the test socket to reduce stray-induced errors. For automated testing, you could use a standard load (eg, 50 pF) and subtract its I_{CC} contribution from the total. The ammeter in series with the V_{CC} line is bypassed with 0.1- and 1-μF capacitors.

For simple measurements, you can set the input's toggle frequency at 200 kHz, with $V_{CC} = 5V$. This yields an ammeter reading in microamps that's equal to C_{PD} in picofarads. You could use other voltages and frequencies, but little variation should result. For example, JEDEC's high-speed-CMOS committee recommends 1 MHz.

To better understand what datasheet C_{PD} means, the following listing describes by part type how each IC is toggled. In measuring C_{PD}, the worst path is always chosen. Moreover, within the constraints listed, as much of the internal circuitry and as many of the outputs as possible are toggled simultaneously.

- **Gates:** All inputs except one are held at either V_{CC} or ground, depending on which state causes the output to toggle. The one remaining input is toggled at a given frequency. C_{PD} is given on a per-gate basis.
- **Decoders:** One input is toggled, thereby causing the outputs to toggle at the same rate. Normally, one of the address-select pins is switched while the decoder is enabled. All other inputs are tied to V_{CC} or ground, whichever enables operation. C_{PD} is expressed on a per - independent - decoder basis.



Notes: 1. OUTPUT = square wave with ≤ 6-nsec rise and fall times; levels = GND and V_{CC}.
2. Bend all output pins from test socket, or use known load and deduct its current from measured I_{CC}.
3. Terminate all unused inputs to GND or V_{CC}.

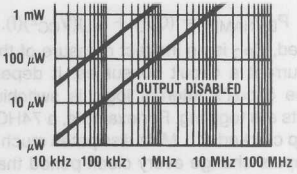
FIGURE 2. Measure equivalent CMOS-system capacitance with this simple test circuit. The text describes how to toggle the various CMOS logic functions (excepting one-shots, of course, which draw dc power).

outputs both enabled and disabled. C_{PD} is measured per multiplexer function.

- **3-state buffers and transceivers:** When the outputs are enabled, C_{PD} is measured as for simple gates; ie, on a per-buffer basis. The same holds true for the 3-state condition. Transceivers are measured per buffer as well, both enabled and disabled.
- **Latches:** The device is clocked and data is toggled every other clock pulse. Other preset or clear inputs are held to enable output toggling. If the device has commonly clocked latches, the clock is toggled and one latch is exercised. 3-state latches are measured with their outputs both enabled and disabled. C_{PC} is given on a per-latch basis.
- **Flip flops:** The same as for latches. The device's inputs are configured to toggle, and any preset or clear inputs are held inactive.
- **Shift registers:** The register is clocked and the serial data input is toggled every other clock pulse, as for latches and flip flops. Other clear or load pins are held inactive, and parallel data inputs are held at V_{CC} or ground. 3-state devices are measured with outputs both enabled and disabled. If the device takes parallel loads only, it's loaded with 10101010... and clocked to shift the data out, then reloaded.
- **Counters:** A signal is applied to its clock input; other clear or load inputs are held inactive. C_{PD} is given for each counter within a package.
- **Arithmetic circuits:** adders, magnitude comparators, encoders, parity generators, ALUs and other miscellaneous circuits. The general rule is to exercise these parts to obtain the maximum number of outputs toggling simultaneously while toggling only one or two inputs.
- **Display drivers:** C_{PD} is generally not required for LED drivers, because the LEDs use so much more power they overshadow the drivers' C_{PD}; moreover, when blanked the drivers are rarely driven at any significant speed. If needed, however, C_{PD} is measured with outputs enabled and disabled, while toggling between a lamp test and blank (if provided), or between a display of numbers 6 and 7. LCD drivers are tested by toggling their phase inputs, which control the segment and backplane waveforms. If either of these driver types has latched inputs, the latches are set to a flow-through mode.
- **One-shots:** In some cases, when a device's I_{CC} is significant, C_{PD} might not be specified. When it is, C_{PD} is tested by toggling one trigger input such that the output is a square wave. The timing resistor is tied to a separate V_{CC} line, to eliminate its power contribution.

FIGURING DYNAMIC SYSTEM POWER

How do you calculate a system's dynamic power? You can do it on several levels, depending on the accuracy needed. The simplest approach is to use a C_{PD} model that's the sum of the CMOS ICs' C_{PD}s and the load capacitances. Then, assuming an average frequency, plug these numbers into **Equation 2** or **Equation 3.**



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FIGURE 3. Output status determines dynamic dissipation in this 3-state-output flip flop. The IC dissipates an order-of-magnitude higher power with its outputs enabled.

The most accurate approach, however, is to determine each component's operating frequency and its capacitive load. This method is used in critical battery powered applications. The following section describes this approach and proposes simplifications. In this approach, system dynamic power is the sum of the individual circuits' power dissipation:

$$P_T = P_1 + P_2 + P_3 + P_4 + \ldots \text{etc}, \quad (4)$$

where P_T is the total power and P_n is the power for each component. By substituting **Equation 3** into **Equation 4,** the total system power is

$$P_T = (C_{P1} + C_{L1})(V_{CC}^2)(f) + (C_{P2} + C_{L2})(V_{CC}^2)(f) + \ldots\text{etc}. \quad (5)$$

In **Equation 5,** load capacitances C_{L1}, C_{L2}, etc are not simply the sum of all individual output loads. C_L is actually dependent on device type. Why? Different devices switch a different number of outputs simultaneously. What's more, these outputs can toggle at a different rate from that of the IC's clock or input. Thus, for an individual IC and its load, the actual power is

$$P_{IC} = V_{CC}^2 [(C_{PD}f) + (C_{L1}f_{L1}) + (C_{L2}f_{L2}) + \ldots], \quad (6)$$

where C_L is the load on each of the simultaneously toggling outputs, and f_L is the toggle rate seen by the load. A good example is the power dissipation of a 4-bit CMOS counter. Here there are four output terms—each output switches at a different frequency. Accordingly, there are four (each) distinct C_L and f_L terms. To simplify **Equation 6,** define an effective load capacitance C_{LE} which is the actual load multiplied by the ratio of the load toggle rate to the IC's toggle frequency:

$$C_{LE} = (C_L)(f_L/f). \quad (7)$$

Substituting **Equation 7** into **Equation 6** and grouping terms,

$$P_{IC} = V_{CC}^2 f(C_{PD} + C_{LE1} + C_{LE2} + \ldots). \quad (8)$$

This procedure simplifies the process because output toggle rates are almost exclusively a binary division of the input clock. Thus, for an accurate calculation of system power, you must calculate it for each IC using **Equation 8** and take the total. The counter is a prime candidate for using **Equation 8.** Here, the first stage's effective output capacitance is half the actual; the second, one-quarter, and so on.

TAILOR f, C TO DEVICE TYPE

To make practical use of the foregoing methods, the following list describes most of the CMOS-logic categories in terms of effective load and operating frequency:

- **Gates and buffers:** Power calculations for these are straightforward. C_{PD}, given for each gate, sums directly with its output load. Operating frequency is the rate at which the output toggles. For disabled 3-state buffers, the power calculation uses the 3-state-output C_{PD} multiplied by the input frequency (no load capacitance included.)
- **Decoders:** Each independent decoder can toggle no more than two outputs at a time. To calculate power consumption, sum C_{PD} with the load on two outputs. The frequency is the rate at which the outputs switch.
- **Multiplexers:** For non-3-state devices, sum the loads on all used outputs and add the sum to C_{PD}. The frequency is that at which the outputs switch. For 3-state devices, use only C_{PD}; the frequency is the inputs' toggle rate.
- **Counters:** The operating frequency for each of a counter's outputs is that of the previous stage divided by two. The loads on lower order stages contribute less current. So to calculate power, sum C_{PD} with one-half the first stage's load plus one-quarter the second stage's, and so on. For decade and other modulo counters, this procedure is slightly different. In general, you can neglect outputs more than four stages removed from the clock. A simple approximation is to sum C_{PD} with the average output load and use the input clock frequency.
- **Latches, flip flops and shift registers:** For these devices, the frequency is the ICs' clock rate. The outputs typically change state at half the clock rate, so when calculating power dissipation, add C_{PD} to half the output load. If the data inputs change more slowly, you can modify the effective load downward by the ratio of the data rate to the clock rate. Again, if the outputs are disabled, no load dissipation exits and you should use the 3-state C_{PD}.

These rules notwithstanding, it's rarely necessary to go through a detailed analysis of each IC. In most instances, a simpler analysis can yield good results. In noncritical applications where power consumption is used to determine the system's power-supply needs, the simpler analysis suffices. Using this method, you estimate the average operating frequency for major sections of the system. Next, sum all the C_{PD}s and effective loads in each section:

$$P_{BLOCK} = V_{CC}^2 f_{AVG} [(C_{P1} + C_{LE1}) + (C_{P2} + C_{LE2}) + \ldots + (C_{Pn} + C_{LEn})]. \quad (9)$$

Thus, to approximate the total system's power consumption, you must approximate the effective loads for each group of devices (or the entire system) and add them together.

Consider a microprocessor-based system using an 8 MHz clock frequency. In this example, you might determine that the bus operates at approximately 2 MHz, random control logic at 4 MHz, and the RAM and I/O devices at 100 kHz. You could estimate an overall system clock to be 1 to 2 MHz, depending on the actual size of each block. Next, you'd sum the C_{PD} and the effective load capacitances—say 2000 and 1000 pF, respectively. The ballpark estimate for system power is

$$P = (5)^2 (1 \text{ MHz})(2000 \text{ pF} + 1000 \text{ pF}) = 75 \text{ mW}. \quad (10)$$

Exceptions to the above rules are one-shot ICs and gates configured as oscillators, which use CMOS in an essentially linear manner. Their power consumption is not strictly attributable to negligible quiescent currents or dynamic switching currents.

Consider one-shots, some of which draw dc current continuously, some only when the output pulse is triggered (check data sheets for the device type you're using). The culprits are the ICs' internal linear CMOS comparators that use dc bias circuits. HC one-shots use several design approaches. One (the 'HC123A/221A/423A) uses a comparator that shuts off after a pulse times out; the second (the 'HC4538) leaves the comparators on at all times.

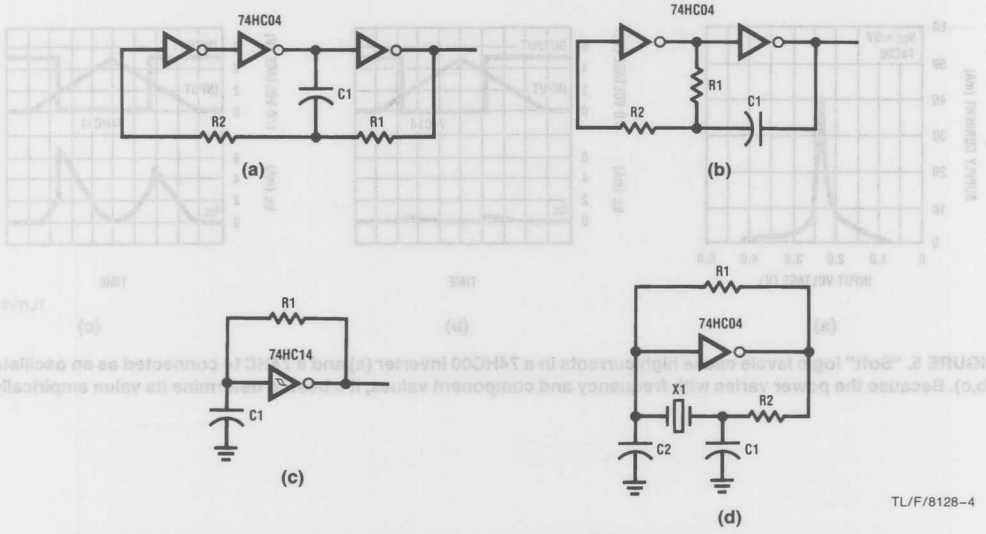


FIGURE 4. Drawing higher-than-calculated power, these CMOS oscillator configurations suffer from "soft" logic levels at their gates' inputs. Circuits (a) through (d) are 3-inverter, 2-inverter, Schmitt-trigger and crystal oscillators, respectively.

A one-shot's overall power consumption is its quiescent power plus the power consumed by its timing elements and C_{PD}. If the comparators turn off, you multiply the quiescent current by the duty cycle of the output pulse. Thus, the overall expression for one-shot power consumption is

$$P_{OS} = (I_{CC})(V_{CC})(D) + (C_{EXT} + C_L + C_{PD})(V_{CC}^2)(f), \quad (11)$$

where P_{OS} is the total power, D the one-shot's duty cycle, C_{EXT} the timing capacitor, C_L the load on both outputs, and f the operating frequency. In general, the C_{PD} term is small at lower frequencies; you can safely set it to zero to simplify the equation.

What about oscillators? The circuits shown in *Figure 4* draw more current at a given operating frequency than you'd calculate using only C_{PD}. This is because in these applications, the inputs to some of the gates are at "soft" logic levels for significant amounts of time. This causes both p- and n-channel transistors to conduct simultaneously and hence draw dc current.

Figure 5a plots current vs input voltage for the 74HC00 gate and gives an idea of the amount of current typically drawn when soft logic levels are applied. The large spike at 2.3V is the result of the output's switching. At low frequencies, the oscillator's supply current can be several milliamps higher than you might expect because of the amount of dc current drawn.

The same is true of a 74HC14 used as an oscillator. *Figure 5b* shows the supply current vs input voltage for the 74HC14 and the 74C14 (or CD40106). Because the actual power consumed vaires with frequency and component values, it's best to determine it empirically. As with the one-shots, the oscillator timing capacitor's contribution to power dissipation can be expressed by $P = V_{CC}(C_t)f$.

MM54HC/74HC logic uses bigger devices and lower transistor thresholds than metal-gate CMOS, so it might be more desirable to use either CD4000 or MM54C/74C logic for lower power oscillators (if operating frequency and output-drive requirements permit.)

MORE SPECIAL CASES: HCT

Because of their unique applications in TTL and NMOS systems, 54HCT/74HCT devices have some additional traits that you should consider in designing systems. In TTL systems, the HCT ICs' inputs are driven under worst-case conditions by TTL levels of 0.5 and 2.4V. With these input levels applied, HCT consumes significant quiescent current: about 200 to 500 μA per input. You must consider this dc current when calculating power.

To see the origins of this quiescent current, refer to *Figure 6,* which shows a typical HCT's input. With a 2.4V input level, the n-channel transistor turns fully on; the p-channel device turns slightly on. This scenario results in a quiescent current dependent on the number of logic-One inputs applied. The 0.5V level is close enough to ground to cause the n-channel transistor to turn off, so HCT ICs draw quiescent current only when its inputs are at a high state.

The I_{CC} values with these logic levels are specified in the HCT data sheets. It's specified on a per-input basis—this allows you some flexibility in determining quiescent power when an IC is driven by both CMOS and TTL. The specified quiescent-current value results in calculated I_{CC} values of several milliamps per IC, significantly less than that of LS TTL circuits.

Note, however, that using this data-sheet approach yields current values roughly five times higher than that actually seen in system designs. The reason for this is that the I_{CC} test is spec'd at $V_{CC} = 5.5V$ and $V_{IN} = 2.4V$, but even worst-case TTL output-High levels are at least 3.4V under these conditions. Output levels can only attain a low 2.4V with $V_{CC} = 4.5V$. Moreover, both TTL and NMOS outputs typically assume levels closer to 3V (at $V_{CC} = 4.5V$), lowering quiescent current more. The point is, don't let I_{CC} specs scare you into thinking CMOS is a power hog.

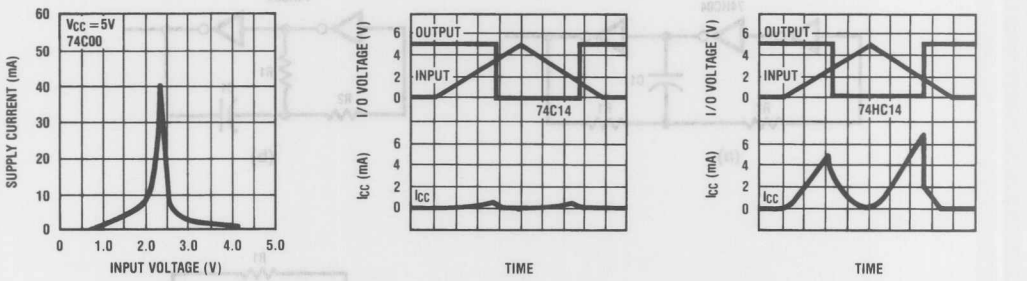


FIGURE 5. "Soft" logic levels cause high currents in a 74HC00 inverter (a) and a 74HC14 connected as an oscillator (b,c). Because the power varies with frequency and component values, it's best to determine its value empirically.

In mixed TTL-CMOS applications, the calculation of power consumed by the HCT logic must take into account both the dynamic and the quiescent currents.The dynamic portion is the same as that for HC logic—in fact, C_{PD} is measured with 0 and 5V input levels to exclude any quiescent current. The static portion is the sum of the number of TTL logic-One inputs times their High-period duty cycle times the current per input. For a single IC, the power consumption is

$$P_{IC} = (V_{CC})(I_{CC})(N)(D) + V_{CC}^2 f(C_{PD} + C_{LE}), \quad (12)$$

where C_{LE} is defined as before, N is the number of TTL-driven inputs and D is the logic-High duty cycle.

I_{CC} is the data sheet's per-input spec. This expression can then be one term in **Equation 4.** If you're using the package-level quiescent current, the terms N and D drop out.

What about a situation in which HC drives HCT? In this scenario, ground and V_{CC} levels are applied, thereby ensuring that the p- and n-channel transistors don't turn on simultaneously. You can thus determine HCT power dissipation just as for HC by using C_{PD}.

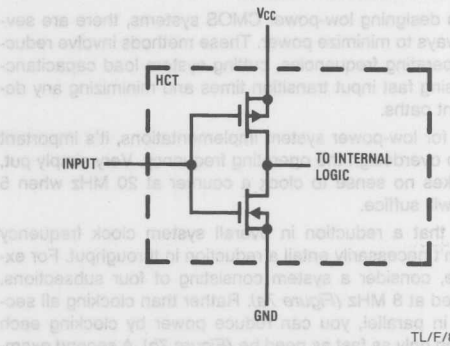


FIGURE 6. TTL-compatible CMOS is a special case. This schematic shows the 54HCT/74HCT family's input buffer. With a 2.4V input applied, the n-channel transistor is fully On; the p-channel, slightly On.

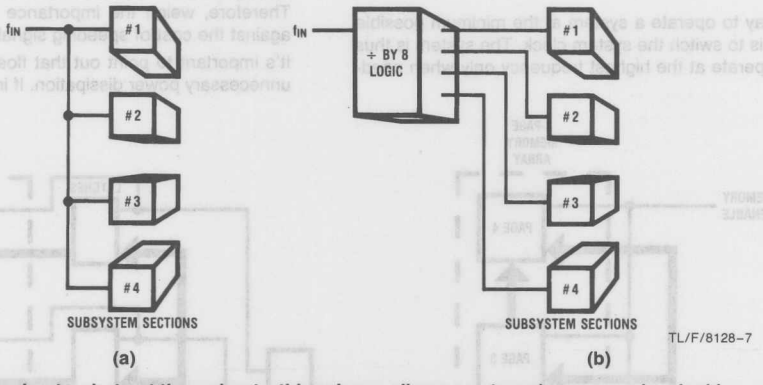


FIGURE 7. Reducing clock rate—but not throughput—this scheme allows you to reduce power by clocking a system's n subsections only as fast as needed, instead of clocking all system blocks at the full clock frequency

ing operating frequencies, cutting system load capacitances, using fast input transition times and minimizing any dc-current paths.

First, for low-power system implementations, it's important not to overdesign the operating frequency. Very simply put, it makes no sense to clock a counter at 20 MHz when 5 MHz will suffice.

Note that a reduction in overall system clock frequency doesn't necessarily entail a reduction in throughput. For example, consider a system consisting of four subsections, clocked at 8 MHz *(Figure 7a).* Rather than clocking all sections in parallel, you can reduce power by clocking each section only as fast as need be *(Figure 7b).* A second example of reducing the overall system clock rate is shown in *Figure 8.*

In (*a*), a CMOS memory array is driven directly from the CPU's address bus. Here, every memory is driven at the bus frequency. If, however, the address is latched by each memory block only when that block is being accessed (*b*), then only the block currently being accessed is clocked. This is why some CMOS RAMs incorporate on-chip address latches.

Another way to operate a system at the minimum possible frequency is to switch the system clock. The system is thus made to operate at the highest frequency only when needed. Two clocks are usually provided by two separate oscillators, either of which can feed a divide-by-two circuit that provides a square-wave output. The flip flop's output is the system clock. The system's μP can set or reset the flip flop so that it can operate at either frequency.

Besides frequency reduction, there are several other methods to save power, including reducing load capacitances. You can accomplish this by reducing wiring capacitance (especially in high-frequency sections) through good layout practices, and by maintaining close proximity between interrelated high-frequency sections. In some instances where you might instinctively parallel several unused inputs, you can achieve lower load capacitance by tying the unused inputs to a supply. In another example, when using RC oscillators, it's best to use the smallest capacitor and the largest resistor possible.

Slow input transitions can cause extra dissipation. If an input signal rises slowly, it causes both input transistors to conduct for a longer time, thereby causing more current to flow. One rule of thumb is if rise and fall times are shorter than 25 nsec, minimal current will flow. But don't go overboard. Be aware that slow transitions are more tolerable in slower operating sections because the transitions occur less often. Therefore, weigh the importance of the extra dissipation against the cost of speeding signals up.

It's important to point out that floating inputs can result in unnecessary power dissipation. If inputs are open, the input

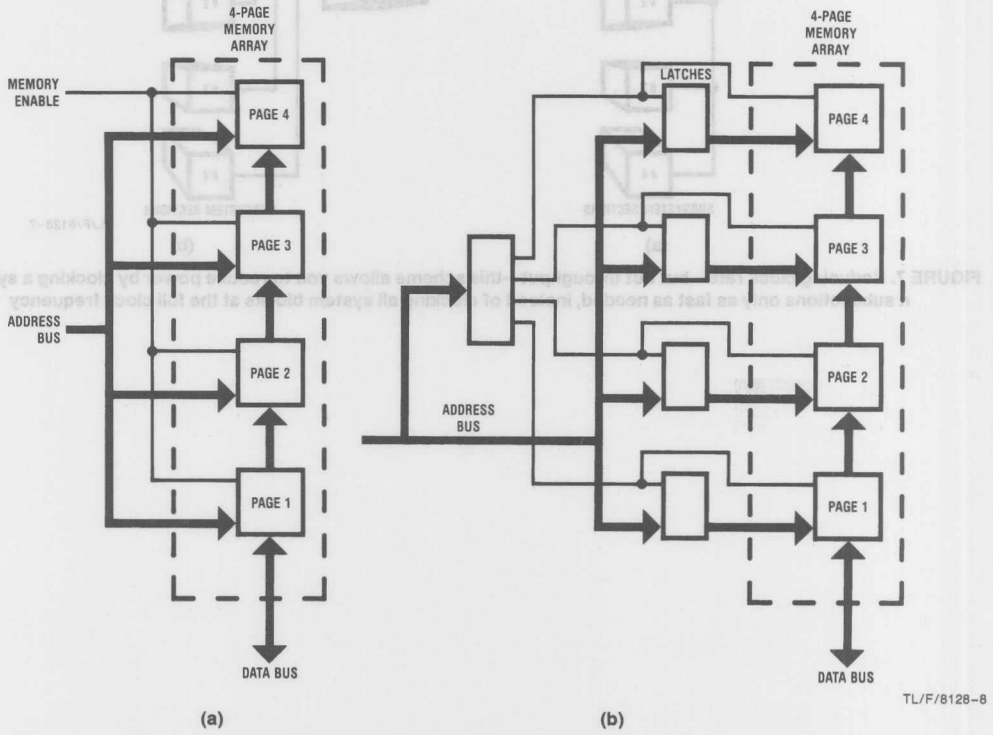


FIGURE 8. Latching memories' addresses (b) can reduce system power. In (a), every memory is driven at the bus frequency. By contrast, in (b)'s configuration, only the memory block being addresed is clocked.

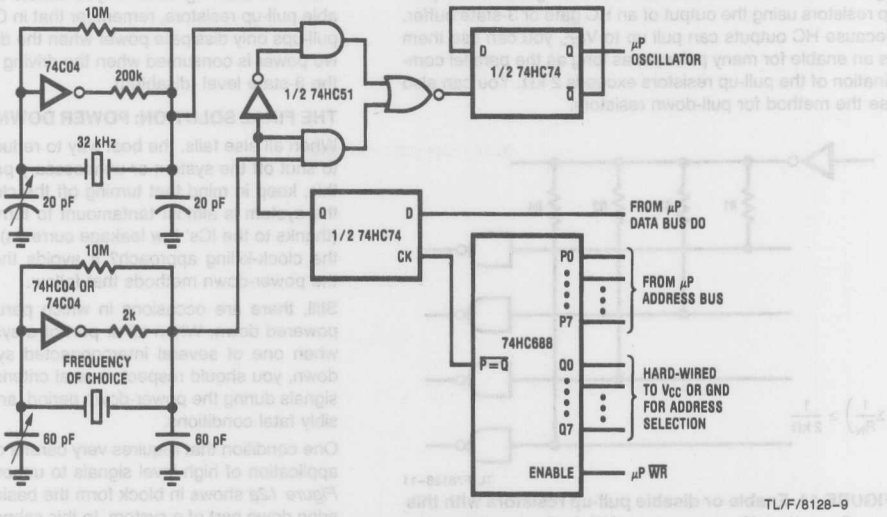


FIGURE 9. Switch your system's clock frequency for reduced power consumption. The circuit shown is a software-selectable oscillator for a microprocessor system.

voltage can float to an indeterminate and intermediate level; thus, don't float CMOS Inputs. This action can turn on both p- and n-channel transistors, resulting in supply-current drain. In bus-oriented systems, don't allow the bus to become completely 3-stated or float for extended periods because this will have the same effect as leaving inputs open.

Bus structures subject to prolonged 3-state conditions should be terminated to ensure that the bus lines pull to either V_{CC} or ground. For short durations, the bus capacitance can maintain valid logic levels, so for short-time floating, pull-up or -down resistors might not be necessary.

Finally, make sure your design ensures solid V_{CC} and ground logic levels at 54HC/74HC inputs. If the logic Low is greater than 0.5V or the logic High is lower than $V_{CC}-0.5V$, then the normally Off p- or n-channel transistor can actually conduct slightly, causing additional I_{CC} to flow (similarly to the previously discussed HCT "soft" levels).

BE WARY OF STATIC LOADS

Previous sections discussed the effects of capacitive loads on system power dissipation. What about resistive loads? In ultra-low-power systems, their contribution can be significant, so it's important to find ways to eliminate or minimize their detrimental effects. The loads could be pull-up resistors, bus terminators, displays, relays or peripheral drivers. Of course, the most obvious way to reduce power is to select low-power relays or displays, for example, and to make resistor values as high as possible. In addition, you can switch these loads out of the circuit when not needed.

Figure 10 shows a circuit that dissipates no static power; you can use it to terminate a 3-state bus to the last active logic level seen on the bus. This technique is useful to ensure the bus doesn't float when 3-stated. The circuit uses a 74HC244 whose input is tied to its output. If the terminating resistors must be completely turned off, use the 3-state Enable.

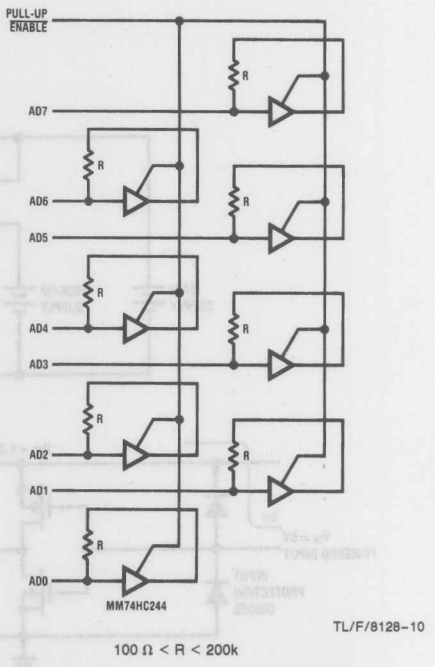


FIGURE 10. Dissipating zero static power, this scheme can serve to terminate a 3-state bus to the last active logic level seen on the bus. To disconnect the terminating resistors, use the 3-state Enable command.

Figure 11 illustrates a method of controlling a series of pull-up resistors using the output of an HC gate or 3-state buffer. Because HC outputs can pull up to V_{CC}, you can use them as an enable for many pull-ups, as long as the parallel combination of the pull-up resistors exceeds 2 kΩ. You can also use the method for pull-down resistors.

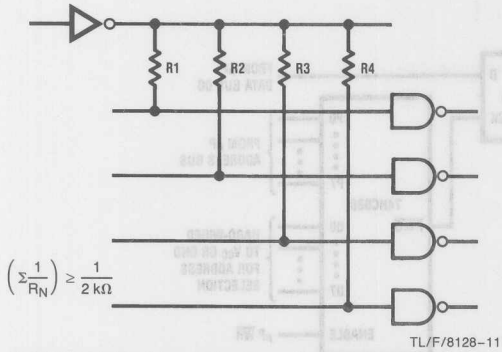


FIGURE 11. Enable or disable pull-up resistors with this configuration. You can use an HC device's outputs to enable several pull-ups. The scheme is also applicable to pull-down resistors.

When considering whether you should add circuitry to disable pull-up resistors, remember that in CMOS systems, the pull-ups only dissipate power when the driving output is low. No power is consumed when the driving output is high or at the 3-state level (disabled).

THE FINAL SOLUTION: POWER DOWN

When all else fails, the best way to reduce system power is to shut off the system or unnecessary parts. Before you do this, keep in mind that turning off the clock to a section of the system is almost tantamount to turning the section off (thanks to the ICs' low leakage currents). The advantage of the clock-killing approach? It avoids the complications of the power-down methods that follow.

Still, there are occasions in which parts of a system are powered down. When all or part of a system is shut off, or when one of several interconnected systems is powered down, you should respect several criteria to avoid spurious signals during the power-down period, and to eliminate possibly fatal conditions.

One condition that requires very careful consideration is the application of high-level signals to unpowered HC devices. *Figure 12a* shows in block form the basic concepts of powering down part of a system. In this scenario, it's possible to apply a logic One to the unpowered CMOS logic. If this happens to either an input *(b)* or a 3-state output *(c),* the device will still be powered.

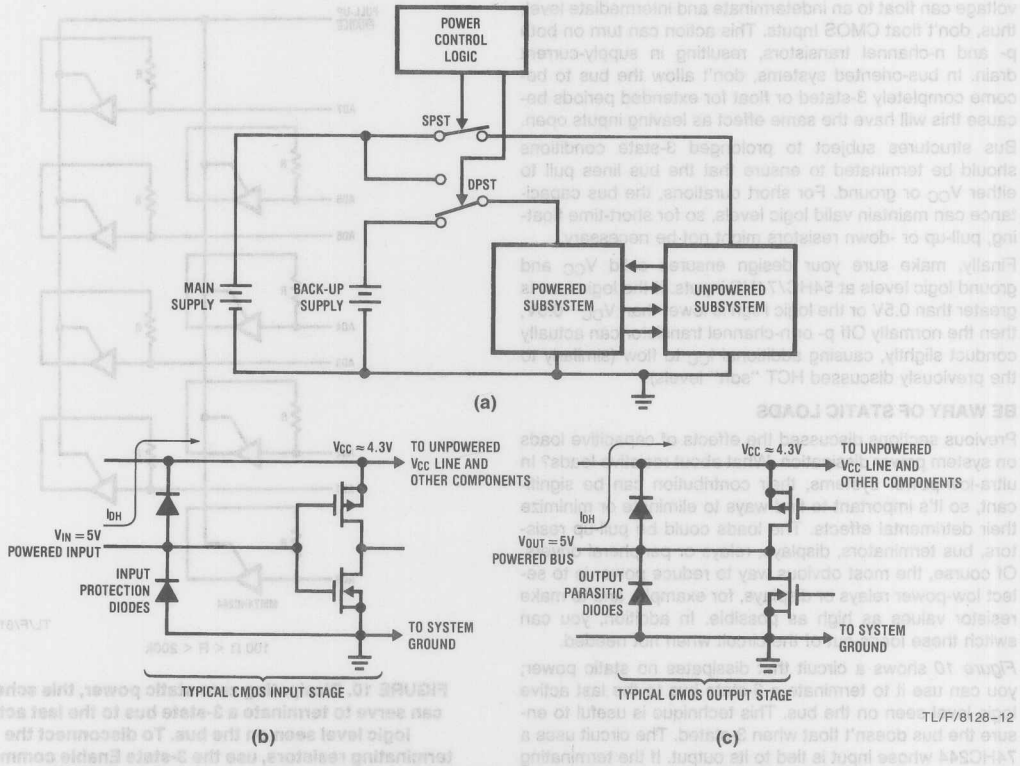


FIGURE 12. This basic power-up and -down system (a) presents dangers to CMOS-logic ICs. As the input (b) and output (c) schematics show, a logic One can actually power up the "unpowered" system, thereby causing damage to input and output diodes.

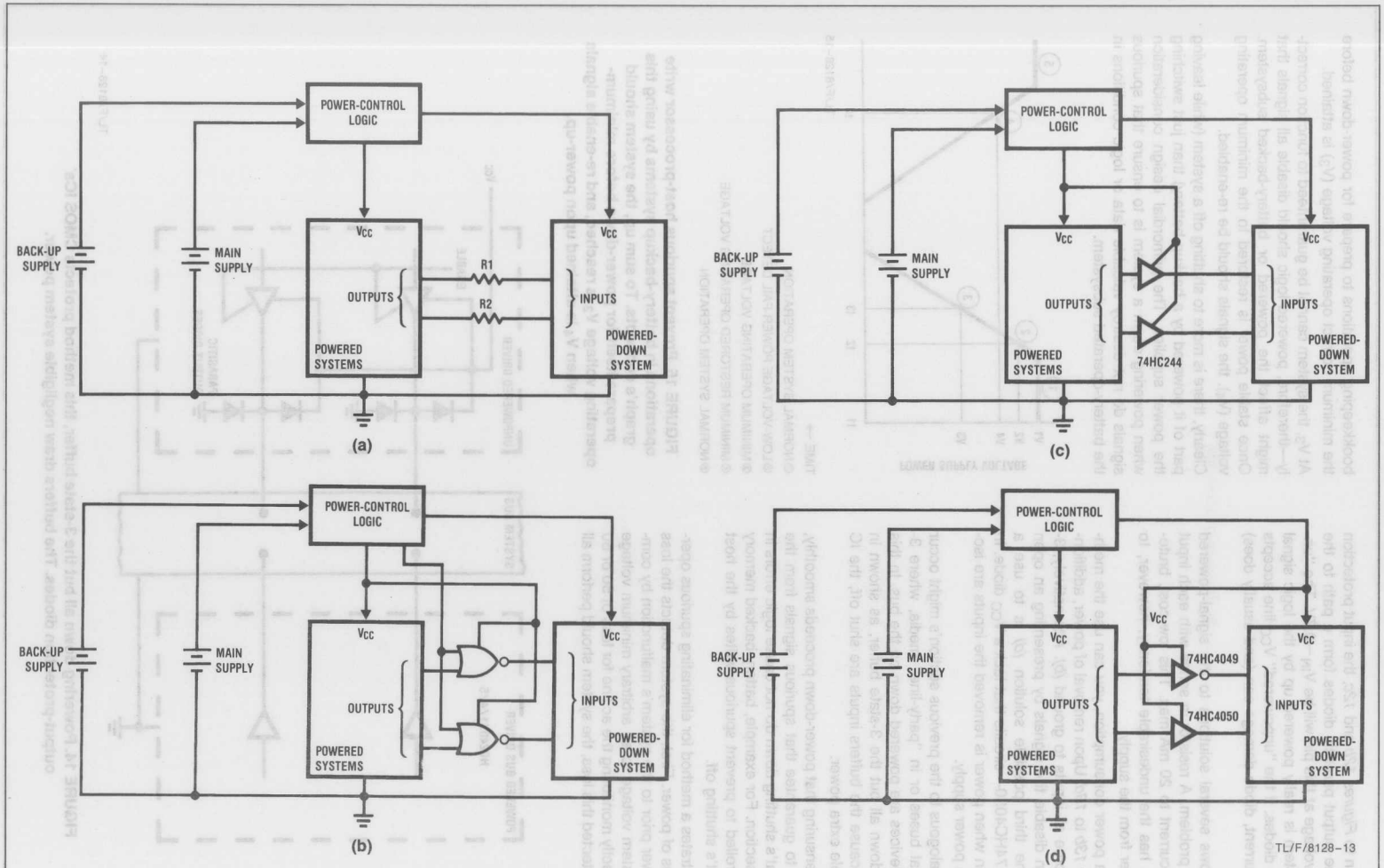


FIGURE 13. Solutions to the problems in *Figure 12*, these configurations protect CMOS circuits' inputs and outputs in power-down situations. The brute-force solution in (a) limits input currents; (b)'s scheme forces inputs to ground; in (c), 3-state gates disable the inputs. In (d), 74HC4049 or -4050 level translators isolate inputs from the power supply.

appreciable current, diode damage can (and usually does) result.

Figure 13 shows several solutions to the signal-powered "unpowered" problem. A resistor in series with each input (*a*) limits the current to 20 mA max. This low-cost, brute-force solution has the undesirable tendency, however, to dissipate power from the supply.

To avoid extra power consumption, you can use the methods in *Figures 13b* to *13d*. Upon removal of power, additional logic can force all inputs to ground *(b)*. Alternatively, 3-state logic can disable the signals by presenting an open circuit *(c)*. The third possible solution *(d)* is to use a 74HC4049 or 74HC4050—circuits that lack a V_{CC} diode. In this case, even when power is removed the inputs are isolated from the power supply.

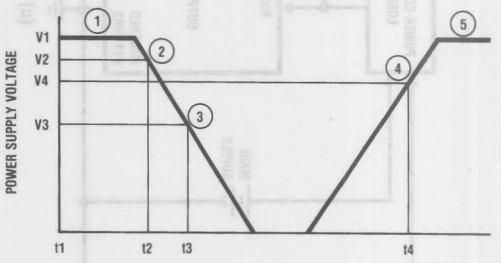
A situation analogous to the previous section's might occur on bidirectional buses or in "party-line" media, where 3-state output devices are powered down on the bus. In this case, power down all but the 3-state buffer, as shown in *Figure 14*. Because the buffers inputs are shut off, the IC draws negligible extra power.

In addition to ensuring that power-down proceeds smoothly, it's important to guarantee that spurious signals from the subsystem that's shutting down do not cause logic errors in the powered section. For example, battery-backed memory must be controlled to prevent spurious writes by the host processor that's shutting off.

Figure 15 illustrates a method for eliminating spurious operation upon loss of power. First, the system detects the loss of system power prior to the system's malfunction by comparing the system voltage to an arbitrary minimum voltage (V_2), or by directly monitoring the ac line for loss of 50 or 60 Hz. Having detected this loss, the system should perform all

Once stable power is restored to the minimum operating voltage (V_4), the signals should be re-enabled.

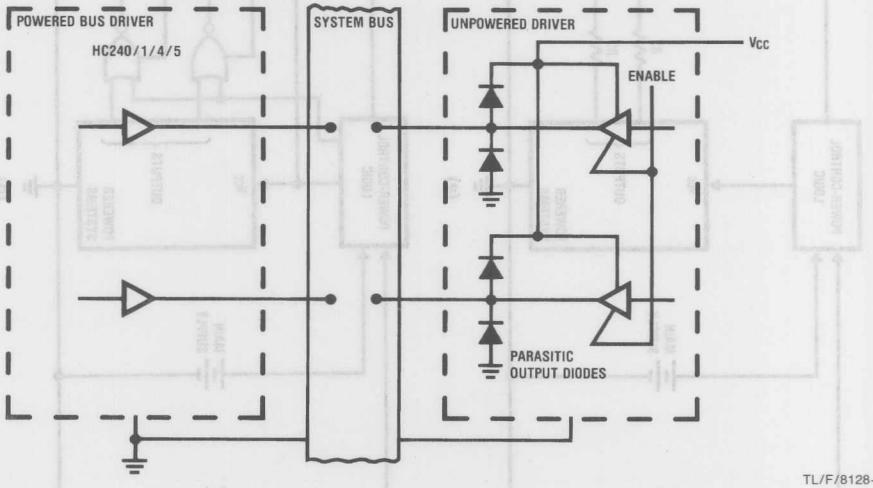
Clearly, there is more to shutting off a system (while leaving part of it powered by a backup battery) than just switching the power supplies. The primordial design consideration when powering down a system is to ensure that spurious signals do not destroy valuable data or logic conditions in the battery-operated subsystem.



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① NORMAL SYSTEM OPERATION
② LOW-VOLTAGE POWER-FAIL DETECT
③ MINIMUM OPERATING VOLTAGE
④ MINIMUM RESTORED OPERATING VOLTAGE
⑤ NORMAL SYSTEM OPERATION

FIGURE 15. Prevent spurious host-processor write operations in battery-backup systems by using this graph's concepts. To sum up, the system should prepare itself for power-down before minimum-operating voltage V_3 is reached, and re-enable signals when V_4 is attained upon power-up.



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FIGURE 14. Powering down all but the 3-state buffer, this method protects CMOS ICs' output-protection diodes. The buffers draw negligible system power.

DC Noise Immunity of CMOS Logic Gates

National Semiconductor
Application Note 377
Vivek Kulkarni

Introduction

The immunity of a CMOS logic gate to noise signals is a function of many variables, such as individual chip differences, fan-in and fan-out, stray inductance and capacitance, supply voltage, location of the noise, shape of the noise signal, and temperature. Moreover, the immunity of a system of gates usually differs from that of any individual gate; thus a generalized analysis of the noise immunity of a logic circuit becomes a very complex process when one takes all the above parameters into consideration.

The complementary structure of the inverter results in a near-ideal input-output characteristic with switching point midway (45%–55%) between the "0" and "1" output logic levels. The result is a high noise immunity (defined as the maximum noise voltage which can appear on the input without switching an inverter from one state to another). National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 45% of the power supply voltage typically will not propagate through the circuit. However, the standard guaranteed value through the industry is 30%.

This note describes the variation of the transfer region (or DC noise immunity) of a multiple-input gate in conjunction with the gate configuration—a consideration important in the system design.

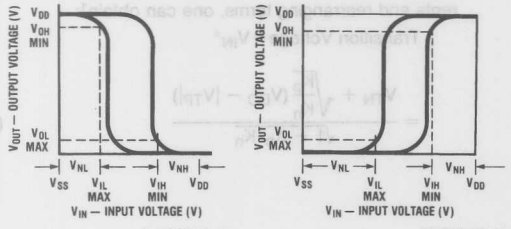


FIGURE 1. Minimum and Maximum Transfer Characteristics for (a) Inverting Logic Function and (b) Noninverting Logic Function

Transfer Characteristics

FIGURE 1 illustrates minimum and maximum transfer characteristics useful for defining noise immunity for an inverter and a non-inverter. Some definitions are as follows:

$V_{IH\ min}$ = the minimum input voltage high-level input for which the output logic level does not change state.

Then:

$V_{NL} = V_{ILmax}$ = "low level" noise immunity

$V_{NH} = V_{DD} - V_{IH}$ = "high level" noise immunity

V_{OHmin} = minimum high level output voltage for rated V_{NL} [for inverting function as in *Figure 1(a)*]

Table 1 shows the UB and B series noise immunity and noise margin ratings determined by the Joint Electron Devices Engineering Council (JEDEC). B series ratings are slightly higher than the UB series because of the buffered nature of these gates.

TABLE I. UB and B Series DC Noise Immunity and Noise Margin ($T_A = 25°C$)

Characteristics	Test Conditions		Input Voltage
	V_O (V)	V_{DD} (V)	(V)
Input Low Voltage V_{IL} max			
B types	0.5/4.5	5	1.5
	1/9	10	3
	1.5/13.5	15	4
UB types	0.5/4.5	5	1
	1/9	10	2
	1.5/13.5	15	2.5
Input High Voltage V_{IH} min			
B types	0.5/4.5	5	3.5
	1/9	10	7
	1.5/13.5	15	11
UB types	0.5/4.5	5	4
	1/9	10	8
	1.5/13.5	15	12.5

Since the MOS transistors are voltage-controlled resistors, the transfer characteristics and consequently the DC noise immunity are determined by the parallel series combination of the transistor impedances in conjunction with the input voltages, the number of inputs, and the gate circuit configuration. This consideration becomes more important for a system designer who has harsh-noise-prone applications.

The value of the standard transistor ON resistance may vary from 10 MΩ down to almost 30Ω (depending on the dimensions of the MOS-FET and applied voltages). For different input conditions, different combinations of the impedances of the N-channel transistors connected in parallel and the P-channel transistors connected in series will come into play for a NOR gate. This is illustrated in *Figure 2*. For a NAND gate, similar considerations hold good and give rise to varying transfer characteristics as shown in *Figure 3*.

Example of CD4001

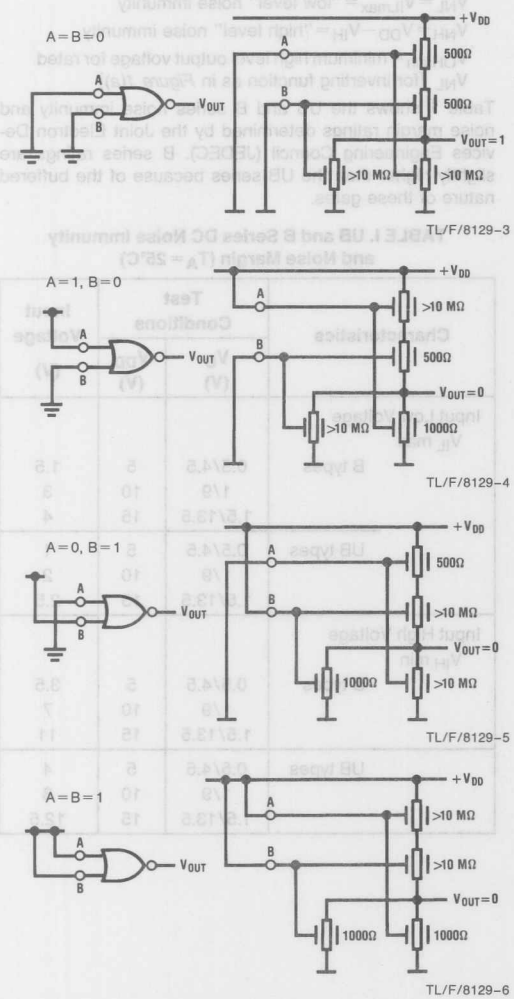


FIGURE 2. Typical Transfer ON/OFF Resistances for Various Input Combinations for CD4001

Analysis

The DC transfer characteristics of the CMOS inverter can be calculated from the simplified DC current-voltage characteristics of the N- and P-channel MOS devices.

In the transfer region, where both transistors are in saturation, the following relationships can be used for an inverter.

N-channel drain current will be:

$$I_{dsn} = \frac{K_n}{2}(V_{IN} - V_{TN})^2 \quad (1)$$

P-channel drain current will be:

$$-I_{dsp} = \frac{K_p}{2}(V_{IN} - V_{DD} - V_{TP})^2 \quad (2)$$

where:

$$K_n = \frac{\mu n\, C_{ox}\, W_n}{L_n},\ K_p = \frac{\mu p\, C_{ox}\, W_p}{L_p}$$

Taking the ratio of (2) and (1):

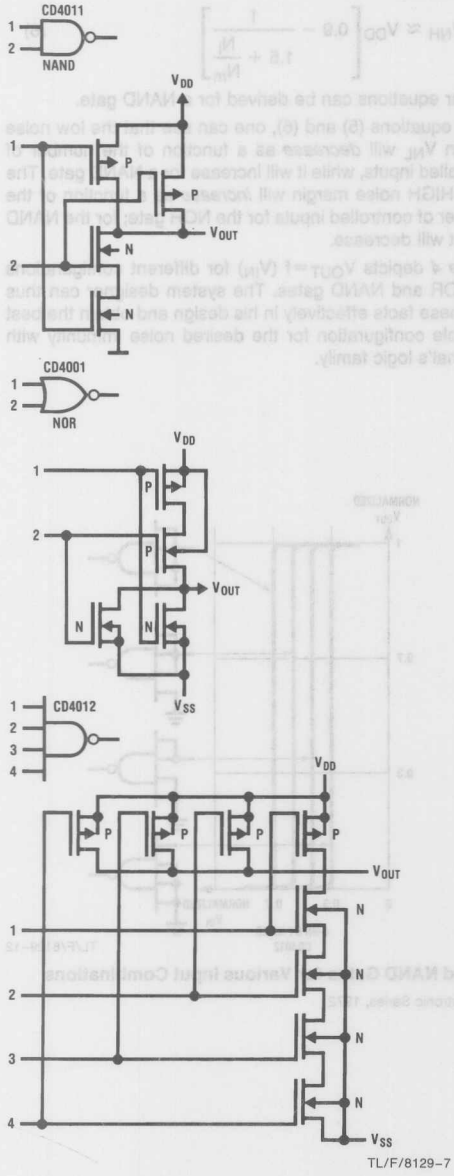
$$\frac{|I_{dsp}|}{I_{dsn}} = \frac{K_p}{K_n} \cdot \frac{(V_{IN} - V_{DD} - V_{TP})^2}{(V_{IN} - V_{TN})^2}$$

$$\frac{K_p}{K_n} = \frac{|Idsp|}{I_{dsn}} \cdot \frac{(V_{IN} - V_{TN})^2}{(V_{IN} - V_{DD} - V_{TP})^2} \quad (3)$$

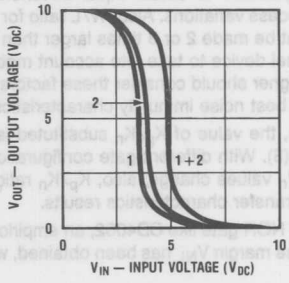
Studies made at National show good correlations between the process monitor pattern and actual device on a wafer for drive currents. Thus the ratio K_p/K_n can be calculated for the actual device if one knows drive currents for the test pattern, widths of N- and P-channel devices and threshold voltages from a given process.

The transition voltage is calculated from basic current equations and from the fact that some current has to flow through P- and N-channel devices. Equating saturation currents and rearranging terms, one can obtain[1]:

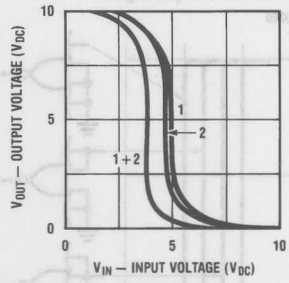
$$\text{Transition Voltage} = V_{IN}^* = \frac{V_{TN} + \sqrt{\frac{K_p}{K_n}}(V_{DD} - |V_{TP}|)}{\sqrt{1 + K_p/K_n}} \quad (4)$$



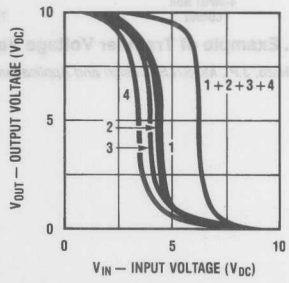
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TL/F/8129–9



TL/F/8129–10

FIGURE 3. Allowed Voltage Transfer Curve Shifts which Result Due to Various Input Combinations of Multiple Input Gates

By selecting $|V_{TP}| = V_{TN}$ and $K_p = K_n$, transition voltage can be designed to fall midway between 0V and V_{DD}—an ideal situation for obtaining excellent noise immunity. However, it is not always possible to obtain equal threshold voltages because of process variations. Also, W/L ratio for a P-channel device must be made 2 or 3 times larger than W/L ratio for an N-channel device to take into account mobility variations. The designer should consider these factors when designing for the best noise immunity characteristics.

In equation (4), the value of K_p/K_n substituted is obtained from equation (3). With different gate configurations, effective W_p and W_n values change; also, K_p/K_n ratio changes and a shift in transfer characteristics results.

For the 4-input NOR gate like CD4002, an empirical relation for the low noise margin V_{NL} has been obtained, which is as follows:

$$V_{NL} \approx V_{DD}\left[\frac{1}{1.5 + \frac{N_i}{N_m}} - 0.1\right] \quad (5)$$

where:

N_i = number of used inputs/gate

N_m = total number of inputs/gate

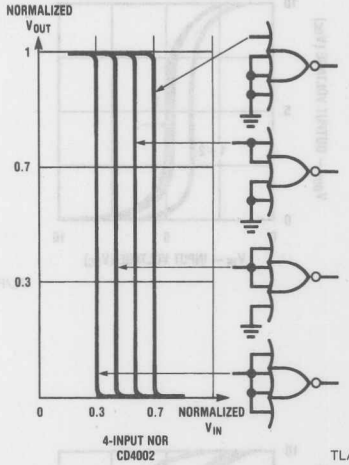
The input voltage high noise margin V_{NH} can be calculated by:

$$V_{NH} \approx V_{DD}\left[0.9 - \frac{1}{1.5 + \frac{N_i}{N_m}}\right] \quad (6)$$

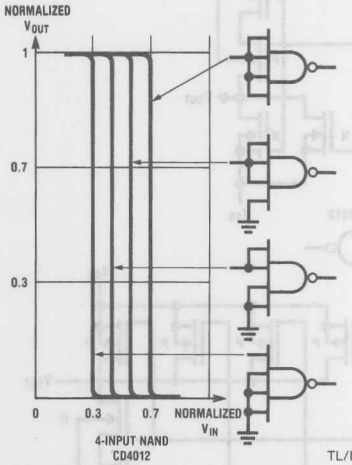
Similar equations can be derived for a NAND gate.

From equations (5) and (6), one can see that the low noise margin V_{NL} will *decrease* as a function of the number of controlled inputs, while it will increase for a NAND gate. The input HIGH noise margin will *increase* as a function of the number of controlled inputs for the NOR gate; for the NAND gate it will decrease.

Figure 4 depicts $V_{OUT} = f(V_{IN})$ for different configurations for NOR and NAND gates. The system designer can thus use these facts effectively in his design and obtain the best possible configuration for the desired noise immunity with National's logic family.



TL/F/8129–11



TL/F/8129–12

FIGURE 4. Example of Transfer Voltage Variation for NOR and NAND Gates for Various Input Combinations

1. Carr, W.N., and Mize, J.P., *MOS/LSI Design and Application*, Texas Instruments Electronic Series, 1972

Follow PC-Board Design Guidelines for Lowest CMOS EMI Radiation

National Semiconductor
Application Note 389
Roger Kozlowski

The application of such high-speed CMOS-logic circuits as the 54HC/74HC family (as compared with CD4000 metal-gate logic) requires special attention to pc-board design to minimize conducted and radiated noise.

The need to reduce a logic system's noise emission is becoming ever more apparent with the increased use of high-speed electronics, and with the progressive tightening of regulations covering the amount of permissible radiated system noise. This article presents empirical and analytical techniques for effective EMI control of 54HC/74HC high-speed CMOS-logic circuitry.

Several sources conduct or radiate EMI from electronic apparatus. Among these are

- antenna loops formed by ICs and their decoupling capacitors
- pc-board traces carrying driving-and driven-chip currents
- common-impedance coupling and crosstalk.

To minimize EMI-related problems, you must reduce all extraneous system noise, reduce the effects of parasitic pc-board trace antennas, and employ effective system shielding. The following sections examine these EMI sources and present techniques of minimizing them for high-speed CMOS logic.

BEWARE COMMON IMPEDANCES

The most obvious precaution to take in any analog or digital design is to minimize the extent of common-impedance paths. *Figure 1* gives a generalized representation of a logic layout in which the earth ground and the signal ground are not common. Methods of reducing EMI focus on the minimization of common-impedance paths, shown here primarily as ground-line impedances Z_1 through Z_4. Signal-line impedances, though not shown here, could also come into play.

These common impedances result in noise emission, arising from the ground-line voltage drops that occur during current switching; you can generally reduce the drops by enlarging the ground conductor in order to reduce its effective impedance. This action has a secondary advantage: The ground trace can form a shield that reduces emission by other circuit traces, particularly in multilayer circuit boards.

Stray coupling capacitances (shown in *Figure 1* as C_1 and C_2) that effectively "bridge" signals from one trace to another constitute a second source of noise. These paths can occur as the result of coupling from one pc-board trace to another or, alternatively, from an IC package to the pc board.

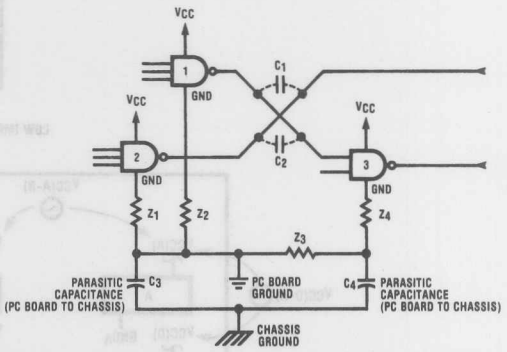
Impedances Z_1 through Z_4 are functions of the thickness of the copper pc-board foil, circuit switching speeds and the effective lengths of the traces. The common-impedance paths provide the coupling by which noise currents are injected, circulated and finally returned to any package on the pc board.

The amount of voltage generated by the noise/switching currents multiplied by the impedances is difficult to predict. However, the higher the impedances, the higher the radiated noise. An easy empirical method that can serve as a general rule is to render the pc board as optically opaque as possible by making ground and supply trace areas as large as possible (*Figure 3*). This measure lowers the trace impedances. As a side benefit, it helps to conserve the etchant bath in the manufacturing process.

MEASURE PC-BOARD NOISE FOR EMI CONTROL

A simple but effective technique for isolating noisy circuit areas is to use a wideband (>100 MHz) oscilloscope with a differential-amplifier front end, as shown in *Figure 2*. You use the scope to "snoop" along the various circuit paths, looking for noisy elements on the pc board.

Noise appears as a small signal voltage across common-impedance paths, as well as along supply traces. *Figure 2* shows the impedance coupling occurs at ground C-B toward ground B-A; ie, noise will likely propagate from package A toward package C.



TL/F/8417–1

FIGURE 1. Common-impedance paths contribute to EMI emissions. They give rise to ground-line voltage drops, as do stray coupling capacitances. The solution? Beef up ground traces; cover the board with them, if possible.

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V_{CC}-supply coupling occurs from package A toward package C. In like manner, coupling occurs from V_{CC} supplies F to C, E to B and D to A. Check all paths to determine the overall noise level of the circuit layout under maximum clocking conditions and data-transfer rates.

This technique helps you look at the overall qualitative noise level of the pc board and helps isolate areas of potential noise upset. It's not, however, a substitute for the use of a qualified EMI facility. Only by rigid testing and measurement under FCC specified conditions can you be assured of EMI-limit certification for electronic equipment.

Typical Switching Characteristics (Assume 5V at 25°C)

Logic Family	Edge Speed V/NSEC	Input Capacitance (pF)	CdV/dt (mA)
74C/CD4000	0.05	5	0.2
74LS	0.38	6	2.3
74HC	0.42	5	2.1
74S	1.0	4	4.0

TRANSITION TIMES AFFECT EMI

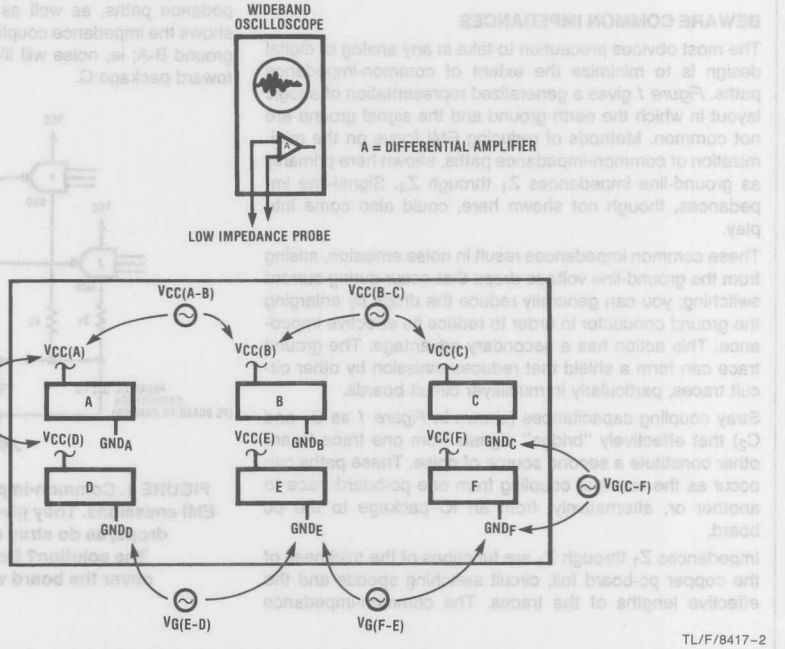
The edge rate of an IC's power-supply spike is primarily a function of its signal rise and fall times and its capacitive load, expressed by C(dV/dt). The edge rate is usually expressed in milliamperes per millisecond. For a fixed signal-line or power-supply-trace inductance, the faster the IC's signal rise and fall times, the greater the potential for radiated noise.

The table shows typical speed values for some popular logic families. C(dV/dt) is a measure of the inherent emission behavior—ie, the higher the switching current, the greater the likelihood of noise-energy emission. You can establish a benchmark of the relative emission by taking the edge rate times the typical input capacitance. As the table shows, HC has a slightly higher edge rate but a slightly lower input capacitance than LS TTL, resulting in a C(dV/dt) figure similar to the latter's.

This conclusion, however, does not take into account other internal spike currents not associated with output loading. These actually increase HC noise slightly. However, HC still achieves approximately the same inherent-noise level as LS TTL, and about 10 times that of CD4000. Don't fall into the trap of believing that because CD4000 and 74C logic use CMOS technology and have low EMI characteristics, HC CMOS logic has low EMI as well.

As seen, the C(dV/dt) figure for the signal lines of 54HC/74HC is about the same as that of LS TTL. Its relative noise is thus about the same. Note that the inherent V_{CC} noise generated by high-speed CMOS is somewhat higher than LS TTL's. This is due to the impedance mismatch of the power supply to the IC's supply lines, and to the slightly greater internal spiking in 54HC/74HC circuits. In spite of this higher noise potential, however, proper layout and supply decoupling yield CMOS EMI characteristics similar to those of LS TTL.

An effective method for reducing EMI is to decouple the power supply by adding bypass capacitors between V_{CC} and ground. This technique is, of course, closely related to general power-supply decoupling, the goal of which is to maintain correct logic levels. The design of effective decoupling and bypass schemes centers on maximizing the charge stored in circuit bypass loops while minimizing the inductances in these loops.



TL/F/8417–2

FIGURE 2. This simple setup for evaluating board noise allows you to isolate problem areas qualitatively. The high-speed oscilloscope's differential-amplifier input detects voltage drops along ground and supply lines.

The high decoupling charge levels ensure adequate short-term supply current during supply spiking that's provoked by logic-element switching. Low shunt inductances guarantee minimum voltage drops arising from transients with fast edge rates.

What are the basic requirements for decoupling a power supply? First, you must match the power supply's impedance to that of the individual components. Any power supply presents a low source impedance to other circuitry, whether it be individual components on the same board, or other boards in a multiboard system. These components or boards can comprise logic, memory, microprocessors, analog functions or combinations thereof. You must match the supply's impedance to the components' in order to lessen the potential for voltage drops caused by IC edge rates, ground- or signal-level shifting, noise-induced currents or voltage reflections.

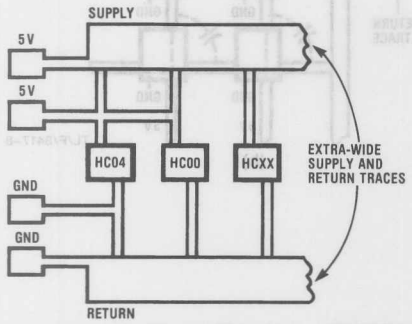
To minimize this mismatch, it's important to use a suitable high-frequency capacitor for bulk decoupling of major circuitry sections, or for entire pc boards in multiboard systems. This capacitor is typically placed at the supply's entry point to the board. It should be an aluminum- or tantalum-electrolytic type having both low equivalent series resistance (ESR) and low equivalent series inductance (ESL). ESR values should range from 1.2 to 4Ω, ESL impedance from 2 to 3Ω (at the system's operating frequency). This capacitor's value is typically 10 to 47 μF. You might additionally need a 0.1 μF high frequency ceramic capacitor if supply noise continues to be a problem.

There exists a second class of decoupling that requires careful examination—that of the ICs themselves. *Figure 4* gives a typical IC's decoupling-circuit model; it shows the parasitic inductances resulting from various lead and trace inductances. The total voltage caused by the switching currents at the IC's pins is the voltage stored in the capacitor, V_{CC}, minus the drops across the capacitor's ESR and series inductances:

$$V_{IC} = V_{CC} - (I)(ESR) + \frac{dI}{dt}(ESL) + L_L + L_{PC} + L_{IC}.$$

Because a capacitor's ESR is typically much smaller than its high-frequency reactance, you can consider the (I)(ESR) term to be negligible. Rearranging the equation and grouping all inductances together yields

$$V_{IC} = V_{CC} - \frac{dI}{dt}(ESL) + L_{TOTAL}.$$



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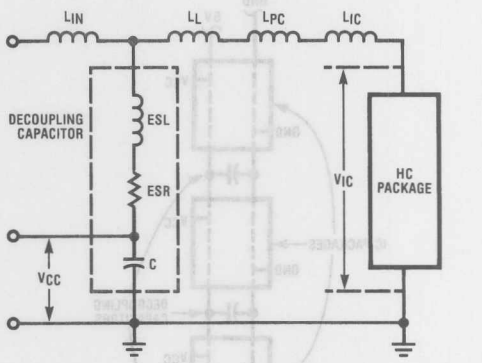
FIGURE 3. Extra-wide supply and return traces help reduce EMI emissions. Make your boards as "optically opaque" as possible.

Using this second equation, you can calculate a circuit's maximum allowable decoupling inductance, given the IC's edge rate and the maximum allowable transient voltage drop. This calculation is applicable to general logic-level noise computations as well. For example, for a 500 mV max drop at V_{CC} = 5V and dI/dt = mA/ms, the total inductance must not exceed 100 nH. You can then use this calculation to determine the maximum distance between the IC and the bypass capacitor if you know the trace inductance per centimeter.

The foregoing considerations apply to the reduction of noise for suppressing EMI. However, minimizing noise will also help retain maximum logic-level noise immunity. Most popular bipolar-logic families require 0.01- to 0.1 μF RF-grade capacitor placement roughly every two to five packages, depending on the exact application. For high-speed CMOS logic, a good rule of thumb is to place these bypasses every three to five ICs, depending on supply-voltage, operating-speed and EMI requirements. In some cases, moreover, it might be helpful to add 1 μF tantalums at major supply-trace branches, particularly on large pc boards.

In addition to reducing the effects of pc-board trace inductance by bypassing, you should observe careful layout procedures to minimize these inductances. You must therefore maintain the close proximity of ICs and decoupling capacitors. In a specific "how-not-to" example, *Figure 5a* shows a poor power-rail layout that even the best decoupling capacitor can not clean up; (*b*) shows the circuit's equivalent series inductances.

In this horror-show scenario, the layout of power-supply and return traces is poor. They're too widely separated, resulting in a large parasitic-antenna loop area, and hence large inductances and much emitted energy. These inductances can result in a significant voltage drop (that the 54HC/74HC logic might tolerate), and they can result in excessive noise generation.



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Notes:

L_{IN} = Total Input Inductance
L_L = Total Capacitor-Lead Inductance
L_{PC} = Total PC-Board-Trace Inductance
L_{IC} = Total IC-Lead Inductance

FIGURE 4. Decoupling is no simple matter, as borne out by this equivalent circuit. The bypass capacitor's ESR and ESL and the supply line's series inductance all play a detrimental role.

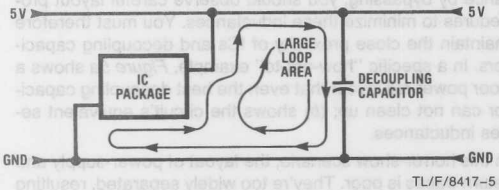
which in turn reduces the line-voltage drop. Part (*b*) shows an alternate orthogonal placement; this geometry results in a similar loop-area reduction (hence EMI reduction), but it needs a greater amount of layout area.

CONTROLLING IMPEDANCES

Along with power-supply decoupling, you must consider effective line lengths and terminations in order to reduce noise emission caused by line reflections and mismatch-induced ringing. Because of the fast edge rates discussed earlier, signal-line lengths and transmission-line effects become important factors. When the signal's transit time is at which these considerations become important, use the following equation:

$$L < 10\frac{t_R}{N},$$

where L = interconnect-trace length in centimeters; t_R = logic rise time in nanoseconds; and N is the number of driven logic inputs. Thus, for a 54HC/74HC logic device driving six other devices, the allowable trace length is 10(6 ns)/6 = 10 cm. This figure represents the maximum allowed trace length to avoid waveform distortion. Implicit in the trace-length calculation is the minimization of pulse reflections, ringing and harmonic generation, which can add to EMI.



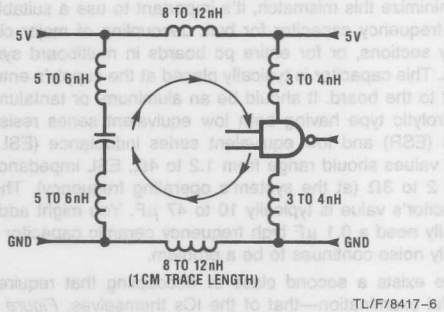
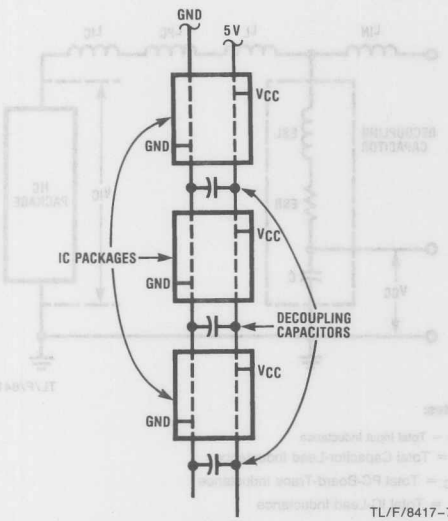


FIGURE 5. This "how-not-to" hookup (a) shows the wrong way to decouple an IC. The layout produces a large loop-antenna area for emitted noise. The equivalent circuit for this configuration is shown in (b).



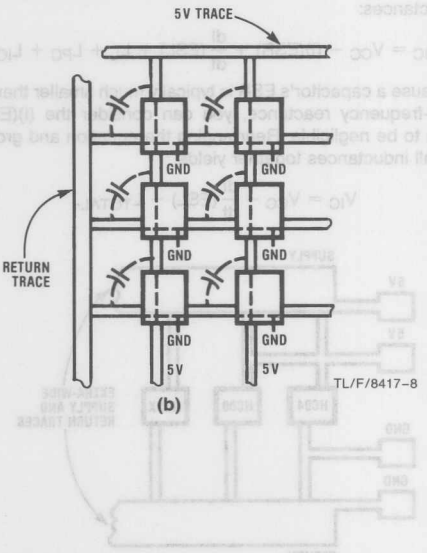


FIGURE 6. These recommended supply and return layouts help reduce EMI. The reason? They minimize loop area and characteristic impedance, thanks to the proximity of the supply and return lines. The orthogonal arrangement in (b) requires more area than (a)'s lateral layout, but it produces similarly effective results.

PLACEMENT IS IMPORTANT

Printed-circuit boards using 54HC/74HC could contain sections of high-speed circuitry combined with sections of low-speed circuitry. *Figure 7* shows the recommended placement of these sections for both single-board (***a***) and multi-board (***b***) systems. In the former situation, it's preferable to group all the high-speed circuitry close together. Grouping the system by speed reduces the overall trace lengths in the high-frequency section, which is critical to reducing the overall EMI.

This line-length reduction cuts line reflections, cross-talk, common-impedance coupling and ringing. Note that the higher speed sections are grouped near the power supply as well. The reason? Switching power supplies can be large sources of radiation; external shielding of both the supply and the high-speed circuitry is therefore advisable.

Relative circuit speeds play the important role here. Consequently, the example doesn't give typical values for low, medium or high frequencies. One possible criterion would be to examine the corner frequency or bandwidth of each IC. Also, you must give consideration to IC-interconnection paths. Grouping logic by speed tends to minimize interconnection lengths in general. Depending on the design, however, this point might not be entirely true in some cases.

Figure 7b shows the grouping of ICs on a pc board used in a multiboard system. In this case, the high-speed circuitry is grouped near the bus connector. The reason for this is that the bus connector usually carries very-high-speed signals; grouping high-frequency circuitry near it minimizes circuit trace lengths. As shown, the lower speed sections are placed further from the edge connector.

SHIELD THE SYSTEM

Even though good layout and pc-board design techniques can greatly reduce EMI, in some cases they're not enough; you must shield the internal circuitry to reduce emissions further. The exact design requirements for effective shielding are beyond the scope of this article. However, the topic deserves brief mention. Typically, shielding is accomplished by enclosing the high-speed circuitry in a metal enclosure that has a good earth- and system-ground connection. Ideally, the enclosure completely seals the internal circuitry.

In practice, however, the system enclosure will have "holes" appearing at the places where the system interfaces to the real world. For example, a display, keyboard or disk drive might require enclosure cutouts to allow cables to enter the system's box. Moreover, vents and fans might be required for cooling.

It's important in critical situations to minimize these holes. In this respect, 54HC/74HC has an advantage over other logic families. Thanks to its lower power consumption, you can in many cases eliminate vents and fans, and thus seal the enclosure more effectively.

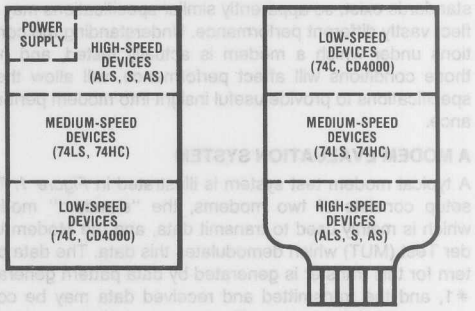


FIGURE 7. Grouping ICs by frequency can help. In (a)'s single-board layout, the high-speed circuitry is placed closest to the power supply. In (b)'s miltiboard system, the high-speed units are the closest to the board connector.

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2. Matisoff, B. S., "Good shielding techniques control EMI and RFI," *EDN*, February 18, 1981, pgs. 123–128.

3. Rappaport, A., "Special Report: Capacitors," *EDN*, October 13, 1982, pgs. 105–122.

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Understanding 300 Baud Modem Specifications

National Semiconductor
Application Note 392
Peter Single

Understanding the specifications commonly used for 300 Baud modems presents a major hurdle for first time modem buyers. Not only are some specifications subtle, but few standards exist, so apparently similar specifications may reflect vastly different performance. Understanding the conditions under which a modem is actually tested, and how those conditions will affect performance, will allow these specifications to provide useful insight into modem performance.

A MODEM EVALUATION SYSTEM

A typical modem test system is illustrated in *Figure 1*. The setup consists of two modems, the "standard" modem which is mainly used to transmit data, and the Modem Under Test (MUT) which demodulates this data. The data pattern for this transfer is generated by data pattern generator #1, and the transmitted and received data may be compared in the data analyzer. The storage oscilloscope may be used to compare transmitted and received data for distortion which is too small to cause errors detectable by the data analyzer.

A phone line simulator and noise generator may be inserted into the signal path to simulate a noisy phone line, so the MUT may be analyzed under operating conditions closely resembling actual conditions.

The data pattern generator #2 is used to exercise the MUT so it is operating under full duplex conditions. As the MUT's modulator and demodulator may interact, it is necessary that the MUT's modulator be fully exercised during modem evaluation.

It is possible to buy equipment which is capable of performing all the functions of data generation, data comparison and data quality analysis (the task of the storage oscilloscope) in one unit. Such equipment is made by several major manufacturers and greatly simplifies modem evaluation. This discussion will not combine these tasks into one unit as this allows greater insight into the parameters being measured and their relevance to the overall system.

It is common to use a modem which is identical to the MUT as the "standard" modem. This allows the total distortion, in both the modulator and demodulator to be evaluated in one measurement. As there is no accepted industry standard "ideal" modem, it is difficult to find a better alternative for the "standard" modem.

TELEPHONE LINE SIMULATORS

Modem performance will vary depending on the phone line through which it transmits. An "ideal phone line" consisting of a resistive "T" network will give generally better performance than a typical phone line, or a very bad phone line, due to the amplitude, phase, harmonic and echo distortion produced by phone lines. Telephone line simulators allow reasonable representation of actual conditions and are controllable in an engineering environment.

There are two types of phone line simulators commonly available. One class of phone line simulators only simulate the amplitude and phase characteristics of a phone line. Although these simulators are designed to operate in a 600Ω system, their input impedance is not representative of a typical phone line. (See paper by Gresh (7) in reading list at end of this article). Some modems have a dynamic range which is sensitive to the impedance "seen" looking into the phone line. (This occurs because a mismatch between the modem and the phone line causes modulation sidebands of the modulator to be reflected back into the demodulator and thus degrade the received signal to noise ratio). Thus these simulators are not particularly suitable for modeling the modem to phone line interface. This type of simulator is available as a sealed unit with input and output terminals. They are available with "typical", "worst case" and other characteristics. An advantage of this type of simulator is that they are simple to use and specify. Some normalized frequency response plots of these simulators are shown in *Figure 2*.

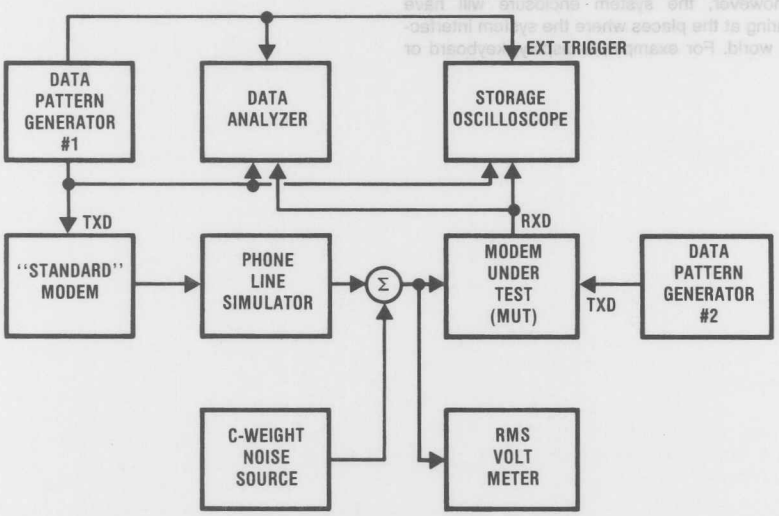


FIGURE 1. Modem Evaluation Block Diagram

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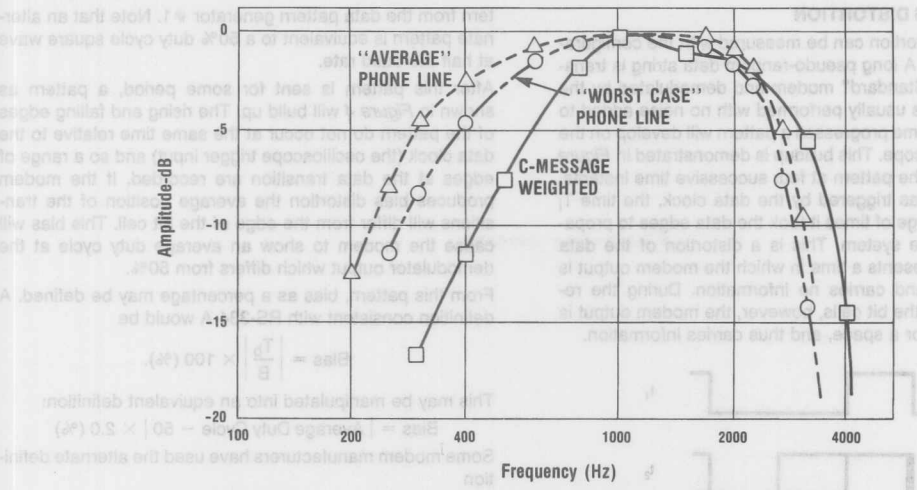


FIGURE 2. Response of Noise Weighting Filter and Phone Lines

A second class of simulators is capable of simulating a wide range of phone lines. These simulate amplitude, phase and input impedance characteristics. They consist of many units each representing a section of phone line wire. These can be interconnected at will to simulate a wide variety of phone line lengths, gauges, and configurations, including tapped and loaded lines. Although this type of simulator is flexible, no modem testing standards exist describing how it should be connected for writing specifications.

Neither of these simulators allow much flexibility in controlling attenuation through the line, or for adding noise to the line. Thus the final line simulator used will generally consist of a commercially available unit with some added hardware to allow controlled noise mixing and signal attenuation.

THE NOISE GENERATOR

The noise generator is used to simulate noise on the phone line which might adversely affect modem performance. Noise generators must be accurately specified before their effect on a given circuit can be evaluated meaningfully.

The spectral properties of noise have considerable influence on its effect on modem performance. Only noise with frequency components close to the tones used by modems will interfere with their operation. Noise with spectral components far from the modem tones will contribute to the noise power in the system and will thus affect a noise measurement, but it will not affect modem performance. It is thus necessary to use noise with well defined frequency characteristics in order to achieve a meaningful noise measurement.

A common choice of noise bandwidth is called "C-Message Weighted". The C-Weighted frequency response is shown in *Figure 2*. This response was chosen to allow comparison of noise power in relation to its effect on the perceived noise of a phone line, i.e., it is a combination of the effect of a telephone earpiece and the human ear. It is thus not entirely appropriate to modem characterization. A disadvantage of the C-Weighted response is the complexity of the filter required to generate it. In spite of these disadvantages the C-Weighted response has become almost the de facto standard of modem testing.

It is important that the noise mixer be on the MUT side of the phone line simulator. If this is not done the phone line simulator will modify the bandwidth of the noise reaching the MUT. The main effect of this is to reduce the amplitude of the noise at the skirts of the C-Weight bandwidth. This causes the noise to be concentrated around the received signal tones, and thus causes an apparent degradation of performance. This performance degradation is often erroneously attributed to the gain and phase distortion produced by the phone line simulator. This is discussed further in the discussion of bit error rate testing later in this article.

THE E.I.A. RS-334-A SPECIFICATION

The RS-334-A specification "Signal Quality at Interface Between Data Terminal Equipment and Synchronous Data Circuit-Terminating Equipment for Serial Data Transmission" published by the Electronic Industries Association (E.I.A.) gives valuable information on the measurement and specification of data distortion.

Unfortunately, many manufacturers do not specify their modems in a manner consistent with E.I.A. RS-334-A. This document discusses "isochronous distortion" of data, which is a measure of the total distortion of a serial data pattern.

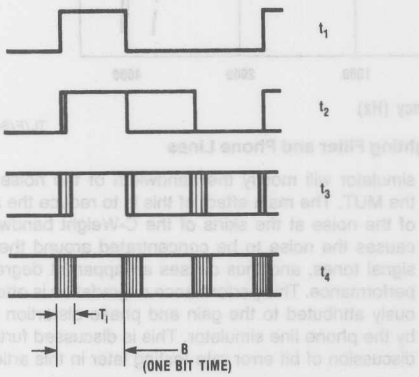
Many modem manufacturers, however, prefer to discuss the data distortion in terms of "bias" and "jitter", which are more intuitive terms than isochronous distortion. Isochronous distortion can be found by summing the effects of bias distortion and jitter, so it is possible to calculate RS-334-A compatible specifications from this data.

E.I.A. make a very important point regarding all bias, jitter and bit error rate measurements and specifications:

"The result of the measurement should be completed by an indication of the period, usually limited, of the observation. For a prolonged modulation (or restitution) it will be appropriate to consider the probability that an assigned value of the degree of distortion will be exceeded."

This is a consequence of measurements made in the presence of random signals, and is typical of most modem parameters. Modems are designed to operate in conditions which are better described by probabilities (e.g. the probability that the input impedance of a phone line will fall inside certain limits, or that the signal to noise ratio at the modem will have a certain value). Thus it is important when writing modem specifications to carefully describe, and be able to interpret, test conditions.

mitted by the "Standard" modem and demodulated by the MUT. This test is usually performed with no noise added to the system. As time progresses a pattern will develop on the storage oscilloscope. This buildup is demonstrated in *Figure 3* which shows the pattern at four successive time instants. As the scope was triggered by the data clock, the time T_j represents a range of times it took the data edges to propagate through the system. This is a distortion of the data edges as it represents a time in which the modem output is indeterminate, and carries no information. During the remaining time of the bit cells, however, the modem output is fixed at a mark or a space, and thus carries information.



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FIGURE 3. Isochronous Distortion Pattern Buildup

From this pattern the isochronous distortion is defined to be

$$D = \frac{T_j}{B} \times 100\%$$

where B is the bit time, and T_j is the total spread of data transitions.

BIT BIAS

"Bit bias" refers to the propensity of a modem demodulator to favor a mark or a space. It is most commonly measured using the setup of *Figure 1* with an alternate (1010...) pattern. After this pattern is sent for some period, a pattern as shown in *Figure 4* will build up. The rising and falling edges of the pattern do not occur at the same time relative to the data clock (the oscilloscope trigger input) and so a range of edges at the data transition are recorded. If the modem produces bias distortion the average position of the transitions will differ from the edge of the bit cell. This bias will cause the modem to show an average duty cycle at the demodulator output which differs from 50%.

From this pattern, bias as a percentage may be defined. A definition consistent with RS-334-A would be

$$\text{Bias} = \left| \frac{T_b}{B} \right| \times 100\ (\%).$$

This may be manipulated into an equivalent definition:

$$\text{Bias} = |\ \text{Average Duty Cycle} - 50\ | \times 2.0\ (\%)$$

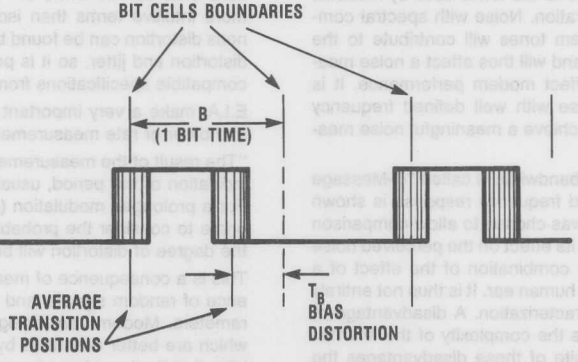
Some modem manufacturers have used the alternate definition

$$\text{Bias} = \left| \frac{T_b}{2 \times B} \right| \times 100\ (\%).$$

There does not appear to be any apparent reason for the variation of specifications used. One possible justification for dividing by two bit times is that the distortion T_b of *Figure 4* could be considered as distortion to both the mark and the following space. Thus the distortion should be divided between the two data bits. When reviewing modem specifications it is important to know which bias definition is being used.

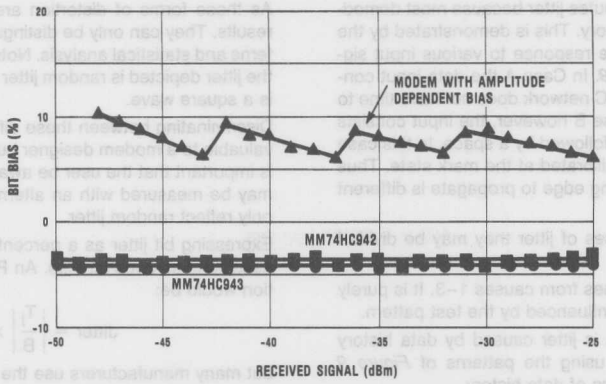
The MM74HC942 and MM74HC943 300 baud modems use the second definition so as to be consistent with other manufacturers of modem components.

Bit bias is amplitude dependant for some modem designs. This makes it difficult to decide under what conditions bias should be specified. *Figures 5* and *6* show the bias for the MM74HC942, the MM74HC943 and another modem plotted against signal strength. Note that for the other modem the bias is signal strength dependant, whereas for the MM74HC942 and MM74HC943 it is not. This demonstrates the necessity for specifying the conditions under which bias is measured, and the extent to which it is design dependent.



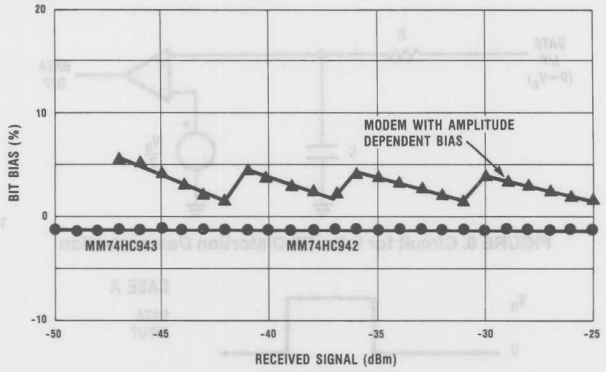
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FIGURE 4. Modem Output Pattern for Bias Measurement



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FIGURE 5. Bit Bias vs Received Signal (Originate Mode)

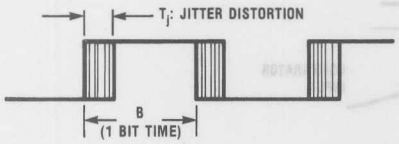


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FIGURE 6. Bit Bias vs Received Signal (Answer Mode)

BIT JITTER

Bit Jitter refers to variation of propagation delay through the data path. The term "jitter" comes from apparent movement of the data edges observed on an oscilloscope. *Figure 7* shows the pattern which will build up on the storage oscilloscope of *Figure 1* if an alternate pattern is being generated by data generator #1. The rising and falling edges of the pattern do not occur at the same time relative to the data clock, producing the variation T_j of these edges. This variation is bit jitter.



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FIGURE 7. Modem Output Pattern Showing Jitter

There are several distinct mechanisms contributing to bit jitter;

1) Intermodulation between data and carrier. 300 baud modems are asynchronous. This means the data can change at any time during a carrier cycle. The ability of a demodulator to detect this data change can vary depending on the time of the data change relative to the carrier. Thus the demodulator response varies, and jitter is produced.
2) Noise. This may come from internal circuitry, or from the phone line. When jitter is evaluated it is usually done with external noise sources squelched, so the modem, rather than the test circuit, may be evaluated.
3) Time quantization (this refers to the finite switching speed of sampled data systems). As the data is not sychronized to the modem clock, the modem may not recognize a data change for an entire clock cycle. This will cause a variation of response.

4) Data history. This contributes jitter because most demodulator circuits have memory. This is demonstrated by the circuit of *Figure 8* whose response to various input signals is shown in *Figure 9*. In Case A the data input consists of one mark. The RC network does not have time to reach equilibrium. In Case B however, the input consists of a sequence of marks followed by a space. In this case the RC network has equilibrated at the mark state. Thus the time it takes the falling edge to propagate is different in the two cases.

In summarizing these causes of jitter they may be divided into two groups.

A) Random Jitter. This comes from causes 1–3. It is purely random and cannot be influenced by the test pattern.

B) Inter Bit Distortion. This is jitter caused by data history and can be measured using the patterns of *Figure 9* which represent extremes of data history.

As these forms of distortion are very similar in their final results. They can only be distinguished using long data patterns and statistical analysis. Note that, referring to *Figure 7*, the jitter depicted is random jitter only since the data pattern is a square wave.

Discriminating between these different jitter mechanisms is valuable to a modem designer but not to a user. However, it is important that the user be aware that a jitter specification may be measured with an alternate pattern, and thus may only reflect random jitter.

Expressing bit jitter as a percentage suffers from alternate definitions as does bit bias. An RS-334-A consistent definition would be:

$$\text{Jitter} = \left|\frac{T_j}{B}\right| \times 100\%$$

but many manufacturers use the definition:

$$\text{Jitter} = \left|\frac{T_j}{2 \times B}\right| \times 100\%.$$

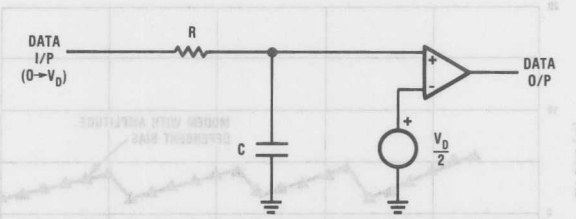


FIGURE 8. Circuit for Inter-Bit Distortion Demonstration

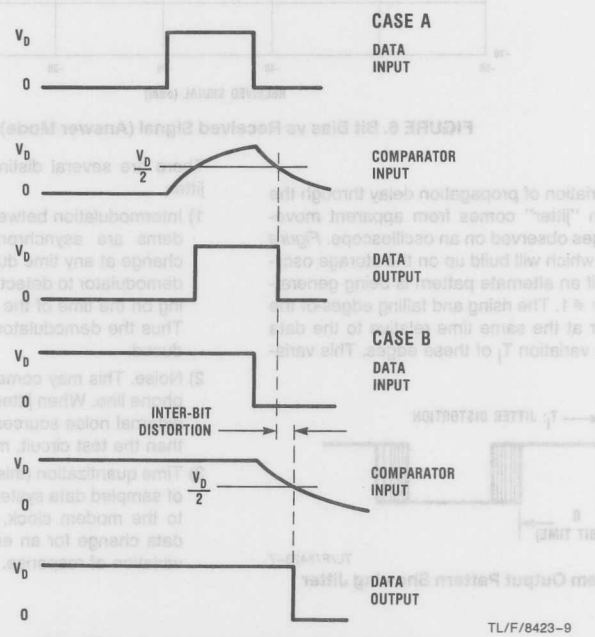


FIGURE 9. Waveforms for Inter-Bit Distortion

Again, the reasons for the differences are not clear but could follow similar lines to those for bias.

For this reason jitter may be specified with less ambiguity by specifying the peak to peak jitter in micro-seconds. Alternately, if jitter is to be expressed as a percentage, the definition should be provided.

Bit jitter, like bit bias, is phone line dependent. For single chip modems it is often measured with an ideal (resistive) phone line as this can be easily performed on currently available integrated circuit test equipment. This will generally give "best case" results.

Some measurements of bit jitter are illustrated in *Figures 10* and *11*. Note the mode and signal strength dependence of the measurements. This data was taken on the MM74HC942 and MM74HC943 monolithic 300 Baud modems using an ideal (resistive) phone line and in full duplex mode, transmitting at −12 dBm.

ISOCHRONOUS DISTORTION, BIAS AND JITTER

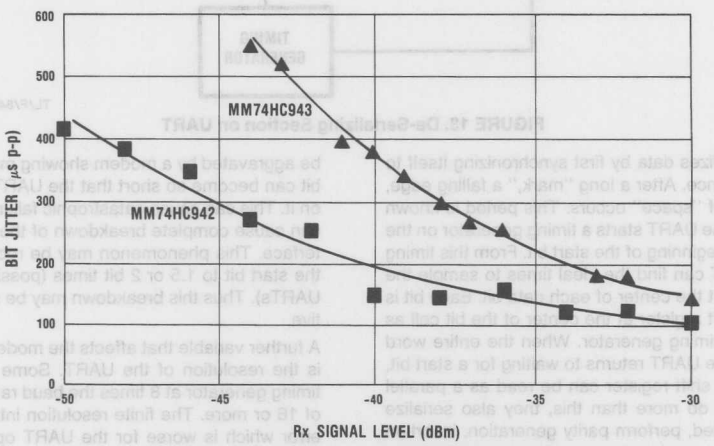
For the modem user, isochronous distortion is probably the most meaningful specification of data distortion. However, some modem manufacturers only provide information on bias and jitter. Thus a conversion from these terms to isochronous distortion would be useful.

Isochronous distortion, being a measure of total distortion, is approximately the sum of bias, random jitter and inter-bit distortion. Before these numbers can be added, it must be assured they have been measured and defined in the manner consistent with specification RS-334-A.

BIAS, JITTER AND UART PERFORMANCE

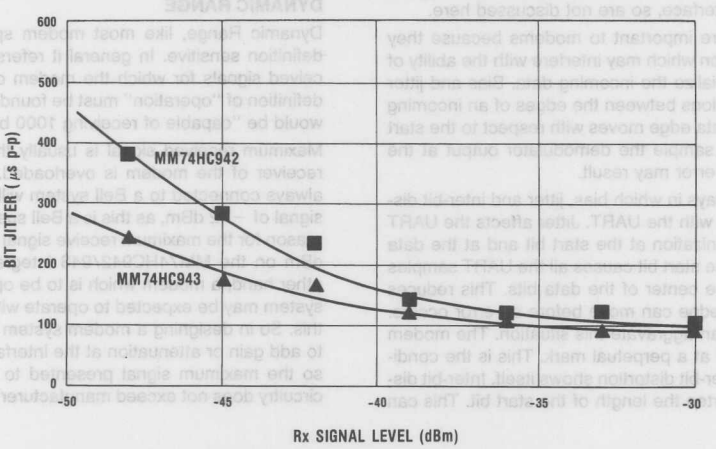
Data distortion is only important insofar as it affects the interface between a modem and the computers which are communicating through it. Generally a computer interfaces to a modem through a UART (Universal Asynchronous Receiver Transmitter). This UART takes byte wide data from the computer and serializes them so they are suitable for transmitting through the modem. The UART at the receiving modem takes this serial data and converts it back into parallel form. Referring to *Figure 1,* UART operation is performed internally by the data generator and analyzer.

Before the effect of data distortion on a UART can be estimated the technique by which a UART performs serial to parallel data conversion must be understood. This is illustrated in *Figures 12* and *13*.



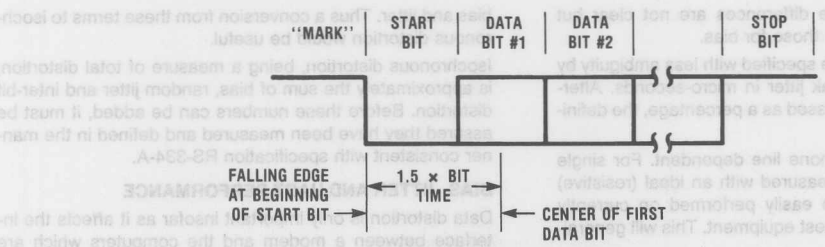
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FIGURE 10. Jitter vs RX Signal (Originate Mode)



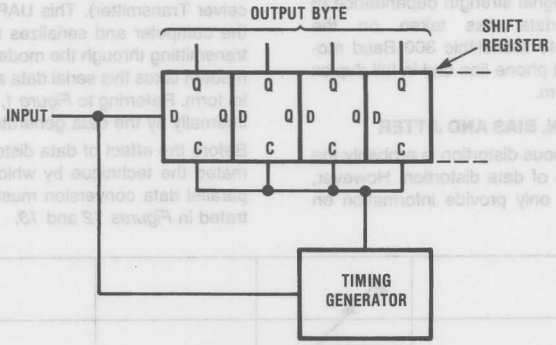
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FIGURE 11. Jitter vs RX Signal (Answer Mode)



TL/F/8423–12

FIGURE 12. Serial Data Input to UART



TL/F/8423–13

FIGURE 13. De-Serializing Section on UART

The UART de-serializes data by first synchronizing itself to the incoming sequence. After a long "mark," a falling edge, and then a period of "space" occurs. This period is known as the "start bit". The UART starts a timing generator on the falling edge at the beginning of the start bit. From this timing generator the UART can find the ideal times to sample the incoming data, i.e. at the center of each data bit. Each bit is strobed into the shift register at the center of the bit cell as determined by the timing generator. When the entire word has been shifted, the UART returns to waiting for a start bit, and the data in the shift register can be read as a parallel word. Most UARTs do more than this, they also serialize data to be transmitted, perform parity generation, insertion and validation, I/O control and many other functions. However these extra functions do not provide insight into the modem to UART interface, so are not discussed here.

Bit bias and jitter are important to modems because they are forms of distortion which may interfere with the ability of the UART to de-serialize the incoming data. Bias and jitter alter the timing relations between the edges of an incoming word. If an output data edge moves with respect to the start bit, the UART may sample the demodulator output at the wrong time, and an error may result.

There are several ways in which bias, jitter and inter-bit distortion can interfere with the UART. Jitter affects the UART at both the synchronization at the start bit and at the data sampling. Jitter at the start bit causes all the UART samples to be offset from the center of the data bits. This reduces the amount a data edge can move before an error occurs. Inter-bit distortion can aggravate this situation. The modem in its "wait" state is at a perpetual mark. This is the condition under which inter-bit distortion shows itself. Inter-bit distortion will thus shorten the length of the start bit. This can be aggravated by a modem showing marking bias. The start bit can become so short that the UART fails to synchronize on it. This can cause catastrophic failure of the system, as it can cause complete breakdown of the modem to UART interface. This phenomenon may be reduced by lengthening the start bit to 1.5 or 2 bit times (possible options on many UARTs). Thus this breakdown may be start bit length sensitive.

A further variable that affects the modem to UART interface is the resolution of the UART. Some UARTs operate the timing generator at 8 times the baud rate, some use a factor of 16 or more. The finite resolution introduces quantization error which is worse for the UART operating at the lower factor.

DYNAMIC RANGE

Dynamic Range, like most modem specifications, is very definition sensitive. In general it refers to the range of received signals for which the modem operates. However a definition of "operation" must be found. A suitable definition would be "capable of receiving 1000 bits without an error".

Maximum received signal is usually the limit at which the receiver of the modem is overloaded. A modem which is always connected to a Bell system will receive a maximum signal of −12 dBm, as this is a Bell specification. This is the reason for the maximum receive signal specification of −12 dBm on the MM74HC942/943 integrated circuits. On the other hand, a modem which is to be operated in a non-Bell system may be expected to operate with larger signals than this. So in designing a modem system it may be necessary to add gain or attenuation at the interface to the phone line so the maximum signal presented to the modem internal circuitry does not exceed manufacturer's recommendations.

It is difficult to measure the maximum signal at which a modem will operate. The mechanism of overload in a modem is highly design sensitive, and results from a complex interaction between the hybrid, the phone line, and the modem's receive filter. This analysis is well beyond the scope of this application note. Many modems will, on the bench, exceed their specification. It is still unwise to operate a modem at a level exceeding the manufacturer's specification, as these designs may fail to operate under some conditions.

Minimum received signal is usually the signal at which the modem begins to make errors in the absence of noise. This may be measured using the circuit of *Figure 1*. The signal is progressively attenuated until the data analyzer begins to record errors. This breakdown of performance is often abrupt; the modem may make no errors at one signal strength, and make only errors when the signal is reduced a further 1 dB.

A modem's dynamic range is often sensitive to the operating mode. Many modems operate to a lower signal level if their transmitter is squelched, or if the transmitter is sending no data but is running, than if the transmitter is sending data. The MM74HC942/943 work to approximately −46 dBm in full duplex mode, and often work to −53 dBm in half duplex operation. The parts are specified to −40 dBm in full duplex conditions and −48 dBm in half duplex conditions.

As noise can cause a modem to make errors when there is good signal strength, dynamic range measurements are always made in the absence of noise. Dynamic range can occasionally be phone line sensitive so conditions should again be specified.

MODEM FILTER SPECIFICATIONS

Some modem manufacturers provide data on their receive filter designs. This data is of more interest to modem designers than modem users.

The "receive filter gain error" refers to the flatness of the receive filter characteristic. It is generally measured between the "mark" and "space" frequencies. As modems transmit data as the frequency of the tone, amplitude errors generally have little effect on performance. The only place this specification may be observed to have effect is in carrier detect circuits. As these circuits follow the receive filter, a filter gain error will cause the trip points to shift depending on the tone transmitted.

The receive filter group delay distortion refers to the group delay difference between the mark and space frequencies. Group delay refers to the time energy takes to pass through a filter. Thus group delay error causes the "mark" energy and the "space" energy to take different times to propagate through the receive filter. As is illustrated in *Figure 14* this causes data to become scrambled, as the period at the data change either has neither mark nor space energy, or has both.

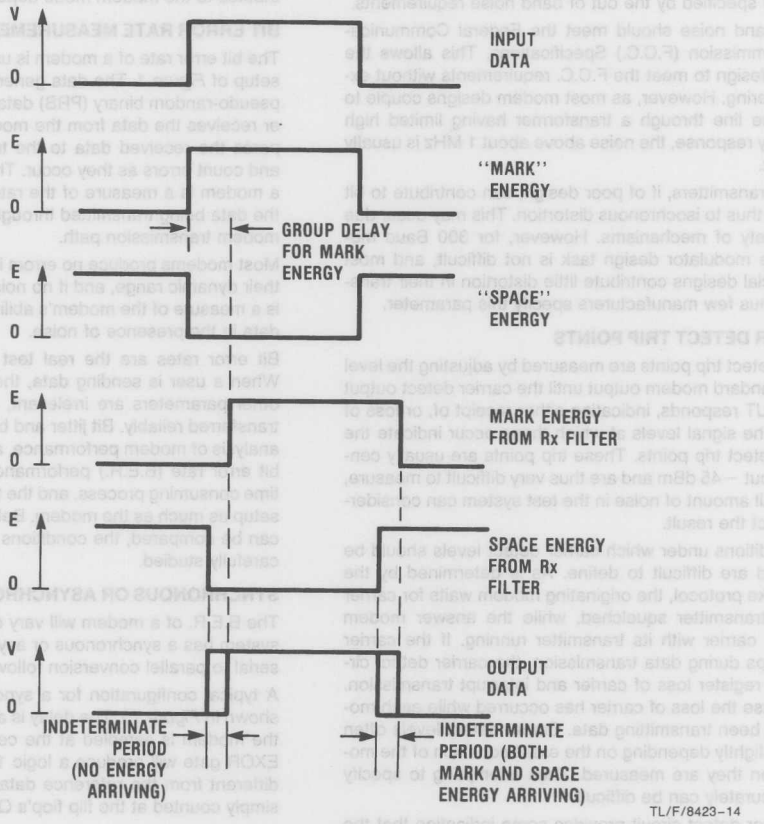


FIGURE 14. Affect of Group Delay on FSK Signals

The main effect of group delay distortion is an increase in bit jitter. This in turn will show up in bit error rate measurements. Group delay distortion does not have as strong an effect on performance as other aspects of modem design, and for this reason is often of little interest, particularly if bit error rates and bit jitter specifications are available.

Note that group delay of the entire system consists of the sum of the group delay of the transmitter, phone line and receive filter. As the group delay of the phone line varies from one line to another there is a lower limit to this distortion which can be achieved. Many modems which do not have the receive filter output available do not specify this parameter.

TRANSMITTER SPECIFICATIONS

Transmitter specifications are usually fairly simple to interpret, but there are some small traps for the unwary.

The second harmonic of the transmitter is more important for some tones than for others. The second harmonic of the originate mode space tone (1070 Hz) falls in the middle of the band in which the originate modem is receiving. This is thus the most important tone for a second harmonic specification. The originate mode mark tone (1270) has a second harmonic outside the band in which the modem is receiving, but it is near enough to this band to have a small effect. The second harmonics of the answer band transmitted tones are both above 4 kHz, and thus only constitute "out of band noise". Many modems thus have their answer band second harmonic specified by the out of band noise requirements.

Out of band noise should meet the Federal Communications Commission (F.C.C.) Specifications. This allows the modem design to meet the F.C.C. requirements without external filtering. However, as most modem designs couple to the phone line through a transformer having limited high frequency response, the noise above about 1 MHz is usually irrelevant.

Modem transmitters, if of poor design, can contribute to bit jitter and thus to isochronous distortion. This may occur due to a variety of mechanisms. However, for 300 Baud modems the modulator design task is not difficult, and most commercial designs contribute little distortion in their transmitter. Thus few manufacturers specify this parameter.

CARRIER DETECT TRIP POINTS

Carrier detect trip points are measured by adjusting the level of the standard modem output until the carrier detect output of the MUT responds, indicating either receipt of, or loss of carrier. The signal levels at which these occur indicate the carrier detect trip points. These trip points are usually centered about −45 dBm and are thus very difficult to measure, as a small amount of noise in the test system can considerably effect the result.

The conditions under which carrier detect levels should be measured are difficult to define. As is determined by the handshake protocol, the originating modem waits for carrier with its transmitter squelched, while the answer modem waits for carrier with its transmitter running. If the carrier level drops during data transmission, the carrier detect circuit may register loss of carrier and interrupt transmission. In this case the loss of carrier has occurred while each modem has been transmitting data. Carrier detect levels often change slightly depending on the exact condition of the modem when they are measured. Thus attempting to specify them accurately can be difficult.

The carrier detect circuit provides some indication that the signal strength is acceptable for modem operation so trip points should be reasonably predictable. The presence of carrier is not, however, a complete assurance that there is another modem on the line (the circuit may trip on noise or speech), or that data present is of acceptable quality (modem performance is often a stronger function of S.N.R. than of signal level, and the carrier detect circuit measures signal level, not S.N.R.).

Some modems, e.g. "dumb" stand alone modems, have only the carrier detect circuit to provide information on the quality of the data being received. For these modems the carrier detect trip point should indicate loss of carrier at the lower limit of the modem's dynamic range. Note that this dynamic range will depend on the operating conditions of the modem, so an adjustable carrier detect trip point is an advantage, allowing the user to optimize the carrier detect trip point for the application.

Some "smart" modems can use more sophisticated data validation techniques than simply measuring the carrier level. For example if the modem has a UART, and the UART has a parity error flag, the modem can directly assess the bit error rate of the line, and judge the line depending on the data quality.

It is thus difficult to assess what constitutes "acceptable" carrier detect operation, as this depends strongly on the modem application.

A non-flat receive filter can cause the carrier detect trip point to be mode and tone dependent. This variation contributes to the modem mode dependence discussed above.

BIT ERROR RATE MEASUREMENTS

The bit error rate of a modem is usually measured using the setup of *Figure 1*. The data generator #1 generates a long pseudo-random binary (PRB) data stream. The data analyzer receives the data from the modem under test, and compares the received data to the transmitted data to detect and count errors as they occur. The bit error rate (B.E.R.) of a modem is a measure of the rate at which errors occur in the data being transmitted through the modem/phone line/modem transmission path.

Most modems produce no errors if they are operating within their dynamic range, and if no noise is present. Thus B.E.R. is a measure of the modem's ability to correctly demodulate data in the presence of noise.

Bit error rates are the real test of modem performance. When a user is sending data, the bit bias, bit jitter and all other parameters are irrelevant, as long as data is being transferred reliably. Bit jitter and bit bias are useful for quick analysis of modem performance, and they somewhat reflect bit error rate (B.E.R.) performance. Measuring B.E.R. is a time consuming process, and the final results reflect the test setup as much as the modem. Before B.E.R. measurements can be compared, the conditions of measurement must be carefully studied.

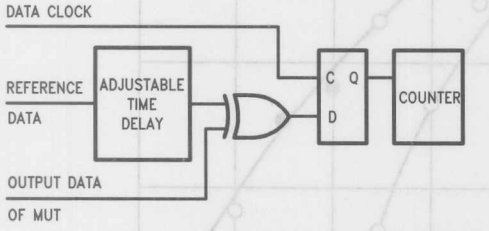
SYNCHRONOUS OR ASYNCHRONOUS OPERATION

The B.E.R. of a modem will vary depending on whether the system has a synchronous or asynchronous system for the serial to parallel conversion following demodulation.

A typical configuration for a synchronous data analyzer is shown in *Figure 15*. The delay is adjusted and the data from the modem is sampled at the center of each bit cell. The EXOR gate will produce a logic 1 if the modem's output is different from the reference data. The errors may then be simply counted at the flip flop's Q output. Note that in most

modem systems using a UART, the data clock is not available.

Systems using a UART must synchronize the data rate clock from the falling edge at the beginning of the start bit, and thus distortion of this edge will adversely affect the ability of the UART to accurately de-serialize the data. Performance is thus not as good as the case of synchronous operation. Thus measuring a modem with synchronous data will not give meaningful data on how the modem will operate with a UART (asynchronous data). As most 300 Baud modems operate with a UART, this test configuration (i.e. asynchronous operation) is the most meaningful way to evaluate them.



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FIGURE 15. Synchronous Data Analyzer

When testing with a UART the word length, parity, start and stop bit length need to be defined. These have less effect on modem performance than noise measurement or deserialization technique.

BIT ERROR RATE AND BLOCK ERROR RATE

Modem specifications vary as to the method of specifying bit errors. If the modem is operating with a UART a noise burst may cause the UART to synchronize incorrectly, causing an entire byte or frame to be received incorrectly. Conversely, multiple bit errors within a byte of data usually only invalidate that single byte. This may be of little significance to the user as many communication protocols require retransmission of the entire block if an error is detected. Some manufacturers thus specify their modems in terms of block error rate rather than bit error rate. This is rare, however.

FURTHER VARIABLES IN MODEM EVALUATION

As is implied by dynamic range specifications, signal amplitude can affect modem performance. This can result from several phenomena. A modem's receive filter has limited dynamic range, with its lower limit set by the filter's noise floor. Thus reducing the signal will affect the S.N.R. at the demodulator, although the S.N.R. at the phone line may remain unaltered. Signal amplitude may also affect modem performance as the hard limiter or A.G.C. (Automatic Gain Control) circuits in the receive path generally have limited dynamic range.

In summary, many variations of configuration can affect modem performance measurements. Unless test conditions are accurately specified the results are virtually meaningless.

Bit error rate measurements were made on the MM74HC943 monolithic 300 Baud modem. The conditions under which they were made is summarized in Table I. These conditions accurately reflect the conditions under which the modem is designed to operate, and are all relevant to the test results.

TABLE I

BIT ERROR RATE MEASUREMENT CONDITIONS

Parameter	Condition
Noise Bandwidth:	C-Weighted
Data Format:	Asynchronous 8 Bit words Even Parity One Start Bit
Data Pattern	511 Bit pseudo-random
Phone Line Simulation	Resistive line
Counted Errors:	All data bits
UART Clock Rate	16 * Data Rate
Standard Modem (transmitter)	Identical to M.U.T.
MUT Transmitter	Transmitting 300 Baud PRB Data
MUT Transmitter Amplitude	Set for "permissive" characteristics

DISCUSSION OF BIT ERROR RATE CURVES

The results of these bit error rate measurements are shown in *Figure 16.* From these curves the signal to noise ratio for a bit error rate of 1.0E-5 can be interpolated. (This is a common value to specify.) It is 3.5 dB in answer mode and 5 dB in originate mode. Note the degree to which the measured points diverge from the curves. This is due to the statistical nature of the test and due to the difficulty of measuring noise using a digital volt meter.

Several different line simulators were tried and bit error rate measurements made for a fixed signal to noise of 3.4 dB. They were 4.7E-5 for a resistive line, 4.3E-5 for an average line, and 4.87E-5 for a worst case line. These measurements differ by less than the accuracy of the test system, indicating the minimal effect of the phone line on the overall system.

SOME MANUFACTURERS OF MODEM TEST EQUIPMENT

(This list is by no means comprehensive.)

Phoenix Microsystems, Inc.
8290 Whitesburg Drive South
P.O. Box 4206
Huntsville, AL 35802

Comstron Corporation
200 East Sunrise Highway
Freeport
N.Y. 11520

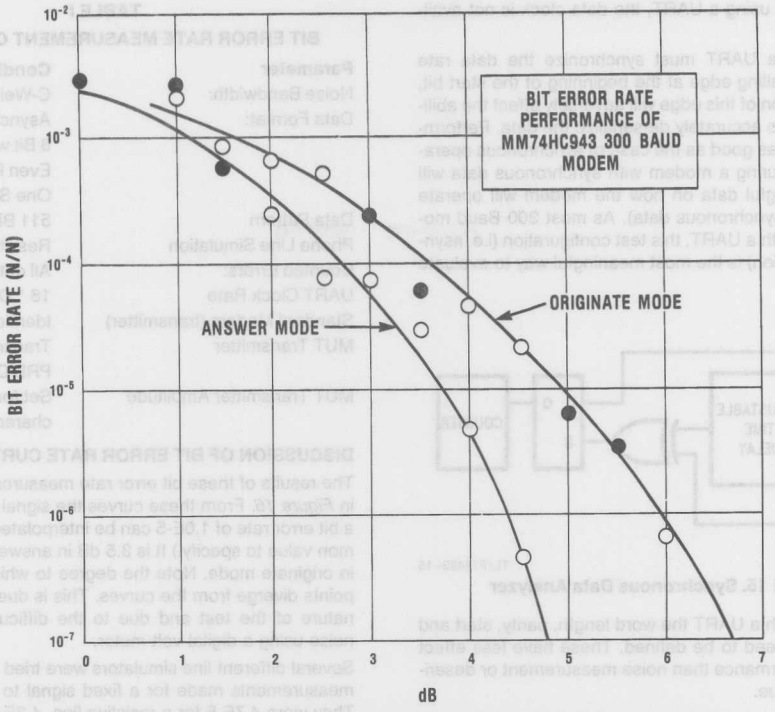
Hewlett Packard Corporation
1820 Embarcadero Rd
Palo Alto
CA 94303

FURTHER READING

(1) Data Sheets for MM74HC942 and MM74HC943 Monolithic 300 Baud Modems, National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051.

(2) "Transmission Parameters Affecting Voiceband Data Transmission—Measuring Techniques" Bell System Data Communications Technical Reference, May '75.

(3) "Data Communications Using Voiceband Private Line Channels" Bell System Technical Reference, Pub 41004, Oct., 73.



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FIGURE 16. Bit Error Rate Performance of MM74HC943 300 Baud Modem

(4) "Data Communications Using the Switched Telecommunications Network" Bell System Data Communications Technical Reference, May '71.

(5) "Use and Evaluation of VA300 (Bell 103A Type) Data Sets" Application Note No. 1, The Vadic Corporation, 916 Commercial, Palo Alto, CA.

(6) "CMOS 300 Baud Modem" *Chan, Single, Deschene*, National Semiconductor Application Note #349 (Reprinted from Midcon/82).

(7) "Physical and Transmission Characteristics of Customer Loop Plant" *P.A. Gresh* Bell Syst Tech J., Dec. '69.

(8) "Signal Quality at Interface Between Data Terminal Equipment and Synchronous Data Circuit-Terminating Equipment for Serial Data Transmission" E.I.A. Standard RS-334-A, Engineering Department, Electronic Industries Association, Aug. '81.

(9) "Data Transmission" *Bennet, Davey* McGraw Hill, 1965.

(10) "Comparison Report of MM74HC942, MM74HC943 versus TMS99532" National Semiconductor Corp, Sept. 1983.

(11) "MM74HC942 and MM74HC943 Design Guide" *Single, Munich* National Semiconductor Application Note 347, Sept. '83.

Transmission-Line Effects Influence High-Speed CMOS

National Semiconductor
Application Note 393
Larry Wakeman



Unlike low-power, metal-gate CMOS, high-speed 54HC/74HC devices readily drive long cable runs and backplanes. While the family maintains CMOS's traditional noise immunity, you must watch transmission-line effects in such applications.

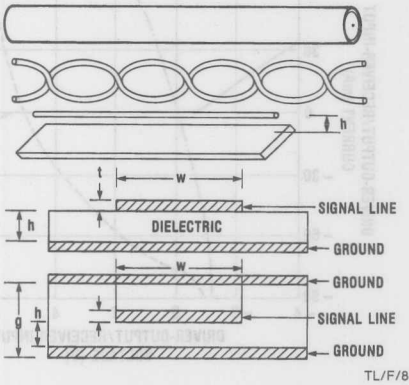
Because of 54HC/74HC high-speed CMOS's short propagation delays and fast rise and fall times, you must understand its transmission-line behavior when driving lines as short as even a foot or two, whether those lines are coaxial cables, twisted pairs or backplanes. Moreover, the devices' fast edge rates increase the likelihood of crosstalk among interconnecting cables.

Despite the need, however, to take design precautions that minimize adverse effects related to high-speed operation, 54HC/74HC logic—unlike slower metal-gate CMOS—includes many features that suit it to driving transmission lines. For example, its symmetrical push-pull outputs result in stiff logic levels, and its high output drive allows fast bit rates.

Another advantage of high-speed-CMOS designs is that they don't prove to be as difficult as those based on other high-speed logic families. In general, high-speed CMOS doesn't require the detailed attention to pc-board layout and transmission-line characteristics that Schottky TTL or ECL designs do. Furthermore, controlling unwanted reflections is easier in the CMOS designs, because 54HC/74HC devices' electrostatic-protection diodes tend to clamp the reflected voltages to the power-supply levels.

MISMATCHES CREATE REFLECTIONS

Transmission-line effects come into play when signal-line lengths are so long that the signal delay down the line and back becomes longer than the waveform's rise or fall time. Mismatches between the line's characteristic impedance and either the driver's output or the receiver's input impedance create signal-line reflections. These in turn cause overshoot and undershoot, which can reduce noise margins and cause excessive delay. *Figure 1* shows various transmission media and their impedances.



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COAXIAL CABLE	Z_o = 50, 75, 125Ω
TWISTED PAIR	Z_o = 50 TO 100Ω
WIRE OVER GROUND	$Z_o = \frac{60}{\sqrt{\epsilon_R}} \ln\left(\frac{4h}{d}\right)$ TYPICALLY Z_o = 120 TO 200Ω
MICROSTRIPLINE	$Z_o = \frac{87}{\sqrt{\epsilon_R + 1.41}} \ln\left(\frac{5.98}{0.8w + t}\right)$ TYPICALLY Z_o = 50 TO 100Ω
STRIPLINE	$Z_o = \frac{60}{\sqrt{\epsilon_R}} \ln\left[\frac{4b}{0.67\pi w(0.8 + \frac{t}{w})}\right]$ $\frac{w}{(b-t)} < 0.35$ AND $t/b < 0.25$ TYPICALLY Z_o = 30 TO 80Ω

FIGURE 1. By using the impedances for various types of signal-transmission lines, you can determine the amount of ringing you'll experience. (Note that ϵ_R is the relative dielectric constant.)

A 54HC/74HC device's output rise and fall times can be as short as 5 ns, and transmission-line effects can become noticeable when lines longer than a foot or two are driven. The length of the signal line at which transmission-line ringing should be considered is:

$$\text{MAXIMUM LINE LENGTH} = \frac{\text{OUTPUT RISE/FALL TIME}}{2(\text{DELAY PER UNIT LENGTH})}$$

The signal delay per unit of line length (t_{PD}) depends on the line's characteristic impedance and the load on the line. For a typical pc-board trace with a groundplane,

$$t_{PD} = 1.017\sqrt{0.47\,\epsilon_R + 0.67}\ \text{ns/ft},$$

where ϵ_R is the relative dielectric constant. Loading the trace with inputs to other gates alters the t_{PD}.

$$t_{PD}\,(\text{ALTERED}) = t_{PD}\sqrt{1 + \frac{C_{IN}}{C_O}},$$

where C_{IN} is the total input capacitance associated with the line, and C_O is the line capacitance per unit of length.

If you know the characteristics of the transmission line, you can use these equations to find the signal-transit time. This time is typically between 1.5 and 2.4 ns/ft for an unloaded line.

In addition to the line's transit time, you need to find its characteristic impedance:

$$Z_O = L_O/C_O,$$

where L_O and C_O are the wire's inductance and capacitance per unit of length. When a 54HC/74HC device drives a transmission line (*Figure 2*), the driver's output looks into the equivalent line impedance. When the output switches, the signal propagated is the result of the voltage divider created by the line and the driver's impedance.

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If the line's electrical length is long compared with the signal's rise time, the mismatch of the line and the CMOS input creates a reflection when the signal reaches the other end of the line. The reflection's magnitude depends on the incident signal's voltage (V_{INC}) and the reflection coefficient (ρ), where

$$\rho = \frac{R_{IN} - Z_O}{R_{IN} + Z_O}.$$

The reflected signal is therefore

$$V_R = V_D (1 + \rho).$$

HIGH INPUT IMPEDANCE DOUBLES REFLECTION

Because a 54HC/74HC device's input impedance is high compared with the line's ($\rho = 1.0$), the reflected voltage at the receiver doubles. This reflection propagates back to the driver, where another reflection is generated (depending on the driver's output impedance). Typical 54HC/74HC output impedances result in reflection coefficients of -0.3 to -0.7.

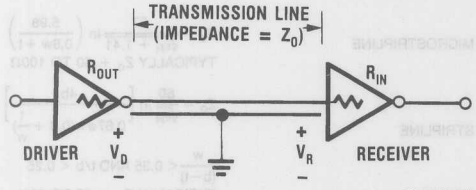
A simplified analysis based on the preceding equations, however, fails to take into account nonlinearity in a 54HC/74HC gate's output impedance. Also, the input of a 54HC/74HC gates has diodes to V_{CC} and ground; these diodes clamp the reflected signal as it tries to exceed the supply level.

A load-line graphic technique overcomes these drawbacks. Illustrating the technique, *Figures 3* and *4* plot the input and output characteristics for a standard and a bus-driver 54HC/74HC IC at $V_{CC} = 5V$. These plots include the effect of the input and output diodes. With these curves, you can approximately determine the ringing for various line impedances when one 54HC/74HC gates drives another.

An example based on a High-to-Low transition on a 200Ω line illustrates how to use the graphs. Starting at the quiescent 5V, 0A point on the logic-One output's curve (*Figure 3*), draw a load line with a slope of $-1/Z_O$ to the logic-Zero output's curve. The voltage at this intersection is the initial output voltage that drives the line after the transition. Then draw a line with a $+1/Z_O$ slope to the input curve. This intersection yields the signal's voltage, including the reflection, when it reaches the receiver. Next, draw another line back to the logic-Zero output curve. This intersection indicates the voltage at the driver when the reflection returns. This process continues until the zigzag load line converges on the 0V, 0A intersection.

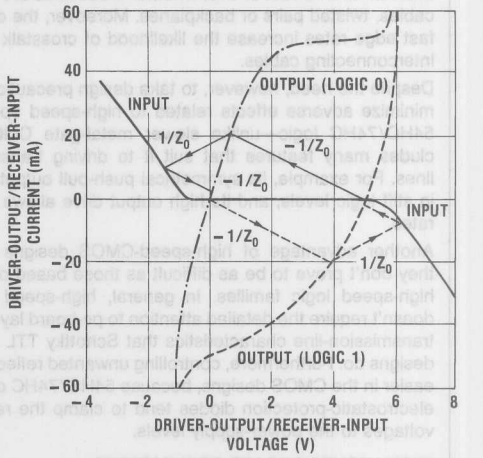
Figure 5 plots the *Figure 3* example's voltages vs propagation delay. *Figure 6* shows real-world waveforms for a 74HC00 device driving another gate through a wire poised above a groundplane ($Z_O = 200\Omega$). Notice that the driver's output level swings further toward the opposite logic level than the graphic method initially predicts, resulting in slightly more-ringing at the receiver as well. This additional ringing is due to either a lower output impedance or a slightly higher line impedance than that used in the paper analysis.

Although line reflections aren't a problem for most designs, you may have to reduce ringing for certain applications, such as those including long cables, backplanes and sensitive circuits that can't tolerate radiated noise and crosstalk. You can use several techniques to reduce ringing. One solution is to use series-terminating resistors (*Figure 7a*). Series termination places a resistor in series with the driver's output to match the output impedance of the driver to that of the line. This procedure eliminates overshoot at the receiver's end of the line but slows down the output signal, and it won't work with buses or backplanes.



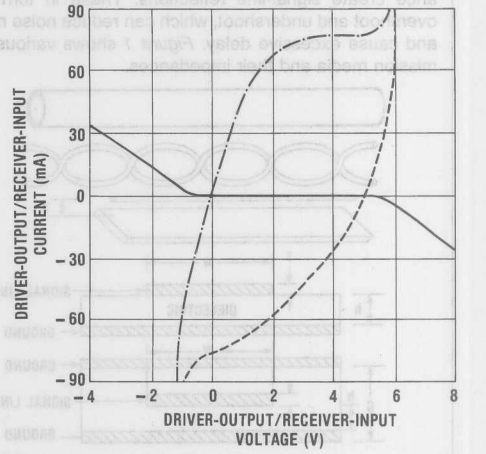
TL/F/8424–2

FIGURE 2. When a high-speed CMOS driver/receiver pair communicates over distances longer than a foot or two, transmission-line effects come into play.



TL/F/8424–3

FIGURE 3. This plot of input and output transfer functions for standard 54HC/74HC high-speed CMOS logic includes the effects of input-protection and parasitic diodes. It provides the basis for a graphic method of determining ringing and overshoot.



TL/F/8424–4

FIGURE 4. Bus-output drivers in the 54HC/74HC high-speed CMOS family exhibit different input and output transfer functions than do the standard parts whose characteristics are shown in *Figure 3*.

PARALLEL TERMINATIONS CAN OVERLOAD CMOS

Parallel termination (*Figure 7b* and *7c*) connects a resistor at the receiver's end of the line to either V_{CC} or ground or to a voltage divider between V_{CC} and ground. The resistor value (or the equivalent resistance of the resistor pair) should match the line's impedance. Normally, a system backplane has one termination per signal line. Some very-high-speed buses, however, can include two termination networks at each end of the backplane for each line.

One problem with parallel termination is that the termination consumes large amounts of power, negating the reason for choosing 54HC/74HC devices to begin with. Moreover, because the termination network must match the line's impedance, parallel termination can overload a 54HC/74HC device's outputs and prevent them from driving the bus to a valid logic level.

Consider, for example, a 150Ω TTL bus with a single termination and the equivalent of a 150Ω termination resistor connected to a 3.5V supply. The worst-case output impedance of a 54HC/74HC bus driver is 100Ω. The dc output voltage for the 54HC/74HC driving a TTL bus to a low level would be V_{OUT} = 3.5V (100Ω/250Ω) = 1.2V, which is too high to represent a valid logic-Zero output. You can use such dc-termination schemes only if a 54HC/74HC device can pull the termination network to within 0.5V of the supply rails (HCT parts work between 0.4 and 2.4V).

Aside from such brute-force power considerations, a subtle problem arises from reflections in certain cases. If the line is long enough to exhibit a significant delay down the line, the ability of the receiving logic element to switch on the original incident-wave front becomes important. If the incident wave isn't of the proper magnitude, the receiver must wait for the reflection before sensing the change at its input. The voltage at the receiver equals the driver's output voltage divided across the driver's output impedance and the line's characteristic impedance. 54HC/74HC gates typically have 40 to 50Ω output impedances, so 54HC/74HC receivers switch on the incident-wave transitions if the line impedances are greater than 150Ω typically.

In general, when replacing LS components with 54HC/74HC units, avoid driving buses with a termination network whose equivalent impedance is less than 500Ω (worst case) terminated to V_{CC} or ground, or 250Ω terminated to 3V.

The TTL termination's impedance isn't the only problem involved in substituting 54HC/74HC parts for TTL. For example, consider the voltages that the termination networks are tied to. Usually, TTL termination networks look like their equivalent impedance tied between 2.5 and 3.5V. Consequently, when these TTL buses are in the high-impedance state, they float toward these voltages, causing the 54HC/74HC circuits to draw I_{CC} currents that are large compared with the currents generated when the bus is terminated to V_{CC} or ground. Also note that some logic errors might develop because the 2.5 to 3.5V range is not a valid 54HC/74HC logic level.

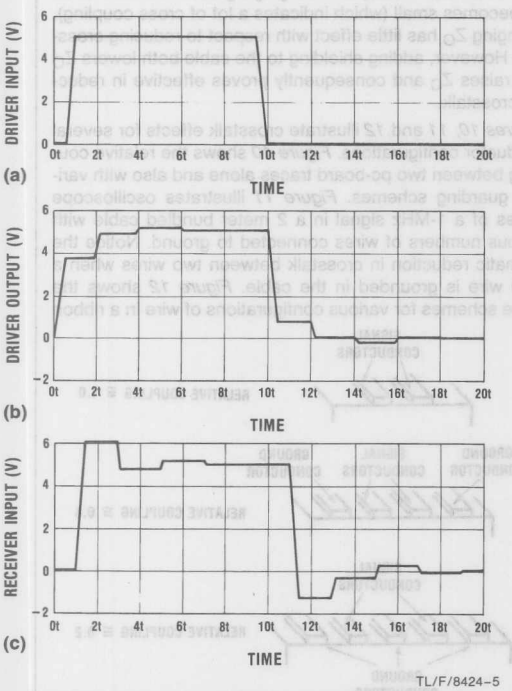


FIGURE 5. Using the plots shown in *Figures 3* and *4* along with the graphic method described in the text, you can construct the driver (b) and receiver (c) waveforms resulting from an input (a).

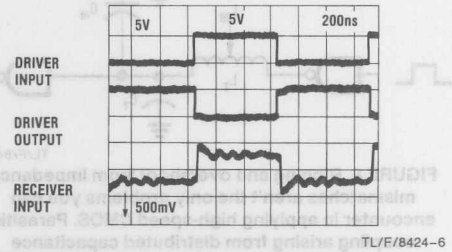


FIGURE 6. A high-speed CMOS device driving another gate through a 28-gauge wire poised above a groundplane (Z_o = 200Ω) exhibits higher ringing and overshoot than predicted in *Figure 5*, thus indicating a lower output impedance or higher line impedance than that used in the prediction.

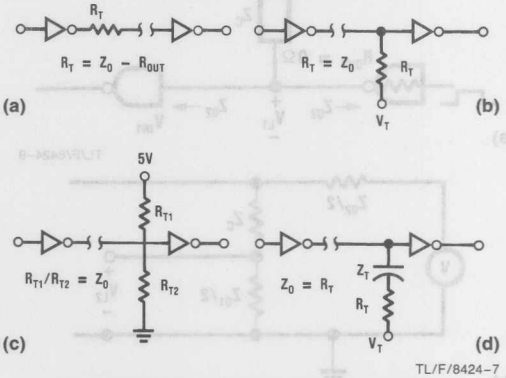
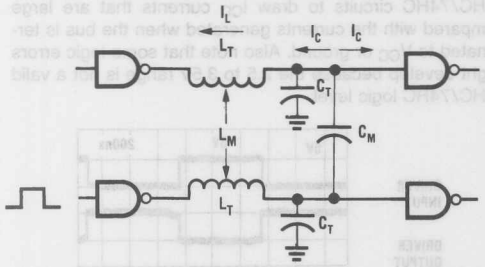


FIGURE 7. The three termination techniques shown here in (a), (b), and (c) work best for conventional TTL. For high-speed CMOS, (d) might provide the best solution.

sitions. This termination scheme doesn't draw any DC power, although it does draw additional AC (dynamic) power. Furthermore, if the bus goes to a high-impedance state, the termination capacitors hold the bus at the last logic level for a short time (perhaps a millisecond), avoiding excessive I_{CC} currents. If the bus has the potential to float for long periods, you might have to add large-value pull-up resistors to ensure that bus leakages don't cause spurious behavior.

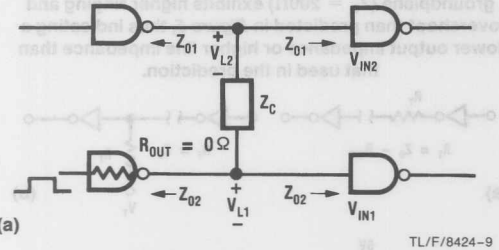
These considerations apply to 54HC/74HC outputs. 54HC/74HC inputs interface easily to any type of bus or transmission line that meets the 54HC/74HC input-voltage requirements.

Eliminating troublesome reflections only handles problems involving a single transmitter/receiver pair. Seldom, however, do transmitter/receiver pairs exist in isolation; they more commonly occur in groups, and the possibility of crosstalk always exists. Parasitic mutual inductance and capacitance associated with system interconnections cause crosstalk.

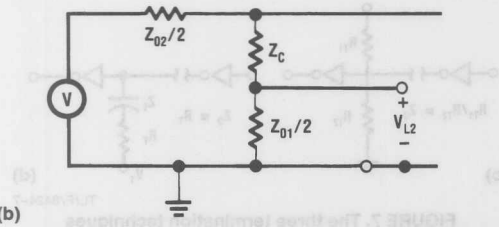


TL/F/8424–8

FIGURE 8. Ringing and overshoot from impedance mismatches aren't the only problems you can encounter in applying high-speed CMOS. Parasitic coupling arising from distributed capacitance and inductance of parallel wires or pc-board traces can cause crosstalk.



TL/F/8424–9



TL/F/8424–10

FIGURE 9. This simplified representation (a) of *Figure 8's* parasitic coupling impedances yields the equivalent circuit shown in (b).

signal lines run in parallel over long distances. Even when using long signal runs, 54HC/74HC devices' noise immunity eases the requirements for crosstalk minimization.

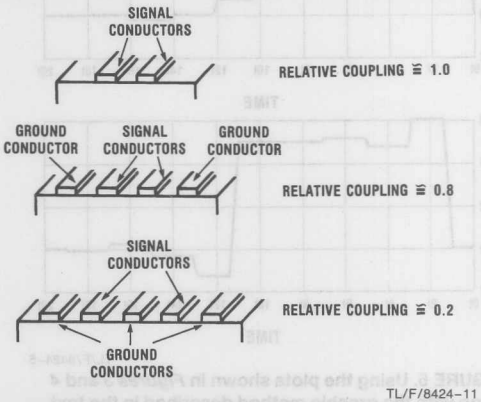
Although you can analyze crosstalk by finding the current coupling caused by distributed capacitance and inductance, the simpler approach based on *Figure 9's* scheme suffices. *Figure 9a* shows two signal lines with an impedance of Z_{O1} and Z_{O2} coupled by Z_C. At the point of coupling, the signal voltage V_{L2} induced into the second line is essentially due to the voltage divider formed by Z_{O1}, Z_{O2} and Z_C (b). The voltage V_{L1} results from V_{OUT} of the first inverter driving the voltage divider formed by the second inverter's R_{OUT} and Z_{O1}. If the driving gate's output impedance is small, then $V_{OUT} = V_{LI} = V_{CC}$ and $Z_{O1} = Z_{O2} = Z_O$. Then the equivalent impedance model of (b) leads to

$$V_{L2} = \frac{Z_{O2}/2}{Z_C + \left(\frac{Z_{O1}}{2}\right) + \left(\frac{Z_{O2}}{2}\right)} \times V_{OUT} = \frac{1}{2}\frac{Z_O}{Z_C + Z_O} V_{CC}.$$

When the signal reaches the receiver, the reflection causes the signal's level to double, and $V_{IN} = 2(V_{L2})$.

Qualitatively, you can see that crosstalk increases as Z_C decreases. Z_C in turn decreases with increasing coupling length (decreasing the spacing between the two connectors) and poor shielding. Lowering Z_O decreases crosstalk but not as dramatically as changing Z_C does. Notice that as Z_C becomes small (which indicates a lot of cross coupling), changing Z_O has little effect with respect to reducing crosstalk. However, adding shielding to the cable both lowers Z_O and raises Z_C and consequently proves effective in reducing crosstalk.

Figures 10, 11 and *12* illustrate crosstalk effects for several conductor configurations. *Figure 10* shows the relative coupling between two pc-board traces alone and also with various guarding schemes. *Figure 11* illustrates oscilloscope traces of a 1-MHz signal in a 2 meter bundled cable with various numbers of wires connected to ground. Notice the dramatic reduction in crosstalk between two wires when a third wire is grounded in the cable. *Figure 12* shows the same schemes for various configurations of wire in a ribbon



TL/F/8424–11

FIGURE 10. Grounding scheme can significantly reduce crosstalk. For example, separating pc-board signal conductors with grounded ones reduces relative coupling from 1 to 0.2.

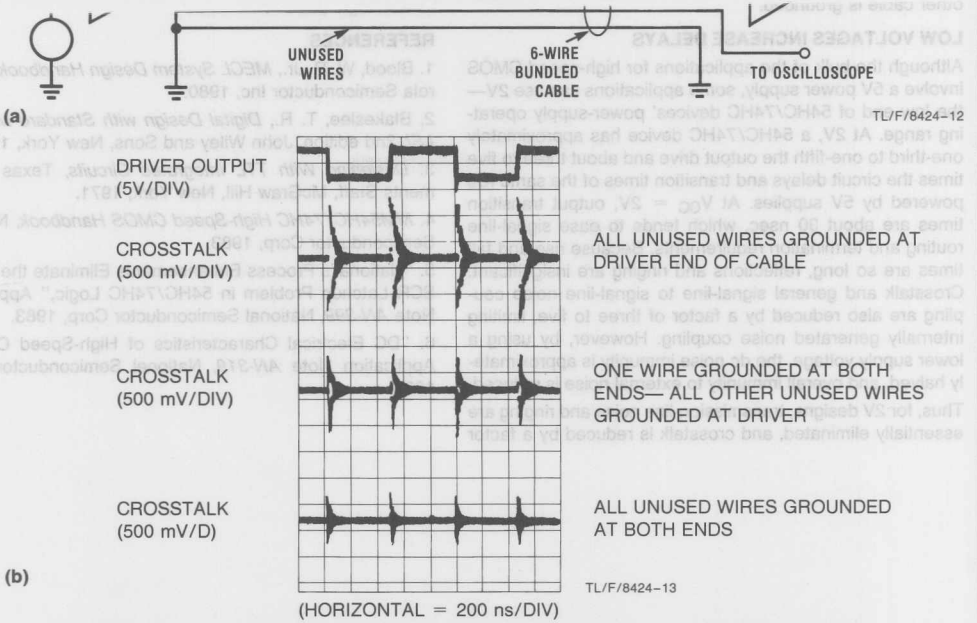


FIGURE 11. The effectiveness of guarding techniques in reducing crosstalk isn't limited to pc boards, as results based on a 6-wire bundled-cable test circuit illustrate (a). Grounding unused wires at both ends yields the best performance (b).

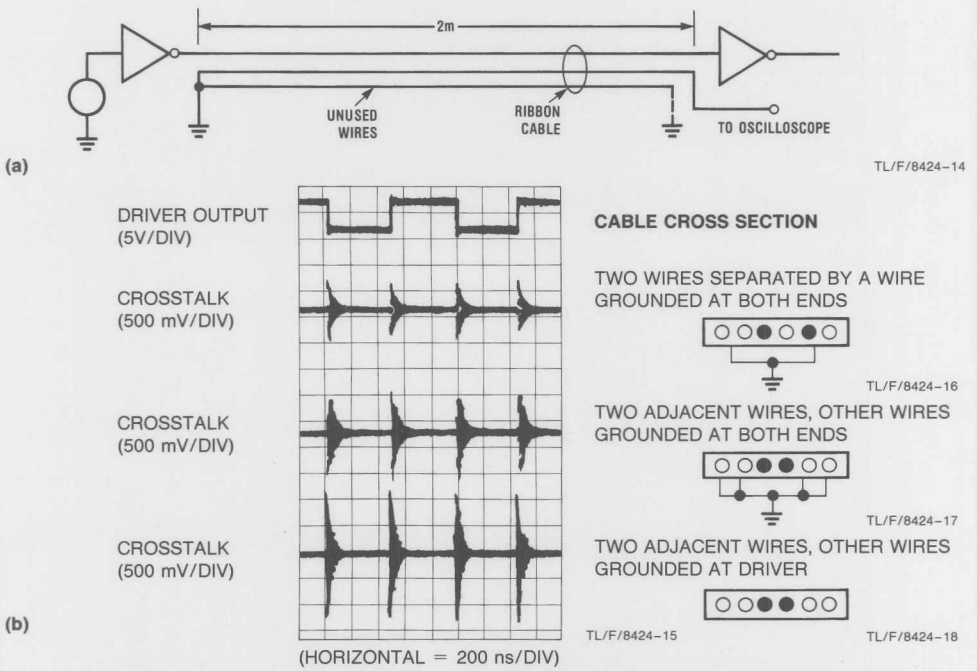


FIGURE 12. To reduce crosstalk between two conductors in a ribbon cable, separating the signal-carrying conductors with ones grounded at both ends proves to be effective.

cable. Here, the lowest crosstalk comes from separating the two signal lines by a ground cable. The most crosstalk occurs when the two cables are adjacent to each other and no other cable is grounded.

LOW VOLTAGES INCREASE DELAYS

Although the bulk of the applications for high-speed CMOS involve a 5V power supply, some applications can use 2V—the low end of 54HC/74HC devices' power-supply operating range. At 2V, a 54HC/74HC device has approximately one-third to one-fifth the output drive and about three to five times the circuit delays and transition times of the same ICs powered by 5V supplies. At V_{CC} = 2V, output transition times are about 30 nsec, which tends to ease signal-line routing and termination requirements. Because rise and fall times are so long, reflections and ringing are insignificant. Crosstalk and general signal-line to signal-line noise coupling are also reduced by a factor of three to five, limiting internally generated noise coupling. However, by using a lower supply voltage, the dc noise immunity is approximately halved, and overall immunity to external noise is reduced.

Thus, for 2V designs, transmission-line noise and ringing are essentially eliminated, and crosstalk is reduced by a factor of two (when device noise-immunity reduction is included). Designing with high-speed CMOS at 2V can best be described as almost identical to trying to design with older CMOS logic at 5V.

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5. "National's Process Enhancements Eliminate the CMOS SCR Latchup Problem in 54HC/74HC Logic," Application Note *AN-399*, National Semiconductor Corp, 1983.

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Monolithic Modem Chip Eases μP's Phone Access

National Semiconductor
Application Note 394
Steve Munich

When mated with a handful of CMOS peripheral ICs, a single-chip CMOS modem device allows you to configure simple, inexpensive microprocessor-telephone interface systems with autodial and autoanswer capabilities

Integrated-circuit modems represent the final link in the chain of devices that connect the digital world of the microprocessor bus to the analog world of the telephone line. The MM74HC943 is such an IC; it's a single-chip and -supply Bell-103 modem whose on-chip analog filtering, carrier-detect circuitry and complete hybrid function spare you the complexities of analog design.

Linked with such CMOS peripheral ICs as the NSC858 UART, the TP5088 DTMF dialer and some 74HC logic, the IC allows the design of relatively inexpensive systems that can profit from the intelligence and flexibility of microprocessor control. What's more, its silicon-gate CMOS process suits the IC to applications in portable, battery-powered, remote and harsh-environment systems. With little difficulty, you can easily integrate the IC into an auto-originate, autoanswer modem in a μP-based system.

Figure 1 shows the basic functional blocks needed to connect a microprocessor bus to a telephone line. The bus decoders are necessary to assign a unique set of addresses to the UART (universal asynchronous receiver/transmitter) and dialer circuit. The dialer circuit must be bus compatible; i.e., it must be capable of accepting binary inputs from the data bus. The dialer can create pulses, as with rotary-dial phones, or it can send DTMF (dual-tone multifrequency) signals to the central office to establish a connection with another phone.

When the modem operates with the dialer to call another system, the calling modem is said to be in the originate mode. When the microcomputer receives a call through the modem interface, the ring-indicator circuit serves to interrupt the microprocessor to answer the call automatically. In this case, the modem goes to the answer mode. The block denoted "hook-switch control" is a logic-controlled relay that connects the system to or disconnects it from the phone line.

Protective circuitry is needed to isolate the microcomputer user from hazards (e.g., lightning) transmitted by the phone line and also to protect the public phone system from anything potentially damaging that may emanate from the user's computer equipment. This circuit also provides a 2-sec billing delay when an incoming call is answered. During this period, data may not be sent or received. These protective-circuitry functions are required (and must be approved) by the FCC (a later section discusses them in detail). The depicted hybrid block performs 2-to-4 wire conversion, necessary because both send and receive frequency bands use the same pair of wires and it's necessary to separate the received signal from the transmitted one.

The next functional block is the modem itself. Modems have only recently become available in integrated-circuit form; two standards currently prevail in the U.S. The 103 standard is for 300-baud, full-duplex communication; the 202 standard allows 1200-baud transmission while receiving at 5 baud, and vice versa. Another standard, the 212, specifies full-duplex, 1200-baud operation.

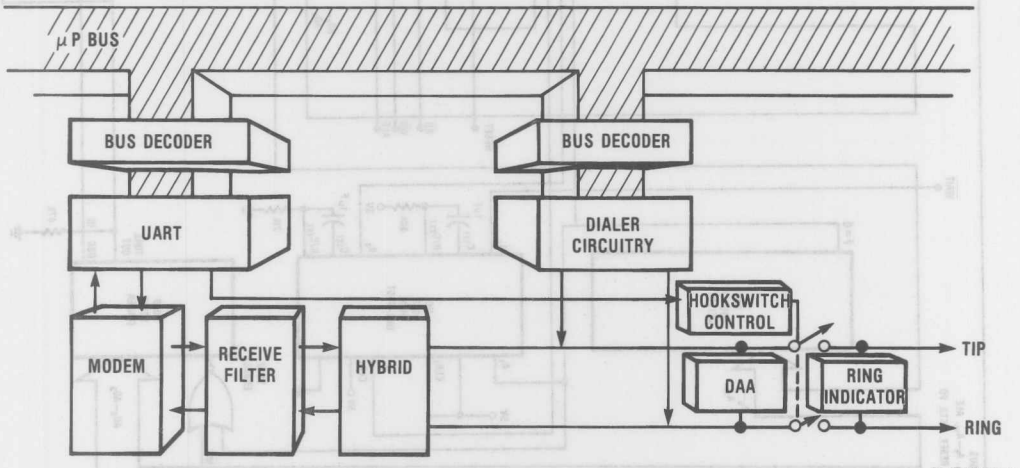


FIGURE 1. A basic microprocessor/telephone-line interface comprises the blocks shown in this diagram. The modem assumes the task of generating and decoding the sine-wave signals that represent marks and spaces in digital communications.

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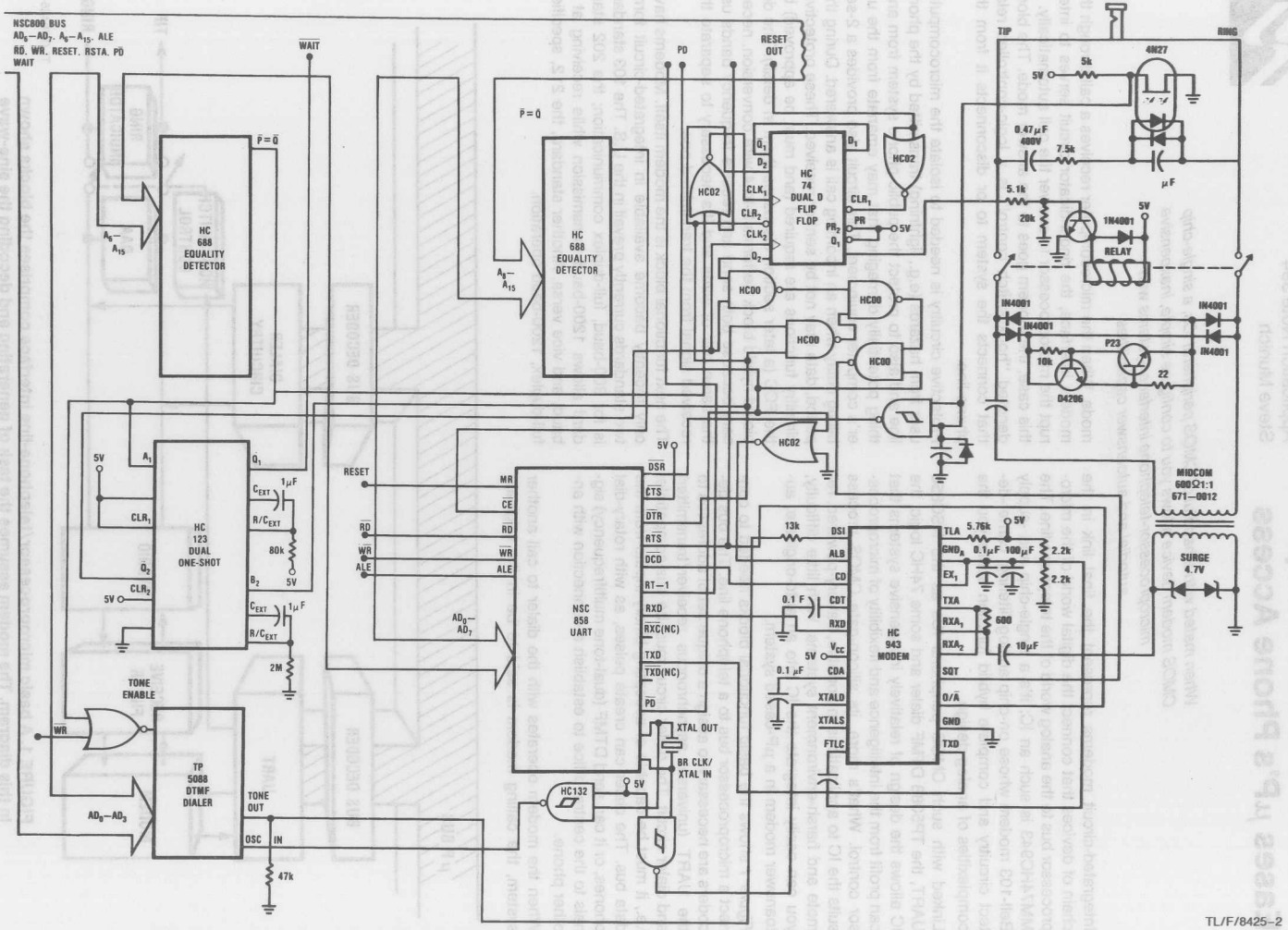


FIGURE 2. A specific implementation of FIGURE 1's diagram, this schematic shows how the 1-chip modem IC fits into a data-communications phone link. The circuit shown is an intelligent, microprocessor-controlled modem board. The logic circuits are all CMOS types, hence the system consumes little power in operating mode and micropower in power-down mode.

In addition to the ICs that satisfy U.S. standards, there are integrated-circuit solutions that conform to European (CCITT) standards. These devices use bit rates that are similar to those for the Bell standards, but they also use a slightly altered set of frequency bands; moreover, they send an extra tone to disable the European phone system's echo suppressors.

Figure 1 also shows a block for an external receive filter that may or may not be needed, depending on which manufacturer's modem chip is used. The modem basically receives a frequency-shift-keyed (FSK) mark (logical One) or a space (logical Zero), and sends serial Ones and Zeros to the UART. At the same time, the modem also receives serial data and synthesizes a phase-continuous sine wave to send to another modem at the other end of the phone line.

Finally, the UART takes parallel data from the microprocessor and feeds a serial data stream to the modem. It also configures the modem's serial output to form a parallel word on the bus. The UART must add start, stop and parity bits to the data word from the bus before transmission of the character and then strip off these same bits at the reception of a character. UARTs have long been available in IC form; they offer various degrees of programmability as well as such features as on-chip baud-rate generation and advanced modem-interface capabilities.

Moving from a block diagram to a specific one, consider the all-CMOS, intelligent-modem board shown in *Figure 2*. This system interfaces with the NSC800 bus; however, you could use any mutiplexed-bus microprocessor. The two -HC688s are bus comparators that are hard wired to generate chip-select signals to the dialer and UART upon accessing the proper memory location. The first -HC688 decodes the eight MSBs from the bus to activate the TP5088 tone generator. When a call is originated, the digits of the phone number are retrieved one at a time from system RAM.

With the modem chip's transmitter squelched, the TP5088 uses the DSI (drive-summing input) pin to the -HC943's line driver for tone transmission. In order to avoid clipping, you must be sure that the TP5088's output signal level does not exceed the transmit level selected by the TLA resistor. Writing the data on bus lines AD_0 through AD_3 to the tone-generator address causes the TP5088's tone-enable input to switch high through the NOR gate. A low-going WR from the bus latches the four bits into the DTMF generator.

When the -HC688's output enables tone generation, it simultaneously fires one of the -HC123 dual one-shots onto the NSC800 bus's Wait line for 80 msec. Thus, one of 16 possible tone combinations feeds through to the central office for 80 ms. Before the generation of the next tone, a software wait loop serves to turn the generator off for 80 ms, i.e., until transmission of the next DTMF tone pair. This action allows for an 80-ms-On, 80-ms-Off make-break ratio, one that works with almost any central-office receiving equipment. You can change this make-break ratio to suit any requirement by altering the software timing and the one-shot's external-component values.

The same bus comparator pulls in the relay to take the phone off-hook. A read to the address of the first -HC688 does not affect the TP5088; instead, it clocks flip flop 1 of the -HC74 dual D flip flop. This action controls the on-/off-hook relay for answering or hanging up the phone connection. Clocking the -HC74 flips the relay into its opposite state; resetting the NSC800 on power-up causes Reset-Out on the bus to become active. This signal, fed into the Clear input of the -HC74's flip flop 1, keeps the connection on-hook when power is first applied to the system. For microprocessors lacking this Reset-Out signal, a power-on reset circuit could provide this function.

Directly connected to the phone line, the ring-indicator circuit tells the microprocessor that the line is ringing locally. When this happens, the optocoupler's transistor toggles on and off, resulting in a long positive pulse from the normally low Schmitt-trigger NAND output. This signal routes to the RC network and Schmitt-trigger NAND gate, which form a simple one-shot. The resistor and capacitor values are such as to convert the ring signal from a series of low-going spikes into a constantly low logic level.

The first pulse sets off the one-shot, which in turn drives the UART's input. The UART can then interrupt the processor as detailed in a later section. The 600Ω 1:1 transformer isolates the line from hazards. The transformer and ring-indicator circuit connect directly to the phone line; therefore, their designs must follow the isolation guidelines in FCC Rules, part 68.

The NSC858 UART (*Figure 3*), a member of the NSC800™ family, features an on-chip baud-rate generator, a power-down mode and extensive interrupt capabilities. It also has two modem-control outputs ($\overline{DTR}$ and $\overline{RTS}$) and three modem-control inputs, ($\overline{DCD}$, $\overline{DSR}$] and $\overline{CTS}$). The absence of an RS-232C connection in this application removes the need for most of these protocols. As a result, except for $\overline{DCD}$, these controls serve as general-purpose I/O controls for the modem's SQT and O/$\overline{A}$ pins and as interrupt inputs.

The NSC858 has internal registers that monitor the status of these inputs; if enabled, the registers cause the UART to interrupt the processor if a data set change occurs (i.e., if a logic level changes on one of the modem-control inputs). This is how the ring-indicator circuit in *Figure 2* is able to generate an interrupt. The UART's $\overline{DCD}$ input is connected to the -HC943's carrier-detect ($\overline{CD}$) output to generate an interrupt upon the loss of carrier to the modem. To see which status change is responsible for the interrupt, software can check the UART's modem-status register.

In this application, the $\overline{RTS}$ output pin serves to control the O/$\overline{A}$ pin on the -HC943. The $\overline{DTR}$ output enters the billing-delay circuit shown in *Figure 4*; its function is to activate or deactivate the squelching function for the -HC943's modulator. Software squelches the modem only by asserting a logical Zero on $\overline{DTR}$ whenever its intent is to open the 3-state output of the modem's sine-wave synthesizer (*Figure 1*) and to allow the tone generator to use the line driver for externally generated tones.

When $\overline{PD}$ goes Low, the -HC943 and -HC858 power down. The TP5088 is in its low-power mode whenever it is not producing tones. $\overline{PD}$ on the NSC800 bus is actually an input to power down the NSC800; therefore, it's assumed that another power-saving control device powers down the whole system. One example of such a device is a real-time clock (for example, the MM58167A) with an alarm-compare interrupt output that can interrupt the processor once during a selected time period.

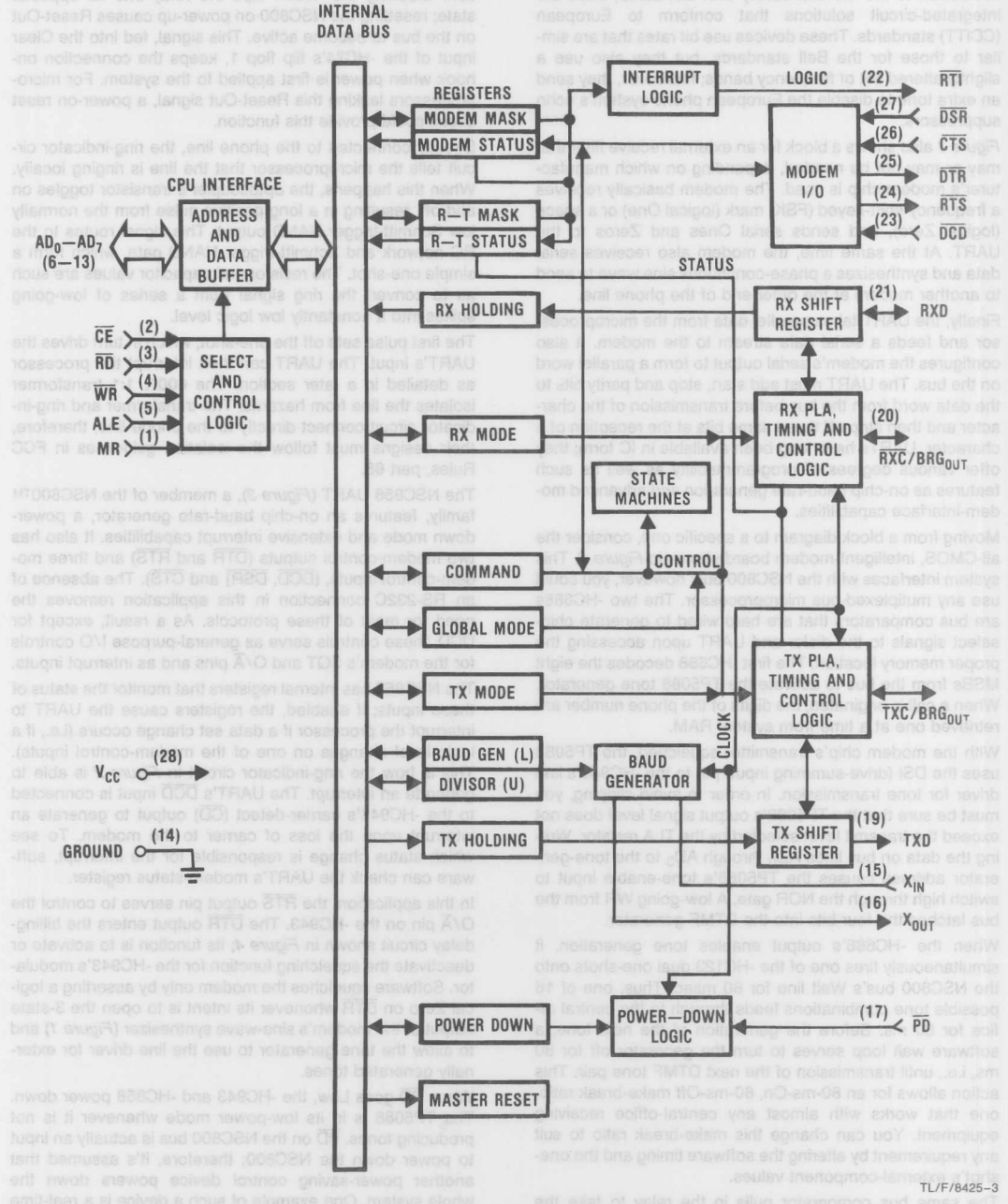


FIGURE 3. Interface between the modem and the μP bus, the UART (Universal Asynchronous Receiver/Transmitter) interrupts the processor upon logic-level changes in the modem-control lines. The UART's modem-status register, upon a software query, reveals which change caused the interrupt. The IC has an on-chip baud-rate generator and features a power-down mode for low power consumption during inactive periods.

The modem, UART and DTMF dialer chip can use a 3.579545 MHz TV color-burst crystal. *Figure 2* shows the UART's crystal oscillator driving the other two devices. Schmitt triggers serve to square up the signals to the other devices. The added input capacitance from the Schmitt triggers slightly alters the oscillator frequency, but not appreciably (less than 0.1%). Note that it's important to balance any added capacitance on both sides of the crystal.

FCC-REGISTERED PROTECTION

Be warned that before you can legally connect any modem to the phone lines, you must obtain FCC approval of the protective circuitry (once known as the data-access arrangement). *Figure 2*'s subsystem is registered as a "data-terminal device"; it must be able to withstand the high voltages specified in part 68 of the FCC's Rules and Regulations. Hybrid modules to perform the protective functions are available from various manufacturers; some come with FCC approval.

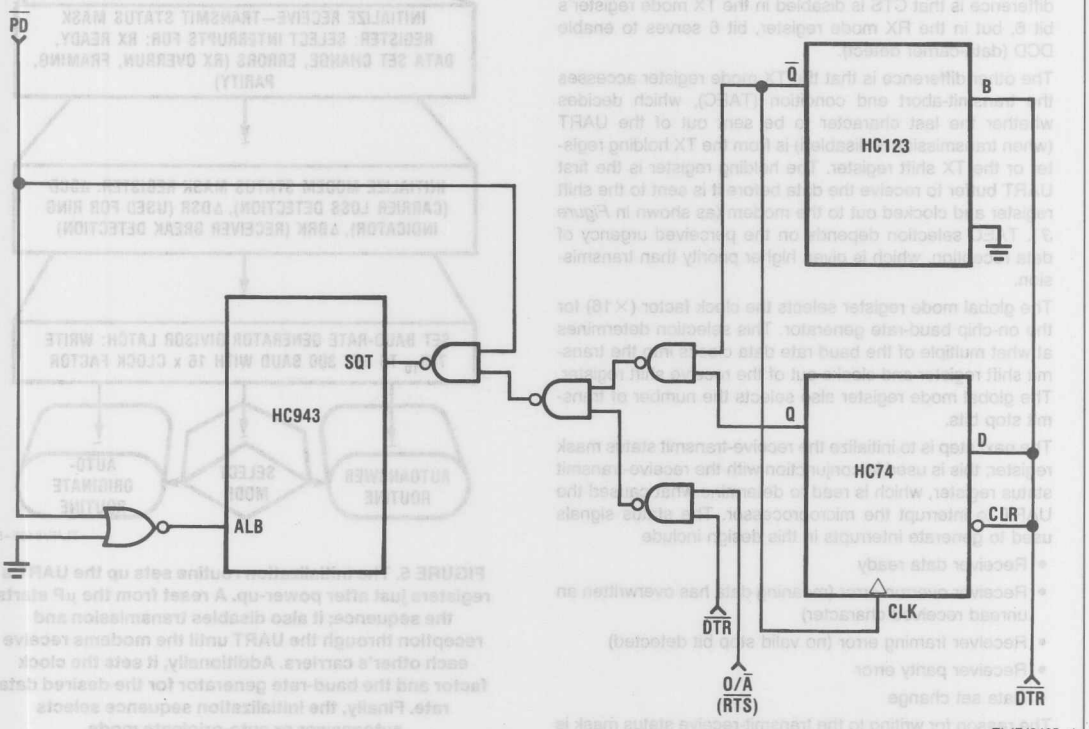
Some of the available modules perform the ring-indicator, billing-delay, filtering, and hybrid functions (as well as other functions). Note, however, that these devices are too expensive for high-volume modem systems. In many cases, moreover, the devices include unneeded or redundant functions. The configuration in *Figure 2* uses a custom protective circuit that includes only the necessary functions, but be aware that the circuit has not undergone the FCC approval process, so it carries no guarantees. For any protective-circuit design, you'd be well advised to obtain the assistance of a qualified consultant in procuring FCC approval.

The billing-delay circuitry is shown in *Figure 4*. It uses an -HC00 quad NAND package, half of an -HC123 dual one-shot and half of an -HC74 dual D flip flop. This circuit keeps the -HC943 squelched for 2 sec after the connection goes off-hook in the answer mode. There is no transmission delay in the originate mode. The 2-sec interval allows the phone company to send supervisory billing tones before the transmission of any data.

The UART's $\overline{DTR}$ output pin is low when the modem is to be squelched; this logic level keeps the flip flop's Q output cleared. This low logic level also masks the one-shot's output, so the signal from the NAND gates to the -HC943's SQT pin remains high, thereby keeping the modem squelched. When the UART brings $\overline{DTR}$ high, the flip flop's Q output stays low while the one-shot is fired. The -HC123's normally high $\overline{Q}$ output is now pulsed low for 2 sec; this action keeps the modem squelched during this time if the answer mode was previously selected.

After the delay, the one-shot's output provides a rising edge to the flip flop's clock to transfer the high-logic-level input from $\overline{DTR}$ to the Q output. The NAND gates now transfer a low level to the modem's SQT pin; as a result, the modem sends a 2025 Hz answer-mode mark. Note that if the system receives a power-down signal from $\overline{PD}$, the modem is not allowed to transmit.

If the microprocessor and firmware were included on the same board for submission to the FCC, separate billing-delay circuitry would not be necessary. A 2-sec software wait loop could instead provide the delay; it would act as the billing-delay circuitry.



TL/F/8425–4

FIGURE 4. The billing-delay circuit initiates or removes the squelch function, providing a 2-sec delay to allow the phone company to send supervisory billing tones before any data transmission.

DON'T FORGET SOFTWARE

The hardware configuration discussed in the preceding section is, of course, useless without proper software routines to control it. This software comprises three phases: initialization, call establishment and information transfer. Upon system power-up, the initialization procedure must reset the UART and prevent the modem from coming up in an arbitrary mode and thereby transmitting a tone.

The call-establishment phase can commence once the user makes his decision to call another modem or enables the system to accept an incoming call. The main program is for full-duplex character transfer once the phone connection is established and the two modems are talking. If the connection is lost for one reason or another, the call-establishment phase is reentered.

The initialization routine of *Figure 5* serves to set up all the UART's registers immediately after power-up. It starts with a hardware reset from the microprocessor (Reset Out for the NSC800), thereby clearing most of the UART's internal registers and disabling the modem-control pins and their associated interrupts. This register-clearing action also temporarily disables transmission and reception through the UART; it's reenabled only after all the registers are correctly set up and the two modems are receiving each other's carriers.

In the initialization of the transmit-mode register, the $\overline{CTS}$ (Clear To Send) pin is normally enabled—however, it's not used in this design, so it's left disabled. In both the transmit- and receive-mode registers, the same parity, data-size and internal-clock bits are written in the initialization word. One difference is that $\overline{CTS}$ is disabled in the TX mode register's bit 6, but in the RX mode register, bit 6 serves to enable DCD (data-carrier detect).

The other difference is that the TX mode register accesses the transmit-abort end condition (TAEC), which decides whether the last character to be sent out of the UART (when transmission is disabled) is from the TX holding register or the TX shift register. The holding register is the first UART buffer to receive the data before it is sent to the shift register and clocked out to the modem (as shown in *Figure 3*). TAEC selection depends on the perceived urgency of data reception, which is given higher priority than transmission.

The global mode register selects the clock factor ($\times 16$) for the on-chip baud-rate generator. This selection determines at what multiple of the baud rate data clocks into the transmit shift register and clocks out of the receive shift register. The global mode register also selects the number of transmit stop bits.

The next step is to initialize the receive-transmit status mask register; this is used in conjunction with the receive-transmit status register, which is read to determine what caused the UART to interrupt the microprocessor. The status signals used to generate interrupts in this design include

- Receiver data ready
- Receiver overrun error (meaning data has overwritten an unread received character)
- Receiver framing error (no valid stop bit detected)
- Receiver parity error
- Data set change

The reason for writing to the transmit-receive status mask is to select those status signals that will be allowed to generate interrupts. A data set change refers to a logic-level change on one of the modem's status input pins. The

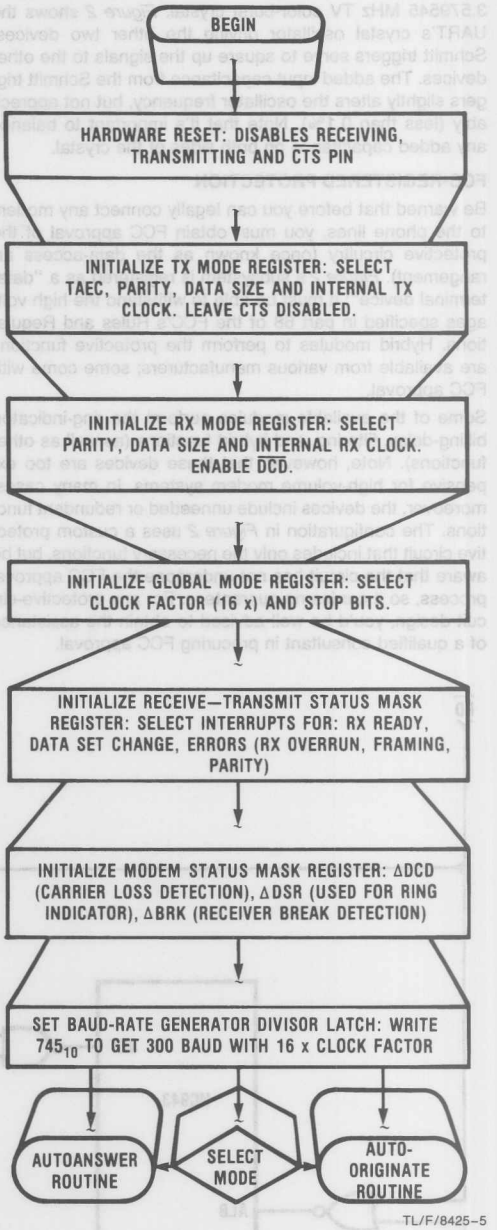


FIGURE 5. The initialization routine sets up the UART's registers just after power-up. A reset from the μP starts the sequence; it also disables transmission and reception through the UART until the modems receive each other's carriers. Additionally, it sets the clock factor and the baud-rate generator for the desired data rate. Finally, the initialization sequence selects autoanswer or auto-originate mode.

UART's modem status mask register masks these signals to determine which ones will be allowed to create a data-set-change interrupt.

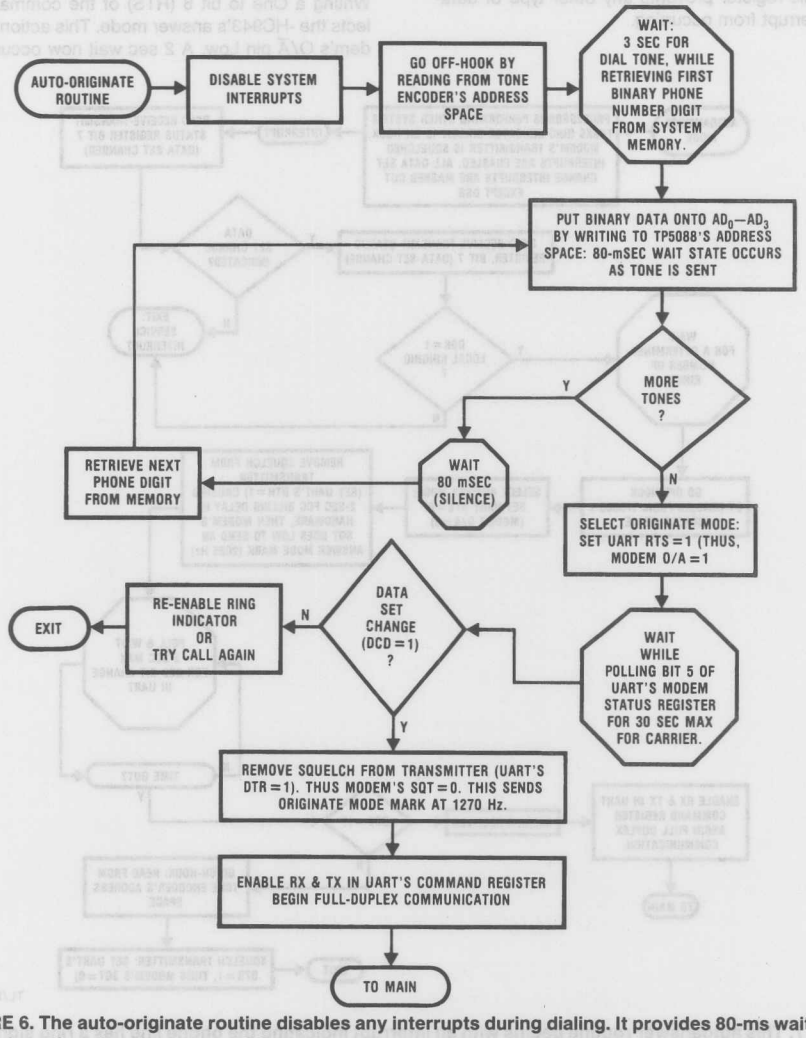
The final area of initialization sets the baud rate for sending data out of the UART's transmit shift register and for clocking data out of the receive shift register. Writing a value of 745_{10} into the baud-rate divisor latch gives 300-baud operation with a 3.579545 MHz crystal, using the previously selected $\times 16$ clock factor.

AUTO-ORIGINATE ROUTINE

The auto originate routine in *Figure 6* begins by disabling interrupts to prevent an incoming call or anything else from taking over the processor and damaging the critical dialing timing. A read to the address occupied by the tone decoder causes the system to go off-hook. It's necessary to wait a suitable amount of time, depending on the phone system's response time, for a dial tone. Dial-tone reception is not acknowledged in this application, so it's best that the wait loop be as long as possible.

Next, the first binary phone-number digit is retrieved from memory and is written onto the AD_0 through AD_3 line from the microprocessor bus. This action automatically puts the μP in wait state for 80 ms (in hardware) while the tone is sent. After this wait, a software wait loop gives 80 ms of silence between tones. The next phone-number digit is then retrieved from memory; the process continues until the number is completely dialed.

At this point, selection of the originate mode occurs by writing a Zero to bit 6 (RTS) in the command register. This action sets the $\overline{RTS}$ pin (which directly feeds $O/\overline{A}$ in the -HC943) High in the UART. Next, a wait loop occurs concurrently with the polling of bit 5 of the modem status register. If, after 30 sec of waiting, no carrier is received (bit 5 = 0), the connection has not been established. A carrier is typically detected in about 10 sec; 30 sec is the maximum.



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FIGURE 6. The auto-originate routine disables any interrupts during dialing. It provides 80-ms wait-state commands to the microprocessor while tones are sent, and 80 ms of silence between tones. If the call is not established within 30 sec, the sequence enables the ring indicator or tries the call again.

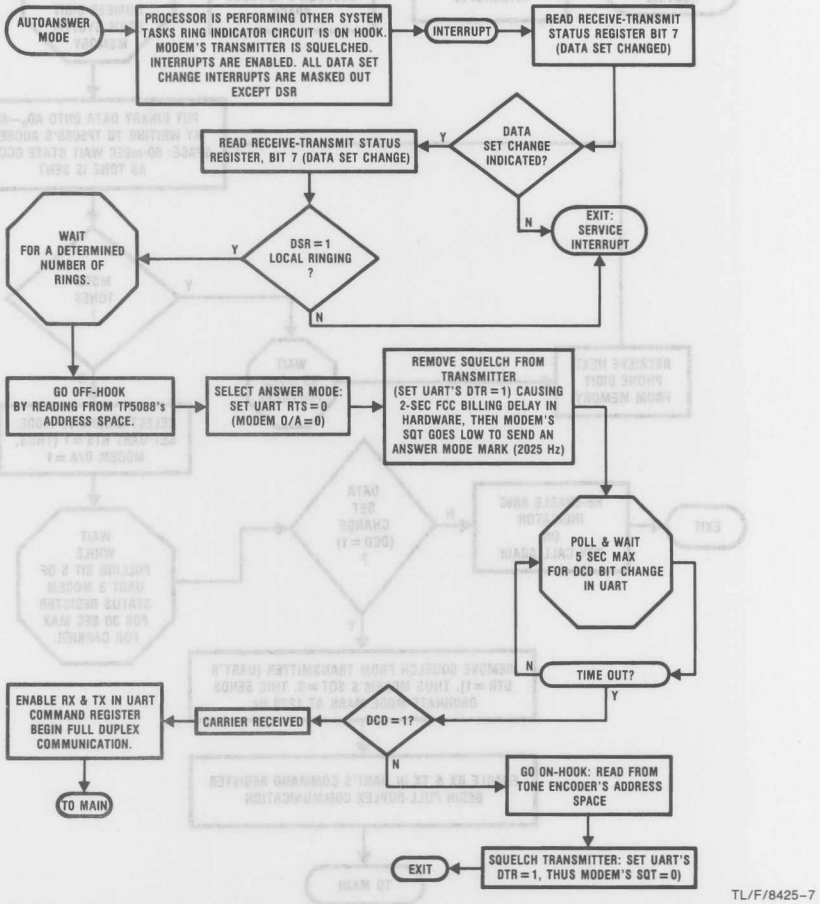
If no carrier is received, you can hang up the connection and call the number again, enter the autoanswer mode, or abandon the call. If the connection is established, and an answer-mode carrier is received, then writing a One to bit 7 (DTR) of the command register removes the squelch previously imposed upon the originate modem's carrier. This action causes the UART's $\overline{DTR}$ pin to switch Low; as a result, SQT = 0 in the modem. Now the UART's command register enables the receiver and transmitter, and full-duplex communication can begin through the main program.

The autoanswer routine of *Figure 7* must begin with an interrupt that indicates that the phone line has a ring signal on the answer modem's side of the telephone line. Before this can occur, it's necessary to enable interrupts. The hookswitch control circuit is still on-hook as it was after power-up. Writing a One to bit 7 of the UART's command register ensures squelching of the modem's transmitter. Writing a One to DSR in the modem mask register and Zeros to all other bits in this register prevents any other type of data-set-change interrupt from occurring.

The system can continue to do other tasks in anticipation of a calling interrupt, providing the preceding conditions do not change. When an interrupt does occur, checking bit 7 of the receive-transmit status register reveals whether a data set change has occurred. If one hasn't occurred, then some other peripheral has interrupted the microprocessor. Upon verification of a data set change, it's necessary to check bit 6 of the modem status register to see whether the $\overline{DSR}$ pin has gone high.

Because all other bits in the modem status mask were masked out, it's unlikely that any other modem status pin has caused the interrupt. Once bit 6 is verified to be high, system interrupts are disabled and the processor's stack popped to prevent an interrupt return. Meanwhile, the phone line still sees a ringing signal, so a wait loop can be inserted for a programmed number of rings before the call is answered. The connection then goes off-hook as a result of reading the tone dialer's address space.

Writing a One to bit 6 (RTS) of the command register selects the -HC943's answer mode. This action brings the modem's O/$\overline{A}$ pin Low. A 2 sec wait now occurs in hardware,



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FIGURE 7. This autoanswer routine begins with an interrupt indicating the phone line has a ring signal at the answer modem. The routine causes the answer modem to listen for the originate modem's carrier; if the carrier is not received within 5 sec, the answer modem's carrier is suppressed and the originate side can attempt a recall.

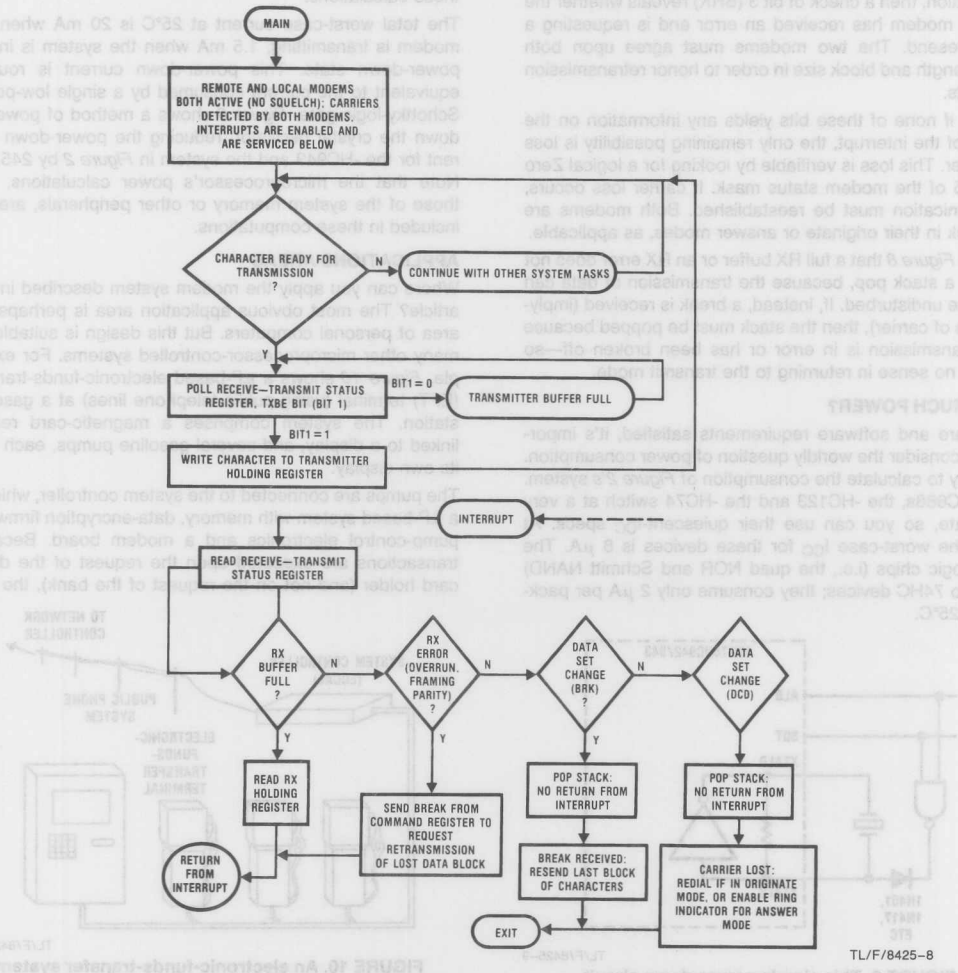
as previously discussed. The originate modem is now waiting in silence. Writing a One to bit 7 (DTR) of the command register now removes the squelch imposed upon the answer modem's transmitter. This operation forces the -HC943's squelch (SQT) pin Low and causes transmission of a 2025 Hz answer-mode mark.

The answer modem is now anticipating the originate modem's 1270 Hz carrier. During a 5 sec max wait, bit 5 (DCD) of the UART's modem-status register is polled for a logical One. If DCD does not go high in this time, the connection goes on-hook and the answer modem's carrier is suppressed by the squelch circuit. The originate modem can now attempt a recall. If the modem receives a carrier within the 5 sec limit, bits 0 and 1 in the command register both go High, enabling both transmission and reception. Full-duplex communication can now begin, and access to the main program for this operation now occurs.

THE MAIN RX/TX PROGRAM

After establishing the phone connection between the two modems, the main program of *Figure 8* controls the reception and transmission of data. The routine begins with the enabling of system interrupts. Transmission uses a well-known polling technique that checks the receive-transmit status register whenever a character is ready for transmission. If the TXBE (transmit buffer empty) bit is Zero, polling of the bit continues until it reads logical One. A character is then written into the transmit holding register and the process continues. The character is also transferred to and clocked out of the transmit shift register and sent to the -HC943; this final process is transparent to the software.

Data reception receives a higher priority than does transmission, in most cases, because a character will be over-



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FIGURE 8. After the establishment of a phone connection, this communications program takes over the management of the modem-to-modem conversation. Because reception is accorded a higher priority than is transmission, it's interrupt driven; i.e., receiving a data word gets top priority. The routine checks for errors and allows for retransmission when an error is detected. In the case of loss of carrier, the sequence arranges for both modems to revert to their autoanswer and auto-originate modes.

written in the UART if it is not read promptly enough. Thus, reception is interrupt-driven. Other UART-oriented functions are interrupt-driven in the main program, but reception of a data word receives top priority.

A read of the receive-transmit status register serves to poll six of its important bits. Bit 0 (Receiver Data Ready) is polled first; if it's a logical One, a read of the RX holding register takes place. This action is followed by an interrupt return that transfers control back to the transmission mode. If bit 0 yields no information, bits 3, 4 and 5 are read in order. If one of these bits reads logical One, this means a receiver-overrun, framing or parity error has occurred; the incoming data is defective and must be retransmitted.

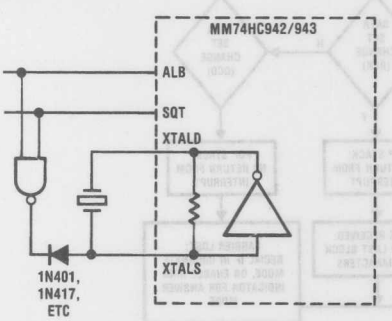
A suitable means of requesting a retransmission of the last block of characters is to transmit a break, which is a continuous string of logical Zeros. Variable break lengths are programmable on the NSC858. If the three bits yield no error information, then a check of bit 3 (BRK) reveals whether the remote modem has received an error and is requesting a block resend. The two modems must agree upon both break length and block size in order to honor retransmission requests.

Finally, if none of these bits yields any information on the cause of the interrupt, the only remaining possibility is loss of carrier. This loss is verifiable by looking for a logical Zero on bit 5 of the modem status mask. If carrier loss occurs, communication must be reestablished. Both modems are put back in their originate or answer modes, as applicable.

Note in *Figure 8* that a full RX buffer or an RX error does not require a stack pop, because the transmission of data can continue undisturbed. If, instead, a break is received (implying loss of carrier), then the stack must be popped because data transmission is in error or has been broken off—so there's no sense in returning to the transmit mode.

HOW MUCH POWER?

Hardware and software requirements satisfied, it's important to consider the worldly question of power consumption. It's easy to calculate the consumption of *Figure 2's* system. The -HC688s, the -HC123 and the -HC74 switch at a very slow rate, so you can use their quiescent-I_{CC} specs. At 25°C, the worst-case I_{CC} for these devices is 8 μA. The other logic chips (i.e., the quad NOR and Schmitt NAND) are also 74HC devices; they consume only 2 μA per package at 25°C.



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FIGURE 9. This simple power-down circuit puts the crystal oscillator to sleep, reducing the modem's quiescent current by 245 μA.

The consumption of the -HC devices is insignificant in comparison with that of the larger circuits in *Figure 2*. The NSC858 uses 5 mA when operating at 300 baud, and it uses, at most, approximately 200 μA in power-down mode. The -HC943 consumes 9 mA max when transmitting at −9 dBm; I_{CC} drops to 250 μA in power-down mode. The resistor divider for the -HC943's analog-ground connection consumes approximately 1 mA. This current is not required by the -HC942; moreover, using an op-amp-generated reference instead of a divider can eliminate it for the -HC943.

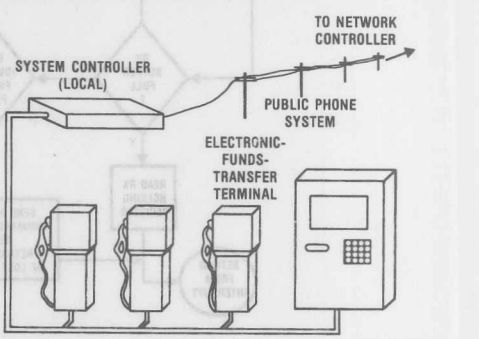
Because the TP5088 never operates at the same time as the modem, and because the modem consumes more power, only the DTMF generator's idle-mode (no tones sent) current of 100 μA is needed. The hook-switch relay typically consumes about 5 mA, but this figure is strongly dependent on the type of relay used. The ring-indicator circuit is line powered; therefore, you need not include its consumption in these calculations.

The total worst-case current at 25°C is 20 mA when the modem is transmitting, 1.5 mA when the system is in the power-down state. This power-down current is roughly equivalent to the current consumed by a single low-power Schottky-logic gate. *Figure 9* shows a method of powering down the crystal oscillator, reducing the power-down current for the -HC943 and the system in *Figure 2* by 245 μA. Note that the microprocessor's power calculations, and those of the system memory or other peripherals, are not included in these computations.

APPLICATIONS AREAS

Where can you apply the modem system described in this article? The most obvious application area is perhaps the area of personal computers. But this design is suitable for many other microprocessor-controlled systems. For example, *Figure 10* shows a μP-based electronic-funds-transfer (EFT) terminal (using public telephone lines) at a gasoline station. The system comprises a magnetic-card reader linked to a display, and several gasoline pumps, each with its own display.

The pumps are connected to the system controller, which is a μP-based system with memory, data-encryption firmware, pump-control electronics and a modem board. Because transactions are executed upon the request of the debit-card holder (and not on the request of the bank), the mo-



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FIGURE 10. An electronic-funds-transfer system allows for gasoline purchases in this example. The gas pumps connect to a system controller that protects data by using an encryption technique. The system uses public phone lines instead of expensive leased lines. The preferred data rate for such proposed systems is 300 baud.

dem circuit of *Figure 2* would be configured as an originate-only system. The answer-routine software and the ring-indicator circuit are not needed.

For central-office receiving equipment that operates on pulses rather than on DTMF tones, the tone-dialing circuitry (TP5088, -HC688 and -HC123) is also unneeded. The microprocessor could toggle the logic-controlled relay to send the dialing pulses while software wait loops control the pulse duration.

For a large number of EFT terminals linked to one system, a subset of the terminals could interface with a network controller that would communicate with the central computer at a much higher data rate than that of any one terminal. The network controller would multiplex the data from the terminals in its local cluster. This configuration would reduce the number of leased lines used from one per terminal to one per controller, substantially reducing system cost.

Most of the risk of opening the public phone system to electronic-funds transfer could be eliminated by using data encryption, with a key that's easily changed electronically (and it should be changed as often as possible). Data encryption handled in hardware would offer the speediest operation. Such networks are common today, except that usually only leased lines are used for EFT. Standards for EFT over the public phone system are currently in development.

In using public phone lines for EFT, the data-transfer rate would necessarily be 300 baud for reliable operation over all the lines in the system. The 212A standard could also apply (it would be as reliable as the 103 standard because it has a 300-baud FSK backup mode), but a single-chip 212A IC could easily attain ten times the cost of the 300-baud -HC943 because of the IC's much greater die size. A smaller number of applications would derive much benefit from the more expensive 212A IC; applications in which very short blocks of data are transferred would glean the least benefit of all.

For example, if the total number of characters (bytes of data) to be transferred is 60, then the transmission time is 2 sec at 300 baud. Using the 212A standard (1200 baud; full duplex), this time would be reduced to 0.5 sec, for a 1.5-sec savings. This time savings is minimal in terms of billing time. And when you consider the total calling time, this 1.5-sec decreased delay does not make the EFT terminal or credit-verification system appreciably more convenient.

Long-distance dialing with a conventional pulse or rotary system can take as long as 10 sec, while DTMF dialing takes 1 sec. The interoffice switching time from dialing completion to remote ring can be as long as 12 sec. Finally, for every data transmission over the phone system, the FCC requires a 2-sec billing delay before data can be sent. So, the total transmission time can be as long as 18sec with DTMF dialing; 26 sec with pulses. It's now evident why the savings of 1.5 out of 18 or 26 sec does not justify the much greater cost of a 212A system in applications using short blocks of data. For a properly engineered EFT system, a 60-character block of data per transaction in both directions is not unreasonably restrictive.

Finally, there are many other applications that could use the public phone lines to transmit data and that could benefit from the advantages of 1-chip modems. These areas include credit-verification terminals, security systems, acoustic modems, cellular telephones, vending machines, electronic-mail terminals and remote utility-metering devices.

ANATOMY OF A 1-CHIP MODEM

The Bell 103 standard specifies the frequency bands for FSK marks and spaces. If the modem originates the call, it transmits a space as a 1070 Hz; sine wave; a mark is at 1270 Hz. It receives a mark as 2225 Hz and a space as 2025 Hz. Consequently, the answer modem receives marks at 1270 Hz and spaces at 1070 Hz; it transmits them at 2225 and 2025 Hz, respectively. Originate and answer modes are selectable on the -HC943's O/$\overline{A}$ pin (*Figure A*).

The transmission level is set by a resistor to the TLA (transmit-level adjust) pin. The resistor values and attendant transmit levels follow the Universal Service Order Code, as shown in the -HC943's data sheet. Raising the SQT pin produces a squelch, causing the modem's sine-wave synthesizer to assume open 3-state outputs. A squelch action is needed when the modem's line driver is being used to send externally generated dial tones, voice transmission or other signals.

The modem IC also has an analog loopback (ALB) pin that, when taken high, allows input data on pin TXD to come out on the RXD pin after a short delay. Analog loopback is useful as a diagnostic tool. When both SQT and ALB are taken high, the -HC943 goes into its power-down mode—I_{CC} drops to 250 μA and the line-driver's 3-state output assumes the open state.

The -HC943 has an on-chip carrier-detect circuit that signals the reception of an adequate carrier (signal from the modem at the other end of the line). When no carrier is present, the modem's $\overline{CD}$ output assumes a logical One. When a carrier at or above -44 dBm is received, $\overline{CD}$ goes low after a time delay that's controllable by the CDT input.

The carrier-detect trip point then drops 3 dB, providing hysteresis to stabilize the $\overline{CD}$ output. Varying the capacitor on the CDT pin changes the carrier-detect turn-on time delay. This capacitor similarly affects carrier-detect turn-off time. The carrier-detect off-to-on times are set to be longer than the on-to-off times. This means the carrier must be present and stable to be acknowledged; and that if the carrier changes from a stable level to a marginal one, it will be quickly rejected.

The -HC943 offers several advantages over other approaches to modem design. One beneficial feature is the fact that the receive filter, carrier-detect circuit and hybrid function are included on the chip (*Figure A*). This inclusion lowers parts count, saves board space and makes the part easy to design in and use.

The IC is also very economical with power, using only 8 mA when transmitting at -9 dBm. It also includes a power-down mode that reduces I_{CC} to 250 μA. The device operates from one 5V supply; this span gives the modem a typical output transmit range of -9 to -12 dBm. A variation, the -HC942, has an output transmit range of 0 to -12 dBm typ when operating from ± 5V supplies.

The -HC943 performs well in the presence of noise. In tests using the industry-standard C-message-weighted noise injected over a resistive phone-line simulator and with the modem's transmitter sending pseudorandom data, the IC received a 511-bit pseudorandom pattern with a bit-error rate of 10^{-5}, or one error in 10^5 bits sent. These tests were conducted with 4.5-dB signal-to-noise ratio. Further bit-error-rate tests are under way; the results will be published soon.

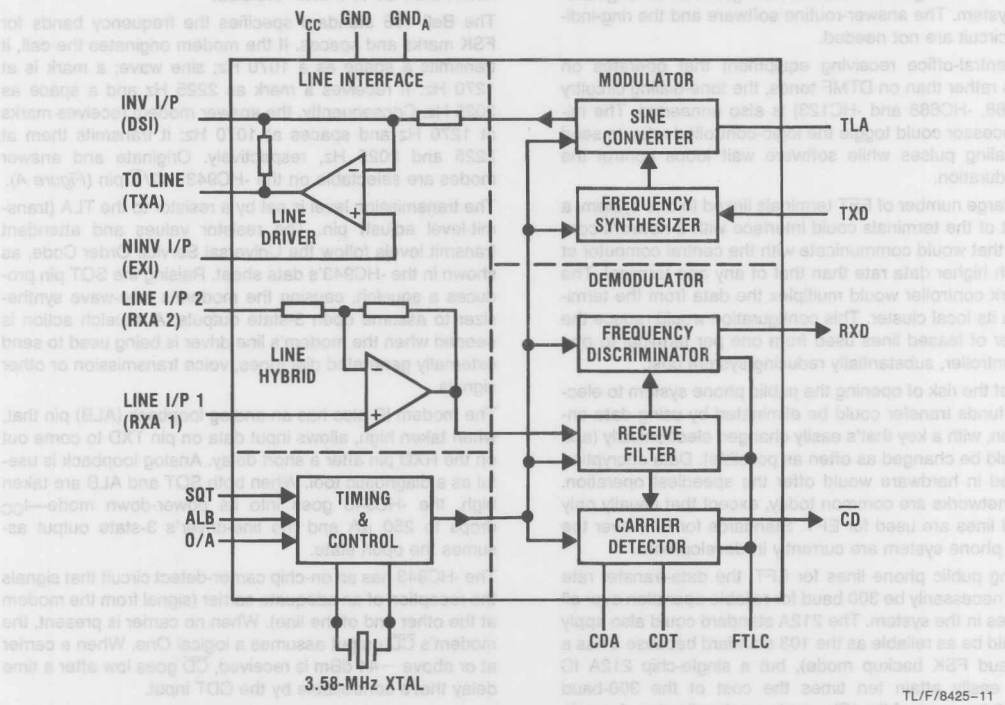


FIGURE A. A 1-chip CMOS modem IC handles 300-baud communications. It generates and receives (and filters) the needed 1070-, 1270-, 2025- and 2225-Hz mark and space signals. Other features include analog loopback, on-chip carrier-detect circuitry, line-interface circuits, and, of course, modulation and demodulation sections. The IC consumes 8 mA in active mode; 250 μA when powered down.

Optimum Hybrid Design

National Semiconductor
Application Note 397
Peter Single

Optimizing the interface between the phone line and a modem can significantly improve modem performance. An increase of 6 dB in transmitted tone rejection can often be achieved. Depending on the modem design this can provide a similar or greater improvement in dynamic range.

The analysis described in this article uses the properties of conformal mappings to produce a solution which is valid for an entire locus of circuits, rather than a single one as is generally the result of circuit analyses.

PART I: PRACTICAL CONSIDERATIONS

Most low speed, full duplex modems use the phone line for transmitting and receiving signals simultaneously. A large part of the circuitry in a Bell 103 modem is devoted to separating the transmitted from the received signals. The telephone line hybrid performs some of this function. By subtracting the transmitted from the received signal some transmitted signal component in the receive path can be eliminated. The receive filter removes much of the remaining transmitted tone but is incapable of removing modulation sidebands and harmonic distortion products of the transmitter. Most receive filters have limited dynamic range specifications, so optimizing the hybrid allows maximum signal to be presented to the receive filter and thus optimizes the overall modem dynamic range.

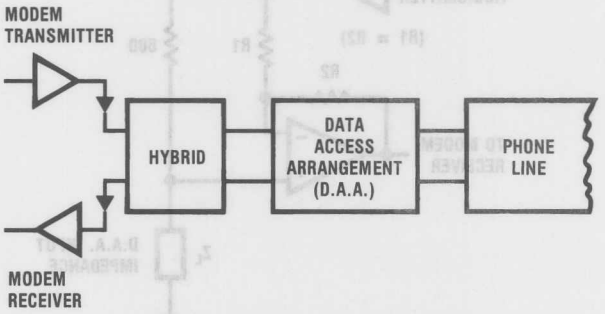
The analysis presented in this article is performed at two frequencies, 1 kHz and 3 kHz. This was done due to the availability of data on the phone line input impedance at these frequencies. The format of the analysis is general, however, and can be applied to any available data.

A block diagram of the phone line, data access arrangement (D.A.A.) and hybrid is shown in *Figure 1.* The D.A.A. provides interfacing between the phone line and the hybrid. A circuit of a typical D.A.A. is shown in *Figure 2.* Many of its components do not affect the A.C. performance of the system, being included to draw line current, provide on/off hook control and perform other similar functions. The hybrid performs two to four wire conversion.

The most common hybrid circuit is shown in *Figure 3.* This circuit is the one used in National Semiconductor's MM74HC942 and MM74HC943 single chip 300 baud modems. Analysis of this circuit reveals it nulls the transmitted signal only for the case where the D.A.A. input impedance is 600Ω. The phone line input impedance, and thus the D.A.A. input impedance varies from line to line, and this ideal case is rare.

By optimizing the hybrid circuit, performance improvements can be achieved. For modems for the consumer market the extra component cost may not justify the performance improvements. For the industrial market however, the performance improvements may outweigh the cost.

The variety of phone line impedances are demonstrated in *Figure 4a.* and *Figure 4b.* As can be seen the impedance varies over a wide range, and 600Ω is not a good approximation of the value. The data for these graphs is from Gresh(2).



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FIGURE 1. Hybrid, D.A.A. and Phone Line

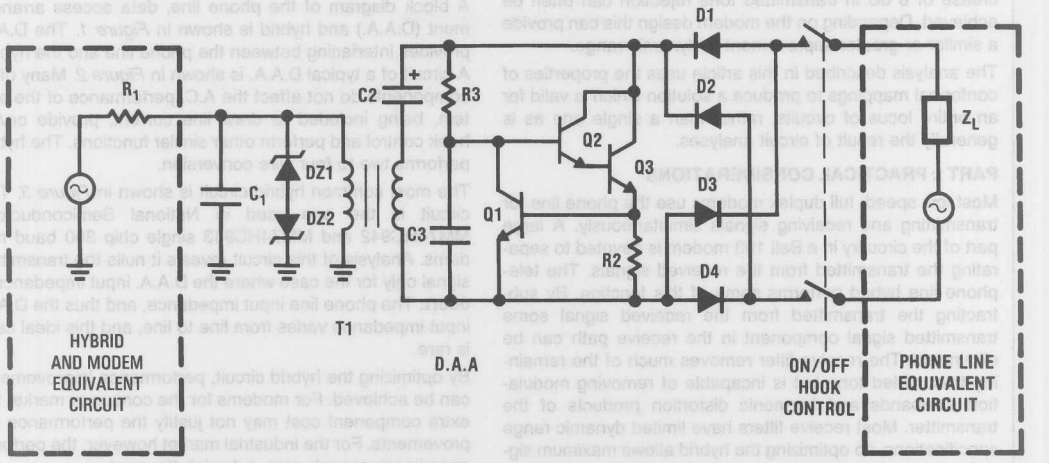


FIGURE 2. D.A.A. Typical Circuit

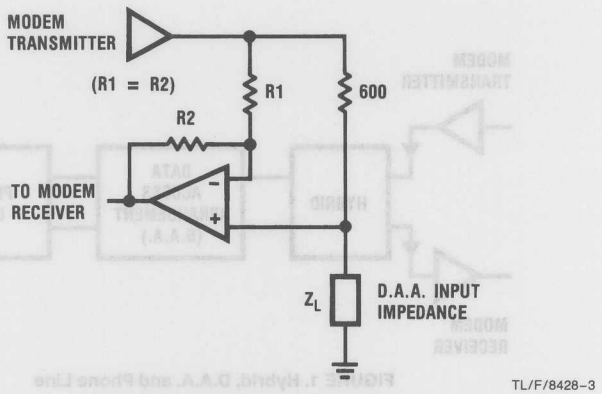


FIGURE 3. Common Hybrid Circuit

Improved Hybrid Topology

A common variation of the circuit of *Figure 3* is to replace R2 with an RC network. This does allow the hybrid to be optimized, but causes the circuit to have a non-flat frequency response from the phone line to the hybrid output. This causes little change in actual performance, but does cause the modem's carrier amplitude detect circuit to trip at different points depending on the mode of the modem (Answer or Originate). This is undesirable.

An improved hybrid circuit is shown in *Figure 5*. This circuit has fixed gain from the phone line to the modem output, and achieves good performance after optimum selection of the components.

This article includes a computer program which optimizes the component values of this circuit. It is possible to use this program without fully understanding the details of its operation, however some of its operation must be understood.

The Hybrid Design Problem

The aim of the hybrid is to minimize the hybrid gain G from the transmitter output to the modem input. Generally, a value Gmax will be chosen that is the maximum tolerable gain. Phase shift does not affect modem performance so the gain G can be a complex number. Thus the modem design goal can be expressed by the equation

$$|G| < Gmax \qquad \text{(Eqn.1)}.$$

Obviously minimizing Gmax would also be a benefit. This equation is the equation of a circle. The range of values of G in complex space is called the "gain space".

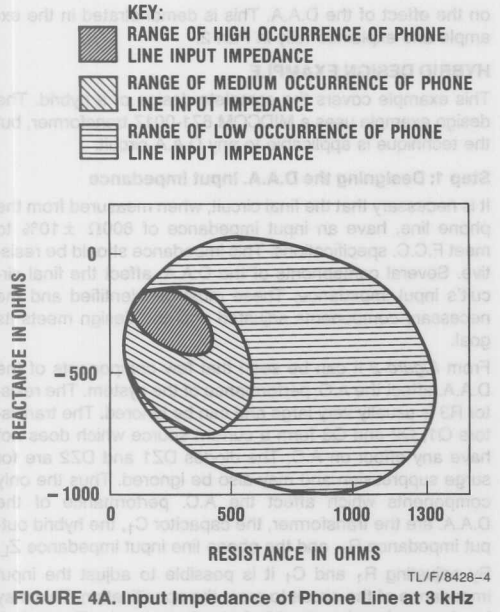


FIGURE 4A. Input Impedance of Phone Line at 3 kHz

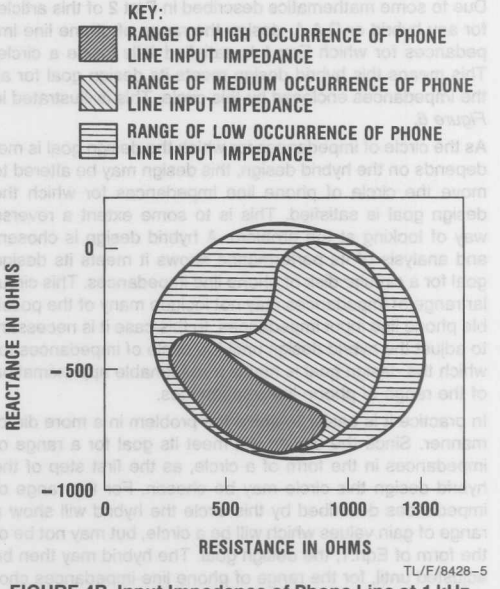


FIGURE 4B. Input Impedance of Phone Line at 1 kHz

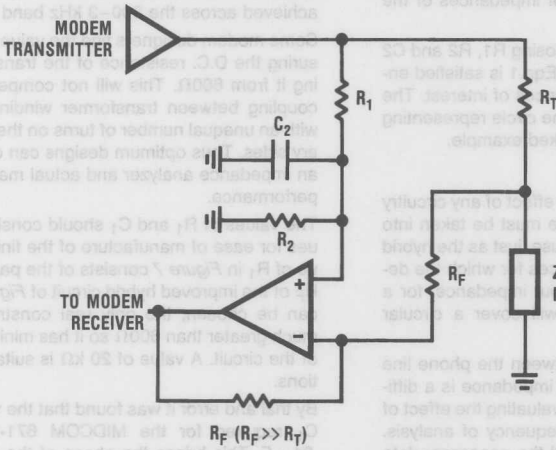


FIGURE 5. Improved Hybrid Topology

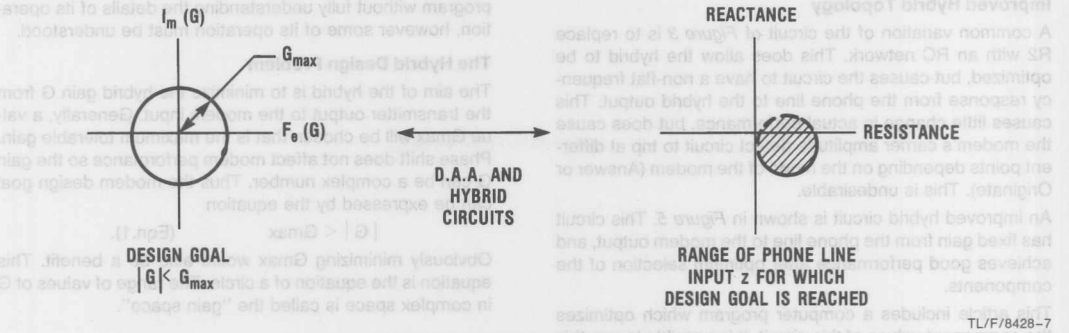


FIGURE 6. Design Solution Space

Due to some mathematics described in Part 2 of this article, for any hybrid or D.A.A. design the range of phone line impedances for which Eqn.1 is satisfied falls inside a circle. This means this hybrid design meets its design goal for all the impedances enclosed by this circle. This is illustrated in *Figure 6.*

As the circle of impedances for which the design goal is met depends on the hybrid design, this design may be altered to move the circle of phone line impedances for which the design goal is satisfied. This is to some extent a reverse way of looking at the problem. A hybrid design is chosen, and analysis of its performance shows it meets its design goal for a circular disk of phone line impedances. This circular range of impedances may not include many of the possible phone line input impedances. In this case it is necessary to adjust the hybrid design until the circle of impedances for which the design goal is met is a reasonable approximation of the range of phone line impedances.

In practice it is easier to solve the problem in a more direct manner. Since the design will meet its goal for a range of impedances in the form of a circle, as the first step of the hybrid design this circle may be chosen. For the range of impedances described by this circle the hybrid will show a range of gain values which will be a circle, but may not be of the form of Eqn.1, the design goal. The hybrid may then be adjusted until, for the range of phone line impedances chosen, the gain is of the form of Eqn.1. At this point the radius of the circle Gmax, is evaluated. This gives the best possible design goal based on the range of impedances of the analysis.

The design problem is thus one of choosing R1, R2 and C2 so the circle of impedances for which Eqn.1 is satisfied encloses the areas of phone line impedances of interest. The constraints applying to the choice of the circle representing the phone line is discussed in the worked example.

The Effect of the D.A.A.

Before the circuit can be optimized the effect of any circuitry between the hybrid and the phone line must be taken into consideration. This is not difficult because, just as the hybrid generated a circular range of impedances for which the design goal was satisfied, the D.A.A. input impedance, for a circular range of load impedances, will cover a circular range.

Understanding exactly the relation between the phone line input impedance and the D.A.A. input impedance is a difficult task. This task is sidestepped by evaluating the effect of the D.A.A. at three points for each frequency of analysis. These points are chosen to provide all the necessary data on the effect of the D.A.A. This is demonstrated in the example and explained fully in Part 2.

HYBRID DESIGN EXAMPLE

This example covers the complete design of a hybrid. The design example uses a MIDCOM 671-0017 transformer, but the technique is applicable to any D.A.A circuit.

Step 1: Designing the D.A.A. Input Impedance

It is necessary that the final circuit, when measured from the phone line, have an input impedance of 600Ω ±10% to meet F.C.C. specifications. This impedance should be resistive. Several components of the D.A.A. affect the final circuit's input impedance. These must be identified and the necessary components adjusted until the design meets its goal.

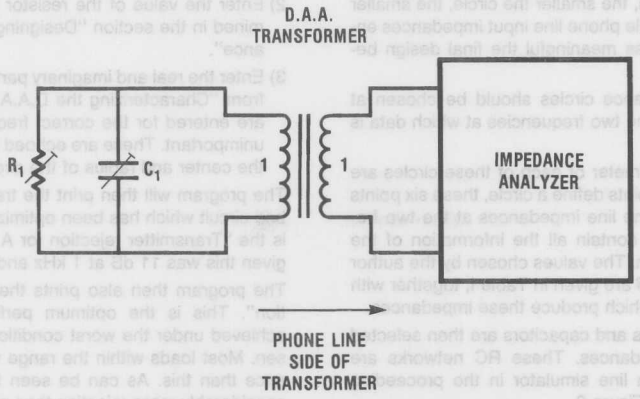
From *Figure 2* it can be seen that few components of the D.A.A. affect the A.C. performance of the system. The resistor R3 is usually very large and can be ignored. The transistors Q1, Q2 and Q3 form a current source which does not have any effect on A.C. The diodes DZ1 and DZ2 are for surge suppression and may also be ignored. Thus the only components which affect the A.C. performance of the D.A.A. are the transformer, the capacitor C_1, the hybrid output impedance R_1, and the phone line input impedance Z_L.

By adjusting R_1 and C_1 it is possible to adjust the input impedance of the circuit to meet the specification. This may be done using the simplified circuit shown in *Figure 7.* It should be done at about 2 kHz so optimum performance is achieved across the 300–3 kHz band of the phone line.

Some modem designers find the value of R_1 simply by measuring the D.C. resistance of the transformer and subtracting it from 600Ω. This will not compensate for incomplete coupling between transformer windings, or a transformer with an unequal number of turns on the primary and secondary sides. Thus optimum designs can only be achieved with an impedance analyzer and actual measurements of circuit performance.

The values of R_1 and C_1 should consist of "preferred" values for ease of manufacture of the finished circuit. The value of R_1 in *Figure 7* consists of the parallel value of R_T and R_F of the improved hybrid circuit of *Figure 5.* At this point R_F can be chosen, the only real constraint being that it be much greater than 600Ω so it has minimal effect on the rest of the circuit. A value of 20 kΩ is suitable for most applications.

By trial and error it was found that the value of the capacitor C_1 required for the MIDCOM 671-0017 transformer is .01 μF. This brings the phase of the transformer input impedance to less than 1 degree. A resistor R_1 of value 601Ω



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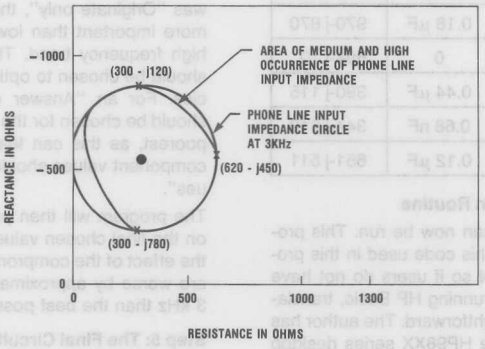
FIGURE 7. Designing D.A.A. Input Impedance

(20k in parallel with 620Ω) gave an input impedance of the network of 603Ω. It could be argued that these adjustments are unnecessary, as a 600Ω resistor and no capacitor will provide an input impedance which is within the F.C.C. specifications. However, some transformers, particulary low quality miniature ones, will cause the final design to fall outside of F.C.C. specifications if these adjustments are not included. They were thus included for completeness.

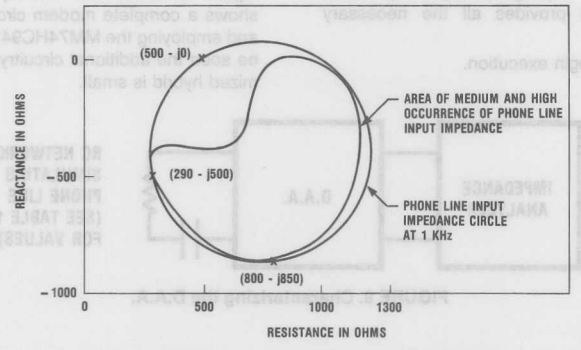
Step 2: Characterizing the Phone Line

The range of impedances seen looking into the phone line must be defined. Since the final circuit works for a circular range of impedances, this range of phone line impedances must be chosen. This is chosen by drawing a circle on a plot of phone line input impedances. This circle is chosen to enclose most values in an efficient manner. This is demonstrated in *Figure 8*.

At this point some engineering discretion must be applied. As a small circle represents a small range of phone line input impedance variation, it is intuitive that an optimized design should have high performance, and the measure of hybrid performance Gmax will be small, indicating high transmitter rejection. Thus the circle chosen should be



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FIGURE 8. Phone Line Input Impedance Circles

small. On the other hand, the smaller the circle, the smaller the percentage of possible phone line input impedances enclosed by it, and the less meaningful the final design becomes.

Phone line input impedance circles should be chosen at both 1 kHz and 3 kHz, the two frequencies at which data is available.

Three points on the perimeter of each of these circles are then chosen. As three points define a circle, these six points define the range of phone line impedances at the two frequencies. These points contain all the information of the circles which were drawn. The values chosen by the author from the data of *Figure 8* are given in Table I, together with R and C combinations which produce these impedances.

Combinations of resistors and capacitors are then selected to simulate these impedances. These RC networks are used as a crude phone line simulator in the proceeding analysis as is shown in *Figure 9*.

Step 3: Characterizing the D.A.A.

The RC networks simulating the phone line are placed on the phone line side of the D.A.A. The input impedance of the D.A.A. is then measured for each RC network at the relevant frequency. This is illustrated in *Figure 9*. The six impedance values measured at this point now completely specify the D.A.A. and phone line. These values are used as inputs for the hybrid optimization program.

TABLE I.

Phone Line and D.A.A. Characterization Impedances

Freq.	Z_{PL}	R	C	Z_{DAA}
1 kHz	290-j 500	290	0.33 μF	419-j 564
1 kHz	800-j 850	800	0.18 μF	970-j 870
1 kHz	500	500	0	594-j 10
3 kHz	300-j 120	300	0.44 μF	390-j 115
3 kHz	300-j 780	300	0.68 nF	344-j 812
3 kHz	620-j 450	620	0.12 μF	651-j 511

Step 4: Running the Optimization Routine

The program included in Part 2 can now be run. This program is written in HP Basic (3). This code used in this program is very similar to FORTRAN so if users do not have access to a machine capable of running HP Basic, translation to FORTRAN should be straightforward. The author has been running the program on the HP98XX series desktop computers. An example of the program output is provided as a guide. The program provides all the necessary prompts. The steps are:

1) Enter the program and begin execution.

2) Enter the value of the resistor R_T of *Figure 5* as determined in the section "Designing the Hybrid Input Impedance".

3) Enter the real and imaginary parts of the 6 measurements from "Characterizing the D.A.A." So long as the values are entered for the correct frequency class the order is unimportant. These are echoed by the program, including the center and radius of the circle defined by them.

The program will then print the transmitter gain for the hybrid circuit which has been optimized for a 600Ω load. This is the "Transmitter rejection for A = 0.25". In the example given this was 11 dB at 1 kHz and only 5 dB at 3 kHz.

The program then also prints the "Best transmitter rejection". This is the optimum performance which can be achieved under the worst conditions within the range chosen. Most loads within the range will show better performance than this. As can be seen from the example this is considerably more rejection than provided by the simple circuit, providing an extra 6 dB at 1 kHz and 7.5 dB at 3 kHz.

The "Optimized A Value" refers to the gain to the non-inverting input of the op-amp for optimum performance.

The "Gain Circle Center" and "Gain Circle Radius" refer to the circle of Eqn.1. These values were calculated inside the program and demonstrate that the final solution has the form of Eqn.1: a circle centered at the origin.

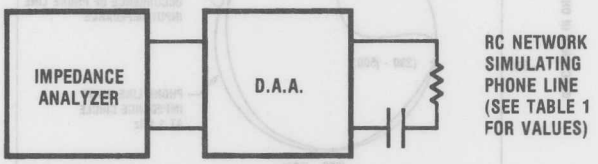
4) Enter a value for R_1 of *Figure 5*. This value is arbitrary, but will affect the final values of R_2 and C_2. 20 kΩ is usually suitable.

The program will then return optimum values of R_2 and C_2 for each frequency. A compromise depending on the actual final design is chosen. For example, suppose the modem was "Originate only", then high frequency performance is more important than low, as the modem receives on the high frequency band. Thus resistor and capacitor values should be chosen to optimize performance at high frequencies. For an "Answer or Originate" modem the values should be chosen for the frequency at which performance is poorest, as this can least be compromised. At this point component values should be rounded off to "preferred values".

The program will then print the actual performance based on the final chosen values. As can be seen in the example the effect of the compromise is not great, as the final values are worse by approximately 2 dB at 1 kHz and 0.2 dB at 3 kHz than the best possible.

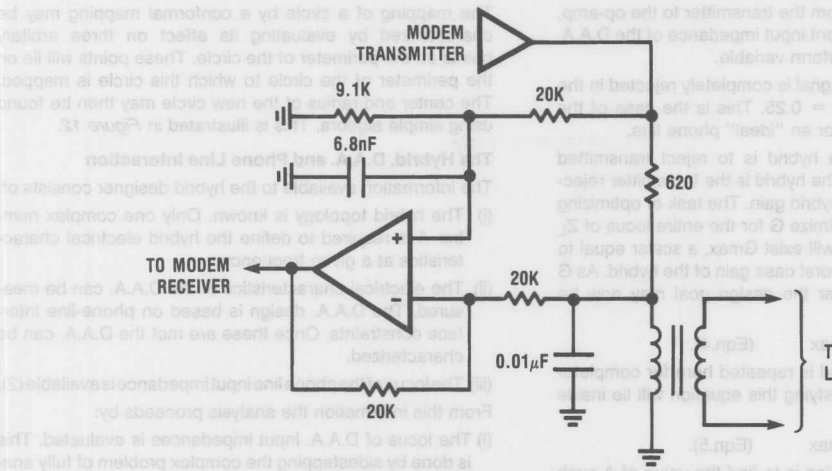
Step 5: The Final Circuit

Figure 10 shows the final hybrid circuit while *Figure 11* shows a complete modem circuit with an optimized hybrid and employing the MM74HC943 single chip modem. As can be seen the additional circuitry required to provide an optimized hybrid is small.



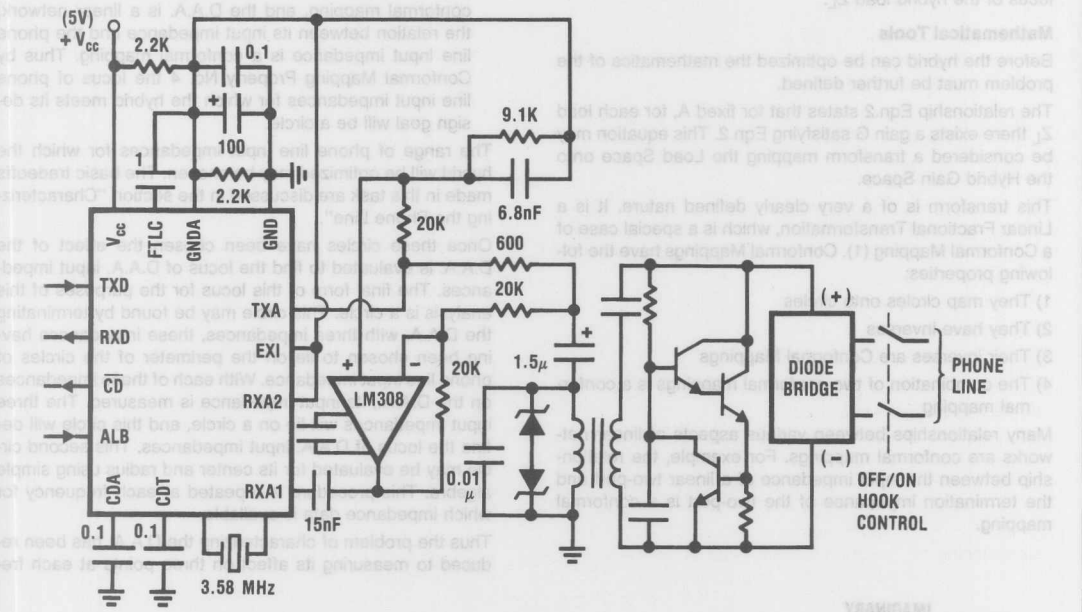
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FIGURE 9. Characterizing the D.A.A.



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FIGURE 10. Optimized Hybrid Circuit



TL/F/8428–13

FIGURE 11. Complete Stand Alone Modem With Optimized Hybrid

PART 2: PROBLEM ANALYSIS

This presents the analysis of the hybrid design problem, and discusses the techniques to optimize the design. The analysis proceeds by first evaluating a performance criterion for a given hybrid design. Then, using a computer program, this performance is optimized.

A block diagram of the functions from the phone line to the modem is shown in *Figure 1*. The analysis of the hybrid optimization problem consists of four parts:

1) Stating the Design Goal

2) Analyzing the Hybrid, D.A.A. and Phone Line Interaction

3) Optimizing the Hybrid Design

4) Realizing the Optimized Hybrid Design

1) The Design Goal

From *Figure 5*, assuming $R_F \gg R_T$ the gain from the transmitter output to the hybrid output is:

$$G = 2.0 \times A - \frac{Z_L}{Z_L + R_T} \quad \text{(Eqn.2)},$$

$$\text{where } A = \frac{R_2}{R_1 + R_2 + sR_1R_2C_2} \quad \text{(Eqn.3)}.$$

is the non-inverting gain from the transmitter to the op-amp, Z_L is the Thevenin equivalent input impedance of the D.A.A. and s is the Laplace Transform variable.

Note that the transmitter signal is completely rejected in the case $R_T = Z_L = 600$, A = 0.25. This is the case of the resistive hybrid designed for an "ideal" phone line.

Since the purpose of the hybrid is to reject transmitted tones, a figure of merit of the hybrid is the transmitter rejection, the reciprocal of the hybrid gain. The task of optimizing the hybird design is to minimize G for the entire locus of Z_L For this locus of Z_L there will exist Gmax, a scalar equal to the absolute value of the worst case gain of the hybrid. As G may be a complex number the design goal may now be written

$$|G| < \text{Gmax} \qquad \text{(Eqn.4)}.$$

(This is Eqn.1 of Part 1 and is repeated here for completeness). The locus of G satisfying this equation will lie inside the circle.

$$|G| = \text{Gmax} \qquad \text{(Eqn.5)}.$$

The goal of the hybrid design is to find the value of A such that Gmax is minimized, and Eqn.4 is satisfied for the entire locus of the hybrid load Z_L.

Mathematical Tools

Before the hybrid can be optimized the mathematics of the problem must be further defined.

The relationship Eqn.2 states that for fixed A, for each load Z_L there exists a gain G satisfying Eqn.2. This equation may be considered a transform mapping the Load Space onto the Hybrid Gain Space.

This transform is of a very clearly defined nature. It is a Linear Fractional Transformation, which is a special case of a Conformal Mapping (1). Conformal Mappings have the following properties:

1) They map circles onto circles
2) They have inverses
3) Their inverses are Conformal Mappings
4) The combination of two conformal mappings is a conformal mapping

Many relationships between various aspects of linear networks are conformal mappings. For example, the relationship between the input impedance of a linear two-port and the termination impedance of the two-port is a conformal mapping.

The mapping of a circle by a conformal mapping may be characterized by evaluating its affect on three arbitary points on the perimeter of the circle. These points will lie on the perimeter of the circle to which this circle is mapped. The center and radius of the new circle may then be found using simple algebra. This is illustrated in *Figure 12*.

The Hybrid, D.A.A. and Phone Line Interaction

The information available to the hybrid designer consists of:

(i) The hybrid topology is known. Only one complex number A is required to define the hybrid electrical characteristics at a given frequency.

(ii) The electrical characteristics of the D.A.A. can be measured. The D.A.A. design is based on phone-line interface constraints. Once these are met the D.A.A. can be characterized.

(iii) The locus of the phone line input impedance is available (2).

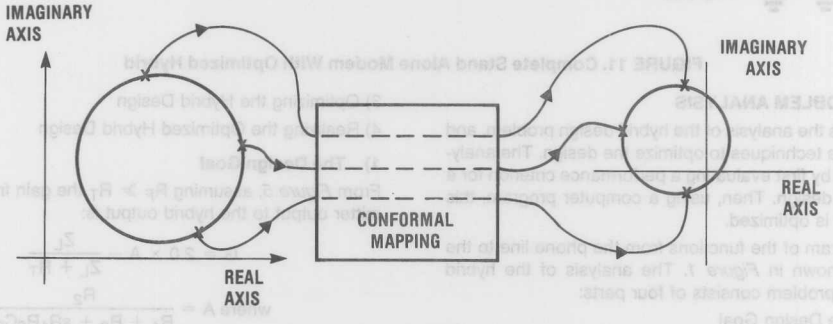
From this information the analysis proceeds by:

(i) The locus of D.A.A. input impedances is evaluated. This is done by sidestepping the complex problem of fully analyzing the D.A.A. The final form of the design goal is in the form of a circle. As the hybrid may be represented by a conformal mapping, and the D.A.A. is a linear network, the relation between its input impedance and the phone line input impedance is a conformal mapping. Thus by Conformal Mapping Property No. 4 the locus of phone line input impedances for which the hybrid meets its design goal will be a circle.

The range of phone line input impedances for which the hybrid will be optimized may be chosen. The basic tradeoffs made in this task are discussed in the section "Characterizing the Phone Line".

Once these circles have been chosen the effect of the D.A.A. is evaluated to find the locus of D.A.A. input impedances. The final form of this locus for the purposes of this analysis is a circle. This circle may be found by terminating the D.A.A. with three impedances, these impedances having been chosen to lie on the perimeter of the circles of phone line input impedance. With each of these impedances on the D.A.A., its input impedance is measured. The three input impedances will lie on a circle, and this circle will define the locus of D.A.A. input impedances. This second circle may be evaluated for its center and radius using simple algebra. This procedure is repeated at each frequency for which impedance data is available.

Thus the problem of characterizing the D.A.A. has been reduced to measuring its affect on three points at each fre-



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FIGURE 12. The Conformal Mapping of a Circle

quency of analysis. These points were carefully chosen to contain all the information necessary for the problem solution so detailed D.A.A. circuit analysis is not necessary.

Maximum Hybrid Gain

Once the circles representing the loci of loads have been defined the maximum hybrid gain may be calculated for the given hybrid parameters. The three points of possible loads defining each load circle are transformed to Gain Space using Eqn.2 and Eqn.3. The three points in Gain Space now define the circle of possible hybrid gain.

Thus the entire range of circuit gains for the entire range of phone line input impedances have been evaluated. This was performed by the two conformal mappings, one from the phone line to the D.A.A. input impedance via the D.A.A. and the second from the D.A.A. input impedance to the hybrid gain via Eqns. 2 and 3.

Once the points defining the circles of possible hybrid gain have been found, they may be solved for their centers and radii. The maximum hybrid gain may be evaluated. By inspection of *Figure 13* the maximum transmit path gain is

$$Gmax = |Cx + jCy| + R \qquad \text{(Eqn.6)}.$$

The analysis thus yields a unique number characterizing the hybrid at each frequency. This number is the worst possible performance for the entire locus of loads selected for the analysis.

Optimizing the Hybrid

As the performance of a hybrid can now be evaluated for any amplifier gain the problem remains to choose the value of A which optimizes hybrid performance. This is done using a simple numerical search algorithm.

First a value of amplifier gain is arbitarily chosen. Four points around this value are then chosen. The distance between the central point and the outer points is arbitrary. The hybrid performance is then evaluated at each of these five points. Based on the behavior at each of these points a search routine may be implemented. This is illustrated in *Figure 14*.

If the best value of A is found to be one of the outer four points, this point is chosen as the central point for another matrix of gain values.

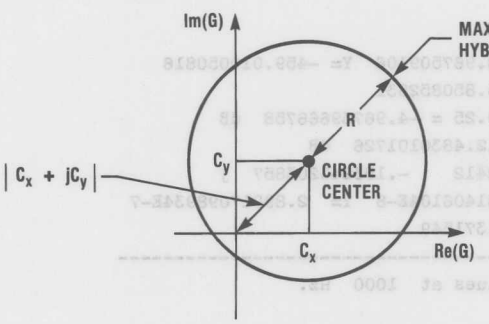
If the best value of A is the central point, the best possible hybrid is inside the area defined by the outer points, so the search increment A_{inc} is halved. This allows greater resolution for the search. The search then continues using the new value of A_{inc}.

This process is repeated until the value of A_{inc} is so small that the optimum value for A is known to be inside a precisely defined area. At this point A is known to within the required accuracy.

Although the optimization routine minimizes Gmax, the final form of the solution is of the form of Eqn.4 and Eqn.5. i.e., the range of hybrid gains for the range of loads is a circle with its center at the origin. Intuitively this is reasonable as the optimum hybrid design will be one that makes most efficient use of the gain space. A proof of this is beyond the scope of this analysis.

Designing the Hybrid

The final problem to be solved is to find a circuit which has the optimum gains A at each of the frequencies of the analysis. The circuit used in Part 1 was found to give sufficient accuracy for engineering purposes. Solving this circuit at one frequency for a necessary gain is straightforward. However, this circuit is not capable of realizing arbitrary gains at each frequency. For this reason a compromise is made. The



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FIGURE 13. The Maximum Hybrid Gain

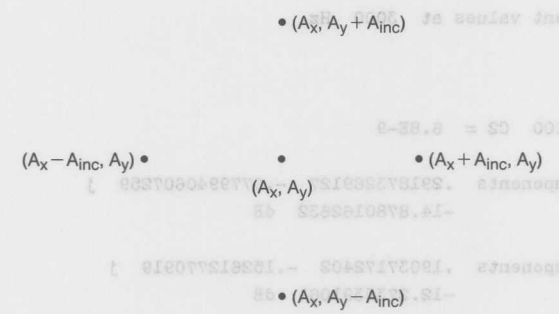


FIGURE 14. Matrix of Points for Numerical Search

circuit components for optimum performance may differ for each frequency. This is due to the complex nature of the phone line input impedance. The circuit performance degradation from choosing fixed values for these components is small as was demonstrated in the example. If desired, a more complex hybrid circuit, capable of realizing the optimum gain at each frequency could be designed. This would not be a difficult task. However, the extra performance may not justify the increased complexity.

Thus, by utilizing a combination of complex number analysis, computer programming and engineering discretion, an apparently intractable problem has been reduced to a simple procedure for optimum hybrid design.

```
          HYBRID OPTIMIZATION ANALYSIS
          ----------------------------
Transformer termination resistance   620
Load circle points at 1 kHz.
 X = 419  Y = -564
 X = 970  Y = -870
 X = 594  Y = -10
Load Circle Center at X= 869.603733515 Y= -401.698832789
Load Circle Radius       478.941952156
Transmitter rejection for A=0.25 = -11.2550722066 dB
Best transmitter rejection -17.19882266 dB
Optimized A value .285309791565  -.0578956604004 j
Gain circle center X= 8.19033644646E-7 Y= -8.34107354335E-7
Gain circle radius    .138055969327
---------------------------------------------------------------
Load circle points at 3 KHz.
 X = 390   Y = -115
 X = 344   Y = -812
 X = 651   Y = -511
Load Circle Center at X=  298.967509106  Y= -459.010050816
Load Circle Radius        355.850852831
Transmitter rejection for A=0.25 = -4.96739666758  dB
Best transmitter rejection -12.4830101726  dB
Optimized A value  .193202972412    -.153240203857  j
Gain circle center X= -7.65881406104E-8  Y=  2.89917098934E-7
Gain circle radius    .237601371549
---------------------------------------------------------------
 Optimum hybrid component values at  1000  Hz.
 R1 =  20000
 R2 =  8451.85356886
 C2 =  5.43598278096E-9
 Optimum hybrid component values at  3000  Hz.
 R1 =  20000
 R2 =  9186.276873
 C2 =  6.6844698044E-9
 Chosen values ; R2= 9100  C2 =  6.8E-9
 At 1 KHz
 A value for chosen components  .291873289127  -.0779940607259  j
 Transmitter rejection          -14.8780162632  dB
At 3 KHz
 A value for chosen components  .19037172402  -.152612770919  j
 Transmitter rejection          -12.2735391061  dB
```

REFERENCES

(1) W. R. Derrick "Introductory Complex Analysis and Applications" Academic Press 1972.

(2) P. A. Gresh "Physical and Transmission Characteristics of Customer Loop Plant" Bell Syst. Tech. Journal, Dec. 1969.

(3) "Basic Language Reference With Extensions 2.0 for the HP Series Desktop Computers", Hewlett Packard Desktop Computer Division, 3404 East Harmony Road, Fort Collins, Colorado 80525.

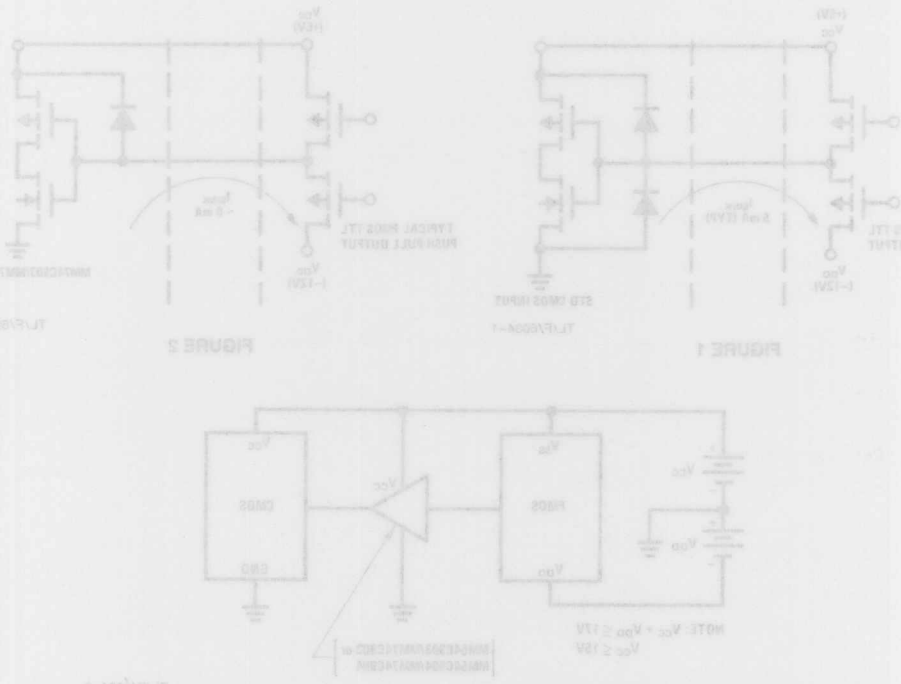
```
100 !                          HYBRID DESIGN PROGRAM
110 !                          ---------------------
120 !                                                P.S. Sept '83
130 !
140 ! This program finds a value of the gain A in the non inverting path of
150 ! a hybrid for optimum operation of the hybrid. The hybrid is optimized
160 ! for an entire locus of loads.
170 !   The locus of loads is assumed to be enclosed by a circle. Three points
180 ! on the perimeter of the circle are used as inputs and these points define
190 ! the circles. This is performed at two frequencies, 1 and 3 kHz.
200 !
210 ! This program is written in HP (Hewlett Packard) Basic 2.0.
220 !   The following variable conventions are used
230 !
240 ! First letter Z : a load point (Z-space)
250 ! First letter A : the gain to the non-inv. input of the op-amp (A-space)
260 ! First letter G : a hybrid gain point (G-space)
270 ! Subscript    x : Real part of a complex variable.
280 ! Subscript    y : Imaginary part of a complex variable.
290 !
300    REAL Ax(3),Ay(3)
310    COM /Z/ REAL Zlx(1:3,1:3),Zly(1:3,1:3),K
320    COM /Circle/ Cx,Cy,R
330    COM /Rtermc/ Rterm
340    !
350    PRINT "          HYBRID OPTIMIZATION ANALYSIS "
360    PRINT "          --------------------------- "
370    !
380    INPUT "Enter transformer termination resistance",Rterm
390    PRINT " "
400    PRINT " Transformer termination resistance",Rterm
410    PRINT " "
420    !
430    ! Read load circle values
440    CALL Readz (Zlx(*),Zly(*),Rterm)
450    !
460 FOR K=1 TO 3 STEP 2 ! Step through two frequencies.
470    PRINT "Load circle points at ";K;" KHz."
480    PRINT " "
490    FOR K3=1 TO 3
500        PRINT " X = ";Zlx(K,K3);" Y ";Zly(K,K3)
510    NEXT K3
520    CALL Cir (Rx,Ry,R,Zlx(K,1),Zly(K,1),Zlx(K,2),Zly(K,2),Zlx(K,3),Zly(K,3))
530    PRINT "Load Circle Center at X= ";Rx;" Y= ";Ry
540    PRINT "Load Circle Radius       ";R
550    PRINT " "
560    CALL Gmax(Gohl,.25,0.,Gohdb)
570    Gohldb=20.*LGT(Gohl)
580    PRINT "Transmitter rejection for A=0.25 = ";Gohdb;" dB"
590    PRINT " "
600    CALL Search (Gmin,Ax(K),Ay(K))
610    CALL Gmax(Goh,Ax(K),Ay(K),Gohdb)
620    PRINT "Best transmitter rejection ";Gohdb;" dB"
```

```
630    PRINT "Optimized A value ";Ax(K);" ";Ay(K);" j"
640    PRINT " "
650    PRINT "Gain circle center X= ";Cx," Y= ";Cy
660    PRINT "Gain circle radius     ";R
670    PRINT "-------------------------------------------------------"
680    PRINT " "
690 NEXT K
700    !
710    CALL Pllrc(Ax(1),Ay(1),Ax(3),Ay(3))
720 END
730   !
740   SUB Search(Gmin,Acenx,Aceny)
750   !
760   ! Search in amplifier gain space (A-space) for
770   ! the amplifier gain constant yielding
780   ! optimum hybrid performance.
790   !   The amplifier gain at this point is
800   ! (Acenx,Aceny) and the hybrid gain is Gmin
810   ! at the worst point.
820   !
830    REAL Gs(1:5),Ax(1:5),Ay(1:5)
840   !
850    Acenx=3. ! Choose arbitrary value to begin search
860    Aceny=0. ! Arbitrary y value
870    Ainc =.5 ! Gain increment: sets size of search area
880   !
890    FOR J=1 TO 1000 ! Dummy loop for search.
900                    Ax(1)=Acenx ! Center of pattern of points
910       Ay(1)=Aceny
920       Ax(2)=Acenx+Ainc  ! These statements
930       Ay(2)=Aceny       ! create the matrix
940       Ax(3)=Acenx-Ainc  ! of points of
950       Ay(3)=Aceny       ! Figure 13.
960       Ax(4)=Acenx       !
970       Ay(4)=Aceny+Ainc  !
980       Ax(5)=Acenx       !
990       Ay(5)=Aceny-Ainc  !
1000      !
1010      FOR K=1 TO 5 ! Evaluate performance at points of matrix
1020        CALL Gmax(Gs(K),Ax(K),Ay(K),Gsdb)
1030      NEXT K
1040      !
1050      Gmin=MIN(Gs(1),Gs(2),Gs(3),Gs(4),Gs(5)) ! Find best point
1060      !
1070      IF (Gmin=Gs(1)) THEN ! Center point is best
1080         IF (Ainc<1.0E-6) THEN Finish ! Search accuracy is 0.K.
1090         Ainc=Ainc/2.0 ! Increase search accuracy
1100         !
1110      ELSE ! Find which point is best
1120         FOR L=2 TO 5 ! Loop thru perimeter points of matrix
1130            IF (Gmin=Gs(L)) THEN ! Best point located
1140               Acenx=Ax(L)
1150               Aceny=Ay(L)
1160            END IF
```

```
1170         NEXT L
1180       END IF
1190     NEXT J
1200 Finish: !
1210 SUBEND
1220   !
1230   !----------------------------------------
1240   !
1250 SUB Gmax(Goh,Ax,Ay,Gohdb)
1260   !
1270   COM /Circle/ Cx,Cy,R
1280   COM /Z/ Zlx(*),Zly(*),Khz
1290   !
1300   ! This sub finds the maximum gain of the hybrid with gain Ax,Ay
1310   ! for the locus of loads defined by Zlxl,Zlyl ...
1320   !
1330    CALL Zltog(Ax,Ay,Zlx(Khz,1),Zly(Khz,1),Gxl,Gyl) ! Find points in Gain
1340    CALL Zltog(Ax,Ay,Zlx(Khz,2),Zly(Khz,2),Gx2,Gy2) ! space for each load
1350    CALL Zltog(Ax,Ay,Zlx(Khz,3),Zly(Khz,3),Gx3,Gy3) ! for given A value.
1360   !
1370    CALL Cir(Cx,Cy,R,Gxl,Gyl,Gx2,Gy2,Gx3,Gy3) ! Find circle in G space
1380    Goh=R+SQR(Cx^2+Cy^2) ! Evaluate maximum gain
1390    Gohdb=20.*LGT(Goh)
1400    !
1410    SUBEND! ------------------------------------------------------------
1420    !
1430    SUB Cir(Cx,Cy,R,Xl,Yl,X2,Y2,X3,Y3)
1440    ! Solves for circle passing thru (Xl,Yl)... for center Cx,Cy and radius R
1450    !
1460    Varl=X2^2-Xl^2+Y2^2-Yl^2
1470    Var2=X3^2-X2^2+Y3^2-Y2^2
1480    Mll=2.*(X2-Xl)
1490    Ml2=2.*(Y2-Yl)
1500    M2l=2.*(X3-X2)
1510    M22=2.*(Y3-Y2)
1520    Mdet=Mll*M22-Ml2*M2l
1530    Cx=(M22*Varl-Ml2*Var2)/Mdet  ! Circle center
1540    Cy=(Mll*Var2-M2l*Varl)/Mdet  ! Circle center
1550    R=SQR((Xl-Cx)^2+(Yl-Cy)^2)  ! Circle radius
1560 SUBEND!----------------------------------------
1570    !
1580 SUB Zltog(Ax,Ay,Zlx,Zly,Gx,Gy)
1590    !
1600    COM /Rtermc/ Rterm
1610    !   This calculates the gain from the transmitter to the hybrid output.
1620    ! Ax and Ay are the real and imaginary parts of the gain to the non-inv
1630    ! input of the op-amp. The value of the line transformer terminating
1640    ! resistor is the variable rterm, passed through common.
1650    !
1660    ! Compute inverting gain
1670    Rden=Zlx+Rterm
1680    Iden=Zly
```

```
1690   Absden=Rden^2+Iden^2
1700   Gxi=(Zlx*(Zlx+Rterm)+Zly^2)/Absden
1710   Gyi=Rterm*Zly/Absden
1720   !
1730   Gx=2.0*Ax-Gxi ! Sum non inverting and inverting
1740   Gy=2.0*Ay-Gyi ! gains
1750 SUBEND!-----------------------------------------------
1760   !
1770   SUB Readz(Zlx(*),Zly(*),Zterm) ! Reads impedance values from user
1780     INPUT "Enter 1 Khz impedance no 1 ",Zlx(1,1),Zly(1,1)
1790     INPUT "Enter 1 Khz impedance no 2 ",Zlx(1,2),Zly(1,2)
1800     INPUT "Enter 1 Khz impedance no 3 ",Zlx(1,3),Zly(1,3)
1810     INPUT "Enter 3 Khz impedance no 1 ",Zlx(3,1),Zly(3,1)
1820     INPUT "Enter 3 Khz impedance no 2 ",Zlx(3,2),Zly(3,2)
1830     INPUT "Enter 3 Khz impedance no 3 ",Zlx(3,3),Zly(3,3)
1840   SUBEND!-----------------------------------------------
1850   !
1860   SUB Pllrc(A1,B1,A3,B3) ! Handles choice of R&C in non-inv. path
1870   !
1880   COM /Z/ Zlx(*),Zly(*),Khz
1890   INPUT " Enter input resistor value",R1
1900   !
1910   CALL Rc(A1,B1,1000.,R1,R2,C2)
1920   CALL Rc(A3,B3,3000.,R1,R2,C2)
1930   !
1940   INPUT " Enter desired values  of  R2,C2 ",R2,C2
1950   PRINT " Chosen values ; R2= ";R2;" C2 = ";C2
1960   FOR Khz=1 TO 3 STEP 2
1970    ! Khz is passed through common
1980    PRINT " "
1990    PRINT "At ";Khz;" KHz"
2000    CALL Eval (R1,R2,C2,1000.*Khz,A,B)
2010   NEXT Khz
2020   !
2030   SUBEND !---------------------------------------------------
2040   !
2050   SUB Rc(A,B,F,R1,R2,C2) ! Finds R2,C2 to give gain A+jB at F Hz.
2060   !
2070   Denom=A^2+B^2
2080   Theta=A/Denom
2090   Phi=-1.0*B/Denom
2100   !
2110   R2=R1/(Theta-1)
2120   C2=Phi/R1/2./PI/F
2130   !
2140   PRINT " "
2150   PRINT " Optimum hybrid component values at ";F;" Hz."
2160   PRINT " R1 = ";R1
```

```
2170    PRINT " R2 = ";R2
2180    PRINT " C2 = ";C2
2190    !
2200    SUBEND !-----------------------------------------------------
2210    !
2220    SUB Eval (R1,R2,C2,F,A,B) ! Evaluates hybrid of R1,R2,C2 at F
2230    !
2240    Theta=R1/R2+1.
2250    Phi=F*2*PI*C2*R1
2260    Denom=Theta^2+Phi^2
2270    A=Theta/Denom
2280    B=-1.0*Phi/Denom
2290    PRINT " A value for chosen components ";A;" ";B;" j"
2300    CALL Gmax(Goh,A,B,Gohdb)
2310    PRINT " Transmitter rejection    ";Gohdb;" dB"
2320    !
2330    SUBEND !-----------------------------------------------------
```



MM54C/MM74C Voltage Translation Buffering

National Semiconductor
Memory Brief 18
John Jorgensen
Thomas P. Redfern

INTRODUCTION

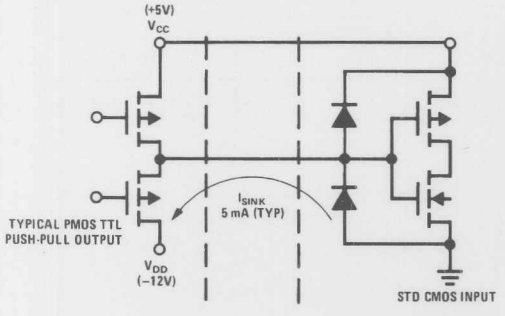
A new series of MM54C/MM74C buffers has been designed to interface systems operating at different voltage levels. In addition to performing voltage translation, the MM54C901/MM74C901 through MM54C904/MM74C904 hex buffers can drive two standard TTL loads at V_{CC} = 5V. This is an increase of ten times over the two LpTTL loads that the standard MM54C/MM74C gate can drive. These new devices greatly increase the flexibility of the MM54C/MM74C family when interfacing to other logic systems.

PMOS TO CMOS INTERFACE

Since most PMOS outputs normally can pull more negative than ground, the conventional CMOS input diode clamp from input to ground poses problems. The least of these is increased power consumption. Even though the output would be clamped at one diode drop (−0.6V), all the current that flows comes from the PMOS negative supply. For TTL compatible PMOS this is −12V. A PMOS output designed to drive one TTL load will typically sink 5 mA. The total power per TTL output is then 5 mA x 12V = 60 mW. The second problem is more serious. Currents of 5 mA or greater from a CMOS input clamp diode can cause four-layer diode action on the CMOS device. This, at best, will totally disrupt normal circuit operation and, at worst, will cause catastrophic failure.

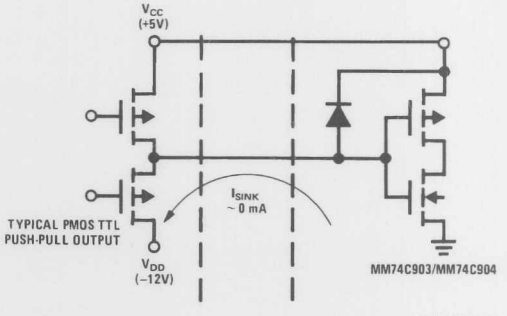
To overcome this problem the MM74C903 and MM74C904 have been designed with a clamp diode from inputs to V_{CC} only. This single diode provides adequate static discharge protection and, at the same time, allows voltages of up to −17V on any input. Since there is essentially no current without the diode, both the high power dissipation and latch up problems are eliminated.

To demonstrate the above characteristics, *Figures 1, 2,* and *3* show typical TTL compatible PMOS circuits driving standard CMOS with two clamp diodes, TTL compatible PMOS driving MM74C903/MM74C904, and the TTL compatible PMOS to CMOS system interface, respectively.



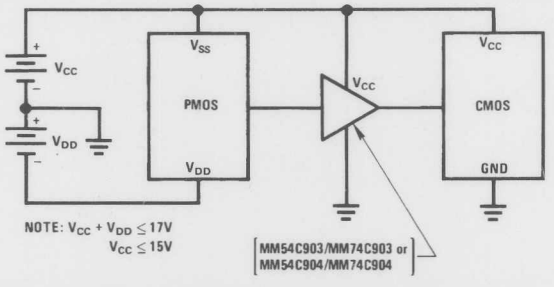
TL/F/6034–1

FIGURE 1



TL/F/6034–2

FIGURE 2

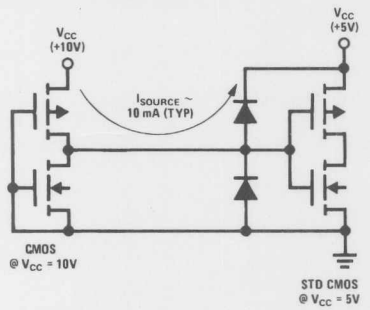


TL/F/6034–3

FIGURE 3. PMOS to CMOS or TTL Interface

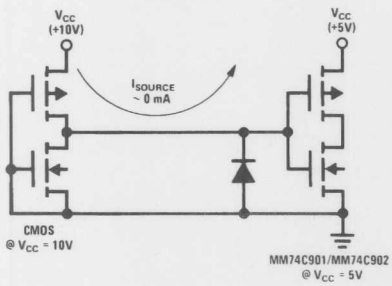
CMOS TO CMOS OR TTL INTERFACE

When a CMOS system which is operating at V_{CC} = 10V must provide signals to a CMOS system whose V_{CC} = 5V, a problem similar to that found in PMOS-to-CMOS interface occurs. That is, current would flow through the upper input diode of the device operating at the lower V_{CC}. This current could be in excess of 10 mA on a typical 74C device, as shown in *Figure 4*. Again, this will cause increased power as well as possible four layer diode action.



TL/F/6034–4

FIGURE 4



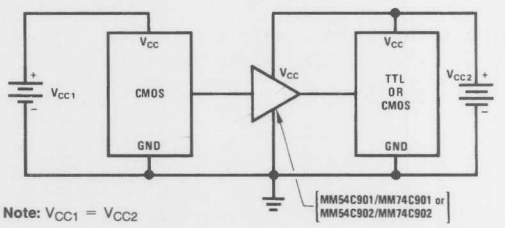
TL/F/6034–5

FIGURE 5

Using the MM74C901 or MM74C902 will eliminate this problem. This occurs simply because these parts are designed with the upper diode removed, as shown in *Figure 5*. With this diode removed the current being sourced goes from about 10 mA to the leakage current of the reverse biased input diode.

Since the MM74C901 and MM74C902 are capable of driving two standard TTL loads with only normal input levels, the output can be used to directly drive TTL. With the example shown, the inputs of the MM74C901 are in excess of 5V. Therefore, they can drive more than two TTL loads. In this case the device would drive four loads with V_{IN} = 10V. If the MM74C902 were used, the output drive would not increase with increased input voltage. This is because the gate of the output n-channel device is always being driven by an internal inverter whose output equals that of V_{CC} of the device.

The example used was for systems of V_{CC} = 10V on one system and V_{CC} = 5V on the second, but the MM74C901 and MM74C902 are capable of using any combination of supplies up to 15V and greater than 3V, as long as V_{CC1} is greater than or equal to V_{CC2} and grounds are common. *Figure 6* diagrams this configuration.

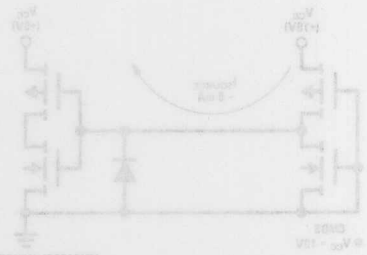


Note: V_{CC1} = V_{CC2}

TL/F/6034–6

FIGURE 6. CMOS to TTL or CMOS at a Lower V_{CC}

The inputs on these devices are adequately protected with the single diode, but, as with all MOS devices, normal care in handling should be observed.



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MM54HC/MM74HC

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National Semiconductor

MM54HC00/MM74HC00 Quad 2-Input NAND Gate

General Description

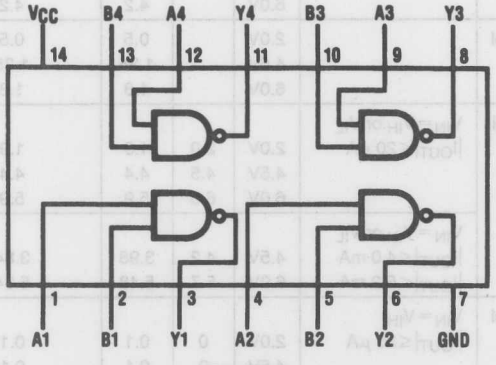
These NAND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

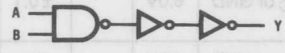


TL/F/5292–1

Top View

Order Number MM54HC00* or MM74HC00*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5292–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

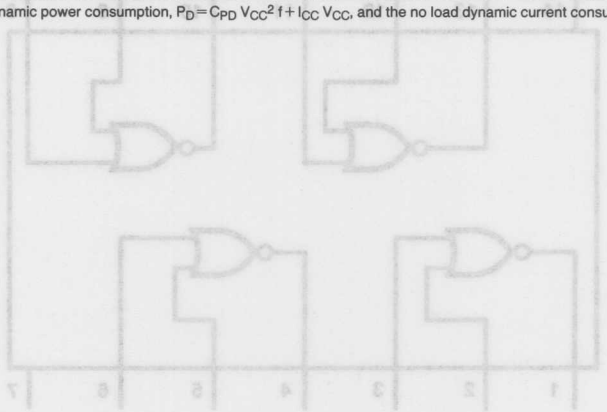
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.





MM54HC02/MM74HC02 Quad 2-Input NOR Gate

General Description

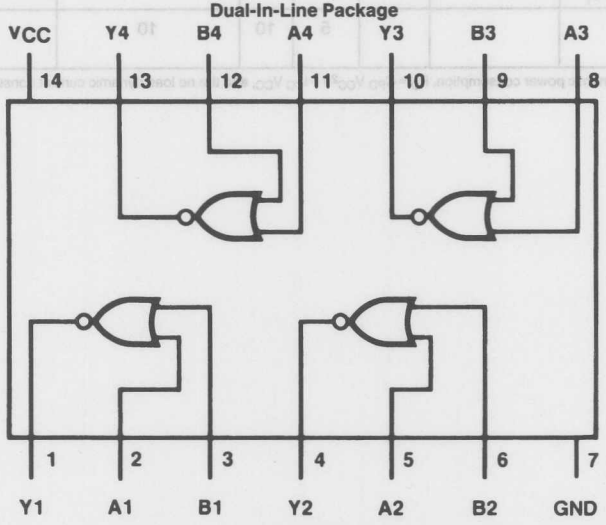
These NOR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5294–1

Top View

Order Number MM54HC02* or MM74HC02*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5294–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

3

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

MM54HC03/MM74HC03 Quad 2-Input Open Drain NAND Gate

General Description

These NAND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

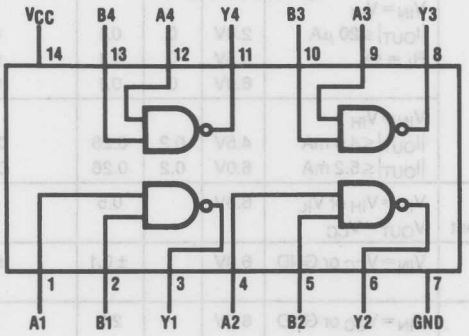
As with standard 54HC/74HC push-pull outputs there are diodes to both V_{CC} and ground. Therefore the output should not be pulled above V_{CC} as it would be clamped to one diode voltage above V_{CC}. This diode is added to enhance electrostatic protection.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

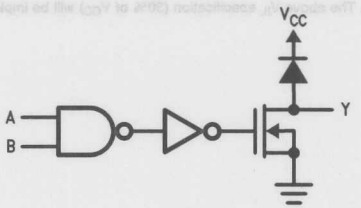


TL/F/5295–1

Top View

Order Number MM54HC03* or MM74HC03*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5295–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \le 20\ \mu A$ $R_L = \infty$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{LKG}	Maximum High Level Output Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}	6.0V		0.5	5	10	μA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

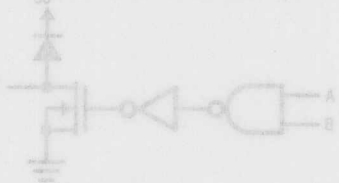
Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.



AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PZL}, t_{PLZ}	Maximum Propagation Delay	$R_L=1$ KΩ	10	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLZ}, t_{PZL}	Maximum Propagation Delay	$R_L=1$ KΩ	2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{THL}	Maximum Output Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$. The power dissipated by R_L is not included.

National Semiconductor

MM54HC04/MM74HC04 Hex Inverter

General Description

These inverters utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

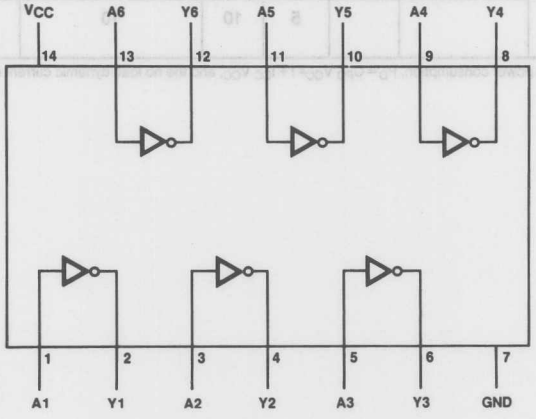
The MM54HC04/MM74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: 10 μW maximum at room temperature
- Low input current: 1 μA maximum

Connection and Logic Diagrams

Dual-In-Line Package



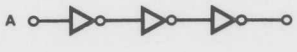
TL/F/5069–1

Top View

Order Number MM54HC04* or MM74HC04*

*Please look into Section 8, Appendix D for availability of various package types.

1 of 6 Inverters



TL/F/5069–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

			Typ	Limit	
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	55	95	120	145	ns
			4.5V	11	19	24	29	ns
			6.0V	9	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HCU04/MM74HCU04 Hex Inverter

General Description

These inverters utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

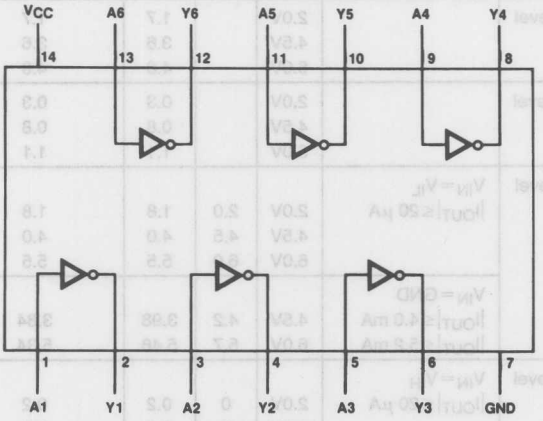
The MM54HCU04/MM74HCU04 is an unbuffered inverter. It has high noise immunity and the ability to drive 15 LS-TTL loads. The 54HCU/74HCU logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns
- Fanout of 15 LS-TTL loads
- Quiescent power consumption: 10 μA maximum at room temperature
- Low input current: 1 μA maximum

Connection and Schematic Diagrams

Dual-In-Line Package

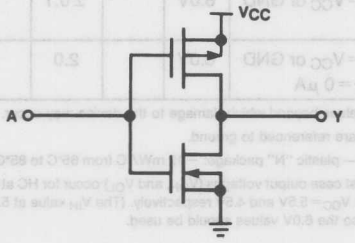


TL/F/5296–1

Top View

Order Number MM54HCU04* or MM74HCU04*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5296–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCU	−40	+85	°C
MM54HCU	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HCU T_A = −40 to 85°C	54HCU T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.7	1.7	V
			4.5V		3.6	3.6	V
			6.0V		4.8	4.8	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.8	0.8	V
			6.0V		1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.8	1.8	V
			4.5V	4.5	4.0	4.0	V
			6.0V	6.0	5.5	5.5	V
		V_{IN} = GND					
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.2	0.2	V
			4.5V	0	0.5	0.5	V
			6.0V	0	0.5	0.5	V
		V_{IN} = V_{CC}					
		$\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

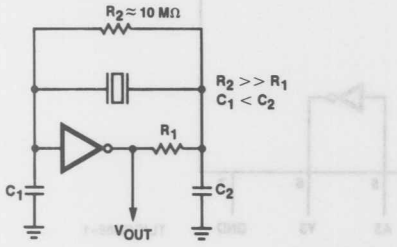
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		7	13	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HCU $T_A=-40$ to $85°C$	54HCU $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	49	82	103	120	ns
			4.5V	9.9	16	21	24	ns
			6.0V	8.4	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		90				pF
C_{IN}	Maximum Input Capacitance			8	15	15	15	pF

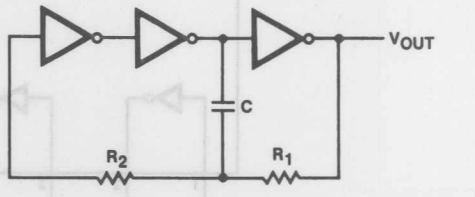
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Typical Applications



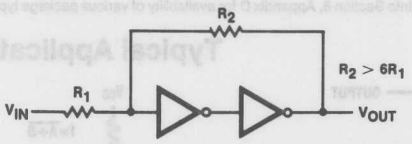
TL/F/5296–3

FIGURE 1. Crystal Oscillator



TL/F/5296–4

FIGURE 2. Stable RC Oscillator



TL/F/5296–5

FIGURE 3. Schmitt Trigger

National Semiconductor

MM54HC05/MM74HC05 Hex Inverter (Open Drain)

General Description

The MM54HC05/MM74HC05 are logic functions fabricated by using advanced silicon-gate CMOS technology, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are also functionally and pin-out compatible with standard DM54LS/DM74LS logic families. The MM54HC05/MM74HC05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

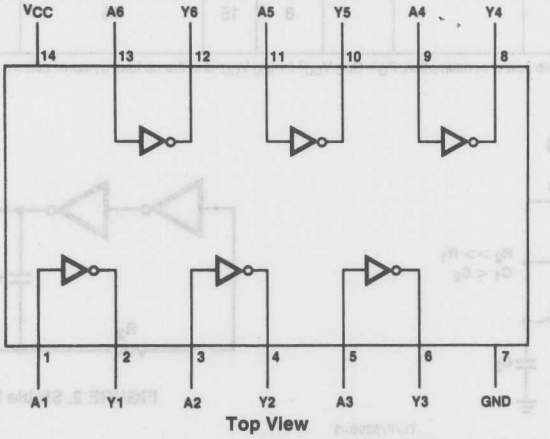
All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

Features

- Open drain for wire-NOR function
- Fanout of 10 LS-TTL loads
- Typical propagation delays:
  t_{PZL} (with 1 kΩ resistor) 8 ns
  t_{PLZ} (with 1 kΩ resistor) 13 ns
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



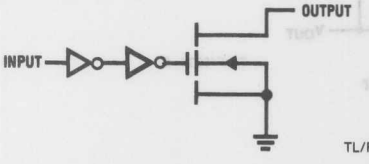
TL/F/9388–1

Top View

Order Number MM54HC05* or MM74HC05*

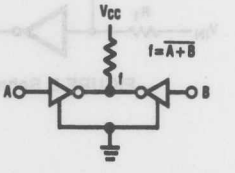
*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



TL/F/9388–2

Typical Application



TL/F/9388–3

Note: Can be extended to more than 2 inputs.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to +85°C	54HC T_A = −55°C to +125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$ $R_L = \infty$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{LKG}	Maximum High Level Output Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}	6.0V		0.5	5	10	μA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PZL}, t_{PLZ}	Maximum Propagation Delay	$R_L = 1\ k\Omega$	8		ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40°C$ to $+85°C$	54HC $T_A = -55°C$ to $+125°C$	Units
				Typ	Guaranteed Limits		
t_{PZL}	Maximum Propagation Delay	$R_L = 1\ k\Omega$	2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{PLZ}	Maximum Propagation Delay	$R_L = 1\ k\Omega$	2.0V	30	90	115	135	ns
			4.5V	13	18	23	27	ns
			6.0V	12	15	20	23	ns
t_{THL}	Maximum Output Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$. The power dissipated by R_L is not included.

National Semiconductor

MM54HC08/MM74HC08 Quad 2-Input AND Gate

General Description

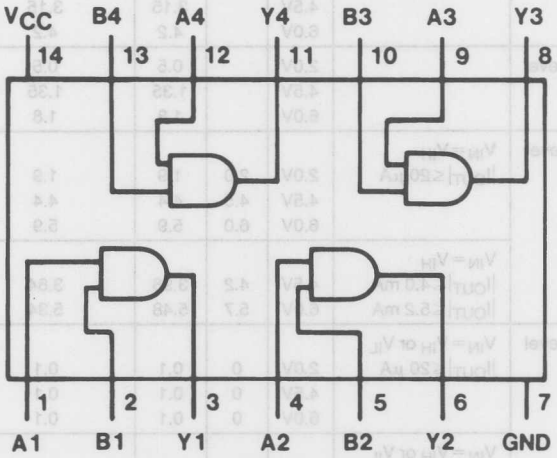
These AND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns (t_{PHL}), 12 ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 2 μA maximum at room temperature
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



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Top View

Order Number MM54HC08 or MM74HC08

*Please look into Section 8, Appendix D for availability of various package types.

3

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

				Limit	
t_{PHL}	Maximum Propagation Delay, Output High to Low		12	20	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		7	15	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay, Output High to Low		2.0V	77	151	175	ns
			4.5V	15	30	35	ns
			6.0V	13	25	30	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		2.0V	30	113	134	ns
			4.5V	10	23	27	ns
			6.0V	8	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	95	110	ns
			4.5V	8	19	22	ns
			6.0V	7	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		38			pF
C_{IN}	Maximum Input Capacitance			4	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HC10/MM74HC10 Triple 3-Input NAND Gate

General Description

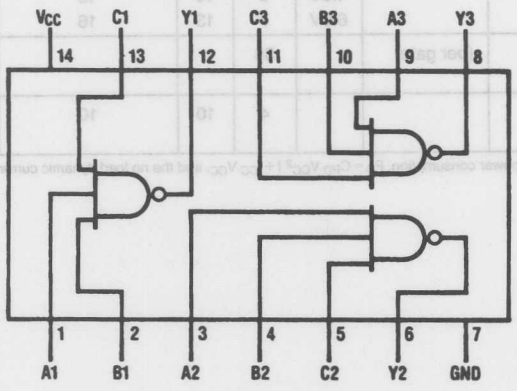
These NAND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

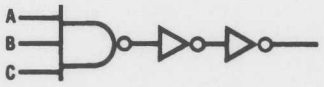


TL/F/5153–1

Top View

Order Number MM54HC10* or MM74HC10*

*Please look into Section 8, Appendix D for availability of various package types.



$Y = \overline{ABC}$

TL/F/5153–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	48	90	113	134	ns
			4.5V	10	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC11/MM74HC11 Triple 3-Input AND Gate

General Description

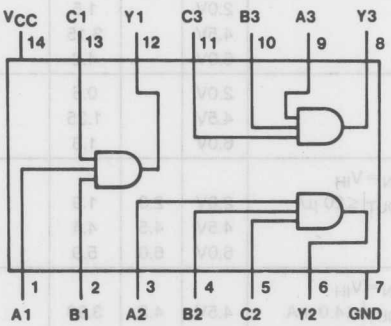
These AND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

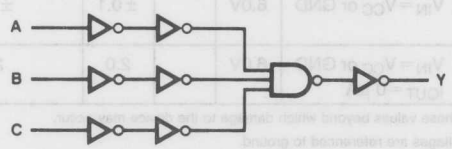


TL/F/5298–1

Top View

Order Number MM54HC11* or MM74HC11*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5298–2

(1 OF 3 GATES)

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

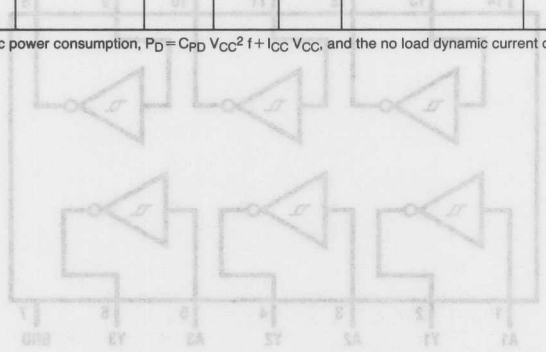
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

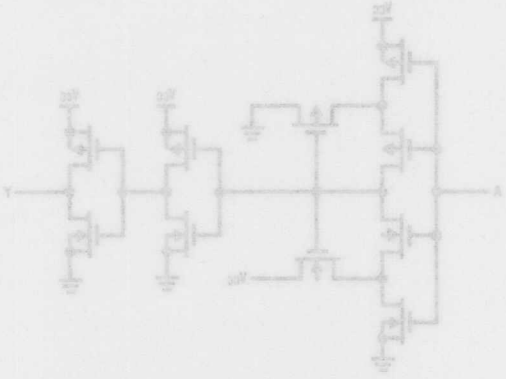
AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC		54HC		Units
					$T_A=-40$ to $85°C$		$T_A=-55$ to $125°C$		
				Typ	Guaranteed Limits				
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	48	125	156		190	ns
			4.5V	18	25	31		38	ns
			6.0V	15	21	27		31	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95		110	ns
			4.5V	8	15	19		22	ns
			6.0V	7	13	16		19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		35					pF
C_{IN}	Maximum Input Capacitance			5	10	10		10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.





3

MM54HC14/MM74HC14
Hex Inverting Schmitt Trigger

General Description

The MM54HC14/MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

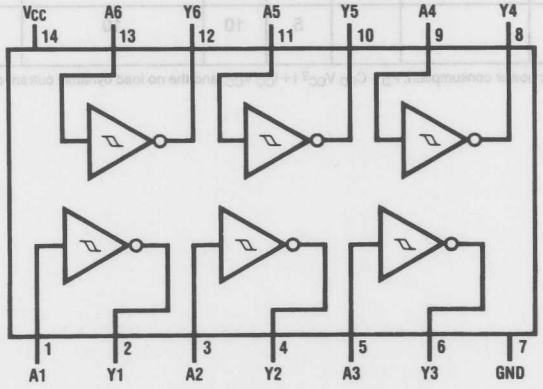
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC}=4.5V

Connection and Schematic Diagrams

Dual-In-Line Package

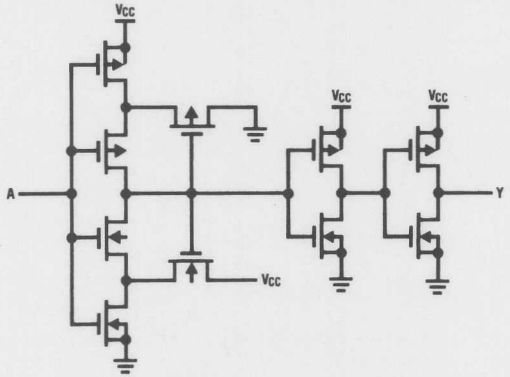


TL/F/5105–1

Top View

Order Number MM54HC14* or MM74HC14*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5105–2

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	V
			4.5V	2.7	2.0	2.0	V
			6.0V	3.2	3.0	3.0	V
		Maximum	2.0V	1.2	1.5	1.5	V
			4.5V	2.7	3.15	3.15	V
			6.0V	3.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage	Minimum	2.0V	0.7	0.3	0.3	V
			4.5V	1.8	0.9	0.9	V
			6.0V	2.2	1.2	1.2	V
		Maximum	2.0V	0.7	1.0	1.0	V
			4.5V	1.8	2.2	2.2	V
			6.0V	2.2	3.0	3.0	V
V_H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	V
			4.5V	0.9	0.4	0.4	V
			6.0V	1.0	0.5	0.5	V
		Maximum	2.0V	0.5	1.0	1.0	V
			4.5V	0.9	1.4	1.4	V
			6.0V	1.0	1.5	1.5	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\lvert I_{OUT}\rvert$ = 20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IL} $\lvert I_{OUT}\rvert$ = 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$ = 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\lvert I_{OUT}\rvert$ = 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\lvert I_{OUT}\rvert$ = 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$ = 5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	22	ns

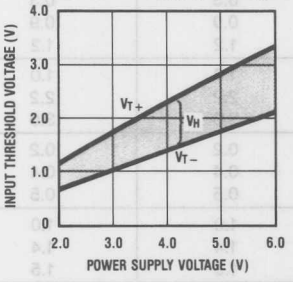
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	11	21	26	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

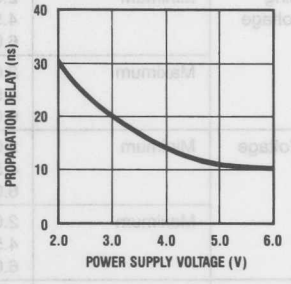
Typical Performance Characteristics

Input Threshold, V_{T+}, V_{T-}, vs Power Supply Voltage



TL/F/5105–3

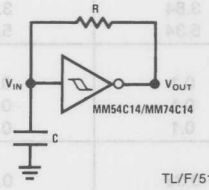
Propagation Delay vs Power Supply



TL/F/5105–4

Typical Applications

Low Power Oscillator

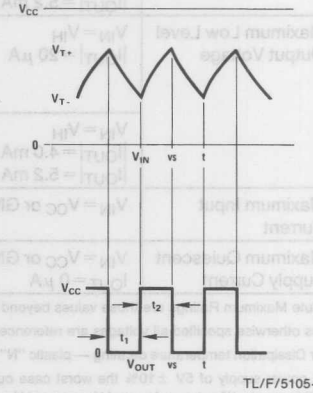


TL/F/5105–5

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC}-V_{T-})}{V_{T-}(V_{CC}-V_{T+})}}$$



TL/F/5105–6

Note: The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$

National Semiconductor

MM54HC20/MM74HC20 Dual 4-Input NAND Gate

General Description

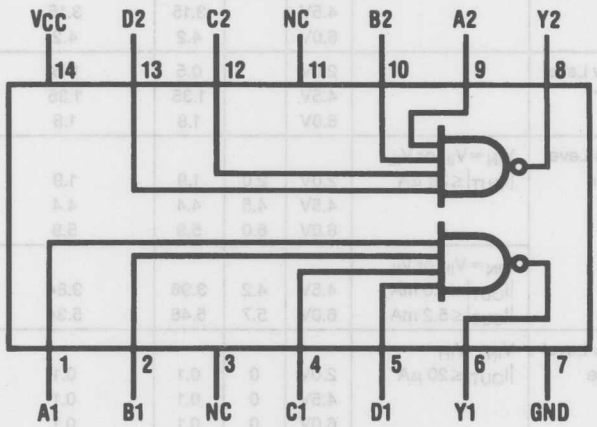
These NAND gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

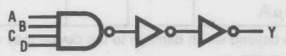


TL/F/5299–1

Top View

Order Number MM54HC20* or MM74HC20*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5299–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH}					
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC27/MM74HC27
Triple 3-Input NOR Gate

General Description

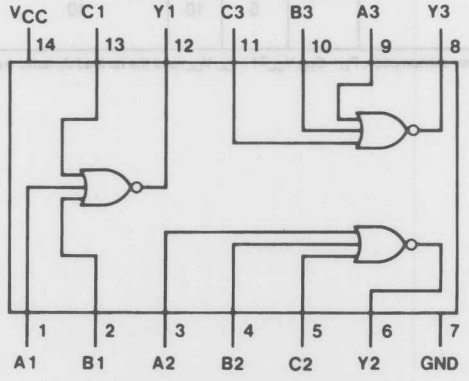
These NOR gates utilize advanced silicon-gate CMOS technology, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide operating supply voltage range: 2–6V
- Low input current: < 1 μA
- Low quiescent supply current: 20 μA maximum (74HC Series)
- Fanout of 10 LS-TTL Loads

Connection and Logic Diagrams

Dual-In-Line Package



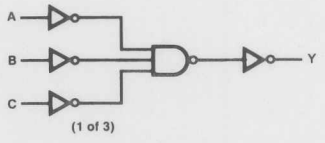
TL/F/5300–1

Top View

Order Number MM54HC27* or MM74HC27*

*Please look into Section 8, Appendix D for availability of various package types.

$$Y = \overline{A + B + C}$$



TL/F/5300–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		36				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

MM54HC30/MM74HC30 8-Input NAND Gate

General Description

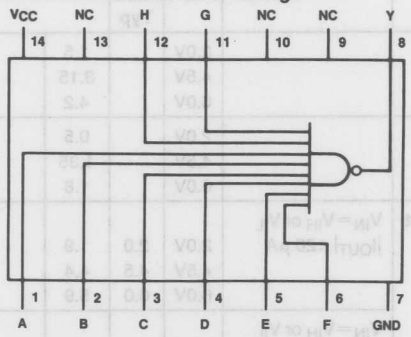
This NAND gate utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. This device has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

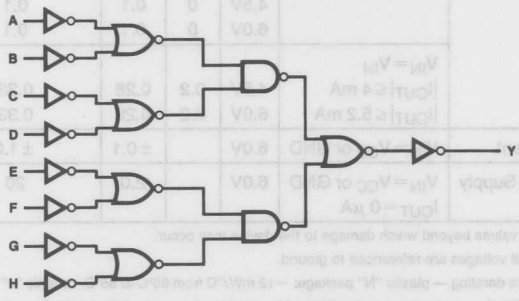


TL/F/5133–1

Top View

Order Number MM54HC30* or MM74HC30*

*Please look into Section 8, Appendix D for availability of various package types.



$Y = ABCDEFGH$

TL/F/5133–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
DC Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$tns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

MM54HC32/MM74HC32
Quad 2-Input OR Gate

General Description

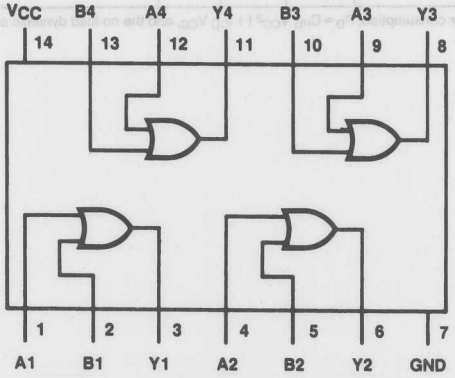
These OR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

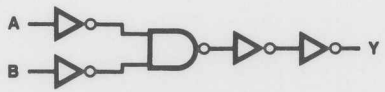


TL/F/5132–1

Top View

Order Number MM54HC32* or MM74HC32*

*Please look into Section 8, Appendix D for availability of various package types.



$Y = A + B$

TL/F/5132–2

(1 of 4)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.7	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC34/MM74HC34 Non-Inverter

General Description

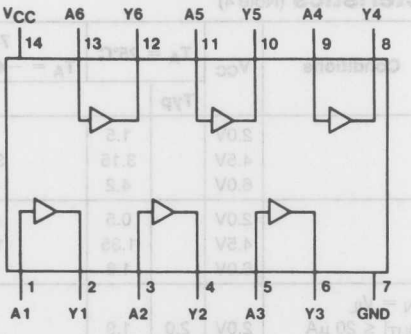
The MM54HC34/MM74HC34 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range, but are functionally as well as pin-out compatible with standard DM54LS/74LS devices. The MM54HC34/MM74HC34 feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

Features

- Fast switching: t_{PLH}, t_{PHL} = 10 ns (typ)
- High fanout: ≥ 10 LS loads

Connection Diagram

Dual-In-Line Package



TL/F/9389–1

Top View

Order Number MM54HC34* or MM74HC34*

*Please look into Section 8, Appendix D for availability of various package types.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{ICC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

(V_{IN}, V_{OUT})			
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to +85°C	54HC T_A = −55 to +125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7 V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN} = V_{IH} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4 V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40 μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C, ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC} and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

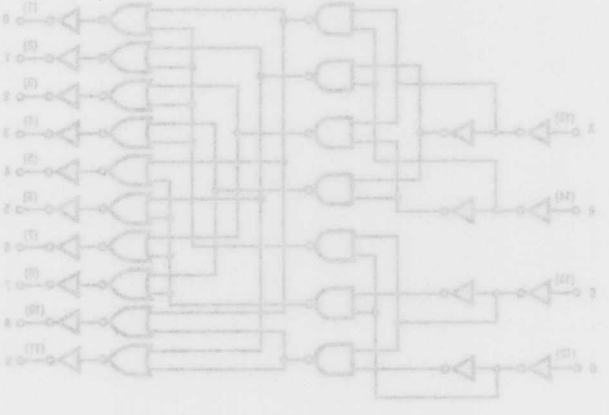
AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10		ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40°C to +85°C	54HC T_A = −55°C to +125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Minimum Propagation Delay		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	17	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	50	75	95	110	ns
			4.5V	10	75	19	22	ns
			6.0V	8	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		26				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



National Semiconductor

MM54HC42/MM74HC42 BCD-to-Decimal Decoder

General Description

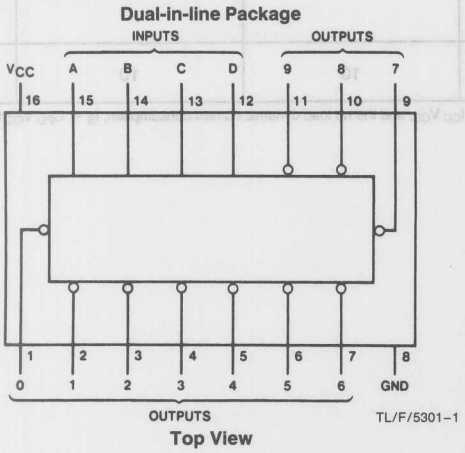
This decoder utilizes advanced silicon-gate CMOS technology. Data on the four input pins select one of the 10 outputs corresponding to the value of the BCD number on the inputs. An output will go low when selected, otherwise it remains high. If the input data is not a valid BCD number all outputs will remain high. The circuit has high noise immunity and low power consumption usually associated with CMOS circuitry, yet also has speeds comparable to low power Schottky TTL (LS-TTL) circuits, and is capable of driving 10 LS-TTL equivalent loads.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide supply range: 2V–6V
- Low quiescent current: 80 μA (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagram



Top View

Order Number MM54HC42* or MM74HC42*

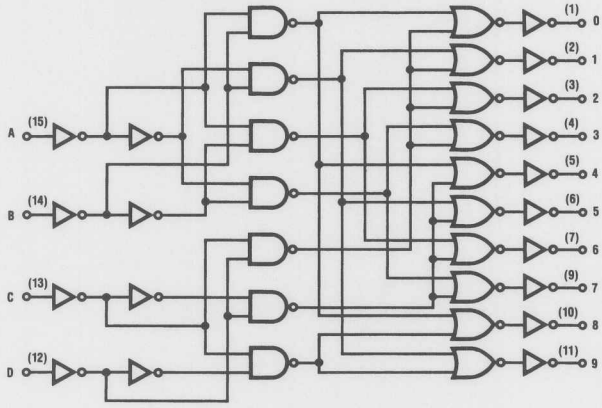
*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level

Logic Diagram



TL/F/5301–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		15	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	75	150	189	224	ns
			4.5V	17	30	38	45	ns
			6.0V	15	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		62				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC51/MM74HC51 Dual AND-OR-Invert Gate
MM54HC58/MM74HC58 Dual AND-OR Gate

General Description

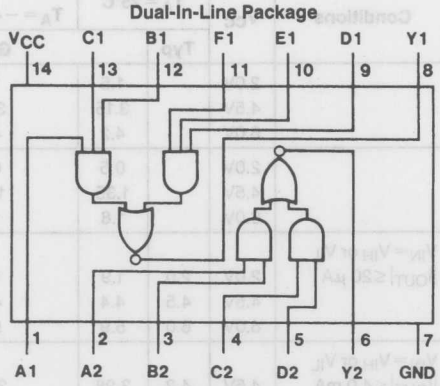
These gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74 Series)
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection Diagrams

Dual-In-Line Package

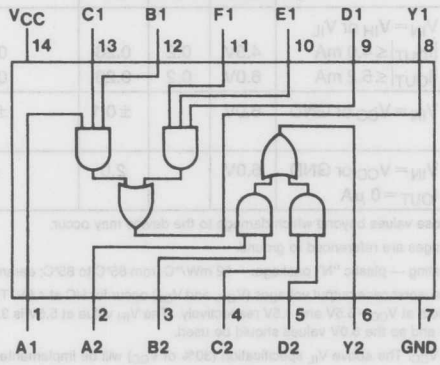


TL/F/5302–1

Top View

Order Number MM54HC51* or MM74HC51*

Dual-In-Line Package



TL/F/5302–2

Top View

Order Number MM54HC58* or MM74HC58*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

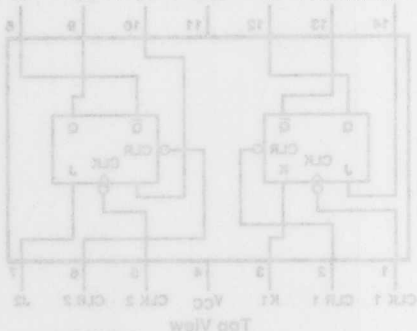
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

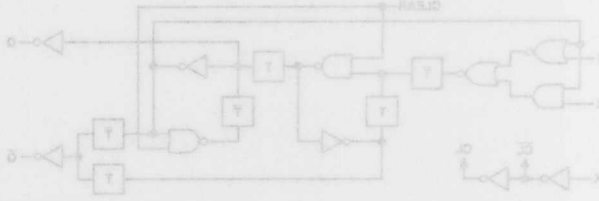
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per AND-OR-Gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.





MM54HC73/MM74HC73
Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent, J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family.

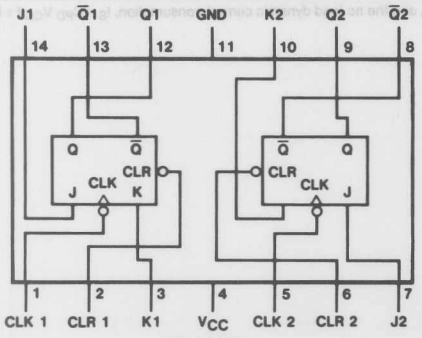
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC Series)
- High output drive: 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



Top View

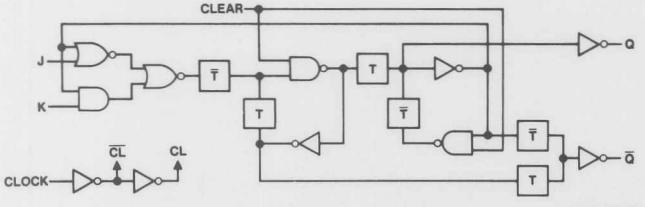
TL/F/5072–1

Order Number MM54HC73* or MM74HC73*

*Please look into Section 8, Appendix D for availability of various package types.

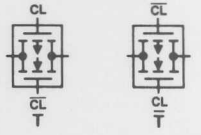
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



TL/F/5072–2

(1 of 2)



TL/F/5072–3

Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Setup Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

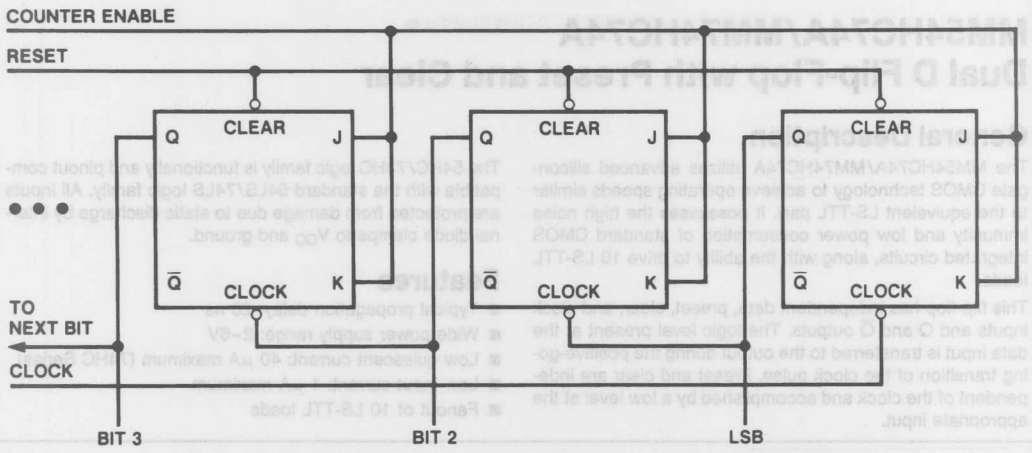
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	70	126	160	185	ns
			4.5V	18	25	32	37	ns
			6.0V	15	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	194	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	32	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15.4	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

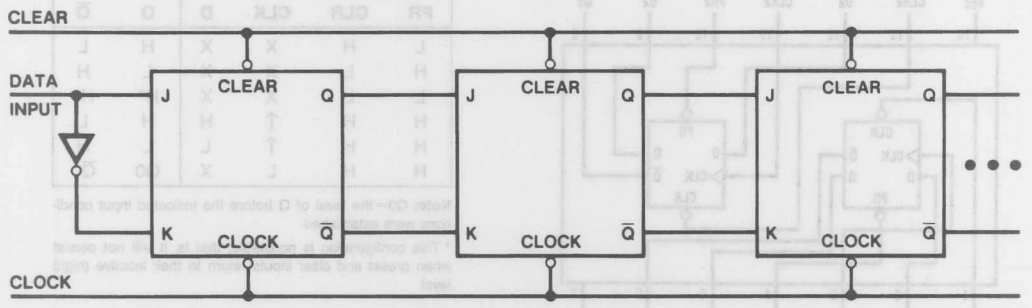
Typical Applications

N Bit Binary Ripple Counter with Enable and Reset



TL/F/5072–4

N Bit Shift Register with Clear



TL/F/5072–5

National Semiconductor

MM54HC74A/MM74HC74A
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HC74A/MM74HC74A utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

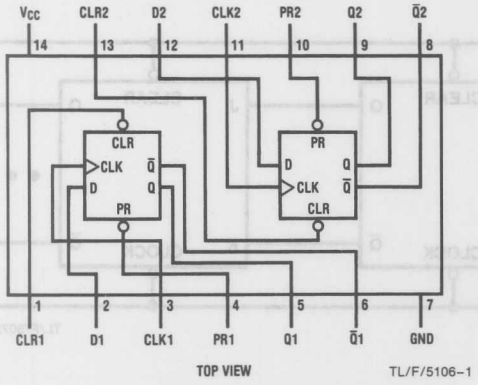
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TOP VIEW

TL/F/5106–1

Order Number MM54HC74A* or MM74HC74A*

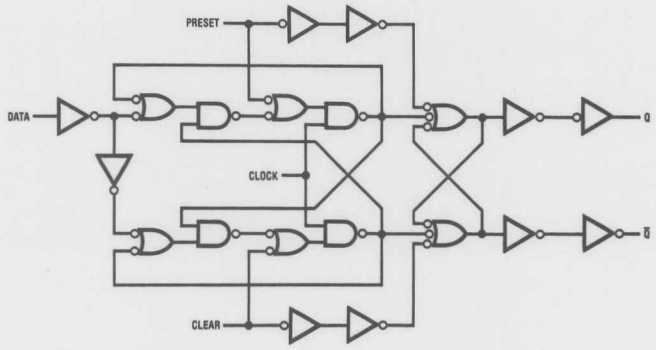
*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



TL/F/5106–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.3	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		72	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		10	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$		17	40	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		6	5	ns
t_s	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	22	6	5	4	MHz
			4.5V	72	30	24	20	MHz
			6.0V	94	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	34	110	140	165	ns
			4.5V	12	22	28	33	ns
			6.0V	10	19	24	28	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear To Q or $\overline{Q}$		2.0V	66	150	190	225	ns
			4.5V	20	30	38	45	ns
			6.0V	16	26	33	38	ns
t_{REM}	Minimum Removal Time Preset or Clear To Clock		2.0V	20	50	65	75	ns
			4.5V	6	10	13	15	ns
			6.0V	5	9	11	13	ns
t_s	Minimum Setup Time Data to Clock		2.0V	35	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	17	20	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum, Pulse Width Clock, Preset or Clear		2.0V	30	80	101	119	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC75/MM74HC75
4-Bit Bistable Latch with Q and $\overline{Q}$ Output

General Description

This 4-bit latch utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption normally associated with standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

This latch is ideally suited for use as temporary storage for binary information processing, input/output, and indicator units. Information present at the data (D) input is transferred to the Q output when the enable (G) is high. The Q output will follow the data input as long as the enable remains high. When the enable goes low, the information that was present at the data input at the time the transition occurred is retained at the Q output until the enable is permitted to go high again.

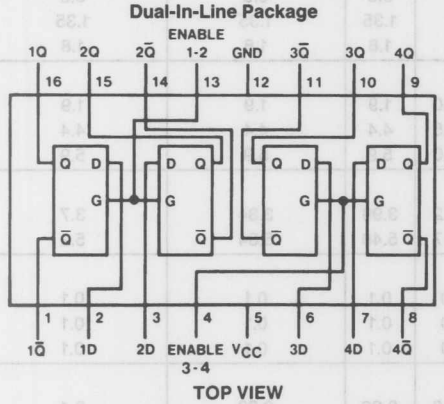
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 12 ns
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TOP VIEW

TL/F/5303–1

Order Number MM54HC75* or MM74HC75*

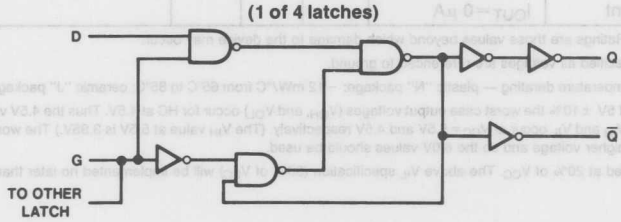
*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level; L = Low Level
X = Don't Care
Q_0 = The level of Q before the transition of G

(1 of 4 latches)



TL/F/5303–2

DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5$V
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5$V
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	-65°C to $+150$°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Temp. Range (T_A)			
MM74HC	-40	$+85$	°C
MM54HC	-55	$+125$	°C
Input Rise or Fall Times			
(t_r, t_f) $V_{CC}=2.0$V		1000	ns
$V_{CC}=4.5$V		500	ns
$V_{CC}=6.0$V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25$°C	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20$ μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0$ μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ± 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5$V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		14	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		10	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		16	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		11	23	ns
t_S	Minimum Set Up Time			20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		2.0V	37	125	156	188	ns
			4.5V	15	25	32	38	ns
			6.0V	14	24	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		2.0V	29	110	138	165	ns
			4.5V	12	22	28	33	ns
			6.0V	11	19	24	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		2.0V	40	145	181	218	ns
			4.5V	18	29	36	44	ns
			6.0V	16	25	31	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		2.0V	36	125	156	188	ns
			4.5V	15	25	31	38	ns
			6.0V	14	22	28	33	ns
t_S	Minimum Set Up Time Data to Enable		2.0V	40	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Enable to Data		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_W	Minimum Enable Pulse Width		2.0V	40	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per commonly clocked latched pair)		40				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC76/MM74HC76 Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize advanced silicon-gate CMOS technology to achieve, the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

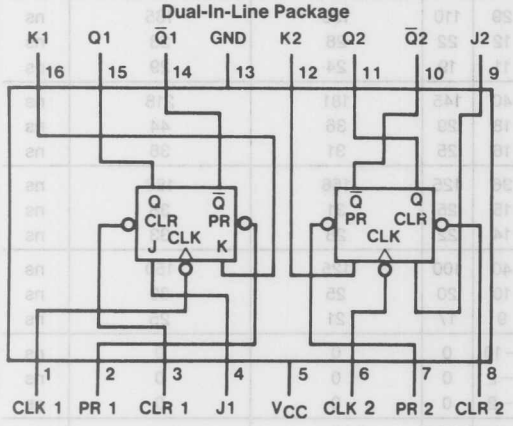
Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC Series)
- High output drive: 10 LS-TTL loads

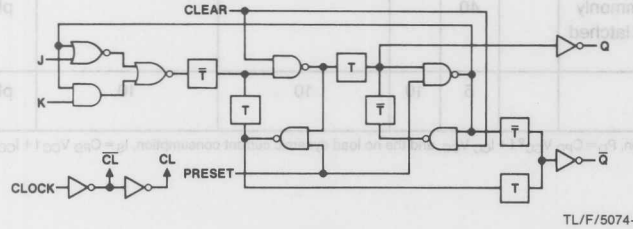
Connection and Logic Diagrams

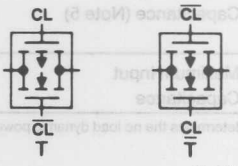


Top View

Order Number MM54HC76* or MM74HC76*

*Please look into Section 8, Appendix D for availability of various package types.





Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed

(1 of 2)

DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5$
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5$
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 50 mA
Storage Temperature Range (T_{STG})	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

(V_{IN}, V_{OUT})			
Operating Temp. Range (T_A)			
MM74HC	-40	$+85$	°C
MM54HC	-55	$+125$	°C
Input Rise or Fall Times			
(t_r, t_f) $V_{CC}=2.0V$		1000	ns
$V_{CC}=4.5V$		500	ns
$V_{CC}=6.0V$		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time		10	20	ns
t_s	Minimum Setup Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width Preset, Clear or Clock		10	16	ns

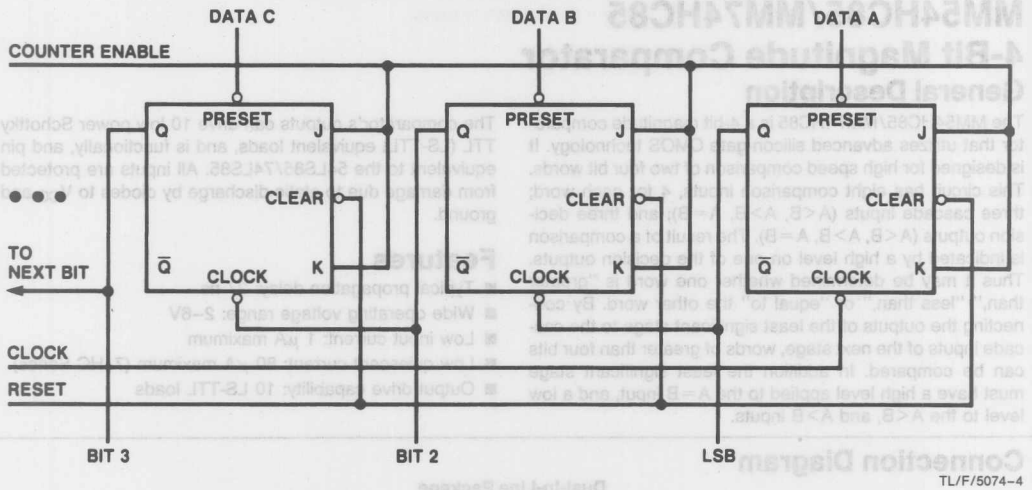
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	100	126	160	183	ns
			4.5V	20	25	31	37	ns
			6.0V	17	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	191	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	33	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V	137	165	210	240	ns
			4.5V	27	33	41	50	ns
			6.0V	23	28	35	40	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_s	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum, Pulse Width, Preset, Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

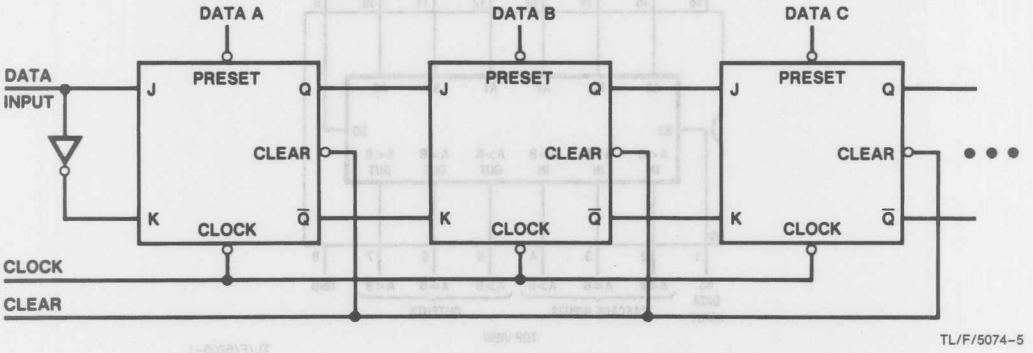
Typical Applications

N Bit Presettable Ripple Counter with Enable and Reset



TL/F/5074–4

N Bit Parallel Load/Serial Load Shift Register with Clear



TL/F/5074–5

3

National Semiconductor

MM54HC85/MM74HC85
4-Bit Magnitude Comparator

General Description

The MM54HC85/MM74HC85 is a 4-bit magnitude comparator that utilizes advanced silicon-gate CMOS technology. It is designed for high speed comparison of two four bit words. This circuit has eight comparison inputs, 4 for each word; three cascade inputs (A<B, A>B, A=B); and three decision outputs (A<B, A>B, A=B). The result of a comparison is indicated by a high level on one of the decision outputs. Thus it may be determined whether one word is "greater than," "less than," or "equal to" the other word. By connecting the outputs of the least significant stage to the cascade inputs of the next stage, words of greater than four bits can be compared. In addition the least significant stage must have a high level applied to the A=B input, and a low level to the A<B, and A>B inputs.

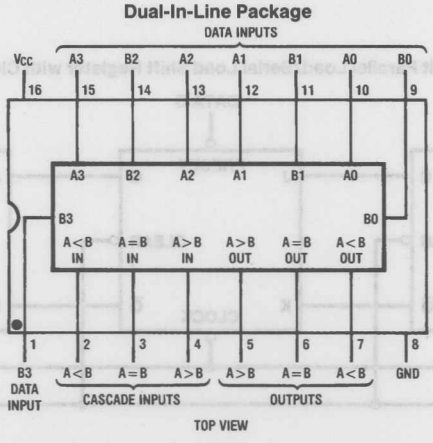
The comparator's outputs can drive 10 low power Schottky TTL (LS-TTL) equivalent loads, and is functionally, and pin equivalent to the 54LS85/74LS85. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 27 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5205–1

Order Number MM54HC85* or MM74HC85*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7 V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4 V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160 μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

t_{PHL}, t_{PLH}	Maximum Propagation Delay A = B Input to A = B Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output		13	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A = B		20	30	ns

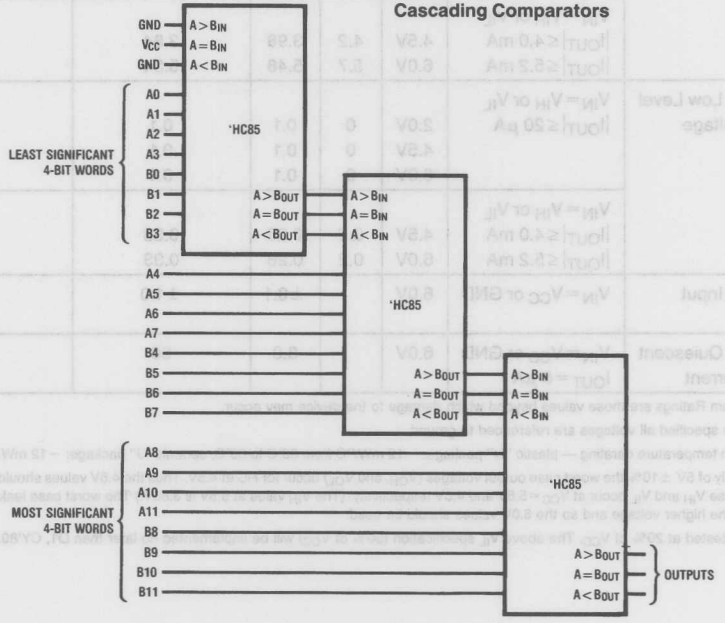
AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to Output		2.0V	100	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A = B Output		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A = B Input to A = B Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output (except A = B)		2.0V	70	155	195	231	ns
			4.5V	16	31	39	46	ns
			6.0V	13	26	33	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

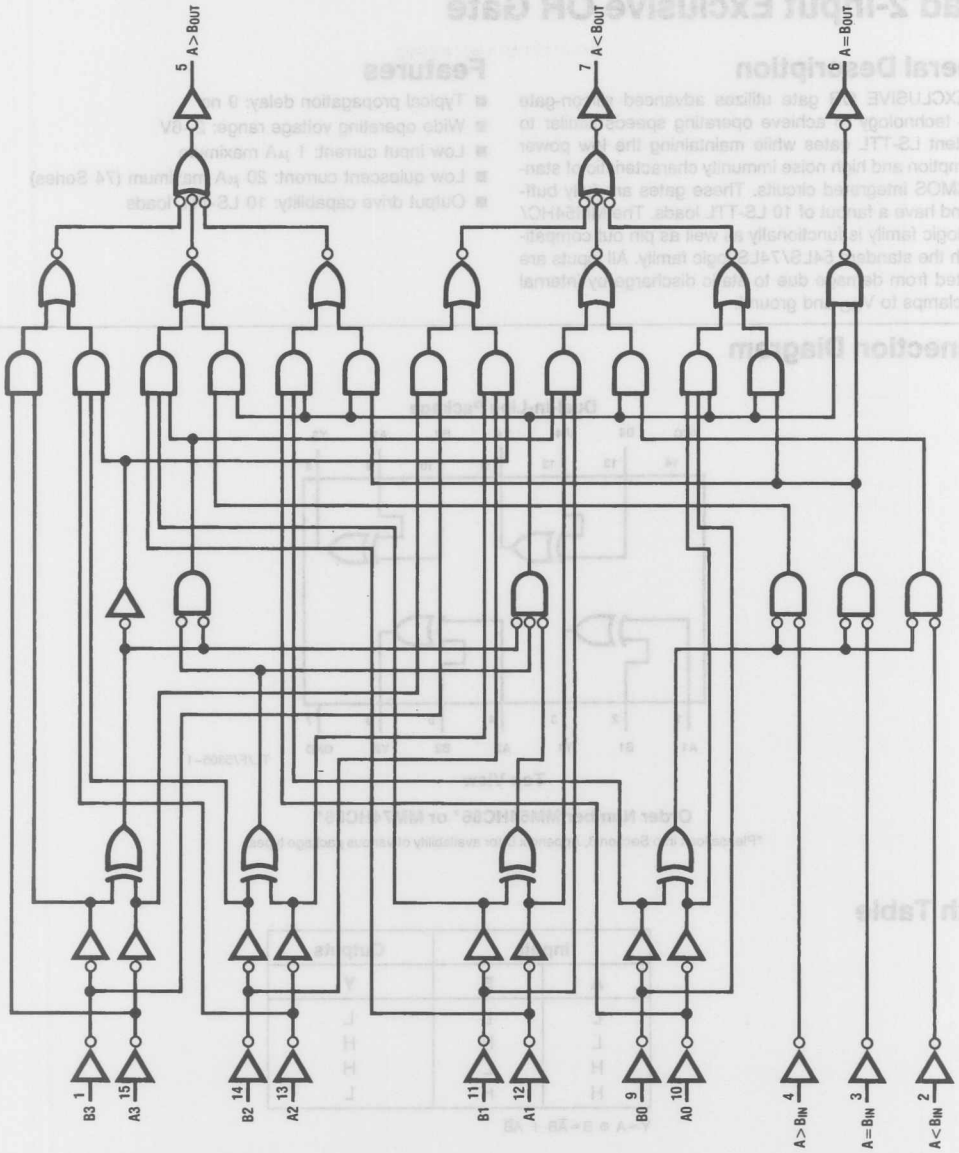
Typical Application

Cascading Comparators



TL/F/5205–4

Logic Diagram



National Semiconductor

MM54HC86/MM74HC86
Quad 2-Input Exclusive OR Gate

General Description

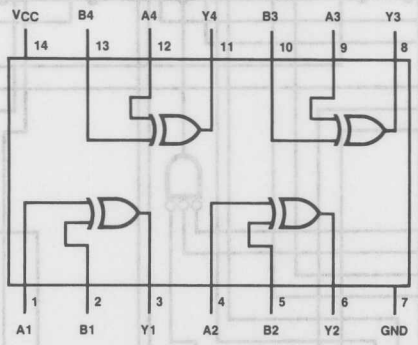
This EXCLUSIVE OR gate utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5305–1

Top View

Order Number MM54HC86* or MM74HC86*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC107/MM74HC107 Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

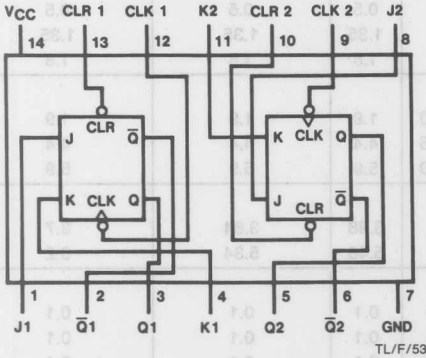
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5304–1

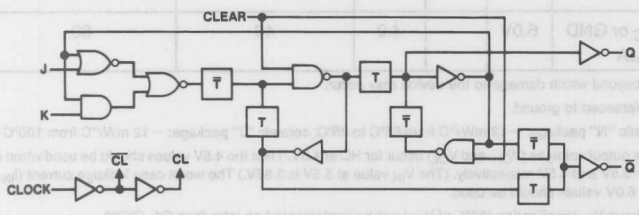
Order Number MM54HC107* or MM74HC107*

*Please look into Section 8, Appendix D for availability of various package types.

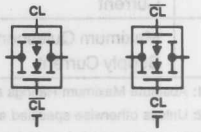
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Logic Diagram



TL/F/5304–2



TL/F/5304–3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

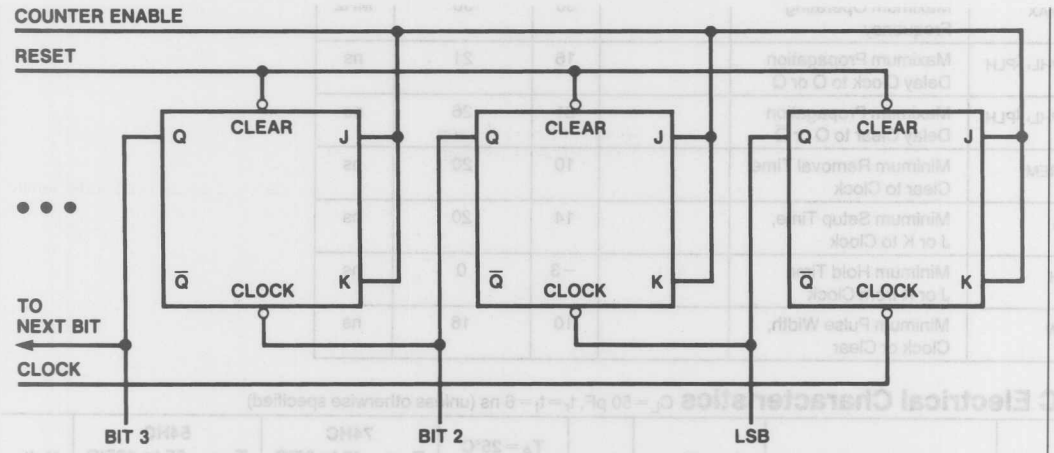
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_s	Minimum Setup Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

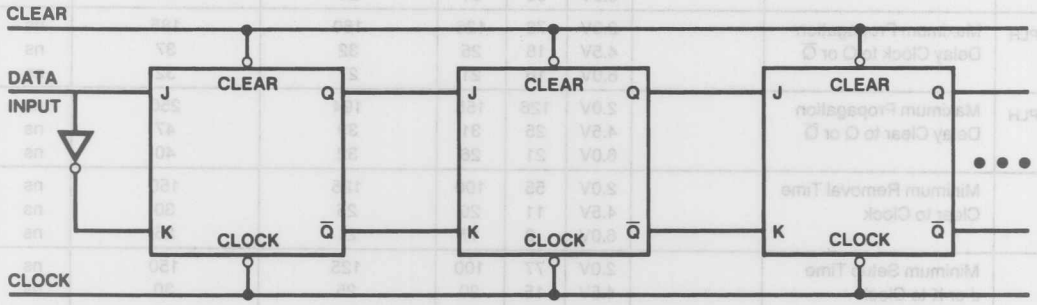
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	70	126	160	185	ns
			4.5V	18	25	32	37	ns
			6.0V	16	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	194	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	32	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_s	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K to Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.



TL/F/5304–4

N Bit Shift Register with Clear



TL/F/5304–5

MM54HC109A/MM74HC109A
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These J-$\overline{K}$ FLIP-FLOPS utilize advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$ PRESET, CLEAR and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

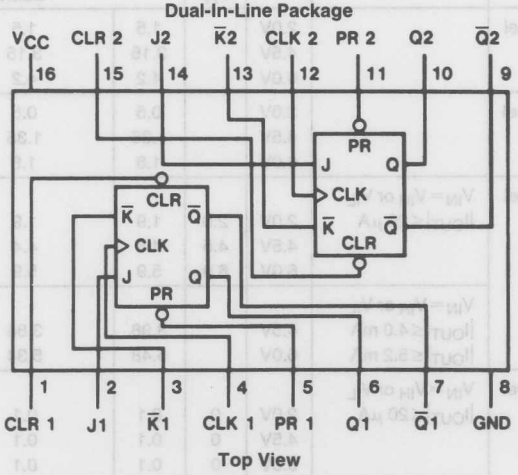
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5306–1

Top View

Order Number MM54HC109A* or MM74HC109A*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		21	42	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Setup Time, J or $\overline{K}$ to Clock			20	ns
t_H	Minimum Hold Time, J or $\overline{K}$ to Clock			0	ns
t_W	Minimum Pulse Width: Preset, Clear or Clock		9	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	4	MHz
			4.5V	27	21	18	MHz
			6.0V	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		2.0V	115	230	290	343	ns
			4.5V	23	46	58	69	ns
			6.0V	20	39	49	58	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V		25	32	37	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_S	Minimum Setup Time J or $\overline{K}$ to Clock		2.0V		100	126	149	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC112/MM74HC112
Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

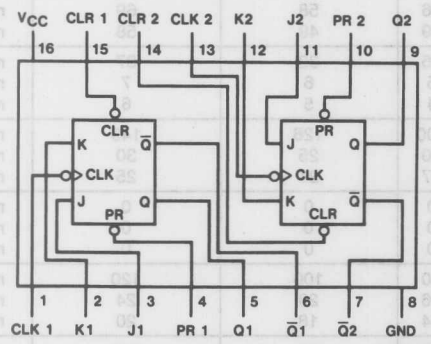
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC Series)
- High output drive: 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

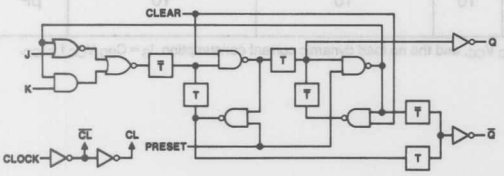


TL/F/5307–1

Top View

Order Number MM54HC112* or MM74HC112*

*Please look into Section 8, Appendix D for availability of various package types.

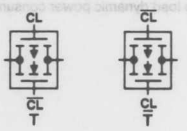


TL/F/5307–2

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed



TL/F/5307–3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

f_{MAX}	Maximum Operating Frequency			30	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$			16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$			21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$			23	28	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			10	20	ns
t_s	Minimum Setup Time J or K to Clock			14	20	ns
t_H	Minimum Hold Time J or K from Clock			−3	0	ns
t_W	Minimum Pulse Width Clock Preset or Clear			10	16	ns

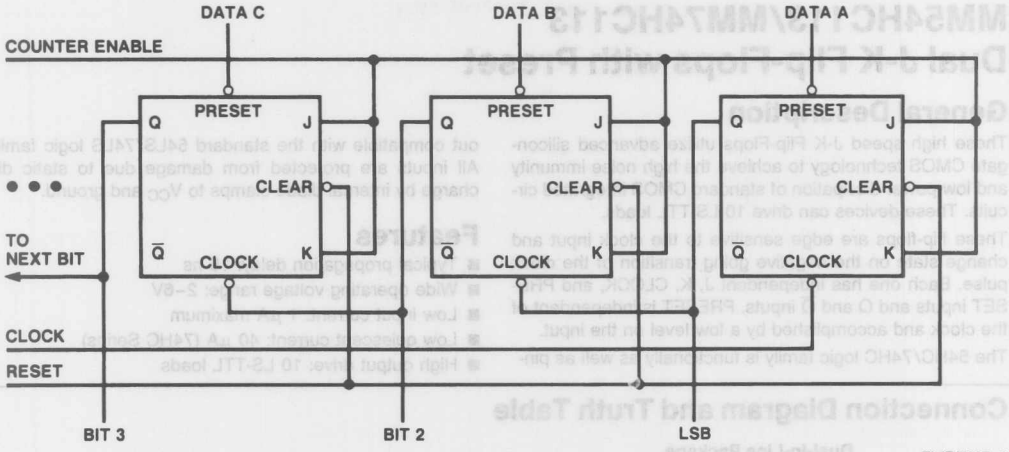
AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	100	126	160	183	ns
			4.5V	20	25	32	37	ns
			6.0V	17	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$		2.0V	126	155	191	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	33	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V	137	165	210	240	ns
			4.5V	27	33	41	50	ns
			6.0V	23	28	35	40	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9.4	17	21	25	ns
t_s	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Preset, Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

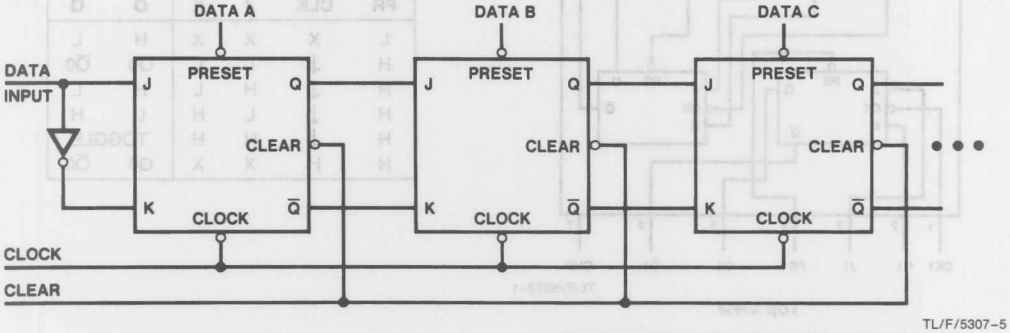
Typical Applications

N Bit Presettable Ripple Counter with Enable and Reset



TL/F/5307–4

N Bit Parallel Load/Serial Load Shift Register with Clear



TL/F/5307–5

National Semiconductor

MM54HC113/MM74HC113
Dual J-K Flip-Flops with Preset

General Description

These high speed J-K Flip-Flops utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and PRESET inputs and Q and $\overline{Q}$ inputs. PRESET is independent of the clock and accomplished by a low level on the input.

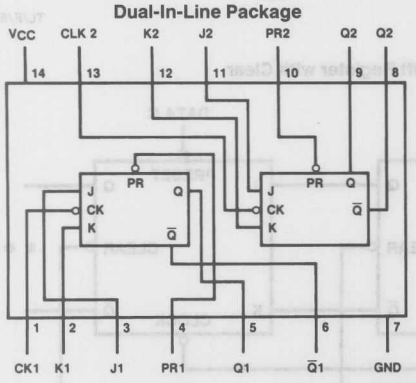
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC Series)
- High output drive: 10 LS-TTL loads

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5073–1

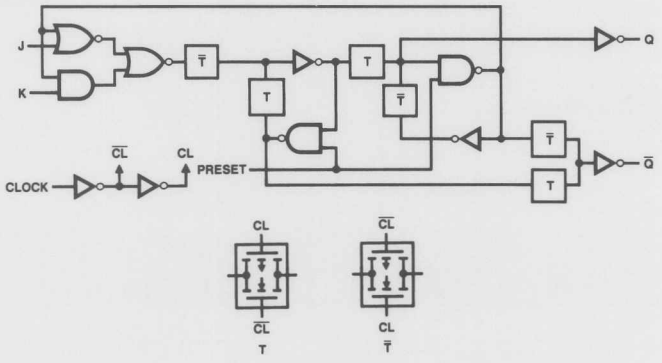
Top View

Order Number MM54HC113* or MM74HC113*

*Please look into Section 8, Appendix D for availability of various package types.

Inputs				Outputs	
PR	CLK	J	K	O	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Logic Diagram



TL/F/5073–2

(1 of 2)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

	Frequency				
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time, Preset to Clock		10	20	ns
t_S	Minimum Setup Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time, J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		10	16	ns

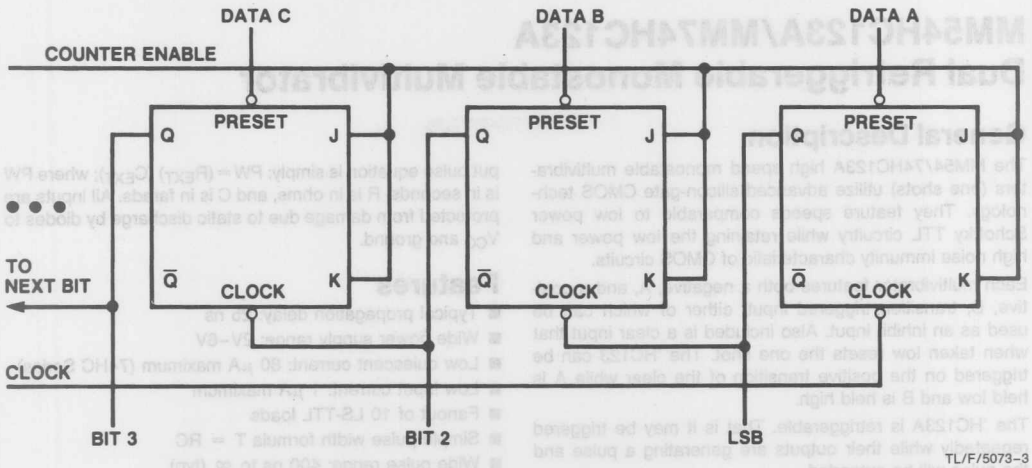
AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	100	125	160	183	ns
			4.5V	20	25	32	37	ns
			6.0V	17	33	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V	137	165	206	239	ns
			4.5V	27	33	41	47	ns
			6.0V	23	28	35	40	ns
t_{REM}	Minimum Removal Time Preset to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

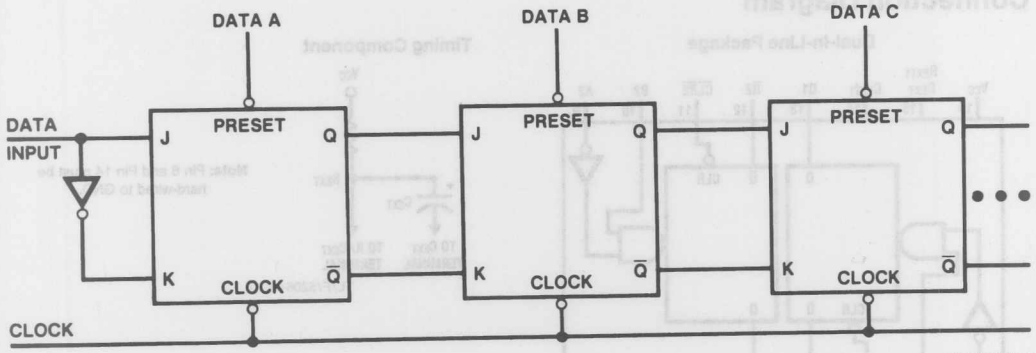
Typical Applications

N Bit Presettable Binary Ripple Counter with Enable



TL/F/5073–3

N Bit Parallel Load/Serial Load Shift Register



TL/F/5073–4

National Semiconductor

MM54HC123A/MM74HC123A
Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC123A high speed monostable multivibrators (one shots) utilize advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC123 can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC123A is retriggerable. That is it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

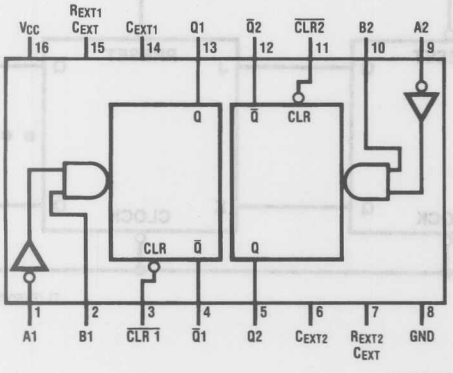
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 25 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: $\pm$5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise and fall times.

Connection Diagram

Dual-In-Line Package

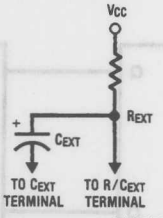


TL/F/5206–1

Top View
Order Number MM54HC123A* or MM74HC123A*

*Please look into Section 8, Appendix D for availability of various package types.

Timing Component



TL/F/5206–2

Note: Pin 6 and Pin 14 must be hard-wired to GND.

Truth Table

Inputs			Outputs	
$\overline{\text{Clear}}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Clear Input)			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$ 20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$ 4.0 mA	4.5V	4.2	3.98	3.84	3.7 V
		$\lvert I_{OUT}\rvert \le$ 5.2 mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$ 20 μA	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le$ 4 mA	4.5V	0.2	0.26	0.33	0.4 V
		$\lvert I_{OUT}\rvert \le$ 5.2 mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN} = V_{CC} or GND	6.0V		±0.5	±5.0	±5.0 μA
I_{IN}	Maximum Input Current (all other pins)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current (standby)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160 μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN} = V_{CC} or GND R/C_{EXT} = 0.5V_{CC}	2.0V	36	80	110	130 μA
			4.5V	0.33	1.0	1.3	1.6 mA
			6.0V	0.7	2.0	2.6	3.2 mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating:

Plastic "N" Package: −12mW/°C from 65°C to 85°C

Ceramic "J" Package: −12mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

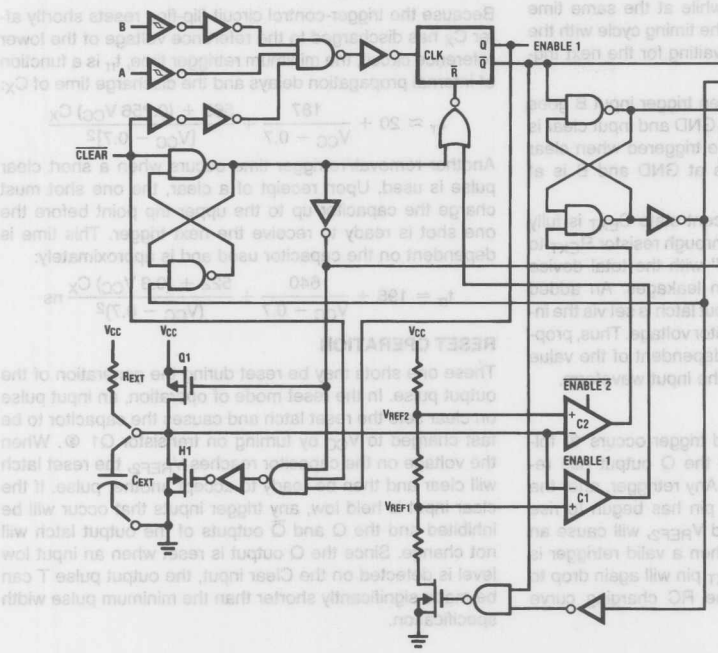
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		25	42	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	ns
				6.0V	21	32	39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	ns
				6.0V	24	38	46	51	ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	ns
				6.0V	19	28	33	36	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	ns
				6.0V	20	29	34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	ns
				6.0V	12	21	27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V		0	0	0	ns
				4.5V		0	0	0	ns
				6.0V		0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF		2.0V	1.5				μs
		$R_{EXT}=2$ kΩ		4.5V	450				ns
		$R_{EXT}=6$ kΩ ($V_{CC}=2V$)		6.0V	380				ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	5.0V	1	0.9	0.86	0.85	ms
			Max	5.0V	1	1.1	1.14	1.15	ms
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (other inputs)				6	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)			70				pF

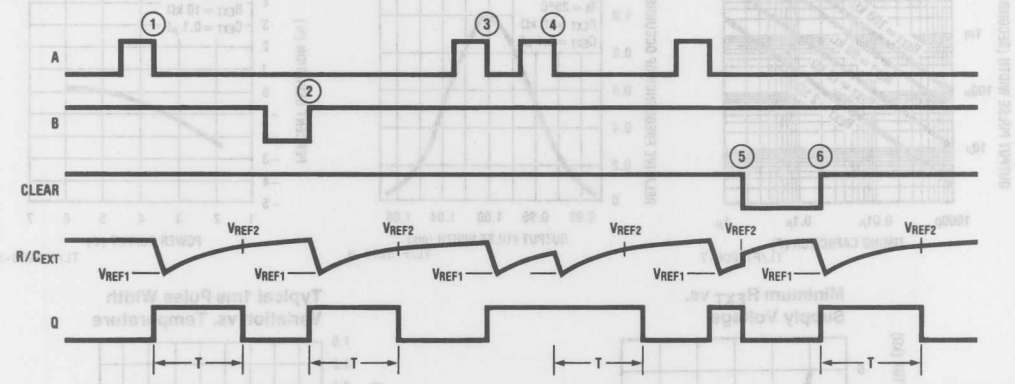
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5206–5

Theory of Operation



TL/F/5206–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER

FIGURE 1

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing re-

sistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC} ②). The 'HC123A can also be triggered when clear goes from GND to V_{CC} (while A is at GND and B is at V_{CC} ⑥).

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC123A is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The 'HC123A is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at the R/C_{EXT} pin has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

$$t_{rr} \approx 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256\,V_{CC})\,C_X}{[V_{CC} - 0.7]^2}$$

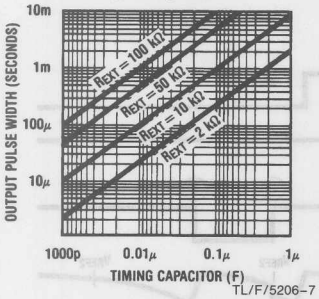
Another removal/retrigger time occurs when a short clear pulse is used. Upon receipt of a clear, the one shot must charge the capacitor up to the upper trip point before the one shot is ready to receive the next trigger. This time is dependent on the capacitor used and is approximately:

$$t_{rr} = 196 + \frac{640}{V_{CC} - 0.7} + \frac{522 + (0.3\,V_{CC})\,C_X}{(V_{CC} - 0.7)^2}\ \text{ns}$$

RESET OPERATION

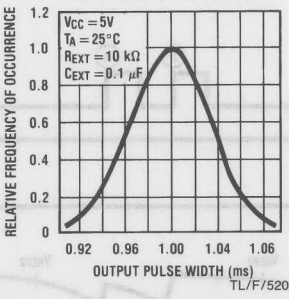
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



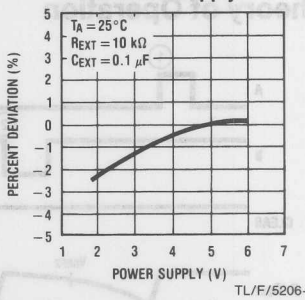
TL/F/5206–7

Typical Distribution of Output Pulse Width, Part to Part



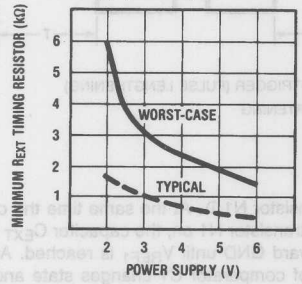
TL/F/5206–8

Typical 1ms Pulse Width Variation vs. Supply



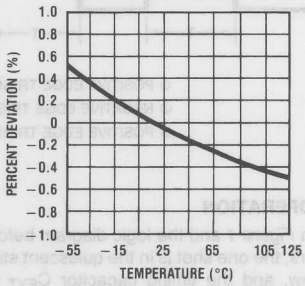
TL/F/5206–9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5206–10

Typical 1ms Pulse Width Variation vs. Temperature



TL/F/5206–11

Note: R and C are not subjected to temperature. The C is polypropylene.

National Semiconductor

MM54HC125/MM74HC125
MM54HC126/MM74HC126
TRI-STATE® Quad Buffers

General Description

These are general purpose TRI-STATE high speed non-inverting buffers utilizing advanced silicon-gate CMOS technology. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM54HC125/MM74HC125 require the TRI-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM54HC126/MM74HC126 require the control input to be low to put the output into high impedance.

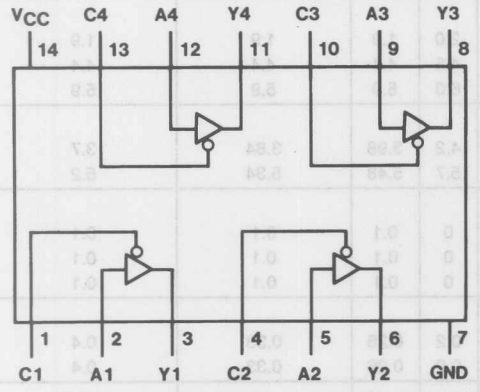
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC)
- Fanout of 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



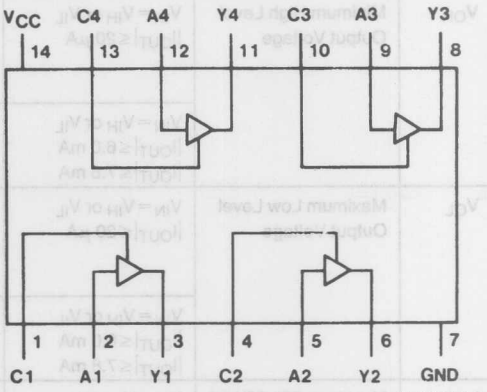
TL/F/5308–1

Top View

Order Number MM54HC125* or MM74HC125*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/5308–2

Top View

Order Number MM54HC126* or MM74HC126*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND C_n = Disabled	6.0V		±0.5	±5	±10	μA
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to High Level	$R_L = 1\ k\Omega$	13	25	ns
t_{PHZ}	Maximum Output Disable Time from High Level	$R_L = 1\ k\Omega$ $C_L = 5\ pF$	17	25	ns
t_{PZL}	Maximum Output Enable Time to Low Level	$R_L = 1\ k\Omega$	18	25	ns
t_{PLZ}	Maximum Output Disable Time from Low Level	$R_L = 1\ k\Omega$ $C_L = 5\ pF$	13	25	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50\ pF$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	Temperature °C				Units
				54HC/74HC $T_A = 25°C$	74HC -40 to $85°C$	54HC -55 to $125°C$		
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		2.0V	40	100	125	150	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	25	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	$C_L = 150\ pF$	2.0V	35	130	163	195	ns
			4.5V	14	26	33	39	ns
			6.0V	12	22	28	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1\ k\Omega$	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 150\ pF$ $R_L = 1\ k\Omega$	2.0V	35	140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V	13	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L = 50\ pF$	2.0V	30	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) Enabled		45				pF
		Disabled		6				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

3

National Semiconductor

PRELIMINARY

MM54HC132/MM74HC132 Quad 2-Input NAND Schmitt Trigger

General Description

The MM54HC132/MM74HC132 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

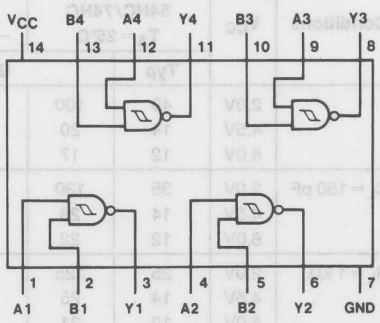
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V

Connection and Logic Diagrams

Dual-In-Line Package

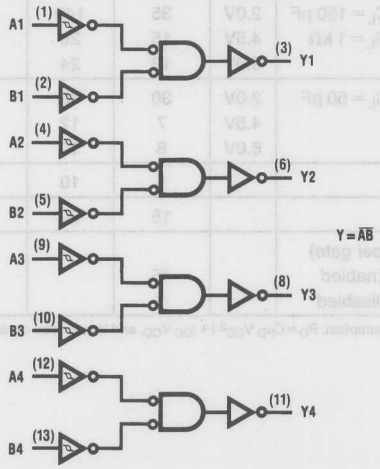


TL/F/5309–1

Top View

Order Number MM54HC132* or MM74HC132*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5309–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage		Min	2.0V		1.0	1.0	1.0	V
				4.5V		2.0	2.0	2.0	V
				6.0V		3.0	3.0	3.0	V
			Max	2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage		Min	2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
			Max	2.0V		1.0	1.0	1.0	V
				4.5V		2.2	2.2	2.2	V
				6.0V		3.0	3.0	3.0	V
V_H	Hysteresis Voltage		Min	2.0V		0.2	0.2	0.2	V
				4.5V		0.4	0.4	0.4	V
				6.0V		0.5	0.5	0.5	V
			Max	2.0V		1.0	1.0	1.0	V
				4.5V		1.4	1.4	1.4	V
				6.0V		1.5	1.5	1.5	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$		2.0V	2.0	1.9	1.9	1.9	V
				4.5V	4.5	4.4	4.4	4.4	V
				6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA		4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA		6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$		2.0V	0	0.1	0.1	0.1	V
				4.5V	0	0.1	0.1	0.1	V
				6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA		4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA		6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2: Unless otherwise specified all voltages are referenced to ground.
Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.
Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		130				pF
C_{IN}	Maximum Input Capacitance				5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC133/MM74HC133 13-Input NAND Gate

General Description

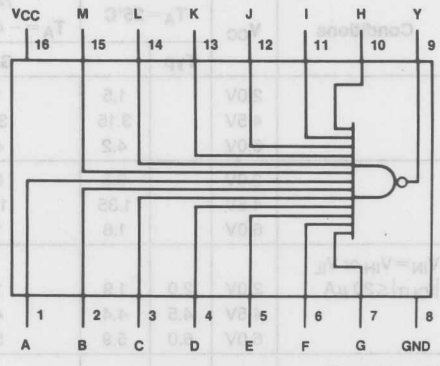
This NAND gate utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

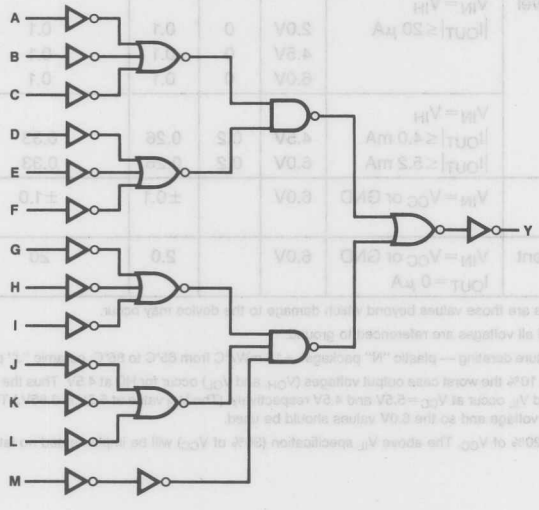


TL/F/5134–1

Top View

Order Number MM54HC133* or MM74HC133*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5134–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

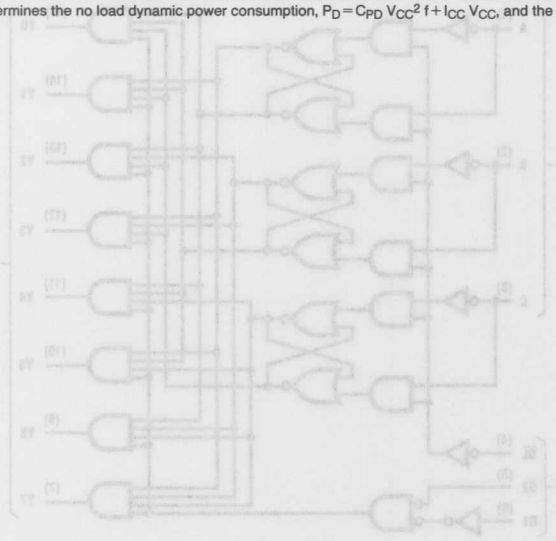
**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



MM54HC137/MM74HC137 3-to-8 Line Decoder With Address Latches (Inverted Output)

General Description

This device utilizes advanced silicon-gate CMOS technology, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

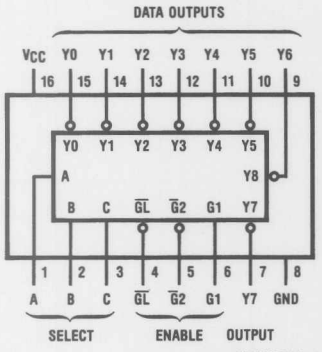
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

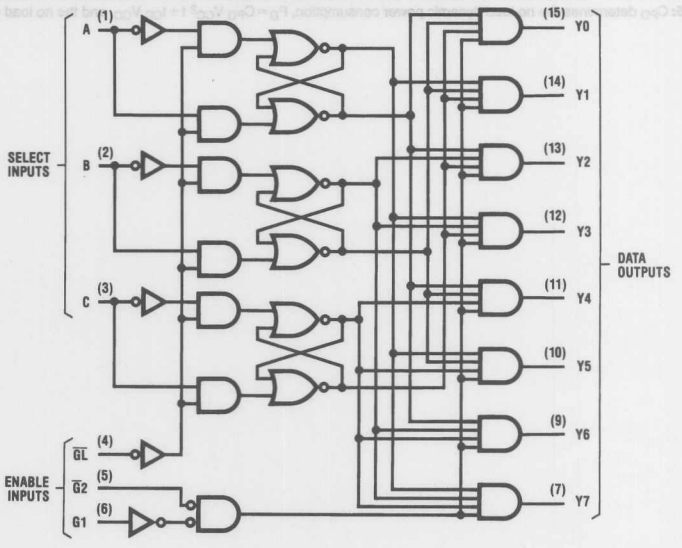
- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing.
- Fanout of 10 LS-TTL loads.

Connection and Functional Block Diagrams

Dual-In-Line Package



TL/F/5310–1



TL/F/5310–2

Order Number MM54HC137* or MM74HC137*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

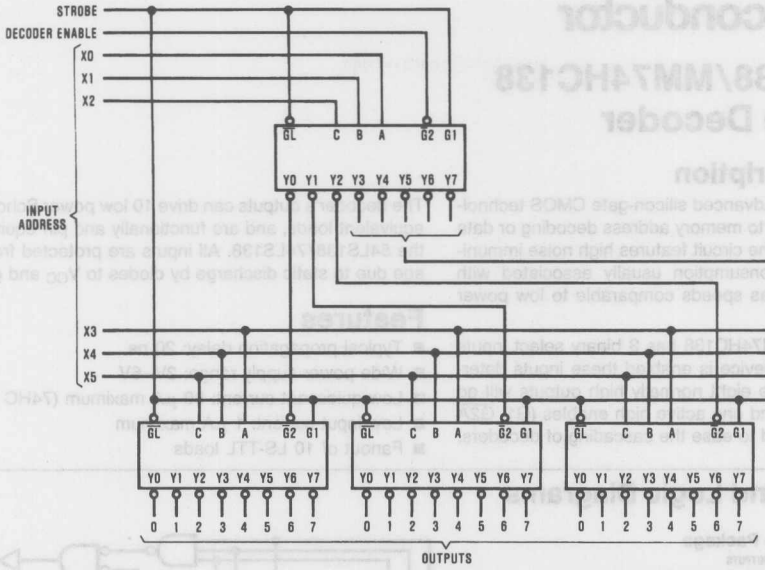
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		14	29	ns
t_{PHL}	Maximum Propagation Delay, A, B or C to any Y Output		20	42	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		12	22	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		15	34	ns
t_{PLH}	Maximum Propagation Delay G1 to any Output		13	25	ns
t_{PHL}	Maximum Propagation Delay GL to any Output		17	34	ns
t_{PLH}	Maximum Propagation GL to Output		15	30	ns
t_{PHL}	Maximum Propagation Delay GL to Output		22	34	ns
t_S	Minimum Setup Time at A, B and C Inputs			20	ns
t_H	Minimum Hold Time at A, B and C Inputs			0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		2.0V	85	170	214	253	ns
			4.5V	17	34	43	51	ns
			6.0V	14	29	36	43	ns
t_{PHL}	Maximum Propagation Delay A, B or C to any Y Output		2.0V	120	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		2.0V	65	130	164	194	ns
			4.5V	13	26	33	39	ns
			6.0V	11	22	28	33	ns
t_{PLH}	Maximum Propagation Delay G1 to Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay G1 to Output		2.0V	98	195	246	291	ns
			4.5V	20	39	49	58	ns
			6.0V	17	33	42	49	ns
t_{PLH}	Maximum Propagation Delay GL to Output		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}	Maximum Propagation Delay GL to Output		2.0V	125	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	21	43	54	63	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$, to any Y Output		2.0V	98	195	246	291	ns
			4.5V	20	39	49	58	ns
			6.0V	17	33	42	49	ns
t_S	Minimum Setup Time at A, B and C inputs		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time at A, B and C inputs		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		8	11	13	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Typical Application



TL/F/5310–3

6-Line to 64-Line Decoder with Input Address Storage

Truth Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L; all others, H							

H = high level, L = low level, X = irrelevant

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MM54HC138/MM74HC138 3-to-8 Line Decoder

General Description

This decoder utilizes advanced silicon-gate CMOS technology, and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC138/MM74HC138 has 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, $\overline{G2A}$ and $\overline{G2B}$) are provided to ease the cascading of decoders.

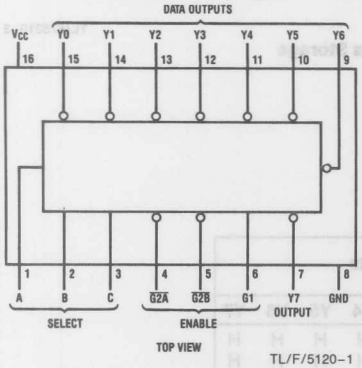
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

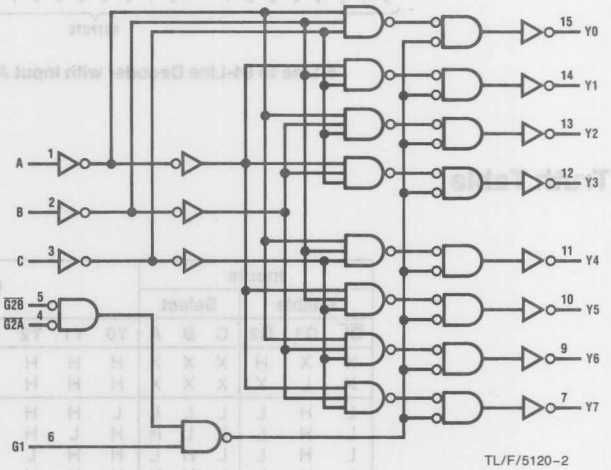
Dual-In-Line Package



TL/F/5120–1

Order Number MM54HC138* or MM74HC138*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5120–2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2}$ = G2A + G2B

H = high level, L = low level, X = don't care

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, Binary Select to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay, Binary Select to any Output		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, G1 to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		23	30	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		18	25	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay Binary Select to any Output Low to High		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay Binary Select to any Output High to Low		2.0V	100	200	252	298	ns
			4.5V	20	40	50	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay G1 to any Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	82	175	221	261	ns
			4.5V	28	35	44	52	ns
			6.0V	22	30	37	44	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		75				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC139/MM74HC139 Dual 2-To-4 Line Decoder

General Description

This decoder utilizes advanced silicon-gate CMOS technology, and is well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC139/MM74HC139 contain two independent one-of-four decoders each with a single active low enable input (G1, or G2). Data on the select inputs (A1, and B1 or A2, and B2) cause one of the four normally high outputs to go low.

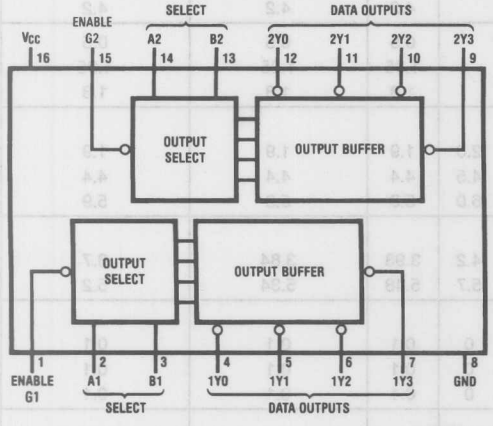
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally as well as pin equivalent to the 54LS139/74LS139. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delays —
  Select to outputs (4 delays): 18 ns
  Select to output (5 delays): 28 ns
  Enable to output: 20 ns
- Low power: 40 μW quiescent supply power
- Fanout of 10 LS-TTL devices
- Input current maximum 1 μA, typical 10 pA

Connection Diagram

Dual-In-Line Package



TL/F/5311–1

Order Number MM54HC139* or MM74HC139*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

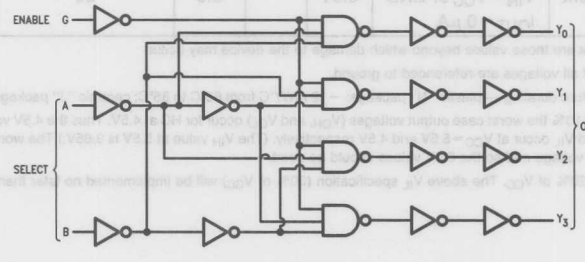
'HC139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

MM54HC139/MM74HC139



TL/F/5311–2

(1 of 2)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 4 levels of delay		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 5 levels of delay		28	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to any Output		19	30	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$		Units
				Typ	Guaranteed Limits				
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 4 levels of delay	(Note 6)	2.0V	110	175	219	254		ns
			4.5V	22	35	44	51		ns
			6.0V	18	30	38	44		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 5 levels of delay	(Note 7)	2.0V	165	220	275	320		ns
			4.5V	33	44	55	64		ns
			6.0V	28	38	47	54		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to any Output		2.0V	115	175	219	254		ns
			4.5V	23	35	44	51		ns
			6.0V	19	30	38	44		ns
t_{TLH}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110		ns
			4.5V	8	15	19	22		ns
			6.0V	7	13	16	19		ns
C_{IN}	Maximum Input Capacitance			3	10	10	10		pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(Note 5)		75					pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Note 6: 4 levels of delay are A to Y1, Y3 and B to Y2, Y3.

Note 7: 5 levels of delay are A to Y0, Y2 and B to Y0, Y1.

3

National Semiconductor

MM54HC147/MM74HC147
10-to-4 Line Priority Encoder

General Description

This high speed 10-to-4 Line Priority Encoder utilizes advanced silicon-gate CMOS technology. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits. This device is fully buffered, giving it a fanout of 10 LS-TTL loads.

The MM54HC147/MM74HC147 features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.

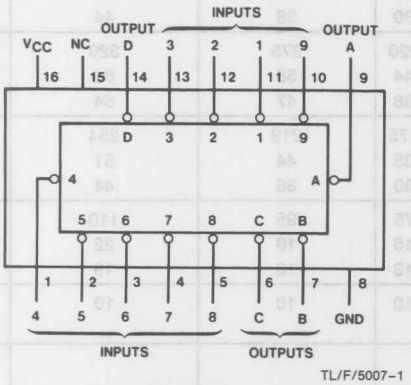
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent power consumption: 40 μW maximum at 25°C
- High speed: 31 ns propagation delay (typical)
- Low input current: 1 μA maximum
- Wide supply range: 2V to 6V

Connection and Logic Diagrams

Dual-In-Line Package

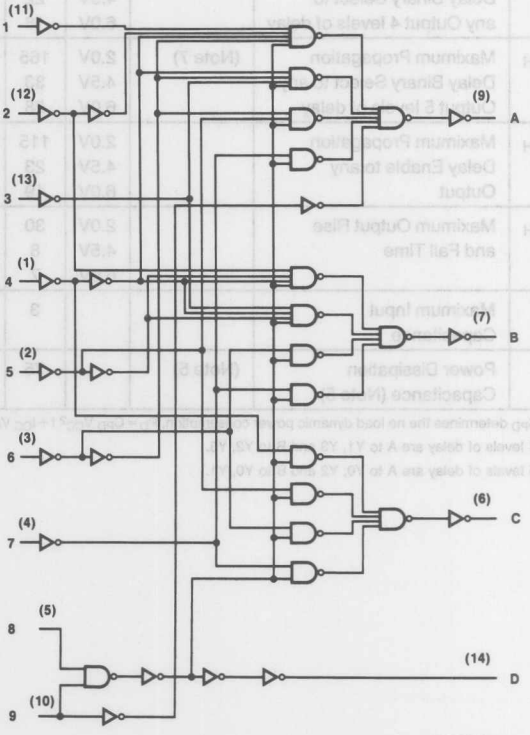


TL/F/5007–1

Top View

Order Number MM54HC147* or MM74HC147*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5007–2

Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.7	3.98	3.84	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		31	38	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	181	220	275	319	ns
			4.5V	36	44	55	64	ns
			6.0V	31	37	47	54	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		180				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC148/MM74HC148 8-3 Line Priority Encoder

General Description

This priority encoder utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LB-TTL.

This priority encoder accepts 8 input request lines 0–7 and outputs 3 lines A0–A2. The priority encoding ensures that only the highest order data line is encoded. Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. All data inputs and outputs are active at the low logic level.

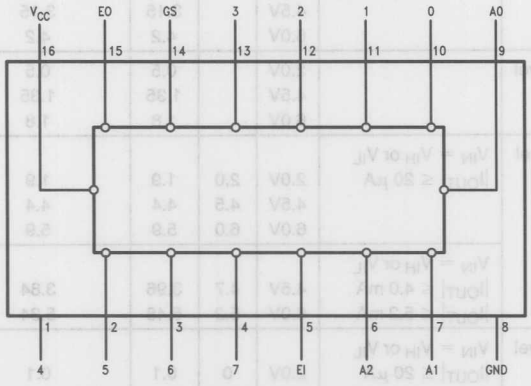
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide supply voltage range: 2V–6V

Connection Diagram

Dual-In-Line Package



TL/F/9390–1

Order Number MM54HC148* or MM74HC148*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High, L = Low, X = irrelevant

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 sec.)	260°C

Operation Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.7	3.96	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C, ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

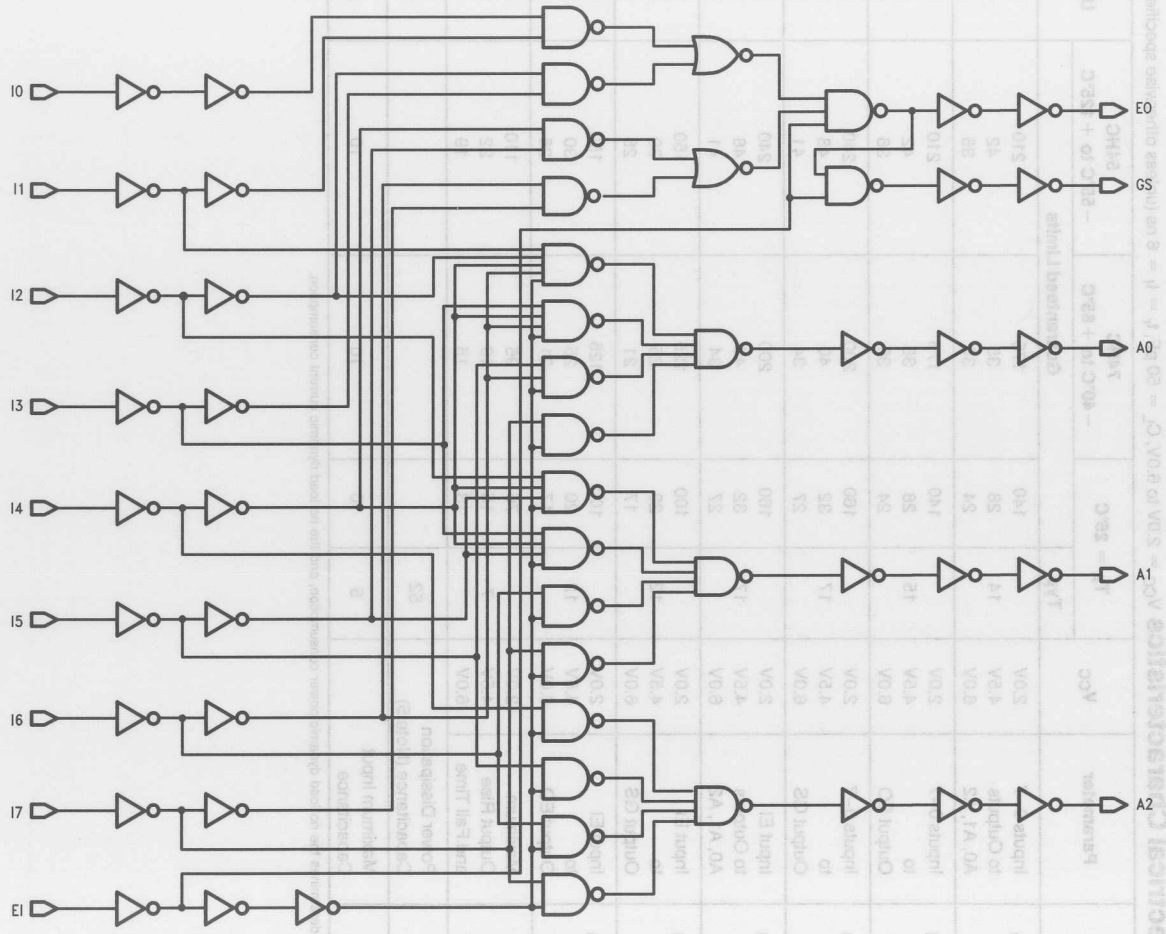
Symbol	Parameter	Conditions	Typ	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Input to Any Output		14	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	V_{CC}	T_A = 25°C	74HC −40°C to +85°C	54HC −55°C to +125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Inputs 0–7	2.0V		140	175	210	ns
	to Outputs	4.5V	14	28	35	42	ns
	A0, A1, A2	6.0V		24	30	36	ns
t_{PHL}, t_{PLH}	Inputs 0–7	2.0V		140	175	210	ns
	to	4.5V	15	28	35	42	ns
	Output EO	6.0V		24	30	36	ns
t_{PHL}, t_{PLH}	Inputs 0–7	2.0V		160	200	240	ns
	to	4.5V	17	32	40	48	ns
	Output GS	6.0V		27	34	41	ns
t_{PHL}, t_{PLH}	Input EI	2.0V		160	200	240	ns
	to Outputs	4.5V	17	32	40	48	ns
	A0, A1, A2	6.0V		27	34	41	ns
t_{PHL}, t_{PLH}	Input EI	2.0V		100	125	150	ns
	to	4.5V	12	20	25	30	ns
	Output GS	6.0V		17	21	26	ns
t_{PHL}, t_{PLH}	Input EI	2.0V		100	125	150	ns
	to	4.5V	12	20	25	30	ns
	Output EO	6.0V		17	21	26	ns
t_f, t_r	Maximum	2.0V		75	95	110	ns
	Output Rise	4.5V	7	15	19	22	ns
	and Fall Time	6.0V		13	16	19	ns
C_{pd}	Power Dissipation Capacitance (Note 5)		52				pF
C_{in}	Maximum Input Capacitance		5	10	10	10	pF

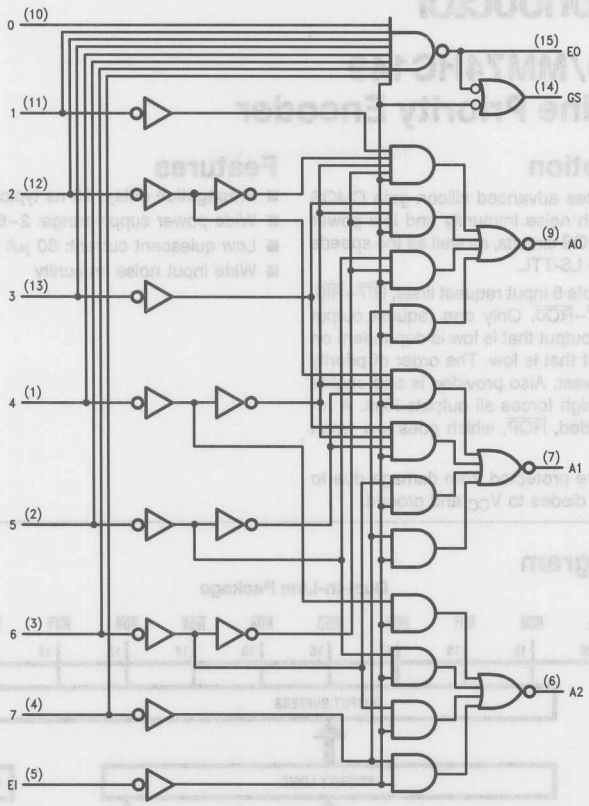
Note 5: C_{pd} determines the no load dynamic power consumption, and the no load dynamic current consumption.

HC148 Schematic for Datasheet



TL/F/9390–3

Logic Diagram



TL/F/9390–2

National Semiconductor

MM54HC149/MM74HC149
8 Line to 8 Line Priority Encoder

General Description

This priority encoder utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. Only one request output can be low at a time. The output that is low is dependent on the highest priority request that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is and enable input, $\overline{RQE}$, which when high forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RIn}$ is active.

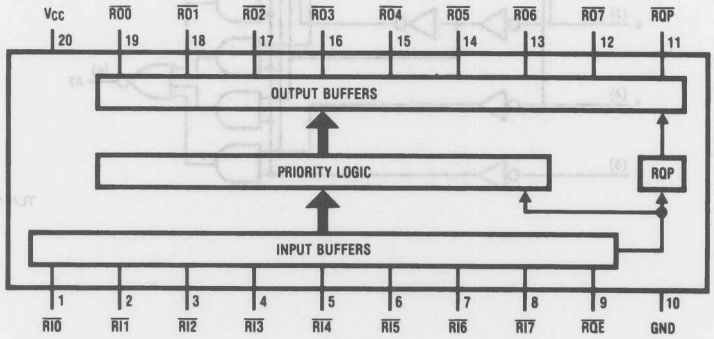
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- Propagation delay: 15 ns typical
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA max (74HC Series)
- Wide input noise immunity

Connection Diagram

Dual-In-Line Package



TL/F/5312–1

Top View

Order Number MM54HC149* or MM74HC149*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns (Note 6)

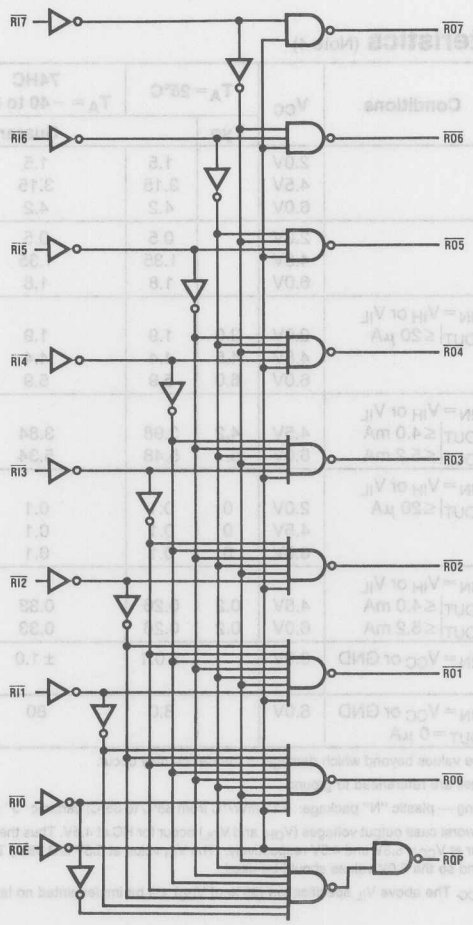
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Input To Any Output		20	33	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any Input To Any Output		2.0V	73	205	310	ns
			4.5V	25	41	62	ns
			6.0V	21	35	53	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	110	ns
			4.5V	8	15	22	ns
			6.0V	7	13	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			50			pF
C_{IN}	Maximum Input Capacitance			7	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Simplified Logic Diagram



TL/F/5312–2

National Semiconductor

MM54HC151/MM74HC151 8-Channel Digital Multiplexer

General Description

This high speed Digital multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HC151/MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

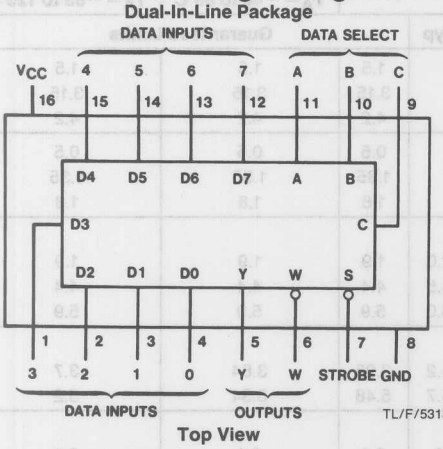
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
  data select to output Y: 26 ns
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum

Connection and Logic Diagrams

Dual-In-Line Package

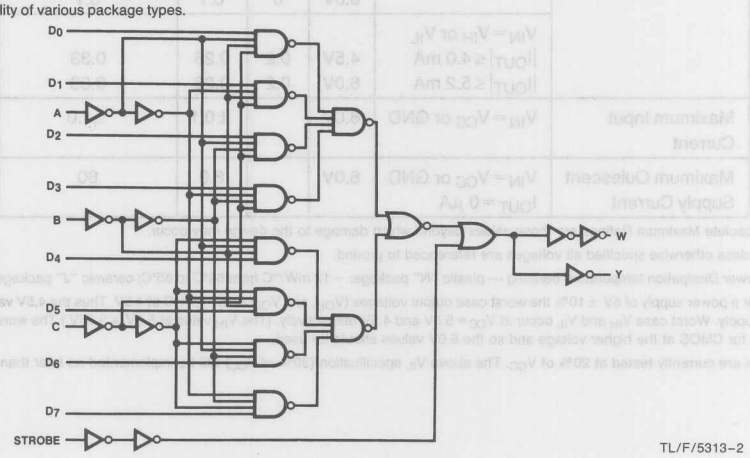


TL/F/5313–1

Top View

Order Number MM54HC151* or MM74HC151*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5313–2

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		24	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		16	21	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V	90	205	256	300	ns
			4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		2.0V	95	205	256	300	ns
			4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to Y		2.0V	70	195	244	283	ns
			4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		2.0V	75	185	231	268	ns
			4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		2.0V	50	140	175	203	ns
			4.5V	21	28	35	41	ns
			6.0V	18	24	30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		2.0V	45	127	159	185	ns
			4.5V	20	25	32	37	ns
			6.0V	17	22	28	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

MM54HC153/MM74HC153 Dual 4-Input Multiplexer

General Description

This 4-to-1 line multiplexer utilizes advanced silicon-gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits. This device is fully buffered, allowing it to drive 10 LS-TTL loads. Information on the data inputs of each multiplexer is selected by the address on the A and B inputs, and is presented on the Y outputs. Each multiplexer possesses a strobe input which enables it when taken to a low logic level. When a high logic level is applied to a strobe input, the output of its associated multiplexer is taken low.

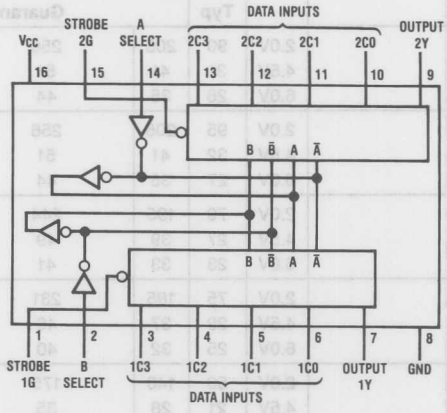
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5107–1

Top View

Order Number MM54HC153* or MM74HC153*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.3	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

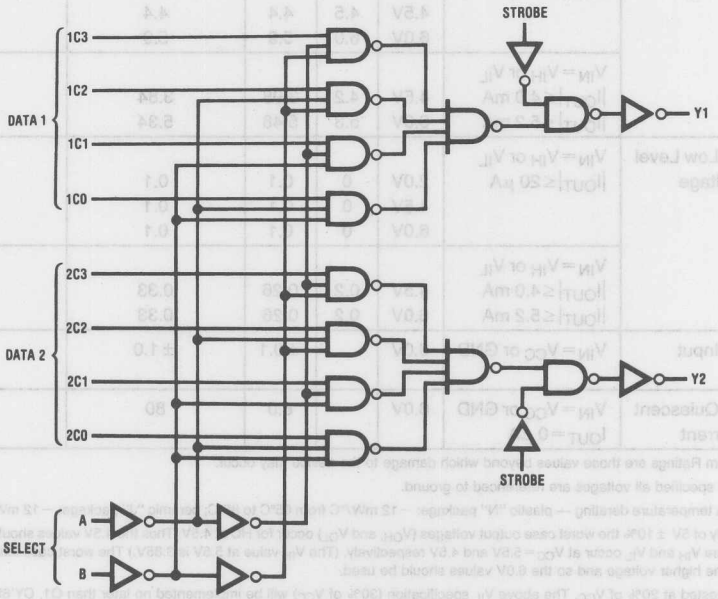
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		26	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		20	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		8	15	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	158	198	237	ns
			4.5V	29	35	44	52	ns
			6.0V	25	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		2.0V	99	126	158	189	ns
			4.5V	22	28	35	42	ns
			6.0V	19	23	29	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		2.0V	50	86	108	129	ns
			4.5V	12	19	24	29	ns
			6.0V	10	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)(per package) Outputs Enabled		90				pF
		Outputs Disabled		25				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5107–2

National Semiconductor

MM54HC154/MM74HC154 4-to-16 Line Decoder

General Description

This decoder utilizes advanced silicon-gate CMOS technology, and is well suited to memory address decoding or data routing applications. It possesses high noise immunity, and low power consumption of CMOS with speeds similar to low power Schottky TTL circuits.

The MM54HC154/MM74HC154 have 4 binary select inputs (A, B, C, and D). If the device is enabled these inputs determine which one of the 16 normally high outputs will go low. Two active low enables ($\overline{G1}$ and $\overline{G2}$) are provided to ease cascading of decoders with little or no external logic.

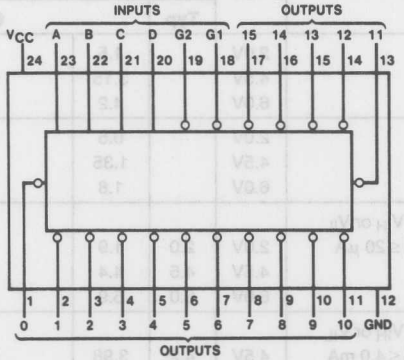
Each output can drive 10 low power Schottky TTL equivalent loads, and is functionally and pin equivalent to the 54LS154/74LS154. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 21 ns
- Power supply quiescent current: 80 μA (74HC)
- Wide power supply voltage range: 2–6V
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5122–1

Top View

Order Number MM54HC154* or MM74HC154*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs						Low Output*
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

*All others high

Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$, $\overline{G2}$ or A, B, C, D		21	32	ns

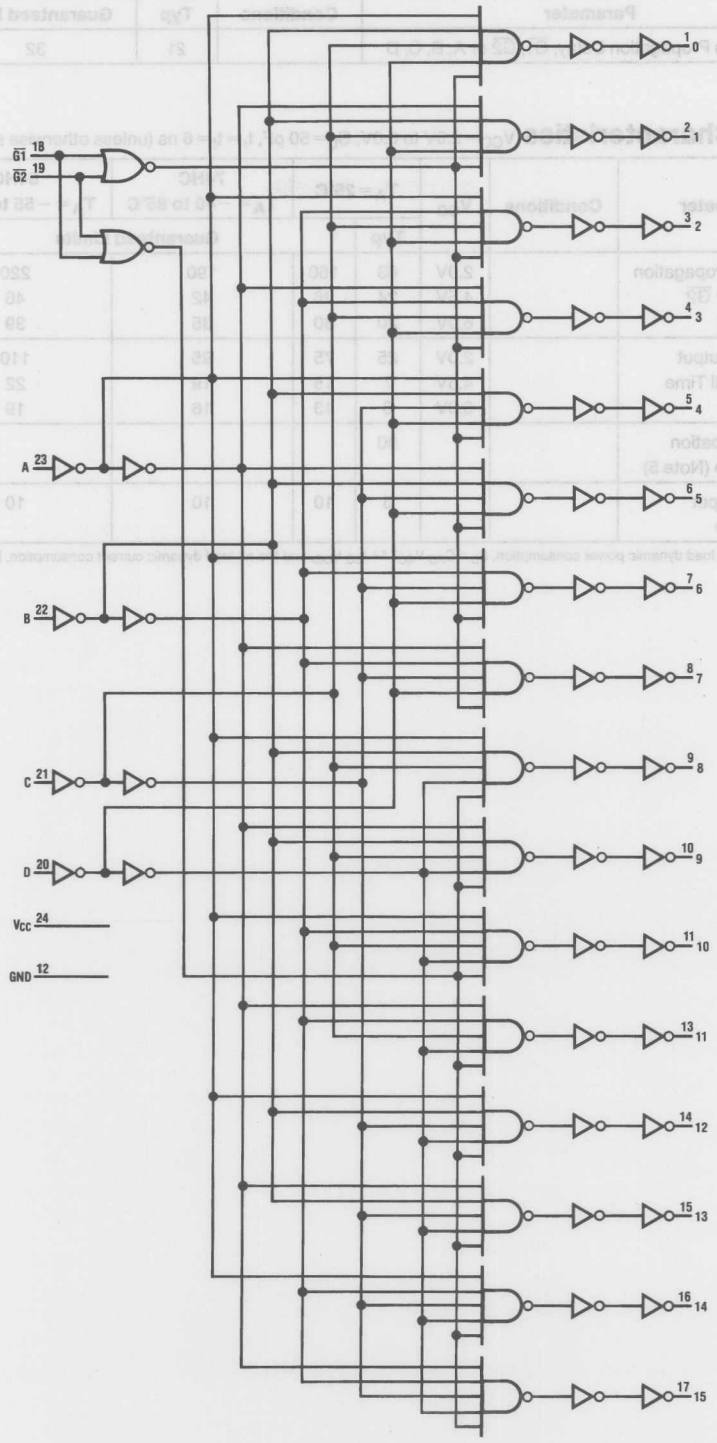
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$ or $\overline{G2}$ or A, B, C, D		2.0V	63	160	190	220	ns
			4.5V	24	36	42	46	ns
			6.0V	20	30	35	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

Logic Diagram



TL/F/5122–2

National Semiconductor

MM54HC155/MM74HC155 Dual 2-To-4 Line Decoder/Demultiplexers

General Description

The MM54HC155/MM74HC155 is a high speed silicon-gate CMOS decoder/demultiplexer. It utilizes advanced silicon-gate CMOS technology and features dual 1-line-to-4-line demultiplexers with independent strobes and common binary-address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is non-inverted at its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without gating.

All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground.

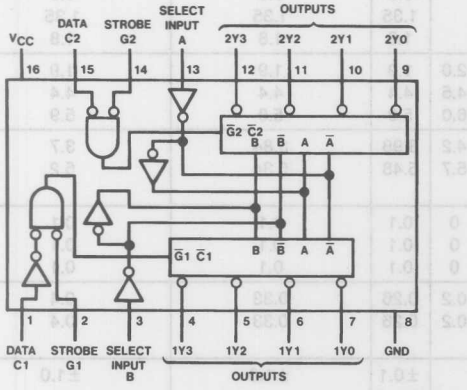
The device is capable of driving 10 low power Schottky TTL equivalent loads.

The MM54HC155/MM74HC155 is functionally and pin equivalent to the 54LS155/74LS155 with the advantage of reduced power consumption.

Features

- Applications
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Typical propagation delay: 22 ns
- Low quiescent current: 80 μA maximum (74HC series)
- Wide operating range: 2V–6V

Connect and Logic Diagram



TL/F/8364–1

Order Number MM54HC155* or MM74HC155*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

2-to-4-Line Decoder or 1-Line to 4-line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
IC	B	A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

IC = inputs C1 and C2 connected together
IG = inputs G1 and G2 connected together
H = high level L = low level X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	20 mA
DC Output Current, per pin (I_{OUT})	25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_l) (Soldering 10 sec)	260°C

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	C
MM54HC	−55	+125	C
Input Rise/Fall Time V_{CC} = 2.0V		1000	ns
(t_r, t_f) V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40° to +85°C	54HC T_A = −55° to +125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA $\lvert I_{OUT}\rvert \le 5.2$ mA	4.5V	4.2	3.98	3.84	3.7	V
			6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA $\lvert I_{OUT}\rvert \le 5.2$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC} and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

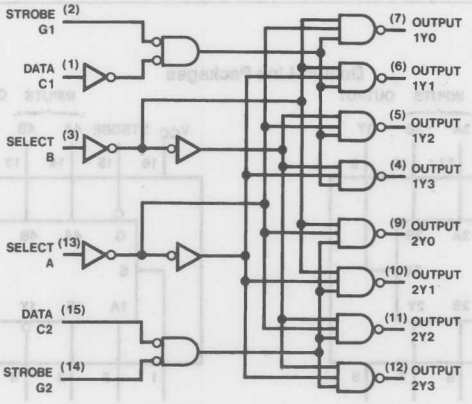
Symbol	Parameter	Conditions	Typ	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 4 Levels of Delay		18	ns

AC Electrical Characteristics (Note 6) C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to +85°C	54HC T_A = −55 to +125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 4 Levels of Delay		2.0V	110	175	219	254	ns
			4.5V	22	35	44	51	ns
			6.0	18	30	38	44	ns
t_{TLH}, t_{TLH}	Maximum Output Rise and FallTime		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(Note 5)		47				pF

Note 5: CPC determines the no load dynamic power consumption, $P_d = C_{PD} V_{CC}^2 f + I_{CC}$, and the no load dynamic current consumption, I_S Q $C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/8364–2

National Semiconductor

MM54HC157/MM74HC157 Quad 2-Input Multiplexer
MM54HC158/MM74HC158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed Quad 2-to-1 Line data selector/Multiplexers utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and STROBE inputs. On the MM54HC157/MM74HC157, when the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0". The MM54HC158/MM74HC158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

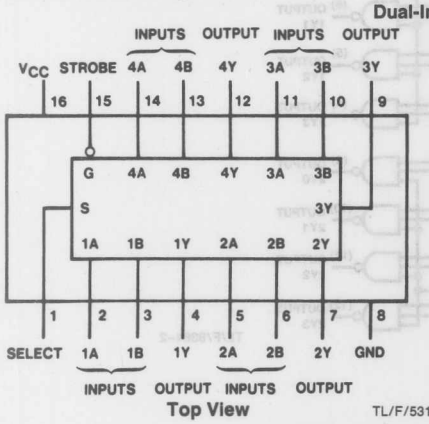
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

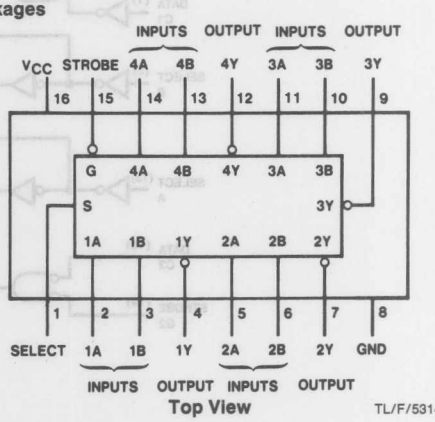
- Typical propagation delay: 14 ns data to any output
- Wide power supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC Series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 μA maximum

Connection Diagrams

Dual-In-Line Packages



Top View TL/F/5314–1



Top View TL/F/5314–2

Order Number MM54HC157/158* or MM74HC157/158*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HC157	HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

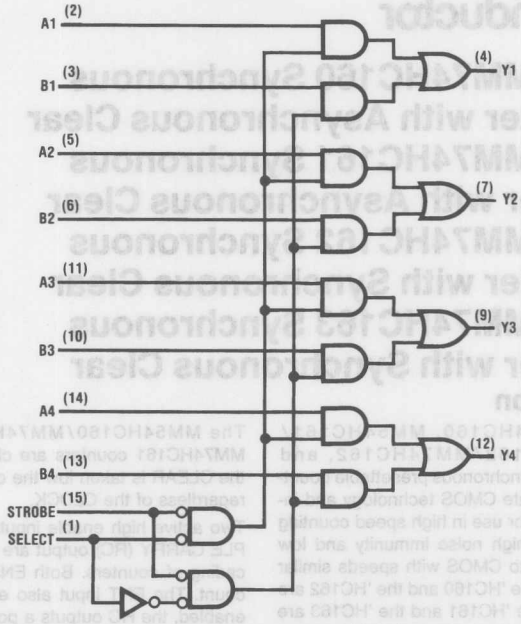
AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		2.0V	58	115	145	171	ns
			4.5V	12	23	29	34	ns
			6.0V	10	20	25	29	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per Multiplexer)		57				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

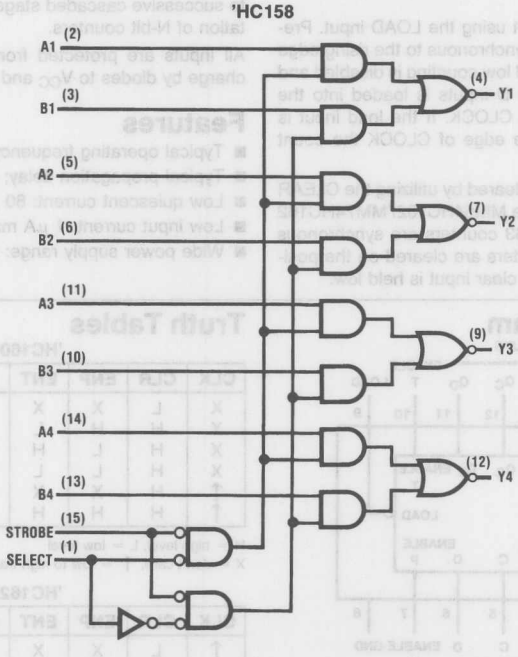
Logic Diagrams

'HC157



TL/F/5314–3

'HC158



TL/F/5314–4

3

MM54HC160/MM74HC160 Synchronous Decade Counter with Asynchronous Clear
MM54HC161/MM74HC161 Synchronous Binary Counter with Asynchronous Clear
MM54HC162/MM74HC162 Synchronous Decade Counter with Synchronous Clear
MM54HC163/MM74HC163 Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HC160/MM74HC160, MM54HC161/MM74HC161, MM54HC162/MM74HC162, and MM54HC163/MM74HC163 synchronous presettable counters utilize advanced silicon-gate CMOS technology and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HC160 and the 'HC162 are 4 bit decade counters, and the 'HC161 and the 'HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the low to high transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HC162/MM74HC162 and MM54HC163/MM74HC163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HC160/MM74HC160 and MM54HC161/MM74HC161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

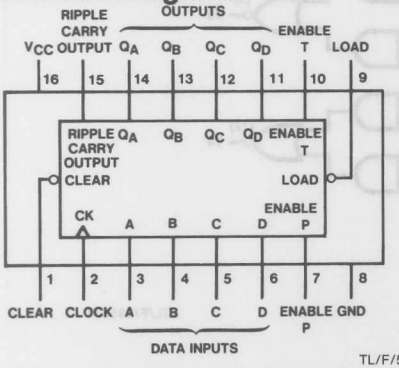
Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40 MHz
- Typical propagation delay; clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V

Connection Diagram



TL/F/5008–1

Order Number MM54HC160/161/162/163* or MM74HC160/161/162/163*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

'HC160/HC161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HC162/HC163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

3

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		43	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to RC		30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		29	34	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, ENT to RC		18	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		27	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	ns
t_H	Minimum Hold Time, Data from Clock			5	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

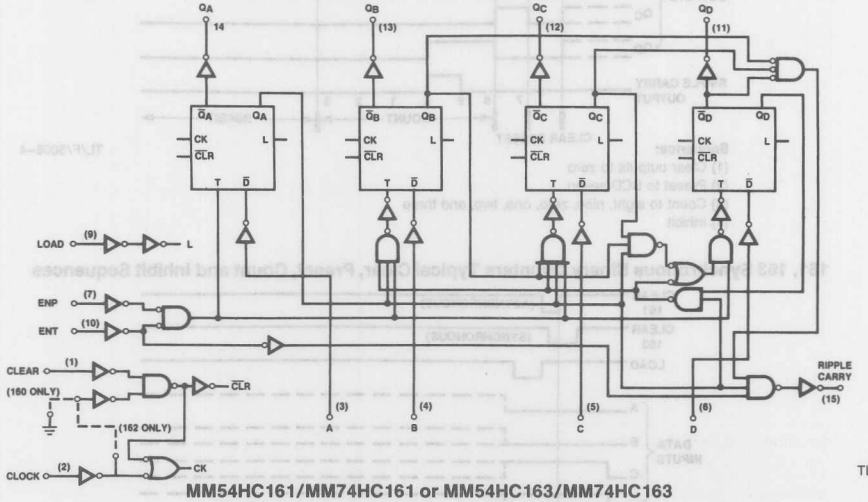
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4	MHz
			4.5V	40	27	21	18	MHz
			6.0V	45	32	25	21	MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		2.0V	100	215	271	320	ns
			4.5V	32	43	54	64	ns
			6.0V	28	37	46	54	ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		2.0V	88	175	220	260	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		2.0V	95	205	258	305	ns
			4.5V	30	41	52	61	ns
			6.0V	26	35	44	52	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V	85	170	214	253	ns
			4.5V	17	34	43	51	ns
			6.0V	14	29	36	43	ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		2.0V	90	195	246	291	ns
			4.5V	28	39	49	58	ns
			6.0V	24	33	42	49	ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		2.0V	80	160	202	238	ns
			4.5V	16	32	40	48	ns
			6.0V	14	27	34	41	ns
t_{PHL}	Maximum Propagation Delay, Clear to RC		2.0V	100	220	275	325	ns
			4.5V	32	44	55	66	ns
			6.0V	28	37	47	55	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		2.0V	100	210	260	315	ns
			4.5V	32	42	52	63	ns
			6.0V	28	36	45	54	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		125	158	186	ns
			4.5V		25	32	37	ns
			6.0V		21	27	32	ns
t_S	Minimum Setup Time Clear or Data to Clock		2.0V		150	190	225	ns
			4.5V		30	38	45	ns
			6.0V		26	32	38	ns
t_S	Minimum Setup Time Load to Clock		2.0V		135	170	200	ns
			4.5V		27	34	41	ns
			6.0V		23	29	35	ns
t_H	Minimum Hold Time Data from Clock		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time Enable, Load or Clear to Clock		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns

				Typ	Guaranteed Limits			
t_W	Minimum Pulse Width Clock, Clear, or Load		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	40	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

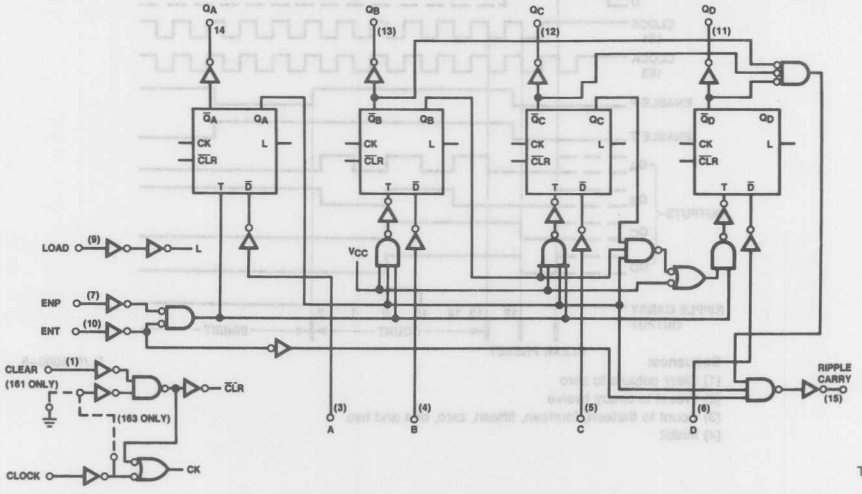
Logic Diagrams

MM54HC160/MM74HC160 or MM54HC162/MM74HC162



TL/F/5008–2

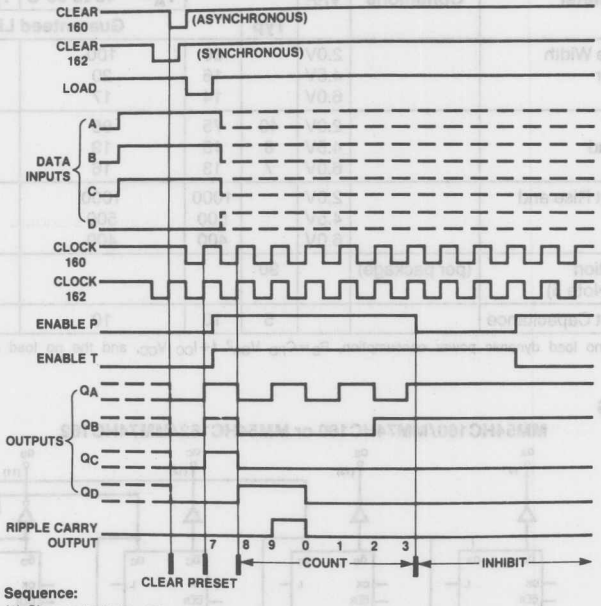
MM54HC161/MM74HC161 or MM54HC163/MM74HC163



TL/F/5008–3

Logic Waveforms

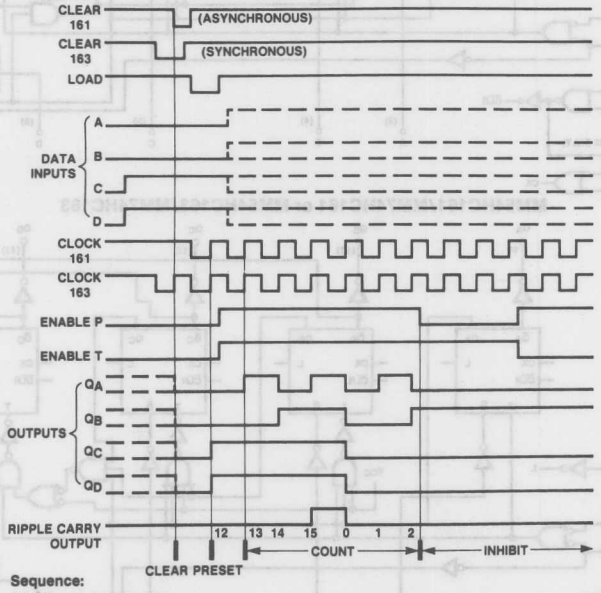
160, 162 Synchronous Decade Counters Typical Clear, Preset, Count and Inhibit Sequences



TL/F/5008–4

Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

161, 163 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences



TL/F/5008–5

Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

National Semiconductor

MM54HC164/MM74HC164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HC164/MM74HC164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-Bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-Bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

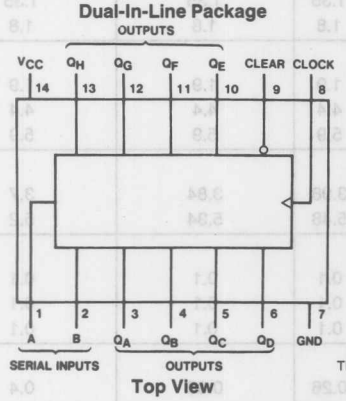
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 19 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

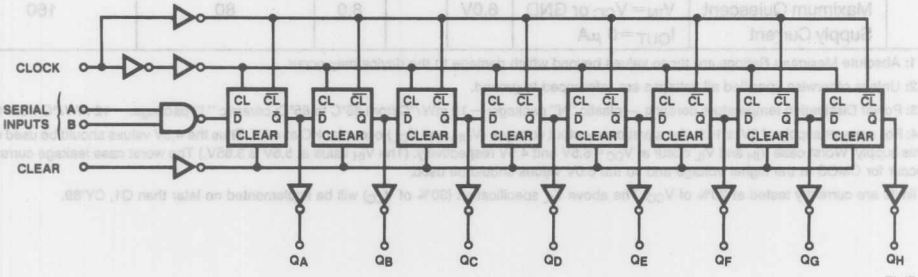


TL/F/5315–1

Top View

Order Number MM54HC164* or MM74HC164*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5315–2

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

3

Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L)	
(Soldering 10 seconds)	260°C

Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		19	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		23	35	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	0	ns
t_S	Minimum Setup Time Data to Clock		12	20	ns
t_H	Minimum Hold Time Clock to Data		1	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	3	MHz
			4.5V	27	21	18	MHz
			6.0V	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V	115	175	218	254	ns
			4.5V	13	35	44	51	ns
			6.0V	20	30	38	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		2.0V	140	205	256	297	ns
			4.5V	28	41	51	59	ns
			6.0V	24	35	44	51	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	−7	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_S	Minimum Setup Time Data to Clock		2.0V	25	100	125	150	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	−2	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	1	5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	22	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V		75	95	110	ns
			4.5V		15	19	22	ns
			6.0V		13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)	5.0V	150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

National Semiconductor

MM54HC165/MM74HC165
Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM54HC165/MM74HC165 high speed PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the SHIFT/LOAD input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

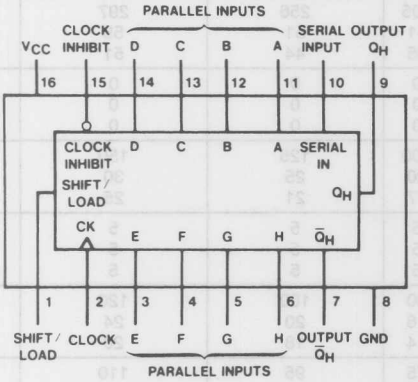
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5316–1

Top View

Order Number MM54HC165* or MM74HC165*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{AN}, Q_{GN} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2–6V	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA V_{CC} = 2–6V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

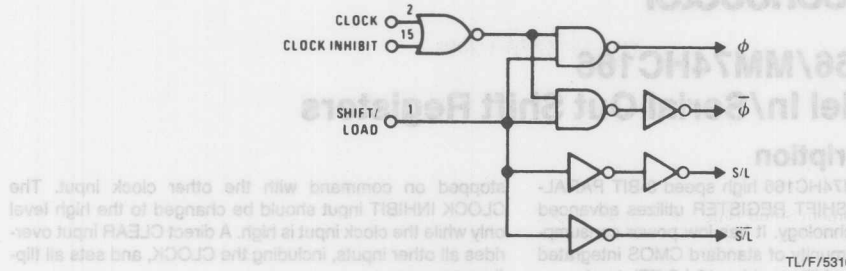
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		10	20	ns
t_S	Minimum Setup Time Serial Input to Clock, Parallel or Data to Shift/Load		11	20	ns
t_S	Minimum Setup Time Shift/Load to Clock		10	20	ns
t_S	Minimum Setup Time Clock Inhibit to Clock			0	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			16	ns
t_W	Minimum Pulse Width Clock				

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

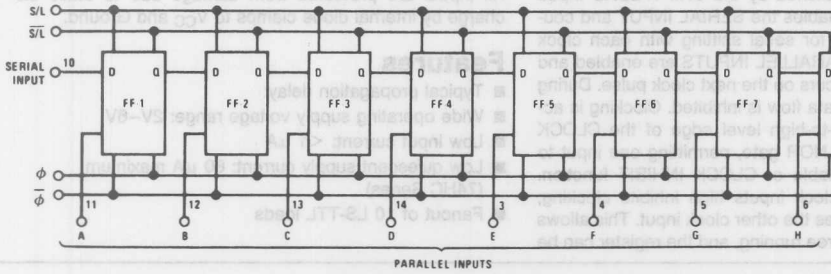
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		2.0V	70	150	189	225	ns
			4.5V	21	30	38	45	ns
			6.0V	18	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/ Parallel Load to Q_H		2.0V	70	175	220	260	ns
			4.5V	21	35	44	52	ns
			6.0V	18	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		2.0V	70	150	189	225	ns
			4.5V	21	30	38	45	ns
			6.0V	18	26	33	39	ns
t_S	Minimum Setup Time Serial Input to Clock, or Parallel Data to Shift/Load		2.0V	35	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time Shift/Load to Clock		2.0V	38	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time Clock Inhibit to Clock		2.0V	35	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width, Clock		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	9	15	19	22	ns
			6.0V	8	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams



TL/F/5316–2



TL/F/5316–3

National Semiconductor

MM54HC166/MM74HC166
8-Bit Parallel In/Serial Out Shift Registers

General Description

The MM54HC166/MM74HC166 high speed 8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These Parallel-In or Serial-In, Serial-Out shift registers feature gated CLOCK inputs and an overriding CLEAR input. The load mode is established by the SHIFT/LOAD input. When high, this input enables the SERIAL INPUT and couples the eight flip-flops for serial shifting with each clock pulse. When low, the PARALLEL INPUTS are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the CLOCK pulse through a 2-input NOR gate, permitting one input to be used as a clock enable or CLOCK INHIBIT function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The CLOCK INHIBIT input should be changed to the high level only while the clock input is high. A direct CLEAR input overrides all other inputs, including the CLOCK, and sets all flip-flops to zero.

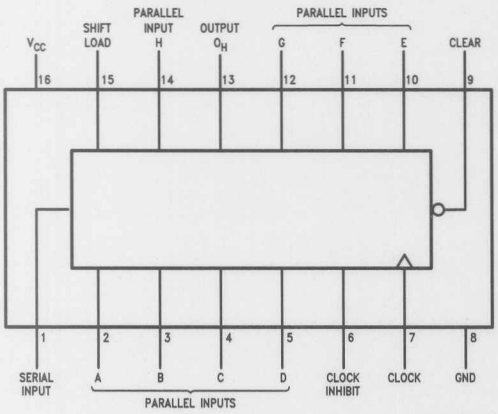
The 54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and Ground.

Features

- Typical propagation delay:
- Wide operating supply voltage range: 2V–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5770–1

Order Number MM54HC166* or MM74HC166*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

a . . . h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to +85°C	54HC T_A = −55°C to +125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7 V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4 V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2V–6V	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA V_{CC} = 2V–6V	6.0V		8.0	80	160 μA

Note 1: Absolute Maximum ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V±10%, the worst-case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus, the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V, respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise noted

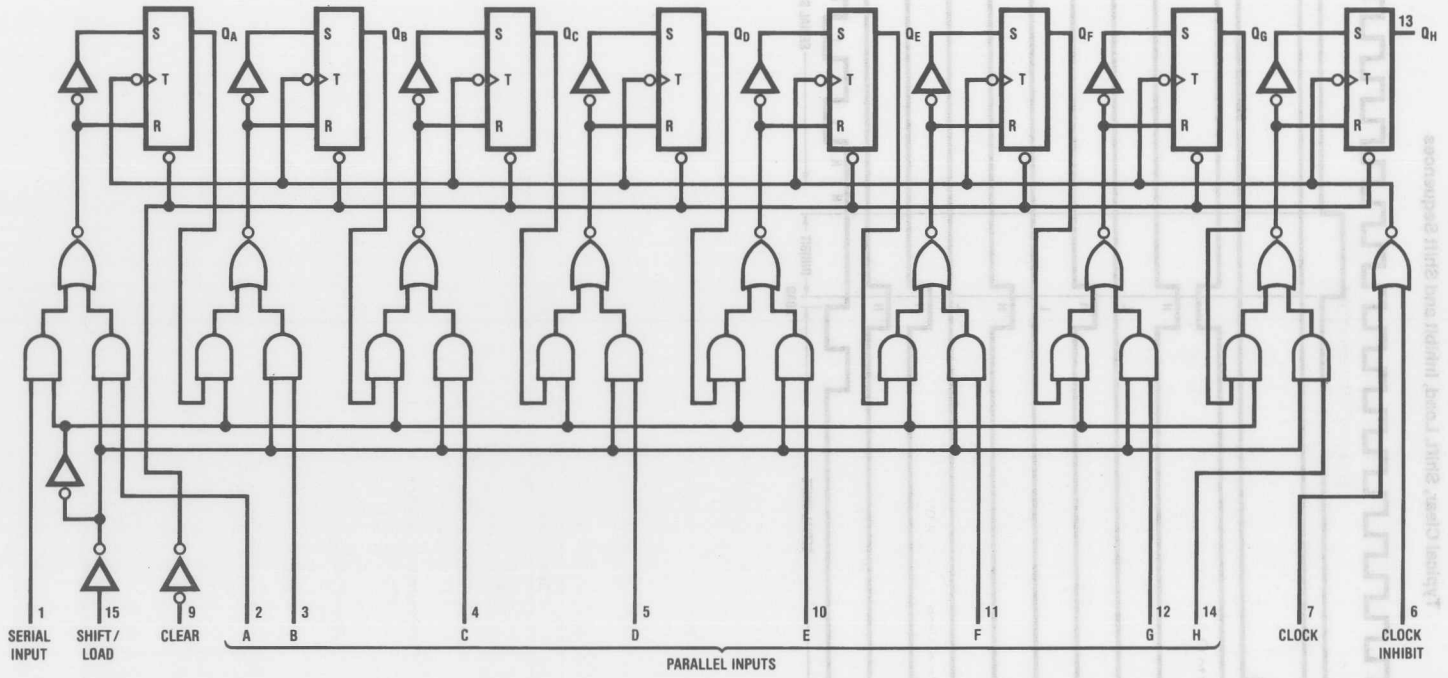
Symbol	Parameter	V_{CC}	$T_A = 25°C$	74HC $T_A = -40°C$ to $+85°C$	54HC $T_A = -55°C$ to $+125°C$	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	2.0V	6	5	4.2	MHz
		4.5V	31	25	21	MHz
		6.0V	36	29	25	MHz
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clock to Q_H	2.0V	140	175	210	ns
		4.5V	28	35	42	ns
		6.0V	24	30	36	ns
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clear to Q_h	2.0V	130	165	195	ns
		4.5V	26	35	39	ns
		6.0V	22	30	33	ns
t_{su}	Minimum Setup Time Shift/Load to Clock	2.0V	80	100	120	ns
		4.5V	16	20	24	ns
		6.0V	14	18	20	ns
t_{su}	Minimum Setup Time Data before Clock	2.0V	80	100	120	ns
		4.5V	16	20	24	ns
		6.0V	14	18	20	ns
t_{REM}	Minimum Removal Time Clear to Clock	2.0V	0	0	0	ns
		4.5V	0	0	0	ns
		6.0V	0	0	0	ns
t_h	Maximum Hold Time Data after Clock	2.0V	0	0	0	ns
		4.5V	0	0	0	ns
		6.0V	0	0	0	ns
t_r, t_f	Maximum Output Rise and Fall Time	2.0V	75	95	110	ns
		4.5V	15	19	22	ns
		6.0V	13	16	19	ns
t_w	Minimum Pulse Width Clock or Clear	2.0V	80	100	120	ns
		4.5V	16	20	24	ns
		6.0V	14	16	20	ns
C_{pd}	Power Dissipation Capacitance (Note 5)	(per package)	100			pF
C_{in}	Maximum Input Capacitance		5	10	10	10	pF

AC Electrical Characteristics $V_{CC} = 5V$, $C_L = 15$ pF, $T_A = 25°C$, $t_r = t_f = 6$ ns unless otherwise noted

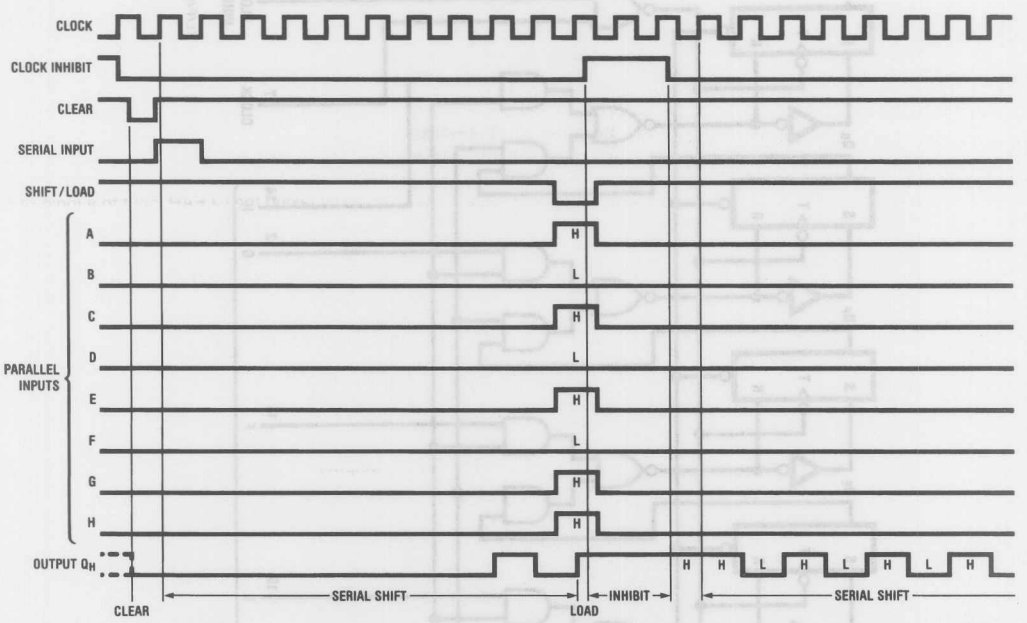
Symbol	Parameter	Typical	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		31	MHz
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clock to Q_h		16	ns
t_{PHL}/ t_{PLH}	Maximum Propagation Delay Clear to Q_h		12	ns
t_{su}	Minimum Setup Time Shift/Load High to Clock		16	ns
t_{su}	Minimum Setup Time Data before Clock		16	ns
t_{REM}	Minimum Removal Time Clear to Clock		0	ns
t_h	Maximum Hold Time Data after Clock		0	ns
t_w	Minimum Pulse Width Clock or Clear		16	ns

Note 5: C_{pd} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5770–2


CLOCK
CLOCK INHIBIT
CLEAR
SERIAL INPUT
SHIFT/LOAD
PARALLEL INPUTS
A
B
C
D
E
F
G
H
OUTPUT Q_H
H
L
H H L H L H L H
CLEAR
SERIAL SHIFT
LOAD
INHIBIT
SERIAL SHIFT

TL/F/5770–3

National Semiconductor

MM54HC173/MM74HC173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54HC173/MM74HC173 is a high speed TRI-STATE QUAD D TYPE FLIP-FLOP that utilizes advanced silicon-gate CMOS technology. It possesses the low power consumption and high noise immunity of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device. The outputs are buffered, allowing this circuit to drive 15 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

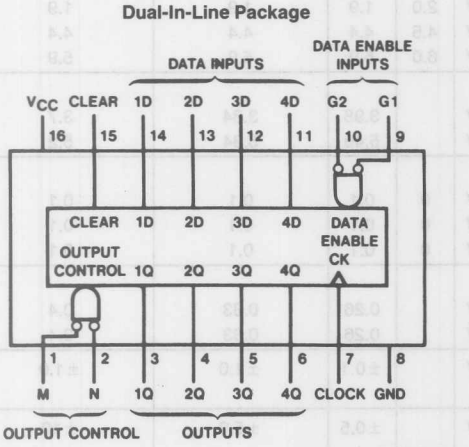
The four D TYPE FLIP-FLOPS operate synchronously from a common clock. The TRI-STATE outputs allow the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip flops to remain in the same state. Clearing is enabled by taking the CLEAR input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating supply voltage range: 2–6V
- TRI-STATE outputs
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 6 mA minimum

Connection Diagram



Top View

Order Number MM54HC173* or MM74HC173*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs					Output
Clear	Clock	Data Enable		Data	Q
		G1	G2	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state: however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q_0 = the level of Q before the indicated steady state input conditions were established

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND Enable = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay: Clock to Q			31	ns
t_{PHL}	Maximum Propagation Delay: Clear to Q		18	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	16	25	ns
t_S	Minimum Data Setup Time			20	ns
t_S	Minimum Data Enable Setup Time			20	ns
t_H	Minimum Data Hold Time			0	ns
t_H	Minimum Data Enable Hold Time			0	ns
t_W	Minimum Clock Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	55	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q	$C_L=50$ pF	2.0V	80	175	220	262	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	23	35	44	53	ns
		$C_L=150$ pF	4.5V	28	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	38	45	ns
		$C_L=150$ pF	6.0V	26	38	48	57	ns
t_{PHL}	Maximum Propagation Delay from Clear to Q	$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ					
		$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	70	150	189	224	ns
			4.5V	20	30	38	45	ns
			6.0V	17	26	32	38	ns
t_S	Minimum Data or Data Enable Setup Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_{REM}	Minimum Removal Time		2.0V		90	112	135	ns
			4.5V		18	22	26	ns
			6.0V		15	19	22	ns
t_H	Minimum Data or Data Enable Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Clear or Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	5	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance	(per flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HC174/MM74HC174 Hex D Flip-Flops with Clear

General Description

These edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

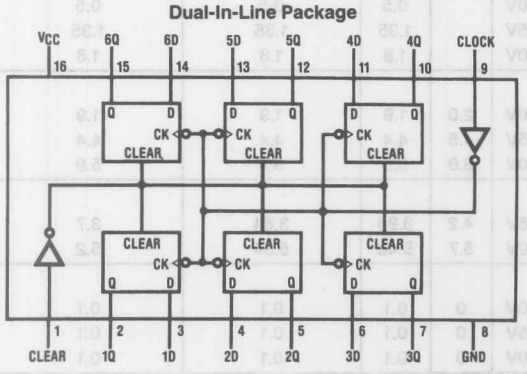
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC174/MM74HC174 is functionally as well as pin compatible to the 54LS174/74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74HC Series)
- Output drive: 10 LSTTL loads

Connection and Logic Diagrams

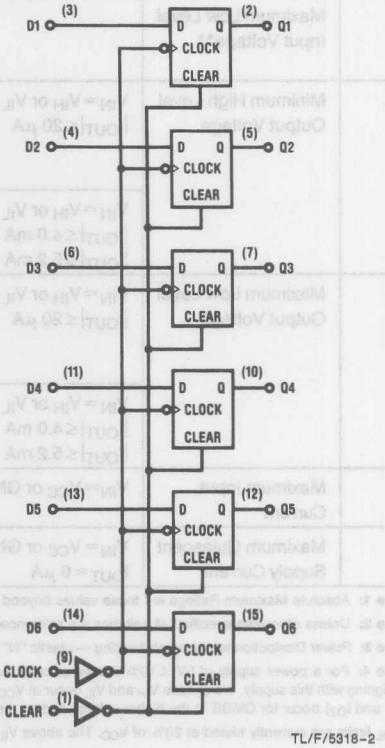
Dual-In-Line Package



TL/F/5318–1

Order Number MM54HC174* or MM74HC174*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5318–2

Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)
L = Low level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady state input conditions were established.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock or Clear to Output		16	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_S	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		0	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	3	MHz
			4.5V	27	21	18	MHz
			6.0V	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock or Clear to Output		2.0V	55	165	206	248	ns
			4.5V	18	33	41	49	ns
			6.0V	16	28	35	42	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t_S	Minimum Setup Time Data to Clock		2.0V	42	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	10	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	35	80	106	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		136				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

MM54HC175/MM74HC175
Quad D-Type Flip-Flop With Clear

General Description

This high speed D-TYPE FLIP-FLOP with complementary outputs utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Information at the D inputs of the MM54HC175/MM74HC175 is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip flop are externally available. All four flip flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four $\overline{Q}$ outputs to a logical "1."

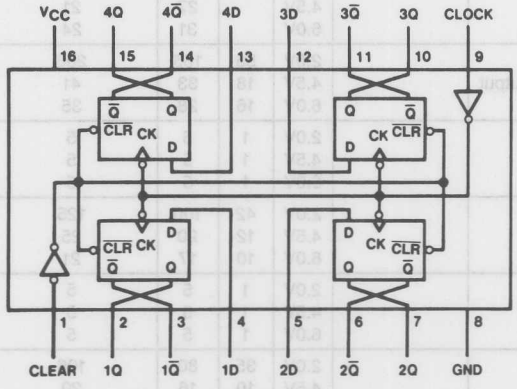
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum (74HC)

Connection Diagram

Dual-In-Line Package



TL/F/5319–1

Top View

Order Number MM54HC175* or MM74HC175*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

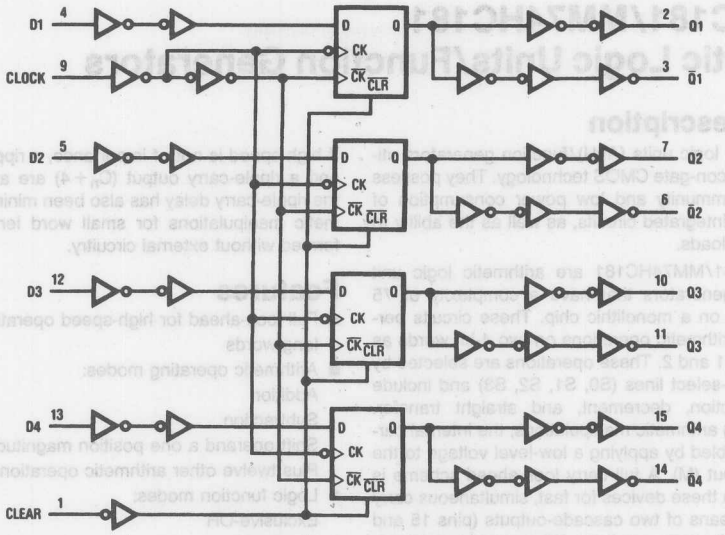
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		60	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		13	21	ns
t_{REC}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Setup Time, Data to Clock			20	ns
t_H	Minimum Hold Time, Data from Clock			0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	12	6	5	4 MHz
			4.5V	60	30	24	20 MHz
			6.0V	70	35	28	24 MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	80	150	190	225 ns
			4.5V	15	30	38	45 ns
			6.0V	13	26	32	38 ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		2.0V	64	125	158	186 ns
			4.5V	14	25	32	37 ns
			6.0V	12	21	27	32 ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		100	125	150 ns
			4.5V		20	25	30 ns
			6.0V		17	21	25 ns
t_S	Minimum Setup Time Data to Clock		2.0V		100	125	150 ns
			4.5V		20	25	30 ns
			6.0V		17	21	25 ns
t_H	Minimum Hold Time Data from Clock		2.0V		0	0	0 ns
			4.5V		0	0	0 ns
			6.0V		0	0	0 ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120 ns
			4.5V	9	16	20	24 ns
			6.0V	8	14	17	20 ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000 ns
			4.5V		500	500	500 ns
			6.0V		400	400	400 ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110 ns
			4.5V	9	15	19	22 ns
			6.0V	8	13	16	19 ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		150			pF
C_{IN}	Maximum Input Capacitance			5	10	10	10 pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5319–2

National Semiconductor

MM54HC181/MM74HC181
Arithmetic Logic Units/Function Generators

General Description

These arithmetic logic units (ALU)/function generators utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The MM54HC181/MM74HC181 are arithmetic logic unit (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the MM54HC182 or MM74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading HC182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the MM54HC182/MM74HC182.

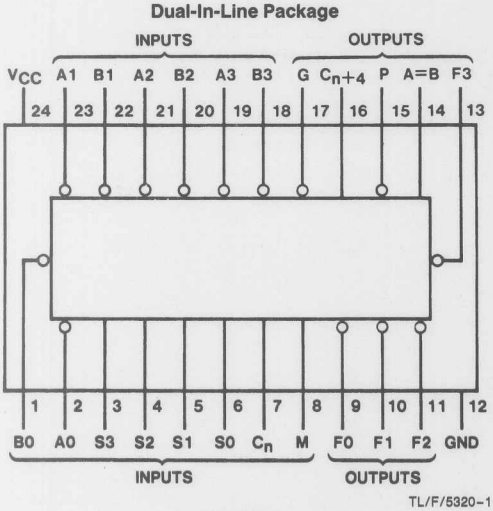
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Features

- Full look-ahead for high-speed operations on long words
- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand a one position magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5320–1

Top View

Order Number MM54HC181* or MM74HC181*

*Please look into Section 8, Appendix D for availability of various package types.

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Outputs
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to produce A—B.

The 181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n=H when performing this comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The MM54HC181/MM74HC181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table 1; those obtained with the signal designations of *Figure 2* are given in Table 2.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table 1)	$\overline{A}$0	$\overline{B}$0	$\overline{A}$1	$\overline{B}$1	$\overline{A}$2	$\overline{B}$2	$\overline{A}$3	$\overline{B}$3	$\overline{F}$0	$\overline{F}$1	$\overline{F}$2	$\overline{F}$3	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_{n+4}	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

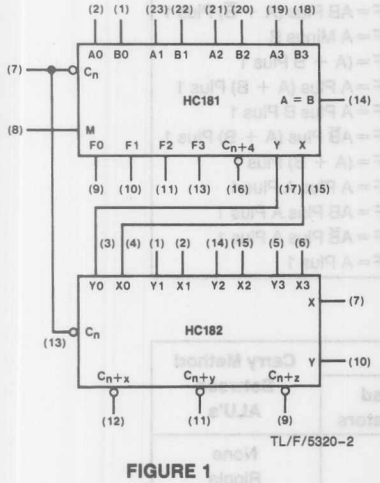


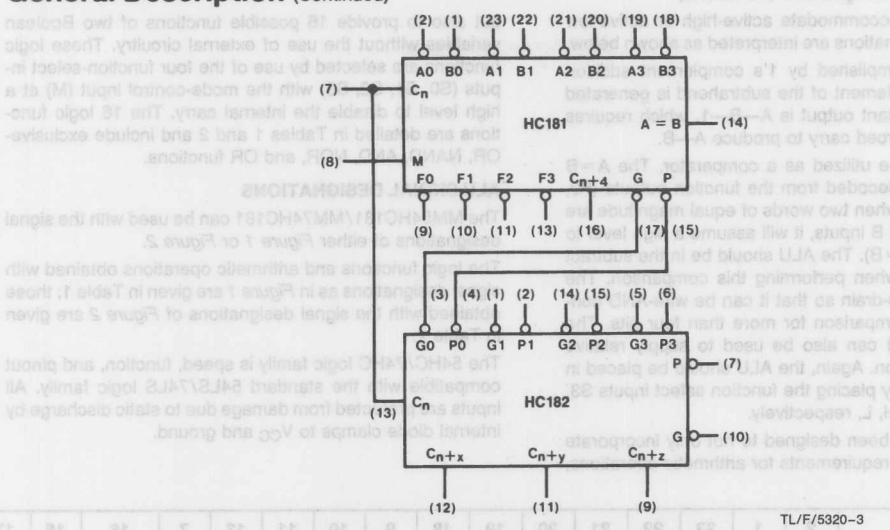
FIGURE 1

Table I

Selection				Active High Data		
				M=H Logic Functions	M=L; Arithmetic Operations	
S3	S2	S1	S0		C_n=H (no carry)	C_n=L (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A Plus 1
L	L	L	H	F=$\overline{A+B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	F=$\overline{A}$B	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Compl)	F=Zero
L	H	L	L	F=$\overline{AB}$	F=A Plus A$\overline{B}$	F=A Plus A$\overline{B}$ Plus 1
L	H	L	H	F=$\overline{B}$	F=(A + B) Plus A$\overline{B}$	F=(A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F=A ⊕ B	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$ + B	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	F=$\overline{A \oplus B}$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\overline{B}$) Plus AB	F=(A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A + $\overline{B}$	F=(A + B) Plus A	F=(A + B) Plus A Plus 1
H	H	H	L	F=A + B	F=(A + $\overline{B}$) Plus A	F=(A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

*Each bit is shifted to the next more significant position.

General Description (Continued)



TL/F/5320–3

FIGURE 2

Table II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A Minus 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	$F = \overline{A} + B$	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	$F = \overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	$F = \overline{A + B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$ Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A + B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage (any output except A = B)	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
I_{LKG}	Maximum Leakage Open Drain Output Current (A = B Output)	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC}	6.0V		0.5	5.0	10	μA
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to C_n+4		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_N+4	M = 0V, S0 = S3 = V_{CC} S1 = S0 = 0V ($\overline{\text{Sum}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_N+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff.}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff.}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	27	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	24	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	19	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = V_{CC} (Logic mode)	25	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	25	37	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to C_n+4		2.0V		125	155	190	ns
			4.5V		25	31	38	ns
			6.0V		22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_n+4	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	110	250	325	375	ns
			4.5V	35	50	63	75	ns
			6.0V	30	43	53	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_n+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V		250	325	375	ns
			4.5V		50	63	75	ns
			6.0V		43	53	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff}}$ mode)	2.0V	65	150	190	225	ns
			4.5V	22	32	40	48	ns
			6.0V	14	28	35	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = V_{CC}, S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	70	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	12	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 ($\overline{\text{Diff}}$ mode)	2.0V	65	165	210	250	ns
			4.5V	23	33	42	50	ns
			6.0V	16	29	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	80	220	275	330	ns
			4.5V	30	44	55	66	ns
			6.0V	25	37	47	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	75	195	244	293	ns
			4.5V	27	39	49	60	ns
			6.0V	24	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V	70	180	225	270	ns
			4.5V	26	36	45	54	ns
			6.0V	21	31	39	47	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V		160	200	290	ns
			4.5V		32	40	48	ns
			6.0V		27	34	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = V_{CC} (Logic mode)	2.0V	180	200	250	300	ns
			4.5V	30	40	50	60	ns
			6.0V	23	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V	180	200	250	300	ns
			4.5V	30	40	50	60	ns
			6.0V	23	34	43	51	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			300				pF
C_{IN}	Maximum Input Capacitance			5	15	15	15	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

Parameter Measurement Information

Logic Mode Test Table Function Inputs: $S1 = S2 = M = V_{CC}$, $S0 = S3 = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase

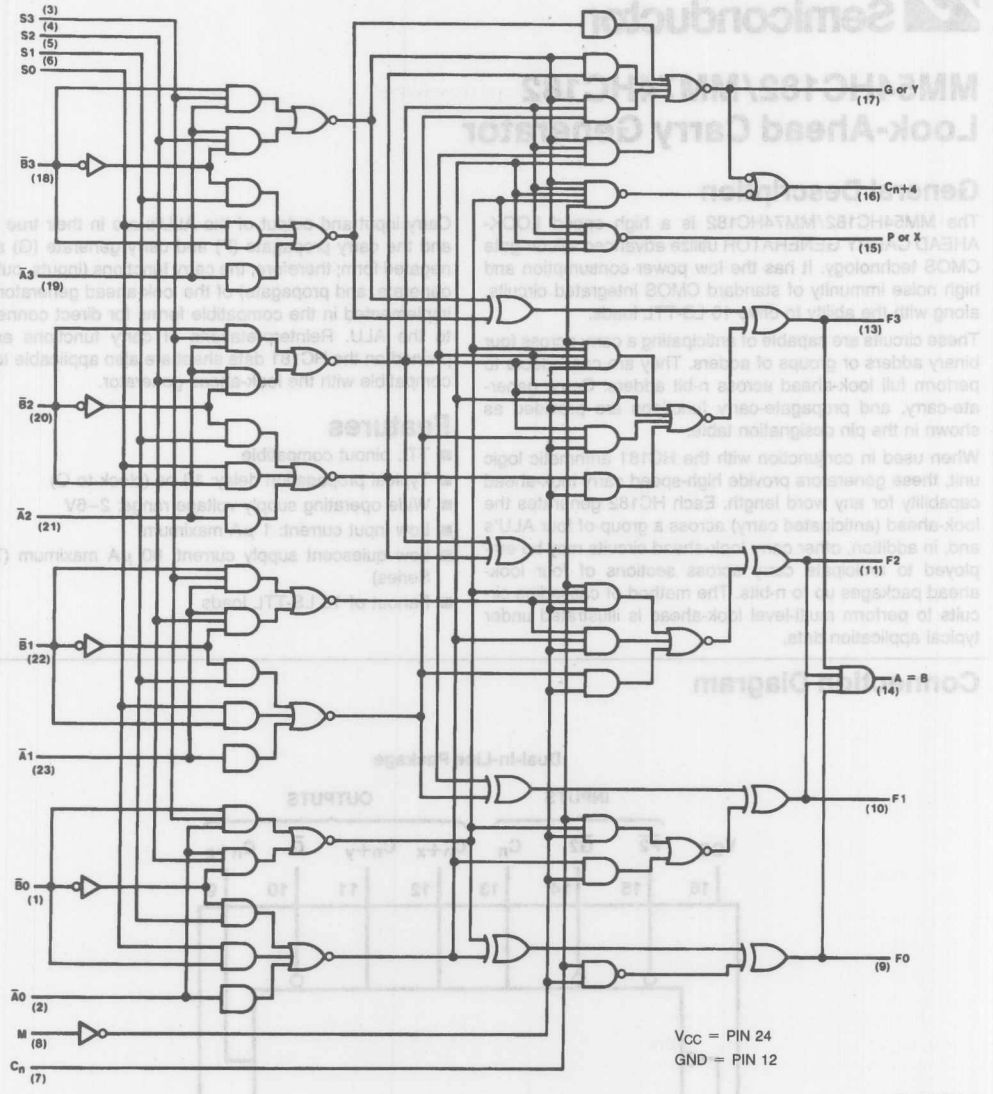
$\overline{\text{SUM}}$ Mode Test Table Function Inputs: $S0 = S3 = V_{CC}$ $S1 = S2 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

$\overline{\text{Diff}}$ Mode Test Table Function Inputs: $S1 = S2 = V_{CC}$, $S0 = S3 = M = 0$ V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram



TL/F/5320–4

National Semiconductor

MM54HC182/MM74HC182 Look-Ahead Carry Generator

General Description

The MM54HC182/MM74HC182 is a high speed LOOK-AHEAD CARRY GENERATOR utilize advanced silicon-gate CMOS technology. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These circuits are capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

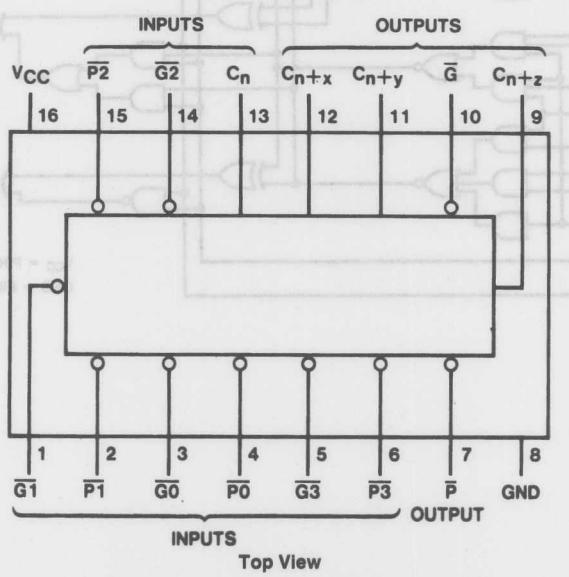
Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator.

Features

- TTL pinout compatible
- Typical propagation delay: 18 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5321–1

Top View

Order Number MM54HC182* or MM74HC182*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	V
						3.7	V
						5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	V
						0.4	V
						0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn to P		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Cn to any output		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn or Gn to any output		23	35	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn to P		2.0V	45	112	140	162	ns
			4.5V	18	28	35	40	ns
			6.0V	15	22	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cn to any output		2.0V	50	125	156	182	ns
			4.5V	20	30	37	44	ns
			6.0V	16	24	30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn or Gn to any output		2.0V	62	155	194	225	ns
			4.5V	25	37	46	54	ns
			6.0V	22	33	42	48	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance			150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Equations

$C_{n+x}=G0+P0\,C_n$

$C_{n+y}=G1+P1\,G0+P1\,P0\,C_n$

$C_{n+z}=G2+P2\,G1+P2\,P1\,P0\,C_n$

$\overline{G}=\overline{G3+P3\,G2+P3\,P2\,G1+P3\,P2\,P1\,G0}$

$\overline{P}=\overline{P3\,P2\,P1\,P0}$

or

$\overline{C}_{n+x}=\overline{Y0\,(X0+C_n)}$

$\overline{C}_{n+y}=\overline{Y1\,[X1+Y0\,(X0+C_n)]}$

$\overline{C}_{n+z}=\overline{Y2\,\{X2+Y1\,[X1+Y0\,(X0+C_n)]\}}$

$Y=Y3\,(X3+Y2)\,(X3+X2+Y1)\,(X3+X2+X1+Y0)$

$X=X3+X2+X1+X0$

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

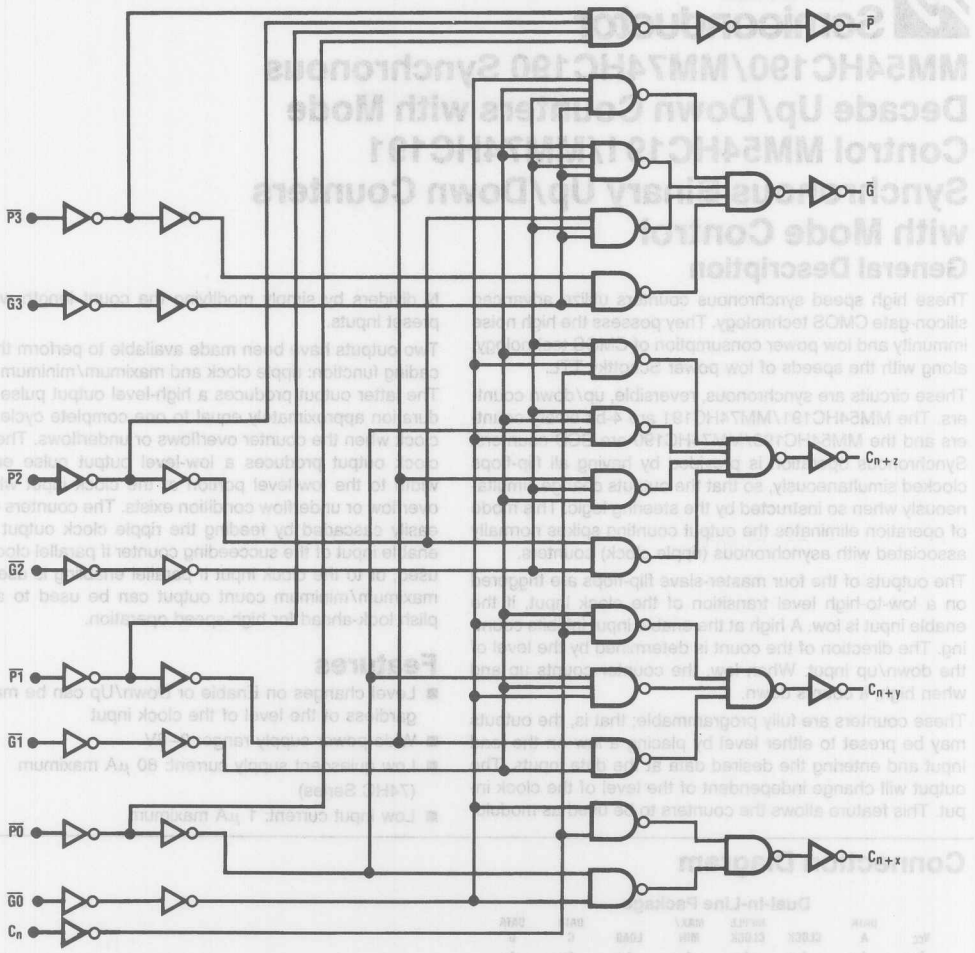
FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

H = high level L = low level X = irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

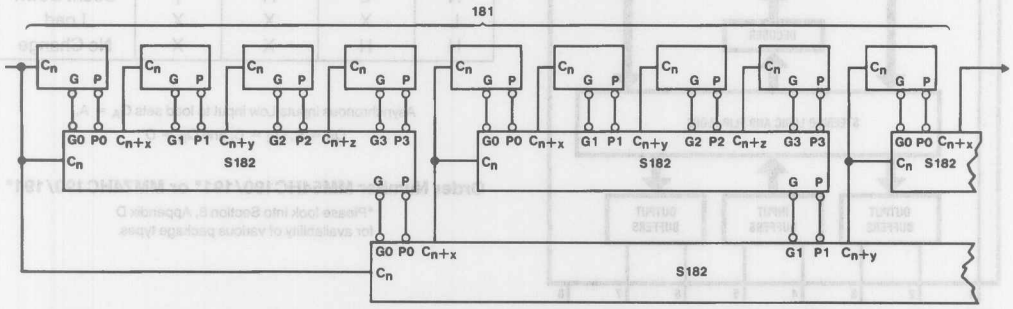
Logic Diagram



TL/F/5321–2

Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs, and F outputs of 181 are not shown.

TL/F/5321–3

MM54HC190/MM74HC190 Synchronous Decade Up/Down Counters with Mode Control MM54HC191/MM74HC191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL.

These circuits are synchronous, reversible, up/down counters. The MM54HC191/MM74HC191 are 4-bit binary counters and the MM54HC190/MM74HC190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

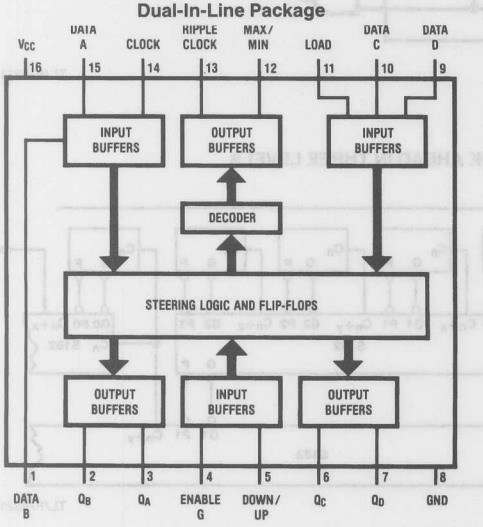
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Level changes on Enable or Down/Up can be made regardless of the level of the clock input
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5322–1

Top View

Load	Enable G	Down/ Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Asynchronous inputs Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

Order Number MM54HC190/191* or MM74HC190/191*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

3

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Typ	Units
f_{MAX}	Maximum Clock Frequency			40	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D	27	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock	16	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D	24	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock	29	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min	22	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock	22	ns
t_W	Minimum Clock, Clear or Load Input Pulse Width			10	ns

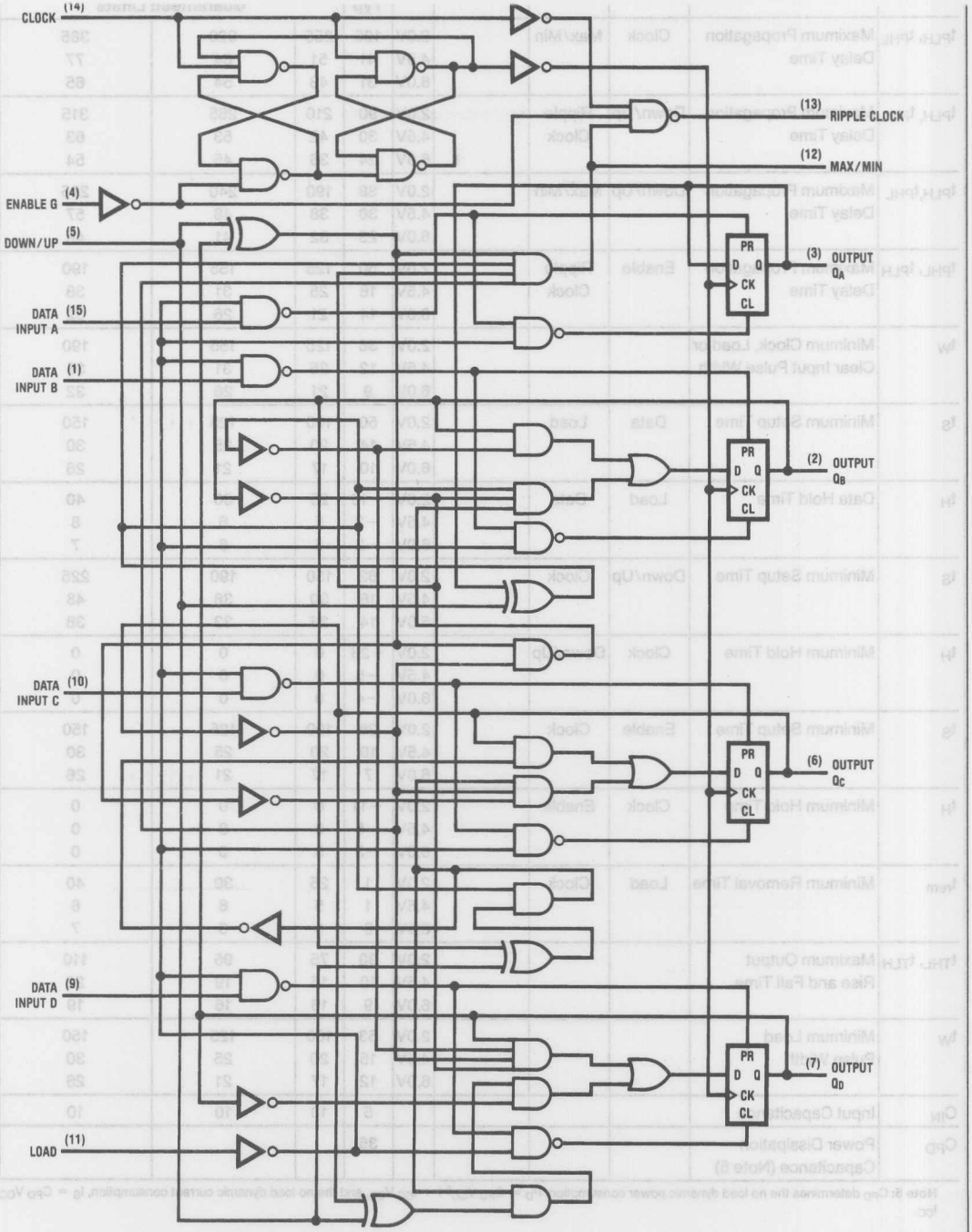
AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
					Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency			2.0V	9	4.0	3.5	2.6 MHz
				4.5V	30	20	16	13 MHz
				6.0V	36	24	19	15 MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D	2.0V	80	220	275	330 ns
				4.5V	27	44	55	66 ns
				6.0V	21	37	47	56 ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D	2.0V	71	200	250	300 ns
				4.5V	25	40	50	60 ns
				6.0V	19	34	43	51 ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock	2.0V	44	125	155	190 ns
				4.5V	25	25	31	38 ns
				6.0V	14	21	26	32 ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D	2.0V	83	215	270	325 ns
				4.5V	29	43	54	65 ns
				6.0V	22	37	46	55 ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		2.0V	125	255	320	385	ns
					4.5V	41	51	64	77	ns
					6.0V	31	43	54	65	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		2.0V	90	210	265	315	ns
					4.5V	30	42	53	63	ns
					6.0V	24	36	45	54	ns
t_{PLH},t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		2.0V	88	190	240	285	ns
					4.5V	30	38	48	57	ns
					6.0V	23	32	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock		2.0V	50	125	155	190	ns
					4.5V	18	25	31	38	ns
					6.0V	14	21	26	32	ns
t_W	Minimum Clock, Load or Clear Input Pulse Width				2.0V	36	125	155	190	ns
					4.5V	12	25	31	38	ns
					6.0V	9	21	26	32	ns
t_S	Minimum Setup Time	Data	Load		2.0V	50	100	125	150	ns
					4.5V	14	20	25	30	ns
					6.0V	10	17	21	26	ns
t_H	Data Hold Time	Load	Data		2.0V	−16	25	30	40	ns
					4.5V	−3	5	6	8	ns
					6.0V	−2	5	6	7	ns
t_S	Minimum Setup Time	Down/Up	Clock		2.0V	62	150	190	225	ns
					4.5V	18	30	38	48	ns
					6.0V	14	26	33	38	ns
t_H	Minimum Hold Time	Clock	Down/Up		2.0V	−23	0	0	0	ns
					4.5V	−5	0	0	0	ns
					6.0V	−4	0	0	0	ns
t_S	Minimum Setup Time	Enable	Clock		2.0V	28	100	125	150	ns
					4.5V	10	20	25	30	ns
					6.0V	7	17	21	26	ns
t_H	Minimum Hold Time	Clock	Enable		2.0V	−11	0	0	0	ns
					4.5V	−5	0	0	0	ns
					6.0V	−3	0	0	0	ns
t_{rem}	Minimum Removal Time	Load	Clock		2.0V	1	25	30	40	ns
					4.5V	1	5	6	8	ns
					6.0V	0	5	6	7	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time				2.0V	30	75	95	110	s
					4.5V	10	15	19	22	ns
					6.0V	9	13	16	19	ns
t_W	Minimum Load Pulse Width				2.0V	53	100	125	150	ns
					4.5V	15	20	25	30	ns
					6.0V	12	17	21	26	ns
C_{IN}	Input Capacitance					5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)					35				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

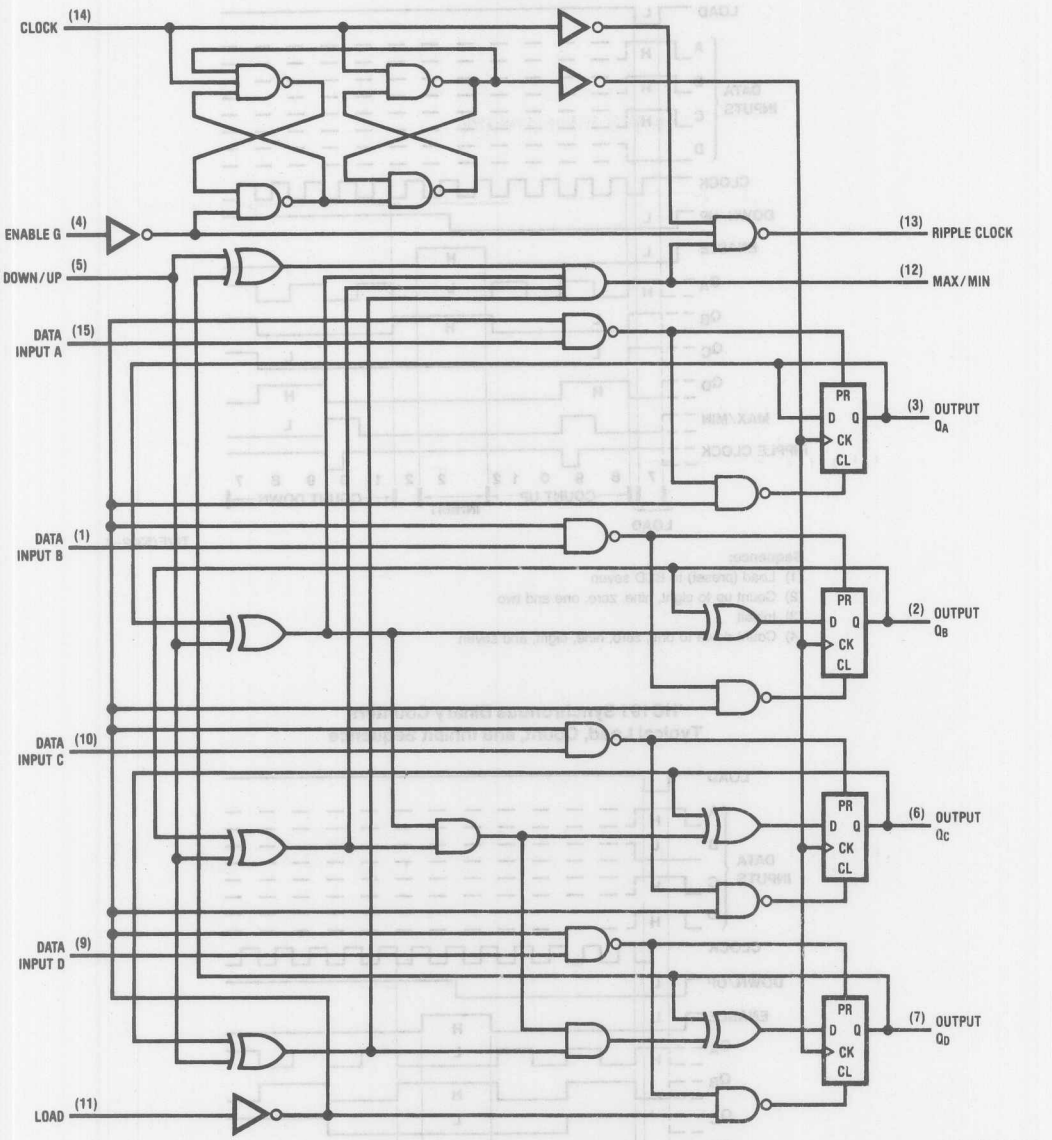


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/5322–2

Logic Diagrams (Continued)

'HC191 Binary Counters

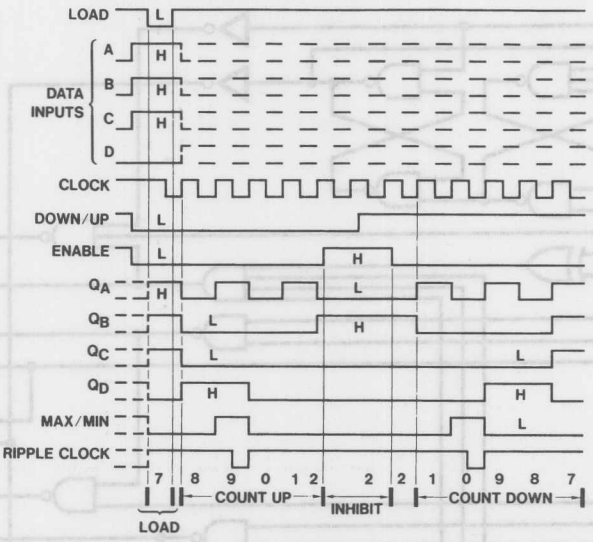


TL/F/5322–3

Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

'HC190 Synchronous Decade Counters
Typical Load, Count, and Inhibit Sequences

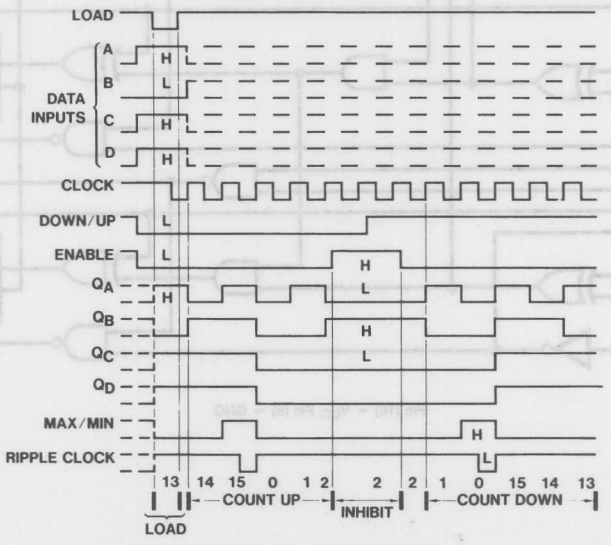


TL/F/5322–4

Sequence:

(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

'HC191 Synchronous Binary Counters
Typical Load, Count, and Inhibit Sequence



TL/F/5322–5

Sequence:

(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

National Semiconductor

MM54HC192/MM74HC192 Synchronous Decade Up/Down Counters
MM54HC193/MM74HC193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HC192/MM74HC192 is a decade counter, and the MM54HC193/MM74HC193 is a binary counter. Both counters have two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition both counters can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

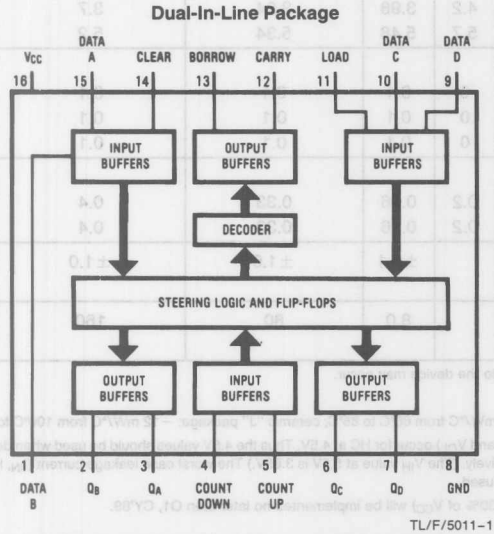
Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counters can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Count up to Q: 28 ns
- Typical operating frequency: 27 MHz
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 4 mA output drive

Connection Diagram



TL/F/5011–1

Order Number MM54HC192/193* or MM74HC192/193*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level
L = low level
↑ = transition from low-to-high
X = don't care

3

Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V
			4.5V	3.15	3.15	3.15	V
			6.0V	4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V
			4.5V	1.35	1.35	1.35	V
			6.0V	1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Symbol	Parameter	Conditions		Typ	Limit	Units
f_{MAX}	Maximum Clock Frequency	Count Up		27	20	MHz
		Count Down		31	24	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry		17	26	ns
t_{PHL}	Maximum Propagation Delay High to Low			18	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Down to Borrow		16	24	ns
t_{PHL}	Maximum Propagation Delay High to Low			15	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q		28	40	ns
t_{PHL}	Maximum Propagation Delay High to Low			36	52	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q		30	42	ns
t_{PHL}	Maximum Propagation Delay High to Low			40	55	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q		35	47	ns
t_W	Minimum Pulse Width	Clear	'HC192	40	52	ns
			'HC193	20	26	ns
		Load	'HC192	40	52	ns
			'HC193	10	20	ns
		Count Up/Down		15	22	ns
t_{SD}	Minimum Setup time	Data to Load		10	20	ns
t_{HD}	Minimum Hold Time			−3	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock			10	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency	Count Up	2.0V	5	3	2.5	2	MHz
			4.5V	25	18	14	12	MHz
			6.0V	29	20	16	13	MHz
		Count Down	2.0V	5	4	3	2	MHz
			4.5V	27	20	16	11	MHz
			6.0V	31	23	18	12	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry	2.0V	30	140	175	210	ns
			4.5V	13	28	35	42	ns
			6.0V	11	24	30	36	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns

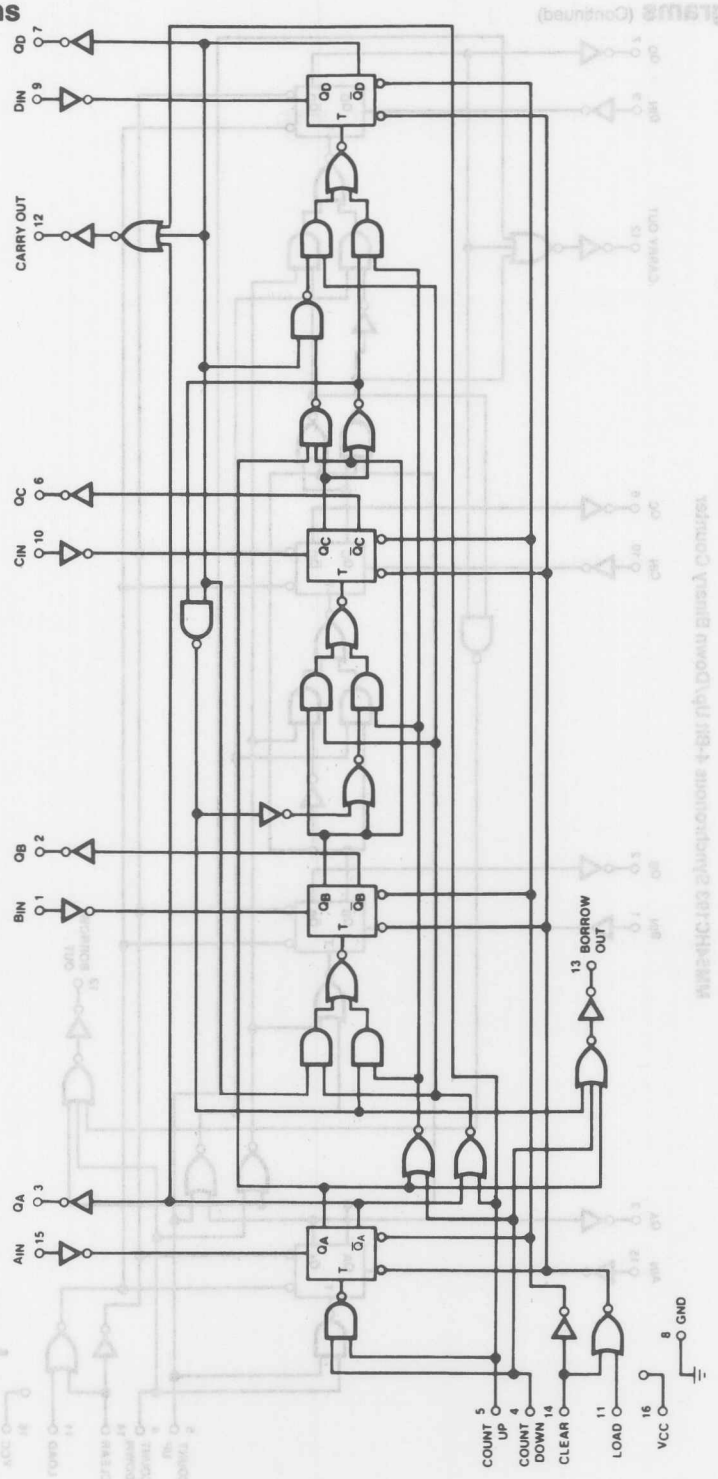
AC Electrical Characteristics (Continued) V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay	Count Down to Borrow	2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q	2.0V	77	215	269	323	ns
			4.5V	35	43	54	65	ns
			6.0V	30	37	46	55	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	95	275	344	413	ns
			4.5V	45	55	69	83	ns
			6.0V	38	47	59	71	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q	2.0V	85	230	288	345	ns
			4.5V	37	46	58	69	ns
			6.0V	30	39	49	59	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	102	290	363	435	ns
			4.5V	47	58	73	87	ns
			6.0V	39	49	61	74	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q	2.0V	85	265	331	398	ns
			4.5V	42	53	66	80	ns
			6.0V	38	45	56	68	ns
t_W	Minimum Pulse Width	Clear or Load 'HC192	2.0V	119	260	325	390	ns
			4.5V	42	52	65	78	ns
			6.0V	38	45	56	68	ns
		Load 'HC193	2.0V	31	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	26	ns
		Count Up/Down	2.0V	43	110	138	165	ns
			4.5V	17	22	28	33	ns
			6.0V	15	19	24	29	ns
		Clear 'HC193	2.0V	70	130	163	195	ns
			4.5V	21	26	33	39	ns
			6.0V	19	22	28	33	ns
t_{SD}	Minimum Setup Time	Data To Load	2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	22	25	ns
t_{HD}	Minimum Hold Time		2.0V	−30	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock	2.0V	−20	10	10	10	ns
			4.5V	−3	10	10	10	ns
			6.0V	−2	10	10	10	ns
t_r, t_f	Maximum Count Up or Down Input Rise & Fall Time		2.0V		500	500	500	ns
			4.5V		300	300	300	ns
			6.0V		200	200	200	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

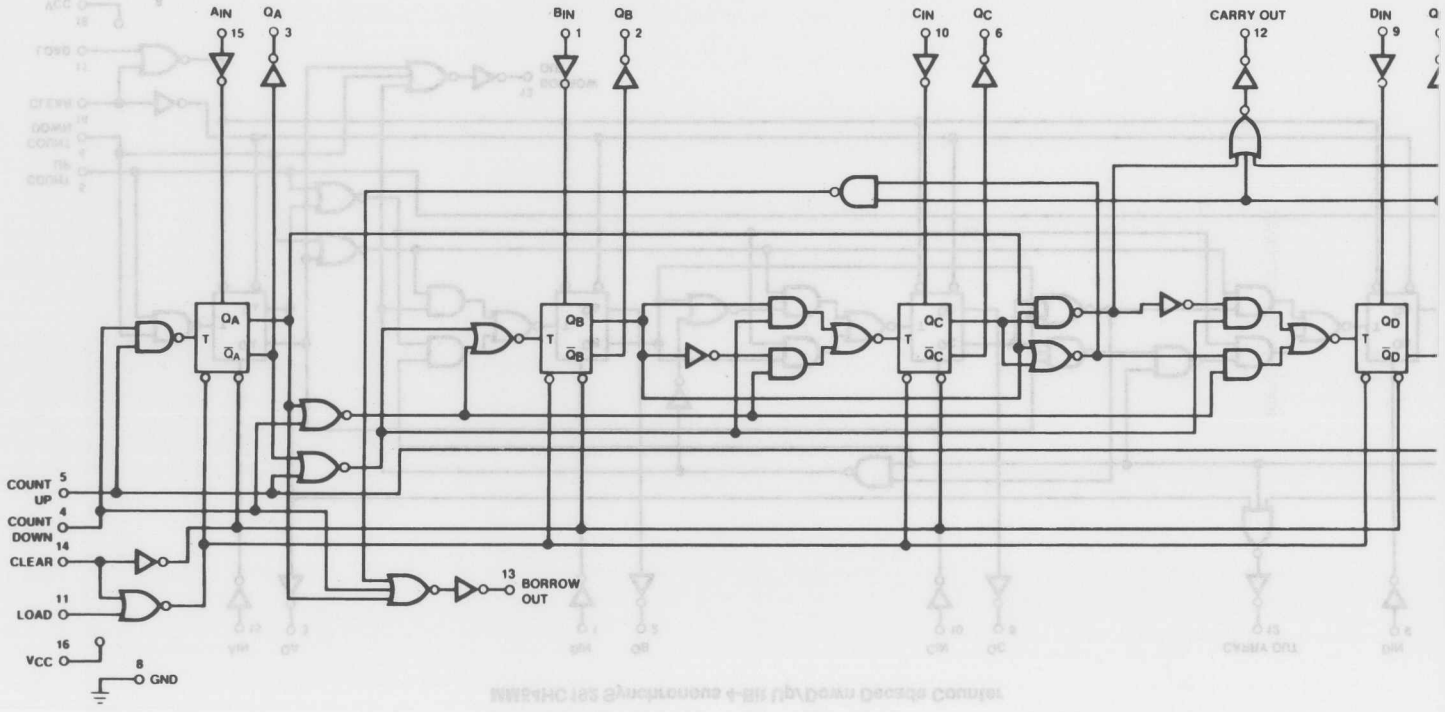
Logic Diagrams

MM54HC192 Synchronous 4-Bit Up/Down Decade Counter



TL/F/5011–2

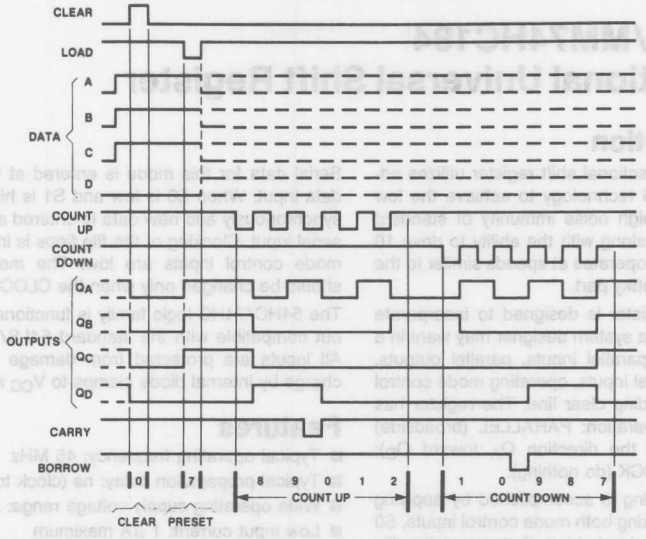
MM54HC193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/

Logic Waveforms

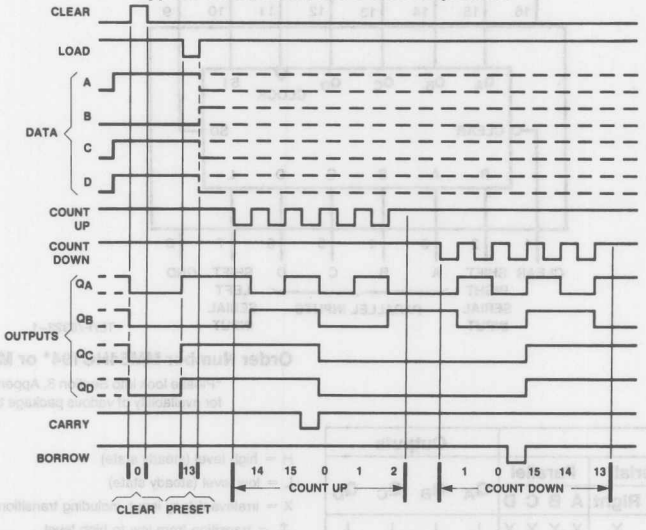
'HC192 Synchronous Decade Counters
Typical Clear, Load, and Count Sequences



TL/F/5011–4

Sequences:
(1) Clear outputs to zero
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

'HC193 Synchronous Binary Counters
Typical Clear, Load, and Count Sequences



TL/F/5011–5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

MM54HC194/MM74HC194
4-Bit Bidirectional Universal Shift Register

General Description

This 4-bit high speed bidirectional shift register utilizes advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads. This device operates at speeds similar to the equivalent low power Schottky part.

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: PARALLEL (broadside) LOAD; SHIFT RIGHT (in the direction Q_A toward Q_D); SHIFT LEFT; INHIBIT CLOCK (do nothing).

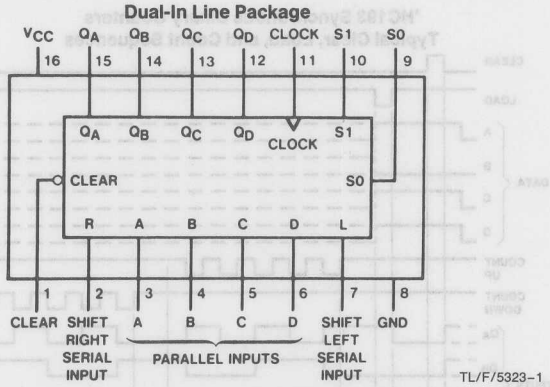
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into their respective flip flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 160 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5323–1

Order Number MM54HC194* or MM74HC194*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S2		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

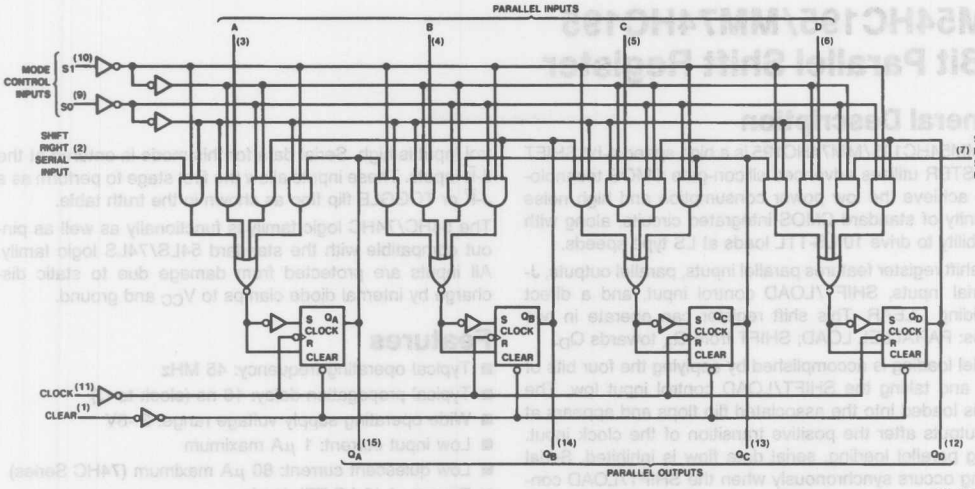
	Frequency				
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		17	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		19	25	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			5	ns
t_S	Minimum Setup Time (A, B, C, D to Clock)			20	ns
t_S	Minimum Setup Time Mode Controls to Clock			20	ns
t_W	Minimum Pulse Width Clock or Reset		9	16	ns
t_H	Minimum Hold Time any Input		−3	0	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

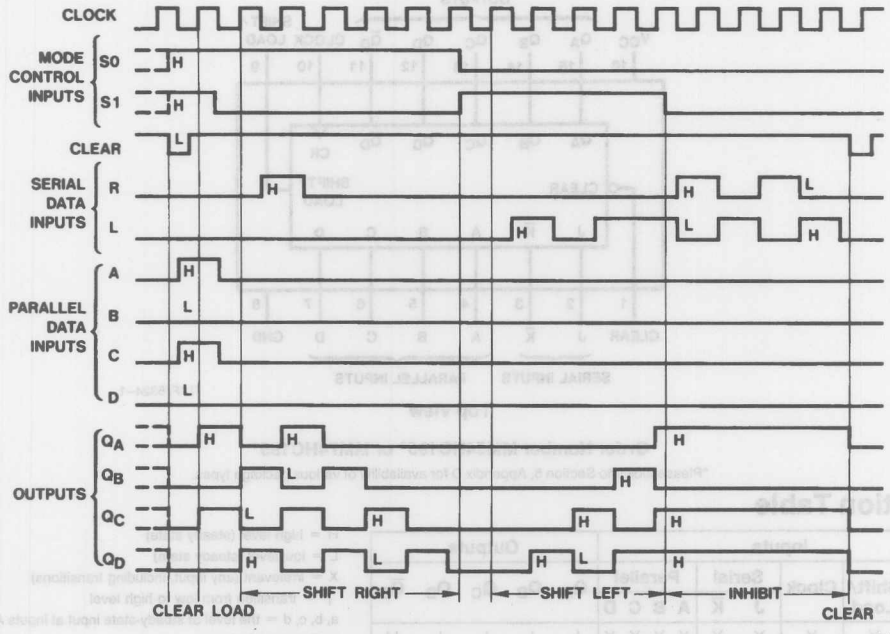
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ		Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V	70	145	183	216	ns
			4.5V	15	29	37	45	ns
			6.0V	12	25	31	37	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		2.0V	80	150	189	216	ns
			4.5V	15	30	37	45	ns
			6.0V	12	26	31	37	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{REM}	Minimum Removal Time Reset Inactive to Clock		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_S	Minimum Set Up Time (A, B, C, or D to Clock)		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Time Mode Controls to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time any Input		2.0V	−10	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Reset		2.0V	30	80	100	120	ns
			4.5V	89	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			77				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic and Timing Diagrams



TL/F/5323–2



TL/F/5323–3

National Semiconductor

MM54HC195/MM74HC195
4-Bit Parallel Shift Register

General Description

The MM54HC195/MM74HC195 is a high speed 4-bit SHIFT REGISTER utilizes advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads at LS type speeds.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, SHIFT/LOAD control input, and a direct overriding CLEAR. This shift register can operate in two modes: PARALLEL LOAD; SHIFT from Q_A towards Q_D.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/LOAD control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/LOAD control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truth table.

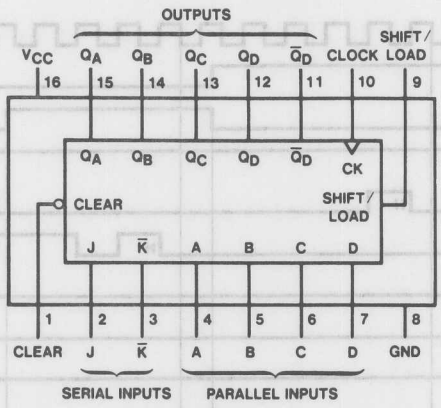
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: 16 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5324–1

Top View

Order Number MM54HC195* or MM74HC195*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

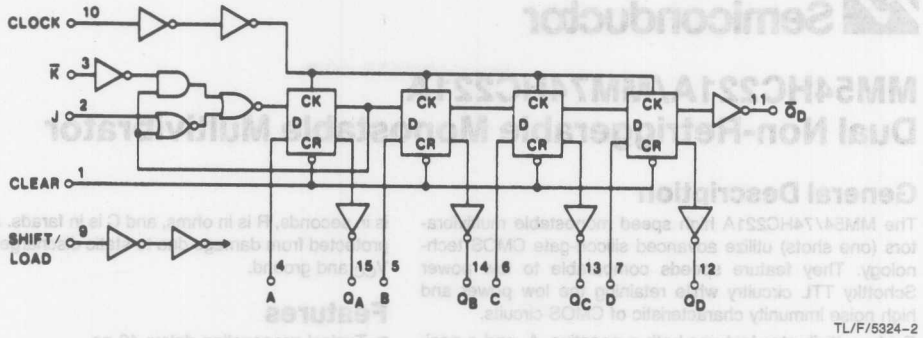
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		14	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		16	25	ns
t_{REM}	Minimum Removal Time, Shift/Load to Clock			0	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			5	ns
t_S	Minimum Setup Time, (A, B, C, D, J, $\overline{K}$ to Clock)			20	ns
t_S	Minimum Setup Time, Shift/Load to Clock			20	ns
t_W	Minimum Pulse Width Clock or Reset			16	ns
t_H	Minimum Hold Time, any Input except Shift/Load			0	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

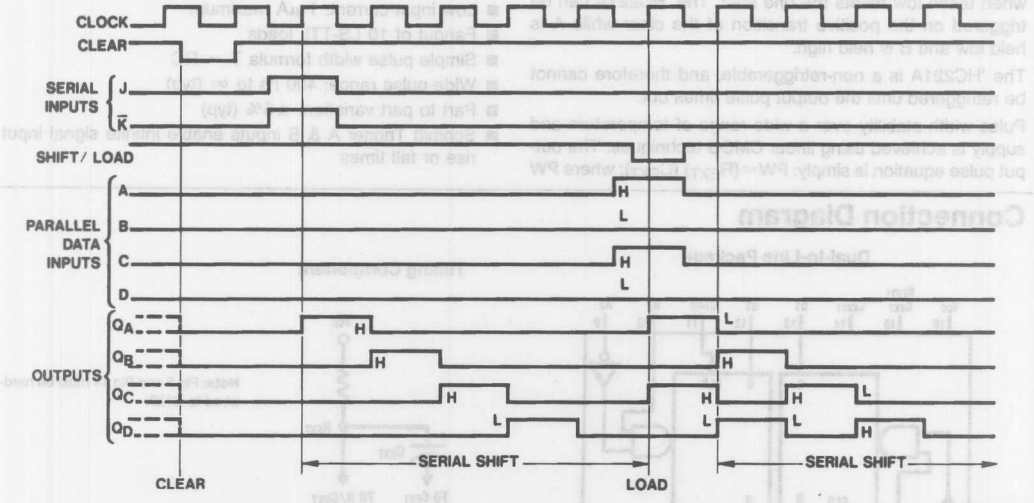
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		2.0V	70	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	12	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	70	145	183	216	ns
			4.5V	15	29	37	43	ns
			6.0V	12	25	31	37	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{REM}	Minimum Removal Time, Shift Load to Clock		2.0V	−2	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_S	Minimum Setup Time, (A, B, C, D, J, $\overline{K}$ to Clock)		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Setup Time, Shift/Load to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time any Input except Shift/Load		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_W	Minimum Pulse Width, Clock or Reset		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic and Timing Diagrams



TL/F/5324–2



TL/F/5324–3

National Semiconductor

MM54HC221A/MM74HC221A
Dual Non-Retriggerable Monostable Multivibrator

General Description

The MM54/74HC221A high speed monostable multivibrators (one shots) utilize advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC221A can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC221A is a non-retriggerable, and therefore cannot be retriggered until the output pulse times out.

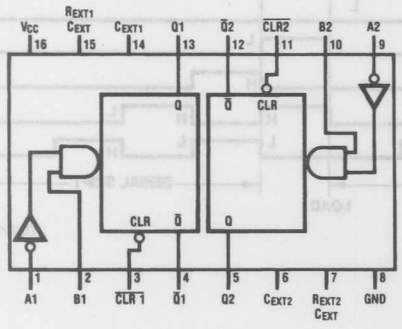
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise or fall times

Connection Diagram

Dual-In-Line Package



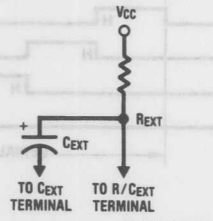
TL/F/5325–1

Top View

Order Number MM54HC221A* or MM74HC221A*

*Please look into Section 8,
Appendix D for availability of various package types.

Timing Component



TL/F/5325–2

Note: Pin 6 and Pin 14 must be hard-wired to GND.

Truth Table

Inputs			Outputs	
$\overline{\text{Clear}}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎏
H	↓	H	⎍	⎏
↑	L	H	⎍	⎏

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎏ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Maximum Input Rise and Fall Time (Clear Input)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN} = V_{CC} or GND	6.0V		±0.5	±5.0	±5.0	μA
I_{IN}	Maximum Input Current (all other pins)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (standby)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN} = V_{CC} or GND R/C_{EXT} = 0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

3

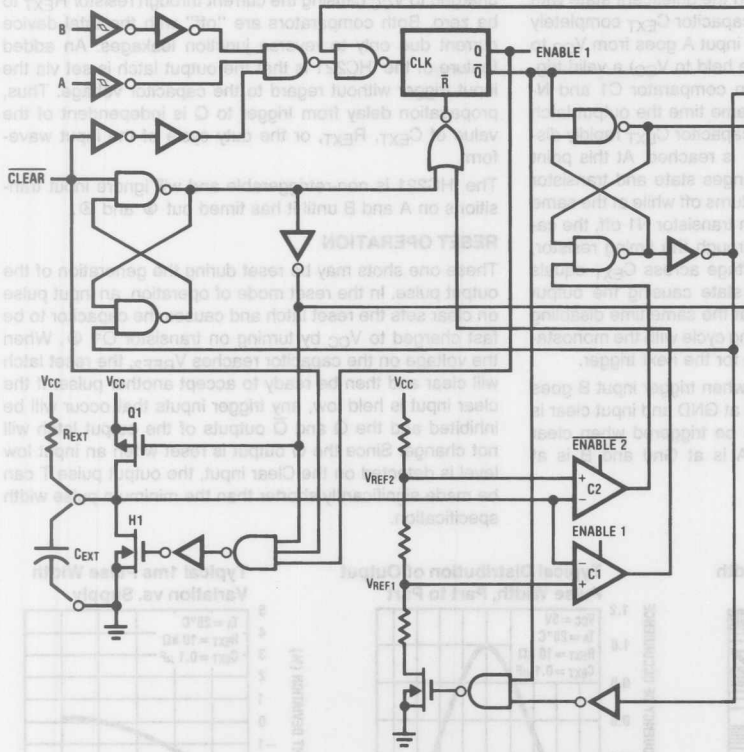
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	36	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		20	31	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns(unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	ns
				6.0V	21	32	39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	ns
				6.0V	24	38	46	51	ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	ns
				6.0V	19	28	33	36	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	ns
				6.0V	20	29	34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	ns
				6.0V	12	21	27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V		0	0	0	ns
				4.5V		0	0	0	ns
				6.0V		0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF		2.0V	1.5				μs
		$R_{EXT}=2$ kΩ		4.5V	450				ns
		$R_{EXT}=6$ kΩ ($V_{CC}=2V$)		6.0V	380				ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	5.0V	1	0.9	0.86	0.85	ms
			Max	5.0V	1	1.1	1.14	1.15	ms
C_{PD}	Power Dissipation Capacitance (Note 5)				87				pF
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (other inputs)				6	10	10	10	pF

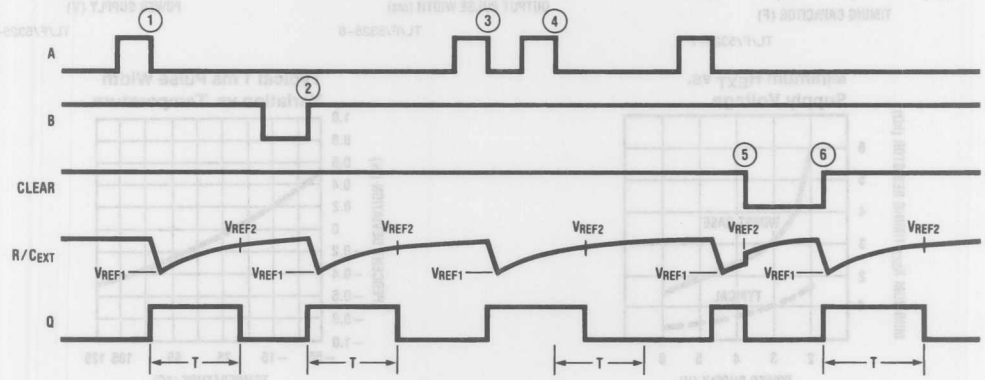
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2 f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC} f+I_{CC}$.

Logic Diagram



TL/F/5325–5

Theory of Operation



TL/F/5325–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ NO RETRIGGERING
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER

FIGURE 1

3

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC} ②). The 'HC221 can also be triggered when clear goes from GND to V_{CC} (while A is at Gnd and B is at V_{CC} ⑤).

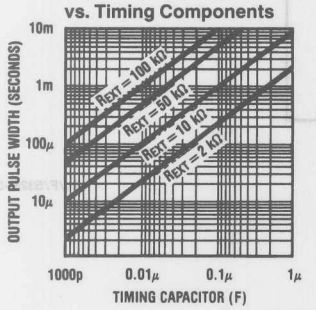
It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC221 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

The 'HC221 is non-retriggerable and will ignore input transitions on A and B until it has timed out ③ and ④.

RESET OPERATION

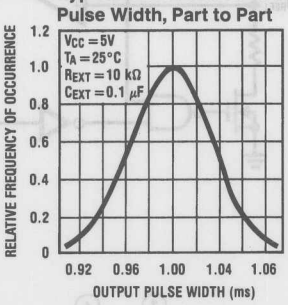
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



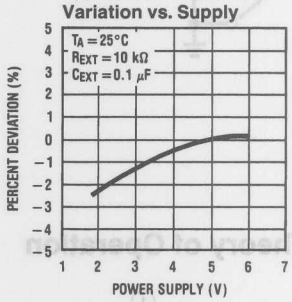
TL/F/5325–7

Typical Distribution of Output Pulse Width, Part to Part



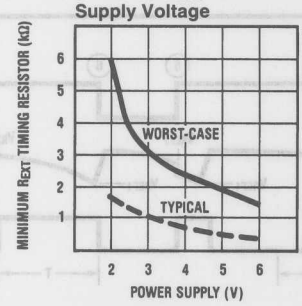
TL/F/5325–8

Typical 1ms Pulse Width Variation vs. Supply



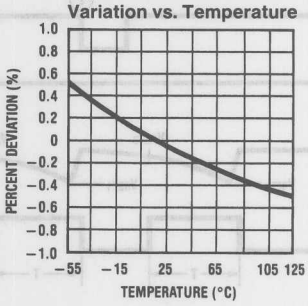
TL/F/5325–9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5325–10

Typical 1 ms Pulse Width Variation vs. Temperature



TL/F/5325–11

Note: R and C are not subjected to temperature. The C is polypropylene.

National Semiconductor

MM54HC237/MM74HC237
3-to-8 Line Decoder With Address Latches

General Description

These devices utilize advanced silicon-gate CMOS technology, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are low unless G1 is high and $\overline{G2}$ is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

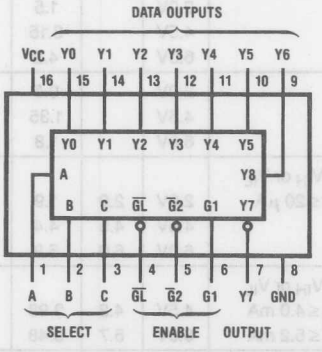
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5326–1

Top View

Order Number MM54HC237* or MM74HC237*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature	
(T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

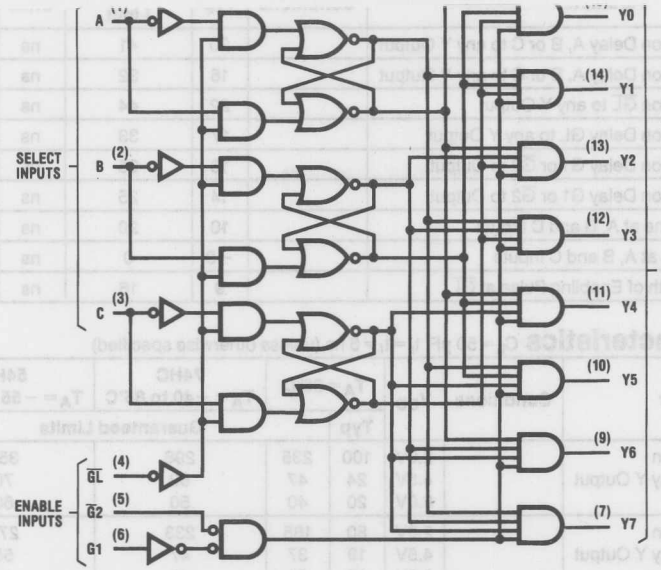
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		20	41	ns
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		16	32	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		22	44	ns
t_{PHL}	Maximum Propagation Delay GL to any Y Output		17	33	ns
t_{PLH}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		16	35	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		14	25	ns
t_S	Minimum Set Up Time at A, B and C Inputs		10	20	ns
t_H	Minimum Hold Time at A, B and C Inputs		−3	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		9	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

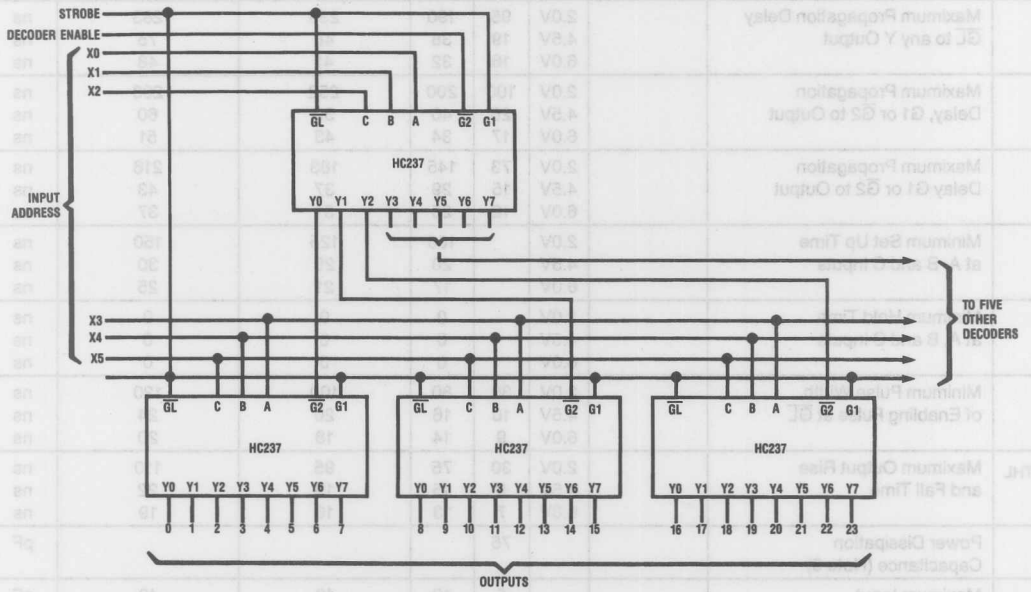
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	100	235	296	350	ns
			4.5V	24	47	59	70	ns
			6.0V	20	40	50	60	ns
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	80	185	233	276	ns
			4.5V	19	37	47	55	ns
			6.0V	17	31	40	47	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		2.0V	125	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	63	ns
t_{PHL}	Maximum Propagation Delay $\overline{GL}$ to any Y Output		2.0V	95	190	239	283	ns
			4.5V	19	38	48	75	ns
			6.0V	16	32	41	48	ns
t_{PLH}	Maximum Propagation Delay, G1 or $\overline{G2}$ to Output		2.0V	100	200	252	298	ns
			4.5V	20	40	50	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		2.0V	73	145	183	216	ns
			4.5V	15	29	37	43	ns
			6.0V	12	25	31	37	ns
t_S	Minimum Set Up Time at A, B and C Inputs		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time at A, B and C Inputs		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.



TL/F/5326–2

Typical Application



TL/F/5326–3

6-Line to 64-Line Decoder with Input Address Storage

National Semiconductor

MM54HC240/MM74HC240 Inverting Octal TRI-STATE® Buffer MM54HC241/MM74HC241 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. Each has a fanout of 15 LS-TTL equivalent inputs.

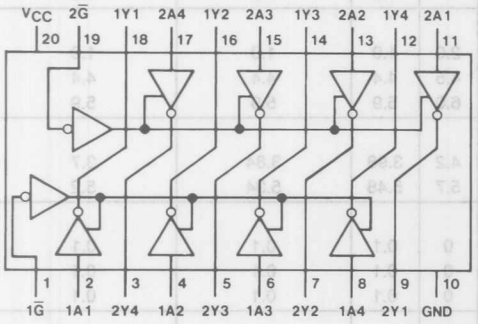
The MM54HC240/MM74HC240 is an inverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls 4 buffers. MM54HC241/MM74HC241 is a non-inverting buffer that has one active low enable and one active high enable, each again controlling 4 buffers. Neither device has Schmitt trigger inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 Series)
- Output current: 6 mA

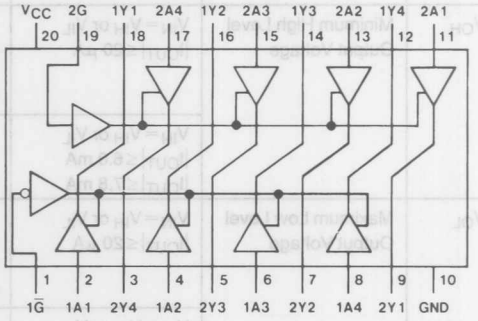
Connection Diagrams Dual-In-Line Packages



TL/L/5020–1

Top View
Order Number MM54HC240/241* or MM74HC240/241*

*Please look into Section 8, Appendix D for availability of various package types.



TL/L/5020–2

Top View
Order Number MM54HC240/241* or MM74HC240/241*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

('HC240)

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

('HC241)

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}, G = V_{IL}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics MM54HC240/MM74HC240 $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ $C_L=45$ pF	14	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics MM54HC240/MM74HC240

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	80	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	28	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable TIme	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	60	75	90	ns
			4.5V	12	15	18	ns
			6.0V	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer) $\overline{G}=V_{IH}$ $\overline{G}=V_{IL}$		12 50			pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

3

t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L = 1\ k\Omega$	$1\overline{G}$	17	28	ns
		$C_L = 45\ pF$	$2\overline{G}$	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Input	$R_L = 1\ k\Omega$	$1\overline{G}$	15	25	ns
		$C_L = 5\ pF$	$2\overline{G}$	13	25	ns

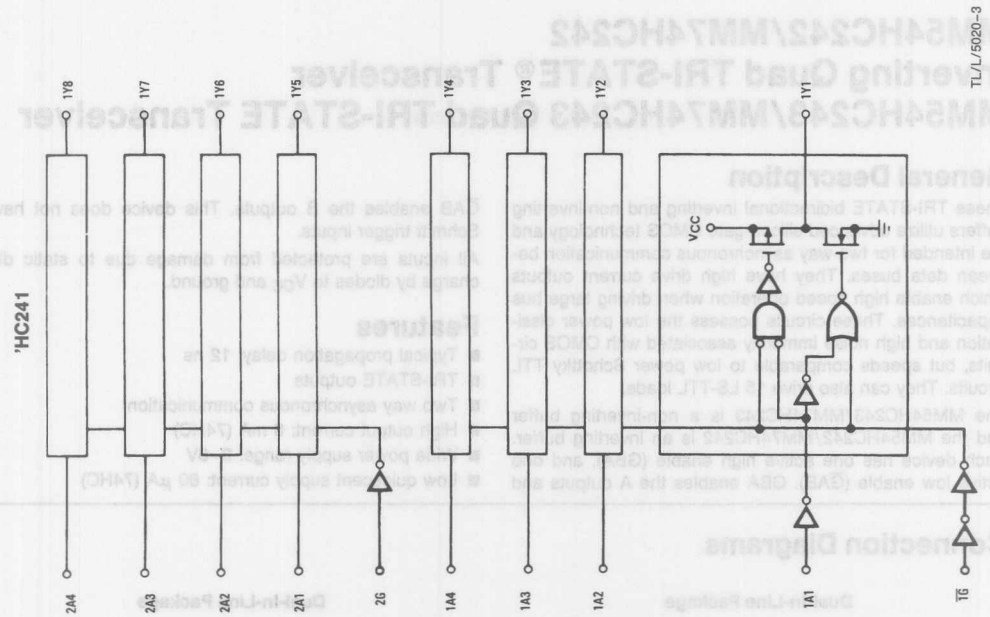
AC Electrical Characteristics MM54HC241/MM74HC241

$V_{CC} = 2.0V$ to 6.0V, $C_L = 50\ pF$, $t_r = t_f = 6$ ns (unless otherwise specified)

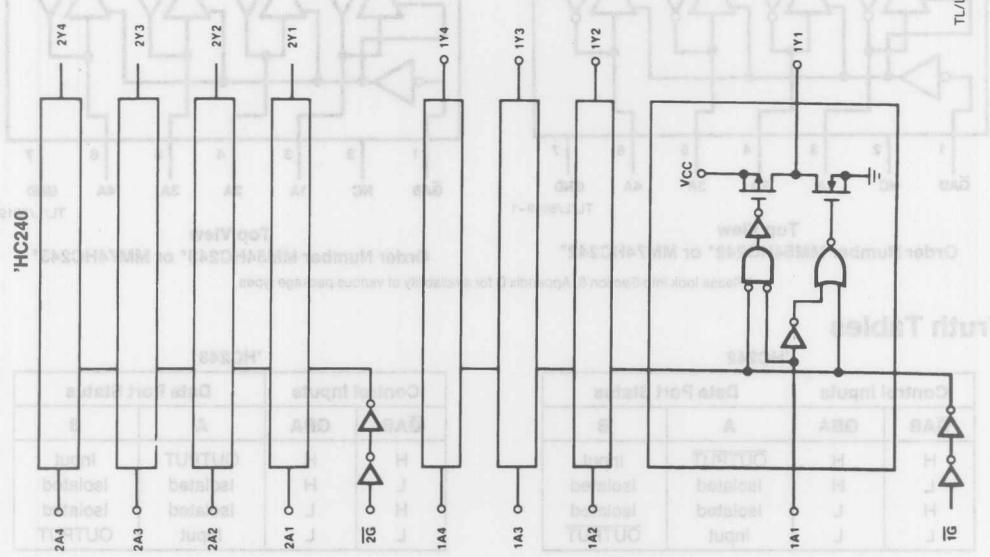
Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50\ pF$	2.0V	58	115	145	171	ns
		$C_L = 150\ pF$	2.0V	83	165	208	246	ns
		$C_L = 50\ pF$	4.5V	14	23	29	34	ns
		$C_L = 150\ pF$	4.5V	17	33	42	49	ns
		$C_L = 50\ pF$	6.0V	10	20	25	29	ns
		$C_L = 150\ pF$	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1\ k\Omega$						
		$C_L = 50\ pF$	2.0V	75	150	189	224	ns
		$C_L = 150\ pF$	2.0V	100	200	252	298	ns
		$C_L = 50\ pF$	4.5V	15	30	38	45	ns
		$C_L = 150\ pF$	4.5V	20	40	50	60	ns
		$C_L = 50\ pF$	6.0V	13	26	32	38	ns
		$C_L = 150\ pF$	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$	2.0V	75	150	189	224	ns
		$C_L = 50\ pF$	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$G = V_{IL}$, $\overline{G} = V_{IH}$		12				pF
		$G = V_{IH}$, $\overline{G} = V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Logic Diagrams



TL/L/5020–3



TL/L/5020–4

National Semiconductor

MM54HC242/MM74HC242 Inverting Quad TRI-STATE® Transceiver MM54HC243/MM74HC243 Quad TRI-STATE Transceiver

General Description

These TRI-STATE bidirectional inverting and non-inverting buffers utilize advanced silicon-gate CMOS technology and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances. These circuits possess the low power dissipation and high noise immunity associated with CMOS circuits, but speeds comparable to low power Schottky TTL circuits. They can also drive 15 LS-TTL loads.

The MM54HC243/MM74HC243 is a non-inverting buffer and the MM54HC242/MM74HC242 is an inverting buffer. Each device has one active high enable (GBA), and one active low enable ($\overline{G}$AB). GBA enables the A outputs and $\overline{G}$AB enables the B outputs. This device does not have Schmitt trigger inputs.

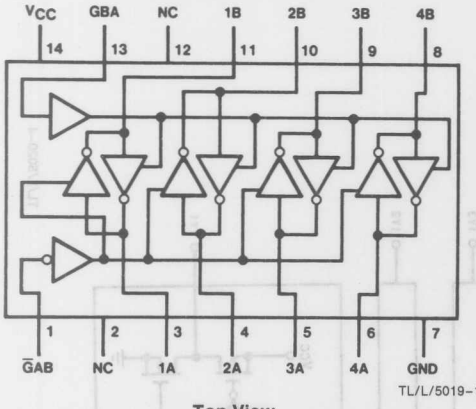
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs
- Two way asynchronous communication
- High output current: 6 mA (74HC)
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74HC)

Connection Diagrams

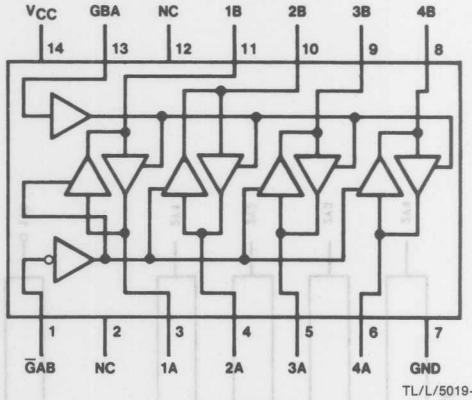
Dual-In-Line Package



TL/L/5019–1

Top View
Order Number MM54HC242* or MM74HC242*

Dual-In-Line Package



TL/L/5019–2

Top View
Order Number MM54HC243* or MM74HC243*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

'HC242

Control Inputs		Data Port Status	
$\overline{G}$AB	GBA	A	B
H	H	$\overline{\text{OUTPUT}}$	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	$\overline{\text{OUTPUT}}$

'HC243

Control Inputs		Data Port Status	
$\overline{G}$AB	GBA	A	B
H	H	OUTPUT	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	OUTPUT

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{GAB}$ = V_{IH}, GBA = V_{IL}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics (MM54HC242/MM74HC242)

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=1k\Omega$ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PHL}	Maximum Output Disable Time from Active Output	$R_L=1$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics (MM54HC242/MM74HC242, MM54HC243/MM74HC243)

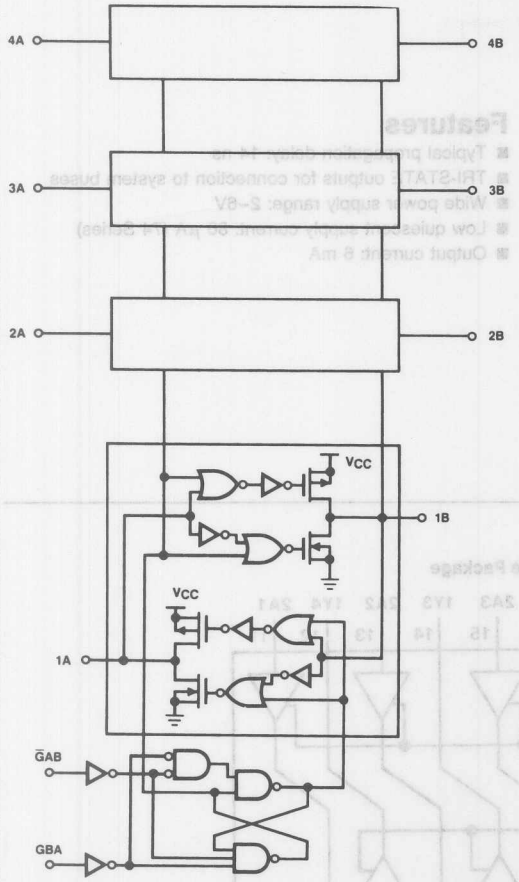
$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	80	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	18	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		Outputs Disabled		12				pF
		Outputs Enabled		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

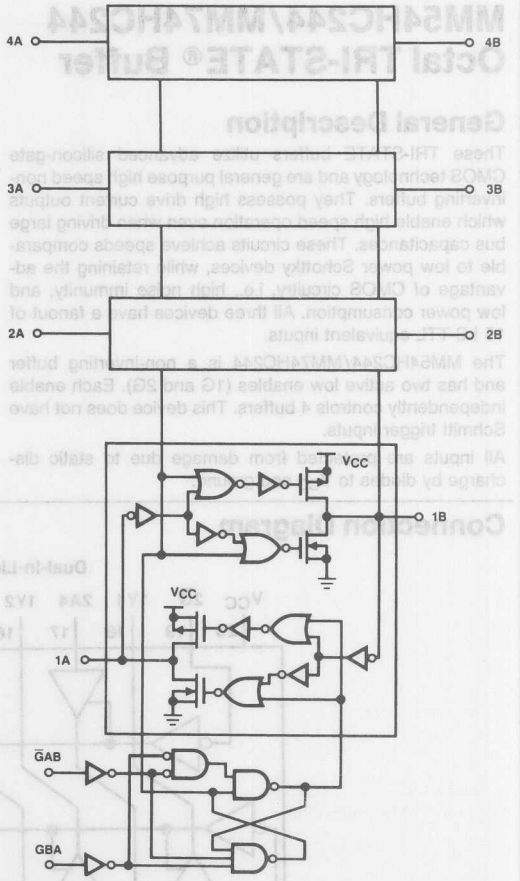
Logic Diagrams

MM54HC242/MM74HC242



TL/L/5019–3

MM54HC243/MM74HC243



TL/L/5019–4

MM54HC244/MM74HC244
Octal TRI-STATE® Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. All three devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC244/MM74HC244 is a non-inverting buffer and has two active low enables (1G and 2G). Each enable independently controls 4 buffers. This device does not have Schmitt trigger inputs.

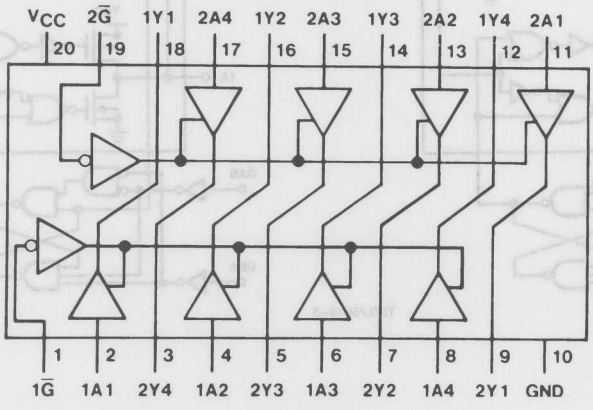
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 Series)
- Output current: 6 mA

Connection Diagram

Dual-In-Line Package



TL/F/5327–1

Top View

Order Number MM54HC244* or MM74HC244*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

'HC244

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH}, or V_{IL} V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics MM54HC244/MM74HC244

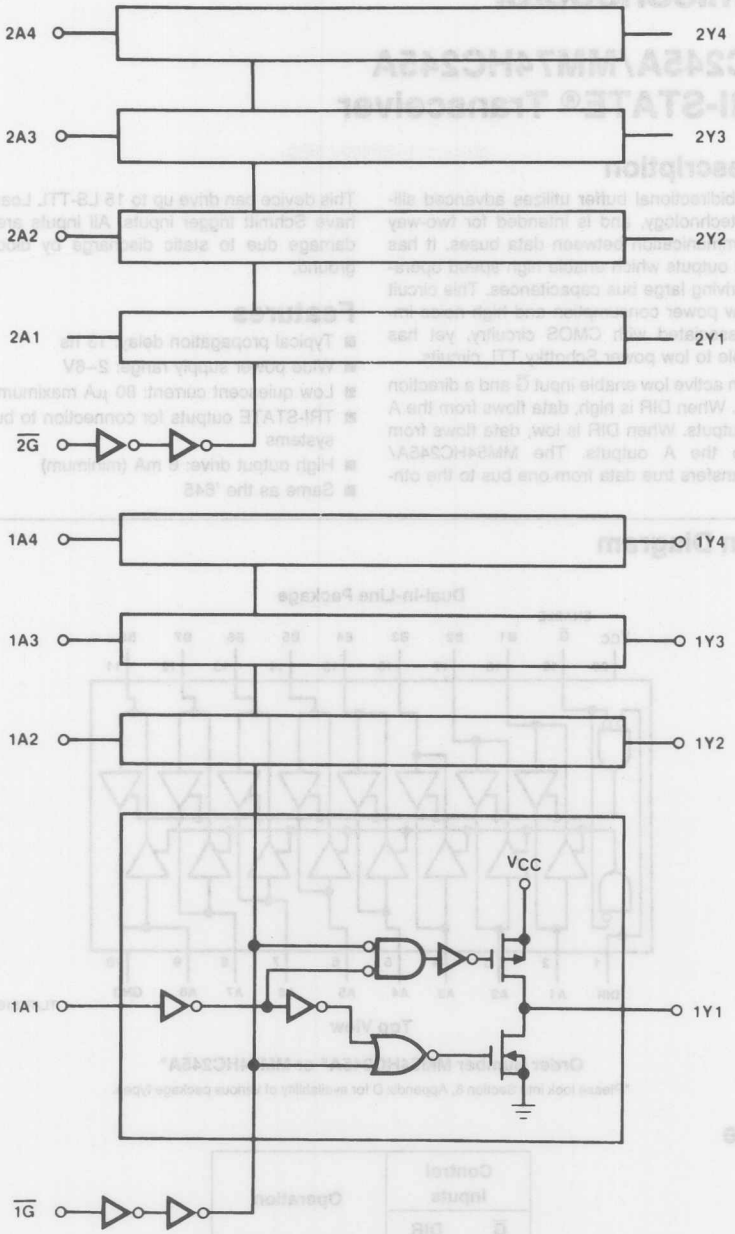
$V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	R_L = 1 kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	R_L = 1 kΩ C_L = 5 pF	15	25	ns

AC Electrical Characteristics $V_{CC} = 2.0V$-$6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	58	115	145	171	ns
		C_L = 150 pF	2.0V	83	165	208	246	ns
		C_L = 50 pF	4.5V	14	23	29	34	ns
		C_L = 150 pF	4.5V	17	33	42	49	ns
		C_L = 50 pF	6.0V	10	20	25	29	ns
		C_L = 150 pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	75	150	189	224	ns
		C_L = 150 pF	2.0V	100	200	252	298	ns
		C_L = 50 pF	4.5V	15	30	38	45	ns
		C_L = 150 pF	4.5V	30	40	50	60	ns
		C_L = 50 pF	6.0V	13	26	32	38	ns
		C_L = 150 pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G} = V_{IH}$		12				pF
		$\overline{G} = V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.


2A4
2Y4
2A3
2Y3
2A2
2Y2
2A1
2Y1
2G
1A4
1Y4
1A3
1Y3
1A2
1Y2
VCC
1A1
1Y1
1G

TL/F/5327–2

National Semiconductor

MM54HC245A/MM74HC245A Octal TRI-STATE® Transceiver

General Description

This TRI-STATE bidirectional buffer utilizes advanced silicon-gate CMOS technology, and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device has an active low enable input $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC245A/MM74HC245A transfers true data from one bus to the other.

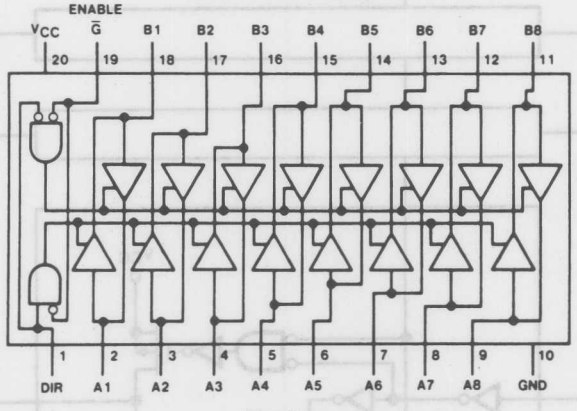
This device can drive up to 15 LS-TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- TRI-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (minimum)
- Same as the '645

Connection Diagram

Dual-In-Line Package



TL/F/5165–1

Top View

Order Number MM54HC245A* or MM74HC245A*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC} +1.5V
DC Input/Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ		Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	V_{IN} = V_{CC} to GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30%) of V_{CC}) will be implemented no later than Q1, CY'89. O = V_{IL}.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

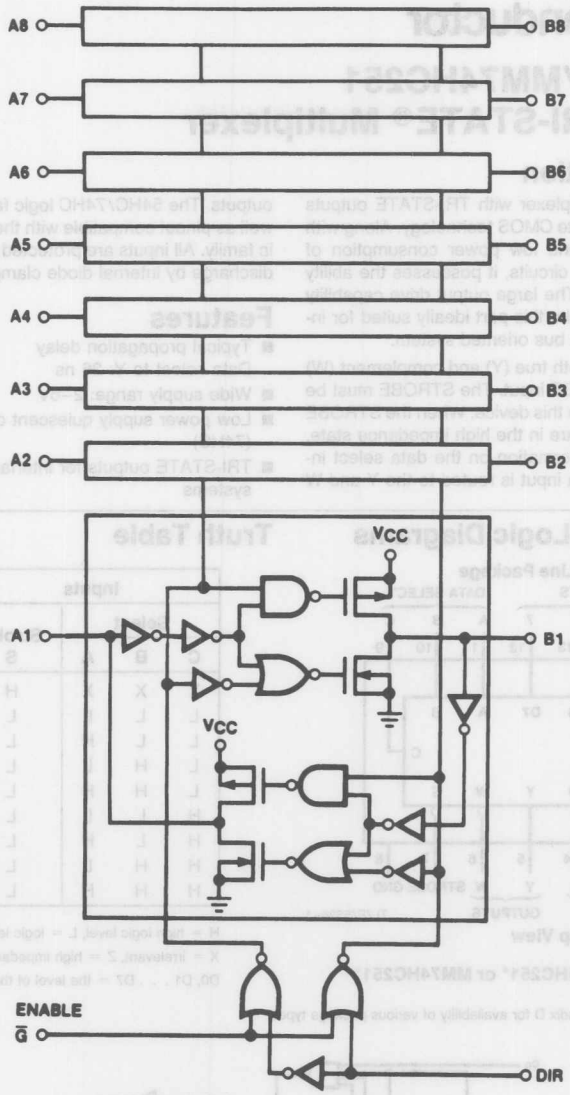
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	12	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	24	35	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	18	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	31	90	113	135	ns
		C_L = 150 pF	2.0V	41	96	116	128	ns
		C_L = 50 pF	4.5V	13	18	23	27	ns
		C_L = 150 pF	4.5V	17	22	28	33	ns
		C_L = 50 pF	6.0V	11	15	19	23	ns
		C_L = 150 pF	6.0V	14	19	23	28	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	71	190	240	285	ns
		C_L = 150 pF	2.0V	81	240	300	360	ns
		C_L = 50 pF	4.5V	26	38	48	57	ns
		C_L = 150 pF	4.5V	31	48	60	72	ns
		C_L = 50 pF	6.0V	21	32	41	48	ns
		C_L = 150 pF	6.0V	25	41	51	61	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	39	135	169	203	ns
			4.5V	20	27	34	41	ns
			6.0V	18	23	29	34	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time	$C_L=50$ pF	2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}=V_{IL}$		50				pF
		$\overline{G}=V_{IH}$		5				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5165–2

MM54HC251/MM74HC251
8-Channel TRI-STATE® Multiplexer

General Description

This 8-channel digital multiplexer with TRI-STATE outputs utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

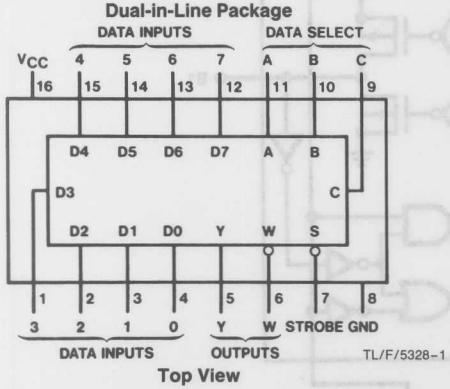
This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs. The 54HC/74HC logic family is speed, function, as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
  Data select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC)
- TRI-STATE outputs for interface to bus oriented systems

Connection and Logic Diagrams

Dual-in-Line Package



Top View

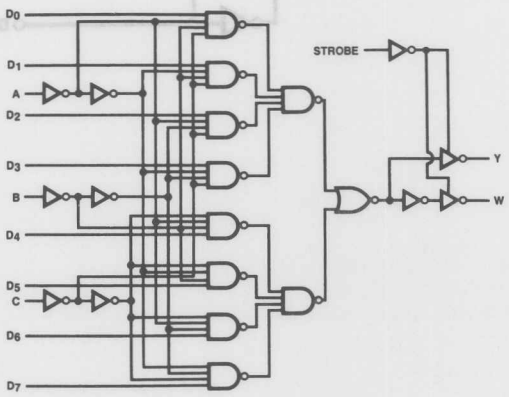
Order Number MM54HC251* or MM74HC251*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input



TL/F/5328–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Leakage Current	Strobe = V_{CC} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		24	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, W Output	$R_L=1$ kΩ $C_L=50$ pF	19	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, Y Output	$R_L=1$ kΩ $C_L=50$ pF	19	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1$ kΩ $C_L=5$ pF	26	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1$ kΩ $C_L=5$ pF	27	35	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V 4.5V 6.0V	90 31 26	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		2.0V 4.5V 6.0V	95 32 27	205 41 35	256 51 44	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to Y		2.0V 4.5V 6.0V	70 27 23	195 39 33	244 49 41	283 57 48	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to W		2.0V 4.5V 6.0V	75 29 25	185 37 32	231 46 40	268 54 46	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time W Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	45 21 18	150 30 26	188 38 33	218 44 38	ns ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	45 21 18	145 29 25	181 36 31	210 42 36	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	60 29 25	220 44 37	275 55 46	319 64 54	ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1$ kΩ	2.0V 4.5V 6.0V	60 30 26	195 39 33	244 49 41	283 57 48	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC253/MM74HC253
Dual 4-Channel TRI-STATE® Multiplexer

General Description

The MM54HC253/MM74HC253 utilizes advanced silicon-gate CMOS technology to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the capability to drive 10 LS-TTL loads. The large output drive and TRI-STATE features of this device make it ideally suited for interfacing with bus lines in bus organized systems. When the output control input is taken high, the multiplexer outputs are sent into a high impedance state.

When the output control is held low, the associated multiplexer chooses the correct output channel for the given input signals determined by the select A and B inputs.

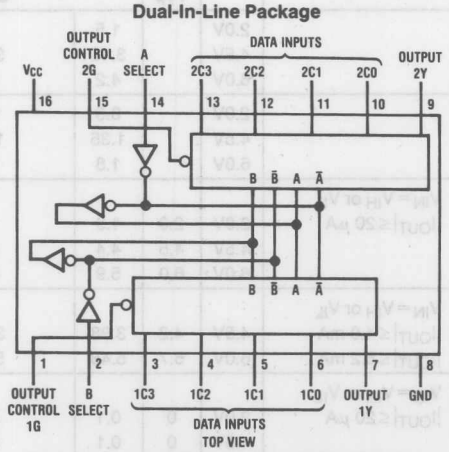
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5108–1

Order Number MM54HC253* or MM74HC253*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	Strobe = V_{CC} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6$ ns, $C_L = 15$ pF

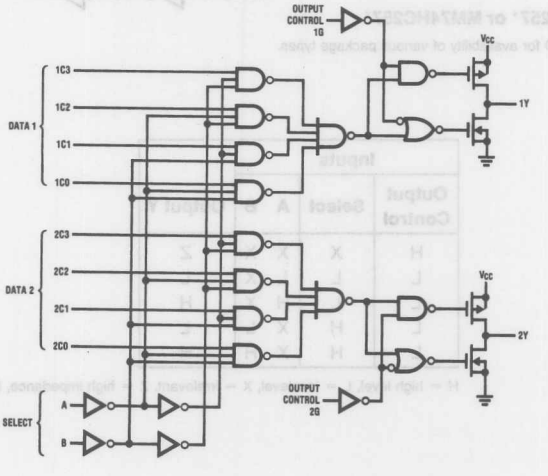
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		24	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		18	23	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output to a Logic Level	$R_L = 1$ kΩ	13	18	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output to High Impedance State	$R_L = 1$ kΩ	18	27	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	198	237	ns
			4.5V	29	44	53	ns
			6.0V	24	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		2.0V	99	158	189	ns
			4.5V	22	35	42	ns
			6.0V	19	29	35	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ	2.0V	63	113	135	ns
			4.5V	14	25	30	ns
			6.0V	12	21	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ	2.0V	90	169	203	ns
			4.5V	20	38	45	ns
			6.0V	17	31	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	95	110	ns
			4.5V	8	19	22	ns
			6.0V	7	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Outputs Enabled		90			pF
		Outputs Disabled		25			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5108–2

National Semiconductor

MM54HC257/MM74HC257
Quad 2-Channel TRI-STATE® Multiplexer

General Description

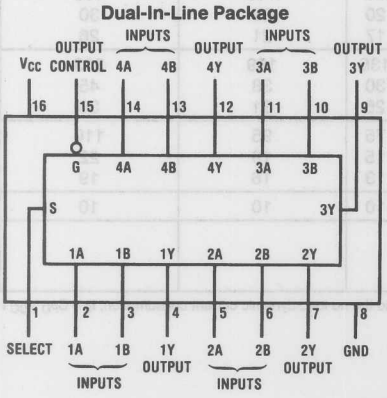
This QUAD 2-TO-1 line data selector/multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive up to 15 LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, the SELECT input chooses whether the A or B input is used.

The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- TRI-STATE outputs for connection to system buses.

Connection and Logic Diagrams

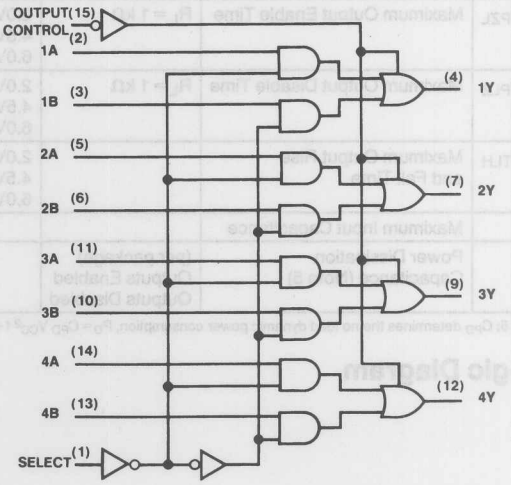


TL/F/5329–1

Top View

Order Number MM54HC257* or MM74HC257*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5329–2

Truth Table

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L = 45$ pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L = 50$ pF	13	21	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L = 1$ kΩ $C_L = 45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L = 1$ kΩ $C_L = 5$ pF	15	25	ns

AC Electrical Characteristics $V_{CC} = 2.0$V to 6.0V, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L = 50$ pF	2.0V	50	100	125	150	ns
		$C_L = 150$ pF	2.0V	70	150	189	224	ns
		$C_L = 50$ pF	4.5V	10	20	25	30	ns
		$C_L = 150$ pF	4.5V	15	30	38	45	ns
		$C_L = 50$ pF	6.0V	9	17	21	25	ns
		$C_L = 150$ pF	6.0V	13	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L = 50$ pF	2.0V	50	100	125	150	ns
		$C_L = 150$ pF	2.0V	70	150	190	221	ns
		$C_L = 50$ pF	4.5V	10	20	29	30	ns
		$C_L = 150$ pF	4.5V	15	30	38	45	ns
		$C_L = 50$ pF	6.0V	10	17	21	25	ns
		$C_L = 150$ pF	6.0V	17	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	75	150	189	224	ns
		$C_L = 150$ pF	2.0V	100	200	252	298	ns
		$C_L = 50$ pF	4.5V	15	30	38	45	ns
		$C_L = 150$ pF	4.5V	20	40	50	60	ns
		$C_L = 50$ pF	6.0V	13	26	32	38	ns
		$C_L = 150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L = 1$ kΩ $C_L = 50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per mux)						
		Enable		30				pF
		Disabled		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

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MM54HC258/MM74HC258 Quad 2-Channel TRI-STATE® Multiplexer (Inverted Output)

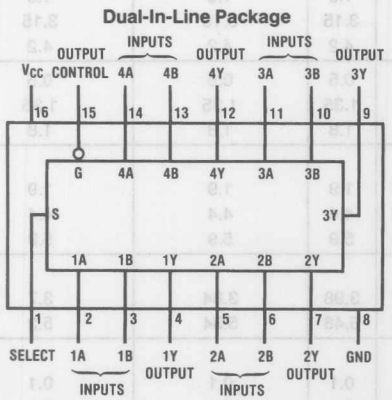
General Description

This Quad 2-to-1 line data selector/multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, these possess the ability to drive LS-TT loads. The large output drive capability with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the Output Control line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the Output Control line is low, $\overline{A}$ or $\overline{B}$ data is selected for the HC258. The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delays: 16 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum (74HC Series)
- TRI-STATE outputs for connection to system buses
- Added circuitry allows data input levels to float during TRI-STATE with no additional power consumption

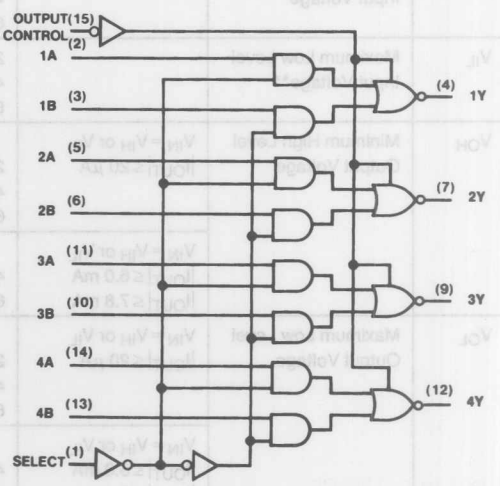
Connection Diagram



Order Number MM54HC258* or MM74HC258*

*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



Truth Table

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SELECT to any Y Output	$C_L=45$ pF	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=45$ pF	16	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L=1$ kΩ $C_L=45$ pF	27	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L=1$ kΩ $C_L=5$ pF	14	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SELECT to any Y Output	$C_L=50$ pF	2.0V		120	150	180	ns
		$C_L=50$ pF	4.5V	17	24	30	36	ns
		$C_L=50$ pF	6.0V		20	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=50$ pF	2.0V		90	115	135	ns
		$C_L=50$ pF	4.5V	14	18	23	27	ns
		$C_L=50$ pF	6.0V		15	20	23	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L=1$ kΩ $C_L=50$ pF	2.0V		160	200	240	ns
		$C_L=50$ pF	4.5V	25	32	40	48	ns
		$C_L=50$ pF	6.0V		27	34	41	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L=1$ kΩ $C_L=50$ pF	2.0V 4.5V 6.0V	15	120 24 20	150 30 26	180 36 31	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V 4.5V 6.0V	8	60 12 10	75 15 13	90 18 15	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per mux) Enable Disabled		44				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

MM54HC259/MM74HC259
8-Bit Addressable Latch/3-to-8 Line Decoder

General Description

This device utilizes advanced silicon-gate CMOS technology to implement an 8-bit addressable latch, designed for general purpose storage applications in digital systems.

The MM54HC259/MM74HC259 has a single data input (D), 8 latch outputs (Q1–Q8), 3 address inputs (A, B, and C), a common enable input ($\overline{G}$), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addressed output. The data is stored when ENABLE transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

If enable is held high and CLEAR is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

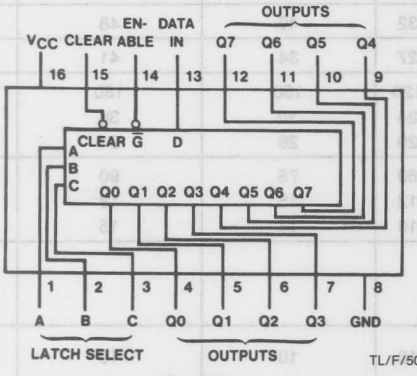
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide supply range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)

Connection Diagram

Dual-In-Line Package



Top View

Order Number MM54HC259* or MM74HC259*

*Please look into Section 8, Appendix D for availability of various package types.

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

D = the level at the data input

Q_{i0} the level of Q_i (i = 0, 1 . . . 7, as appropriate) before the indicated steady-state input conditions were established.

Truth Table

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics (V_{CC} = 5.0V, T_A = 25°C, $t_r = t_f$ = 6 ns, C_L = 15 pF unless otherwise specified.)

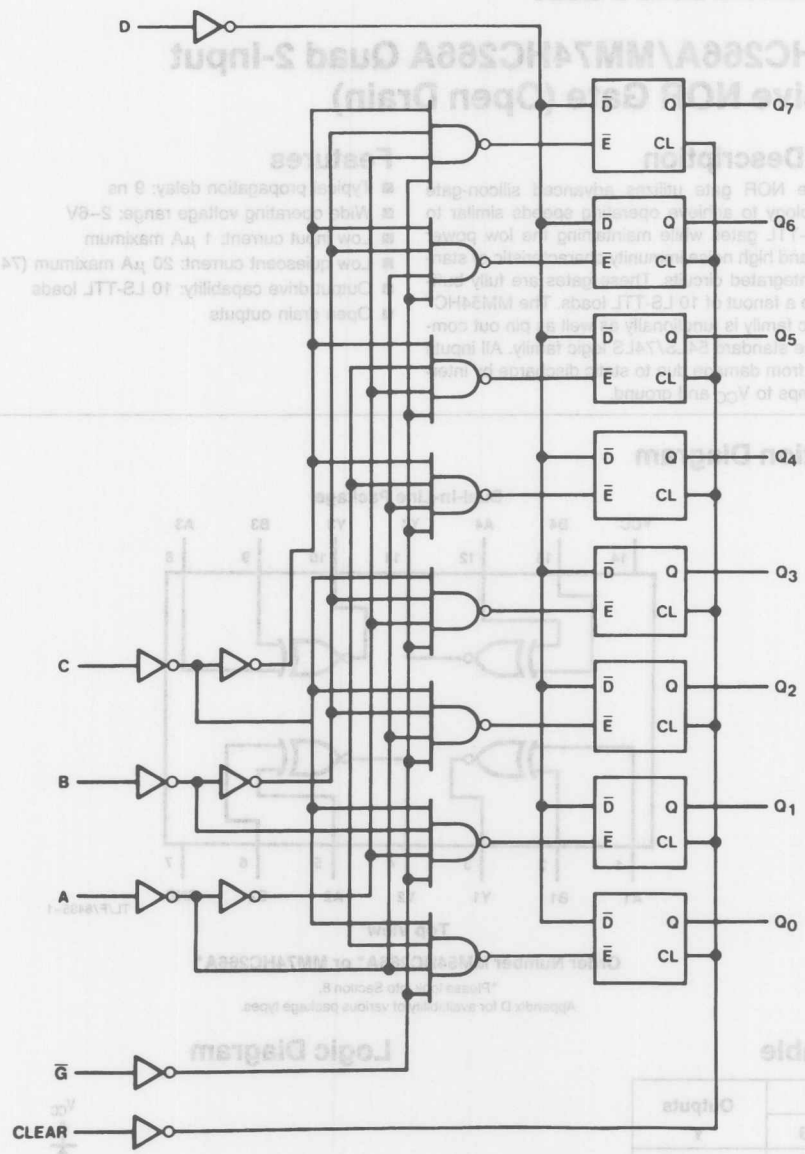
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		20	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		20	35	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		17	27	ns
t_W	Minimum Enable Pulse Width		10	16	ns
t_W	Minimum Clear Pulse Width		10	16	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	ns
t_s	Minimum Setup Time Select or Data to Enable		15	20	ns
t_H	Minimum Hold Time Data or Address to Enable		−2	0	ns

AC Electrical Characteristics $t_r = t_f$ = 6 ns, C_L = 50 pF, V_{CC} = 2.0V–6.0V

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		2.0V	60	180	225	250	ns
			4.5V	19	37	46	52	ns
			6.0V	17	32	40	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		2.0V	72	220	275	310	ns
			4.5V	21	43	54	60	ns
			6.0V	18	37	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		2.0V	65	200	250	280	ns
			4.5V	27	40	50	58	ns
			6.0V	23	35	44	50	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		2.0V	50	150	190	210	ns
			4.5V	18	31	39	44	ns
			6.0V	16	26	32	37	ns
t_W	Minimum Pulse Width Clear or Enable		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_s	Minimum Setup Time Address or Data to Enable		2.0V		100	125	150	ns
			4.5V		20	25	28	ns
			6.0V		15	19	25	ns
t_H	Minimum Hold Time Address or Data to Enable		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5006–2

MM54HC266A/MM74HC266A Quad 2-Input Exclusive NOR Gate (Open Drain)

General Description

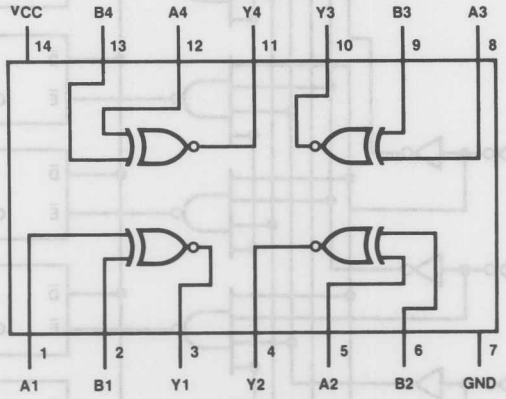
This exclusive NOR gate utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/MM74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads
- Open drain outputs

Connection Diagram

Dual-In-Line Package



TL/F/8435–1

Top View

Order Number MM54HC266A* or MM74HC266A*

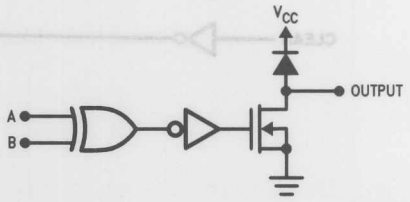
*Please look into Section 8,
Appendix D for availability of various package types.

Truth Table

Inputs		Outputs
A	B	Y
L	L	Z
L	H	L
H	L	L
H	H	Z

$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

Logic Diagram



TL/F/8435–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN}=V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7 V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4 V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40 μA
I_{OZ}	Maximum TRI-STATE® Leakage Current	V_{IN}=V_{IL} or V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5.0	±10.0 μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLZ}, t_{PZL}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PLZ}, t_{PZL}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{THL}	Maximum Output Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Three State Output Capacitance Output in TRI-STATE				10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC273/MM74HC273 Octal D Flip-Flops with Clear

General Description

These edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

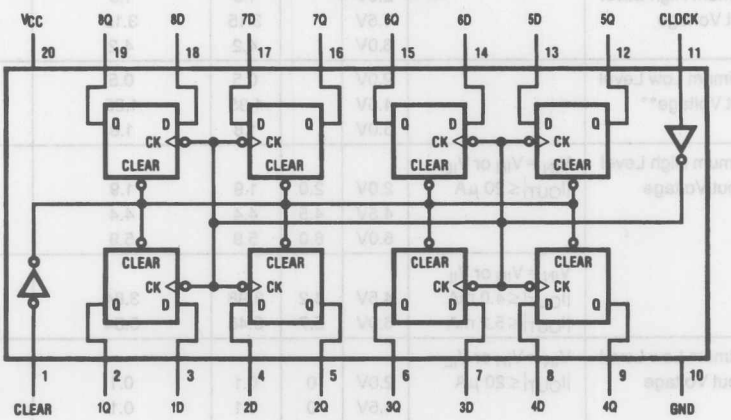
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC273/MM74HC273 is functionally as well as pin compatible to the 54LS273/74LS273. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74 Series)
- Output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5331–1

Top View

Order Number MM54HC273* or MM74HC273*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

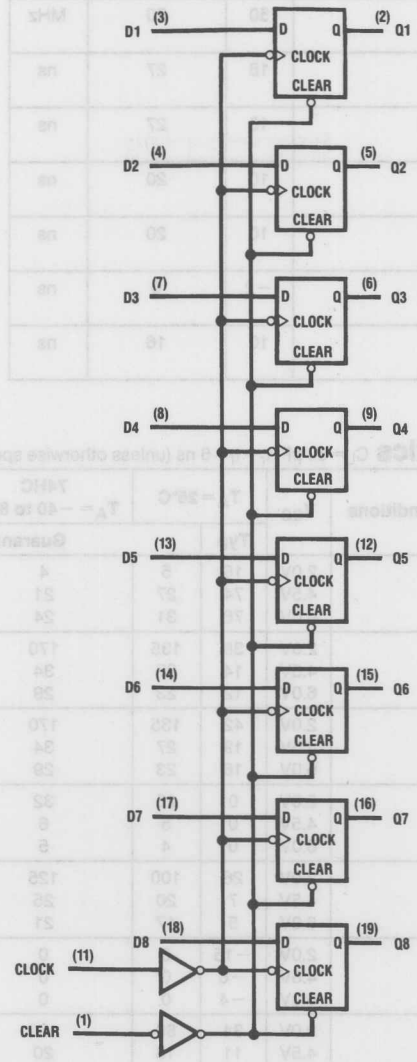
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		18	27	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		18	27	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_s	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		−2	0	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	16	5	4	3	MHz
			4.5V	74	27	21	18	MHz
			6.0V	78	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V	38	135	170	205	ns
			4.5V	14	27	34	41	ns
			6.0V	12	23	29	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		2.0V	42	135	170	205	ns
			4.5V	19	27	34	41	ns
			6.0V	18	23	29	35	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	0	25	32	37	ns
			4.5V	0	5	6	7	ns
			6.0V	0	4	5	6	ns
t_s	Minimum Setup Time Data to Clock		2.0V	26	100	125	150	ns
			4.5V	7	20	25	30	ns
			6.0V	5	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	−15	0	0	0	ns
			4.5V	−6	0	0	0	ns
			6.0V	−4	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	34	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	11	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		45				pF
C_{IN}	Maximum Input Capacitance			7	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5331–2

National Semiconductor

MM54HC280/MM74HC280
9-Bit Odd/Even Parity Generator/Checker

General Description

The MM54HC280/MM74HC280 utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits. It possesses the ability to drive 10 LS-TTL loads.

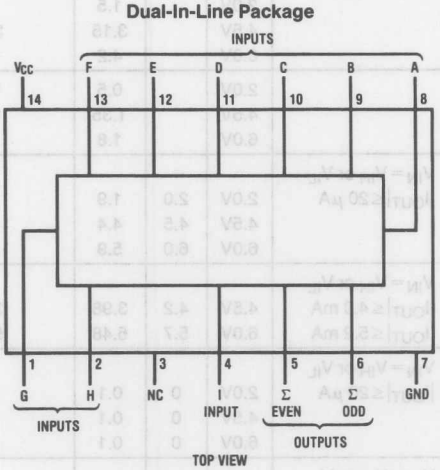
This parity generator/checker features odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading devices. The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 28 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5121–1

Order Number MM54HC280* or MM74HC280*

*Please look into Section 8, Appendix D for availability of various package types.

Function Table

Numbers of Inputs A thru 1 that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

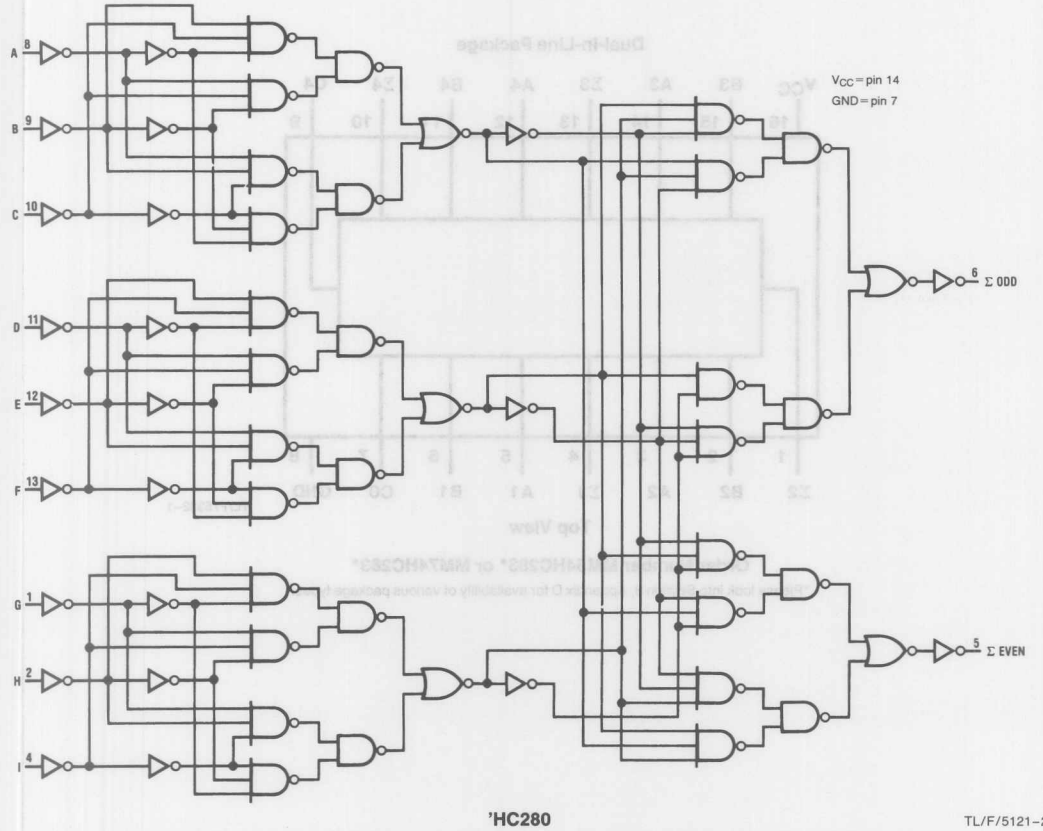
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		28	35	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			83				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



'HC280

TL/F/5121–2

National Semiconductor

MM54HC283/MM74HC283
4-Bit Binary Adder with Fast Carry

General Description

This full adder performs the addition of two 4-bit binary numbers utilizing advanced silicon-gate CMOS technology. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

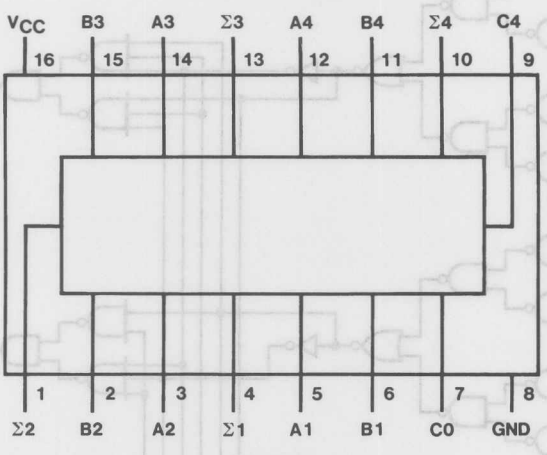
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide supply range: 2V to 6V
- Low quiescent power consumption: 8 μA at 25°C
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



Top View

Order Number MM54HC283* or MM74HC283*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +1.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ1 or Σ2		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ3		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ4		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to Σ1		17	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		22	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to C4		22	32	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ1 or Σ2		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ3		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ4		2.0V	65	162	202	243	ns
			4.5V	24	34	43	51	ns
			6.0V	19	28	35	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to Σ1		2.0V	60	150	188	225	ns
			4.5V	22	33	41	50	ns
			6.0V	18	27	34	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		2.0V	70	175	219	263	ns
			4.5V	26	39	49	59	ns
			6.0V	21	32	40	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to C4		2.0V	70	175	219	263	ns
			4.5V	26	39	49	59	ns
			6.0V	21	32	40	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			6	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			150				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table

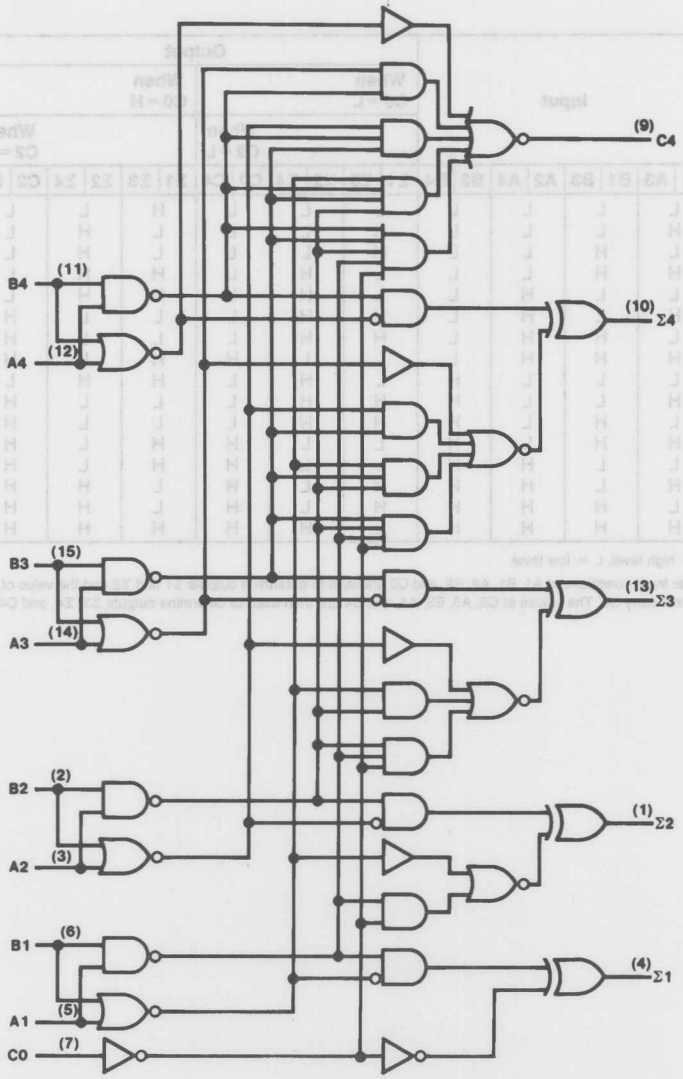
Input								Output									
								When C0 = L						When C0 = H			
												When C2 = L					When C2 = H
A1	A3	B1	B3	A2	A4	B2	B4	Σ1	Σ3	Σ2	Σ4	C2	C4	Σ1	Σ3	Σ2	Σ4	C2	C4
L		L		L		L		L		L		L		H		L		L	
H		L		L		L		H		L		L		L		H		L	
L		H		L		L		H		L		L		L		H		L	
H		H		L		L		L		H		L		H		H		L	
L		L		H		L		L		H		L		H		H		L	
H		L		H		L		H		H		L		L		L		H	
L		H		H		L		H		H		L		L		L		H	
H		H		H		L		L		L		H		H		L		H	
L		L		L		H		L		H		L		H		H		L	
H		L		L		H		H		H		L		L		L		H	
L		H		L		H		H		H		L		L		L		H	
H		H		L		H		L		L		H		H		L		H	
L		L		H		H		L		L		H		H		L		H	
H		L		H		H		H		L		H		L		H		H	
L		H		H		H		H		L		H		L		H		H	
H		H		H		H		L		H		H		H		H		H	

H = high level, L = low level

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4

Logic Diagram

'HC283



TL/F/5332–2

National Semiconductor

MM54HC298/MM74HC298
Quad 2-Input Multiplexers With Storage

General Description

These high speed quad two input multiplexers with storage utilize advanced silicon-gate CMOS technology. Both circuits feature high noise immunity and low power consumption associated with CMOS circuitry, along with speeds comparable to low power Schottky TTL logic.

These circuits are controlled by the signals WORD SELECT and CLOCK. When the WORD SELECT input is taken low Word 1 (A1, B1, C1 and D1) is presented to the inputs of the flip-flops, and when WORD SELECT is high Word 2 (A2, B2, C2 and D2) is presented to the inputs of the flip-flops. The selected word is clocked to the output terminals on the negative edge of the clock pulse.

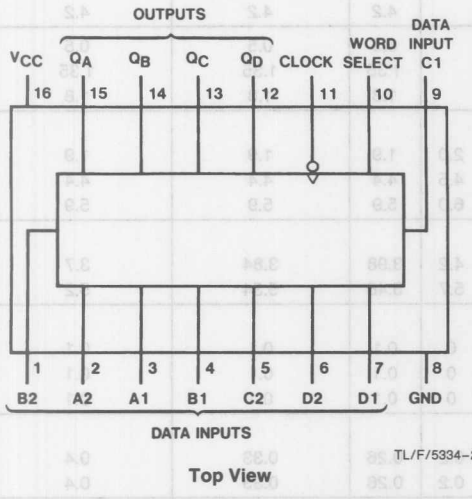
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, clock to output: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum

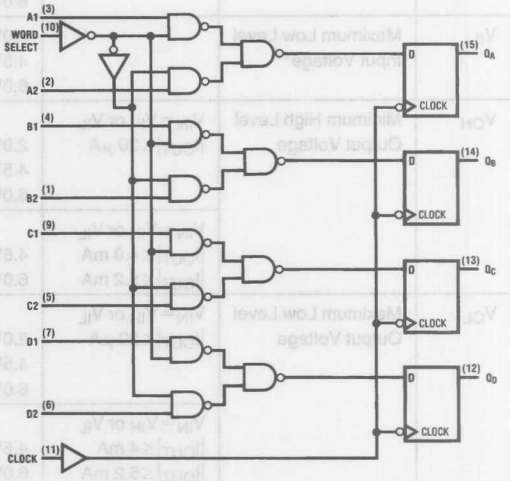
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5334–2

Top View



TL/F/5334–1

Order Number MM54HC298* or MM74HC298*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↓ = Transition from high to low level
a1, a2, etc. = The level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = The level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

Distributors for availability and specifications.

(Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter		Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			21	32	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	32	ns
t_W	Width of Clock Pulse, High or Low Level			10	16	ns
t_{SETUP}	Setup Time	Data		5	20	ns
		Word Select		10	20	
t_{HOLD}	Hold Time	Data		−2	0	ns
		Word Select		−2	0	

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter		Conditions	V_{CC}	54HC/74HC $T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
					Typ	Guaranteed Limits			
t_{PLH}	Propagation Delay Time Low-to-High Level Output			2.0V	75	185	231	278	ns
				4.5V	25	37	46	56	ns
				6.0V	20	31	39	47	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output			2.0V	75	185	231	278	ns
				4.5V	25	37	46	56	ns
				6.0V	20	31	39	47	ns
t_W	Width of Clock Pulse High or Low Level			2.0V	35	80	100	120	ns
				4.5V	10	16	20	24	ns
				6.0V	9	14	18	21	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			2.0V	90	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
t_{SETUP}	Setup Time	Data		2.0V	35	100	125	150	ns
				4.5V	5	20	25	30	ns
				6.0V	4	17	21	25	ns
		Word Select		2.0V	40	100	125	150	ns
				4.5V	10	20	25	30	ns
				6.0V	9	17	21	25	ns
t_{HOLD}	Hold Time	Data		2.0V	−10	0	0	0	ns
				4.5V	−3	0	0	0	ns
				6.0V	−2	0	0	0	ns
		Word Select		2.0V	−10	0	0	0	ns
				4.5V	−3	0	0	0	ns
				6.0V	−2	0	0	0	ns
C_{PD}	Power Dissipation Capacitance (Note 5)				28				pF
C_{IN}	Maximum Input Capacitance				5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

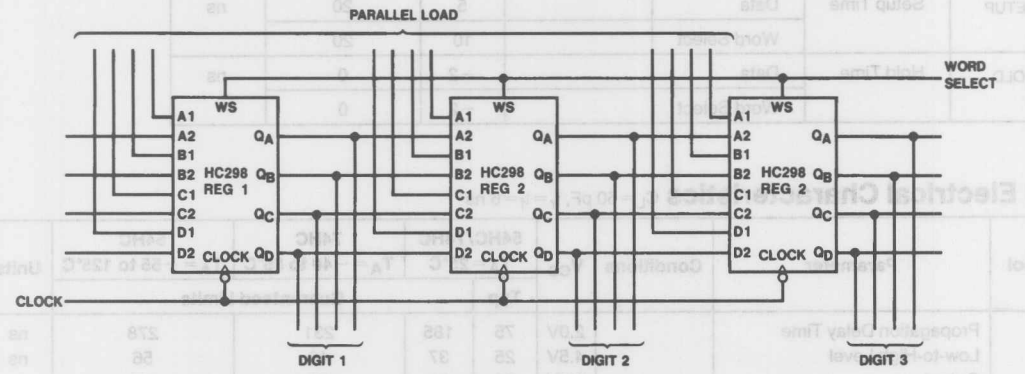
Typical Applications

Figure 1 illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.

When the word select input is high and the registers are clocked, the contents of Register 1 is transferred (shifted) to Register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

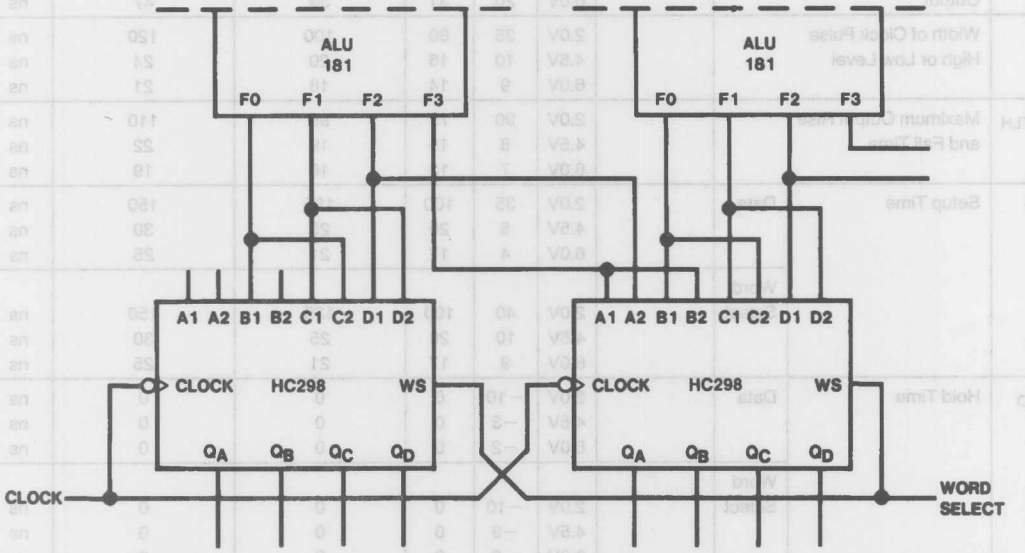
Another function that can be implemented with the MM54HC298/MM74HC298 is a register that can be designed specifically for supporting multiplier or division operations. *Figure 2* is an example of a one place/two place shift register.

When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.



TL/F/5334–3

FIGURE 1



TL/F/5334–4

FIGURE 2

National Semiconductor

MM54HC299/MM74HC299
8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes advanced silicon-gate CMOS technology. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HC299/MM74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines S0 and S1 high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

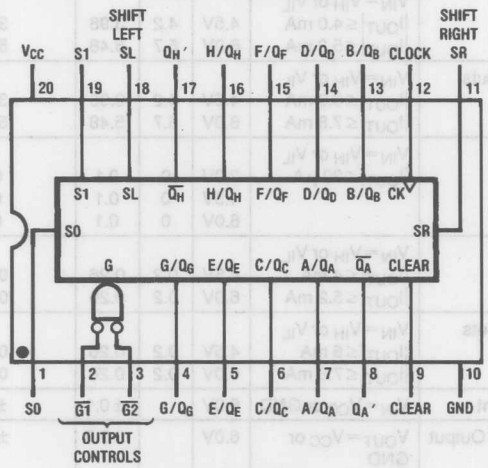
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency 40 MHz
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HC)
- High output drive for bus applications
- Low quiescent current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5207–1

Order Number MM54HC299* or MM74HC299*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA ($Q_{A'}$, $Q_{H'}$)
	±35 mA (others)
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V
			4.5V	3.15	3.15	3.15	V
			6.0V	4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V
			4.5V	1.35	1.35	1.35	V
			6.0V	1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	$Q_{A'}$ & $Q_{H'}$ Outputs	V_{IN} = V_{IH} or V_{IL}						V
		$\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
	A/Q_A thru H/Q_H Outputs	V_{IN} = V_{IH} or V_{IL}						V
		$\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	$Q_{A'}$ and $Q_{H'}$ Outputs	V_{IN} = V_{IH} or V_{IL}						V
		$\lvert I_{OUT}\rvert \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
	A/Q_A thru H/Q_H Outputs	V_{IN} = V_{IH} or V_{IL}						V
		$\lvert I_{OUT}\rvert \le 6$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Currrent	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±0.5	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=45$ pF

Symbol	Parameter		Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			40	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $Q_{A'}$ or $Q_{H'}$			25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to $Q_{A'}$ or $Q_{H'}$			39	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A–Q_H		$C_L=45$ pF	25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A–Q_H		$C_L=45$ pF	28	40	ns
t_{PZL}, t_{PZH}	Maximum Enable Time		$C_L=45$ pF $R_L=1$ kΩ	10	35	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time		$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_S	Minimum Setup Time	Select			20	ns
		Data			20	ns
t_H	Minimum Hold Time	Select			0	ns
		Data			0	ns
t_W	Minimum Pulse Width			12	20	ns
t_{REM}	Clear Removal Time				10	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3.5	MHz
			4.5V		25	20	18	MHz
			6.0V		29	23	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $Q_{A'}$ or $Q_{H'}$		2.0V	15	170	210	240	ns
			4.5V	27	38	48	54	ns
			6.0V	25	35	44	49	ns
t_{PHL}	Maximum Propagation Delay, Clear to $Q_{A'}$ or $Q_{H'}$		2.0V	70	200	250	280	ns
			4.5V	30	44	55	62	ns
			6.0V	26	38	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A–Q_H	$C_L=50$ pF	2.0V	65	170	210	240	ns
		$C_L=150$ pF	2.0V	100	206	260	295	ns
		$C_L=50$ pF	4.5V	27	38	48	54	ns
		$C_L=150$ pF	4.5V	34	46	57	66	ns
		$C_L=50$ pF	6.0V	25	35	44	49	ns
		$C_L=150$ pF	6.0V	31	39	49	55	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A–Q_H	$C_L=50$ pF	2.0V	70	200	250	280	ns
		$C_L=150$ pF	2.0V	110	236	295	325	ns
		$C_L=50$ pF	4.5V	30	44	55	62	ns
		$C_L=150$ pF	4.5V	37	52	65	75	ns
		$C_L=50$ pF	6.0V	26	38	46	52	ns
		$C_L=150$ pF	6.0V	32	46	57	64	ns

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		$T_A = -40$ to 85°C	$T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L = 1\ k\Omega$						
		$C_L = 50$ pF	2.0V	70	160	200	225	ns
		$C_L = 150$ pF	2.0V	90	220	275	310	ns
		$C_L = 50$ pF	4.5V	22	32	40	45	ns
		$C_L = 150$ pF	4.5V	30	44	55	62	ns
		$C_L = 50$ pF	6.0V	19	28	34	38	ns
		$C_L = 150$ pF	6.0V	24	47	47	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$, $C_L = 50$ pF	2.0V	70	160	200	225	ns
			4.5V	22	32	40	45	ns
			6.0V	19	28	34	38	ns
t_S	Minimum Setup Time, Data Select S_L or S_R		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time, Data Select S_L or S_R		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{REM}	Minimum Clear Removal Time		2.0V		10	10	10	ns
			4.5V		10	10	10	ns
			6.0V		10	10	10	ns
t_W	Minimum Pulse Width, Clock and Clear		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	100	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time, Clock		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance	Outputs Enabled		240				pF
		Outputs Disabled		110				pF
C_{IN}	Maximum Input Capacitance Capacitance			5	10	10	10	pF
C_{OUT}	Maximum TRI-STATE Output Capacitance			15	20	20	20	pF

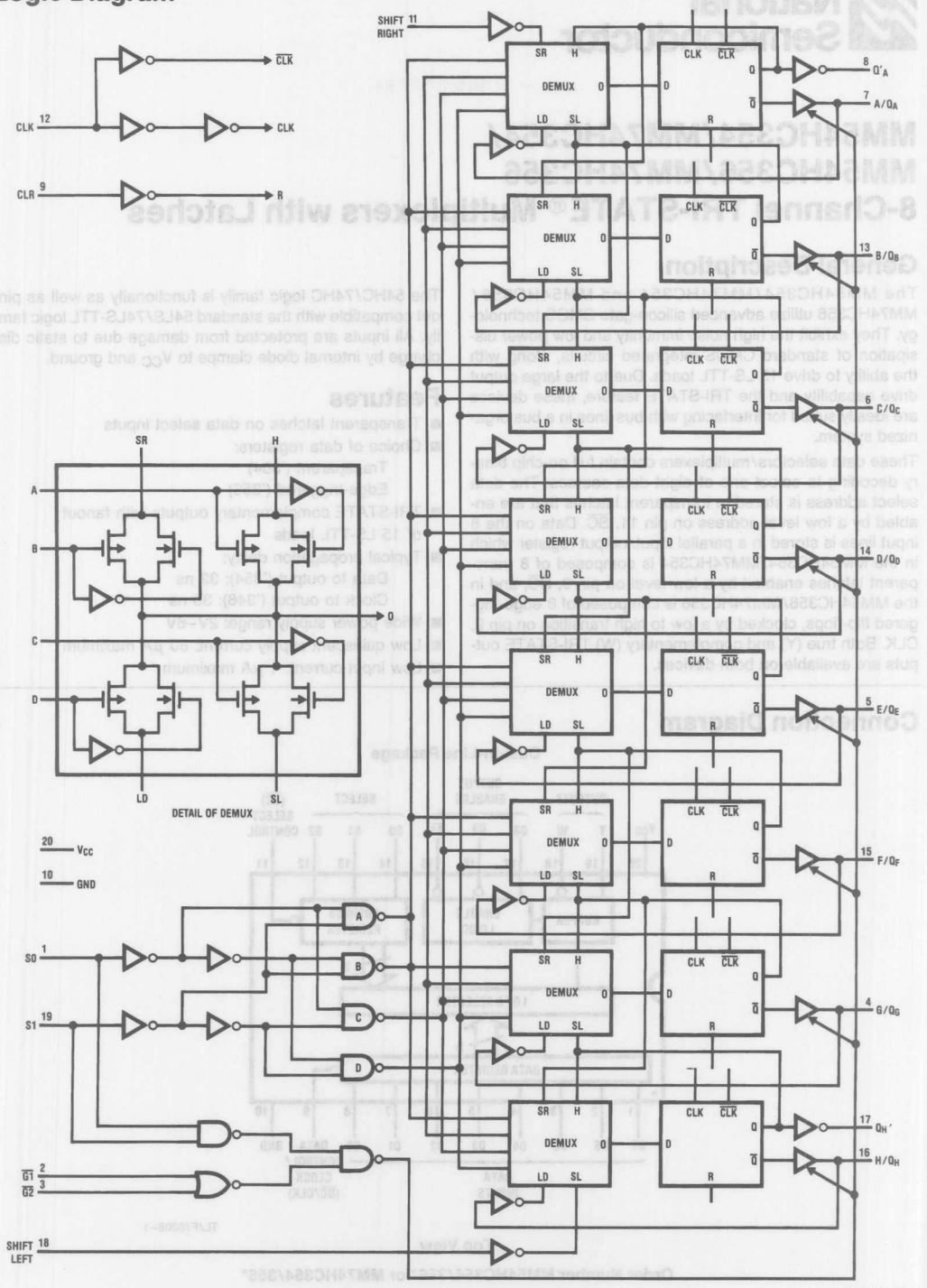
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L or H	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Logic Diagram



National Semiconductor

MM54HC354/MM74HC354/ MM54HC356/MM74HC356 8-Channel TRI-STATE® Multiplexers with Latches

General Description

The MM54HC354/MM74HC354 and MM54HC356/MM74HC356 utilize advanced silicon-gate CMOS technology. They exhibit the high noise immunity and low power dissipation of standard CMOS integrated circuits, along with the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data select address is stored in transparent latches that are enabled by a low level address on pin 11, $\overline{SC}$. Data on the 8 input lines is stored in a parallel input/output register which in the MM54HC354/MM74HC354 is composed of 8 transparent latches enabled by a low level on pin 9, $\overline{DC}$, and in the MM54HC356/MM74HC356 is composed of 8 edge-triggered flip-flops, clocked by a low to high transition on pin 9, CLK. Both true (Y) and complementary (W) TRI-STATE outputs are available on both devices.

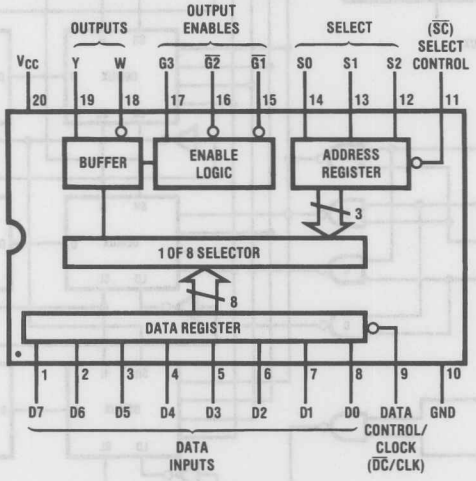
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS-TTL logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Transparent latches on data select inputs
- Choice of data registers:
  - Transparent ('354)
  - Edge-triggered ('356)
- TRI-STATE complementary outputs with fanout of 15 LS-TTL loads
- Typical propagation delay:
  - Data to output ('354): 32 ns
  - Clock to output ('346): 35 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5208–1

Top View

Order Number MM54HC354/356* or MM74HC354/356*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert < 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G1}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	$C_L = 45$ pF	32	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	$C_L = 45$ pF	38	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L = 45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L = 45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ $C_L = 45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 5$ pF	23	32	ns
t_S	Minimum Setup Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or $\overline{DC}$		10	15	ns

MM54HC356/MM74HC356

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	$C_L = 45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L = 45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L = 45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ $C_L = 45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 5$ pF	23	32	ns
t_S	Minimum Setup Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or CLK		10	15	ns

AC Electrical Characteristics MM54HC354/MM74HC354 (Continued)

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	C_L = 50 pF	2.0V	90	235	294	352	ns
		C_L = 150 pF	2.0V	100	275	344	412	ns
		C_L = 50 pF	4.5V	35	47	59	70	ns
		C_L = 150 pF	4.5V	40	55	68	83	ns
		C_L = 50 pF	6.0V	26	40	50	60	ns
		C_L = 150 pF	6.0V	32	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	C_L = 50 pF	2.0V	115	270	337	405	ns
		C_L = 150 pF	2.0V	125	310	387	465	ns
		C_L = 50 pF	4.5V	40	54	68	82	ns
		C_L = 150 pF	4.5V	46	62	78	93	ns
		C_L = 50 pF	6.0V	32	46	58	69	ns
		C_L = 150 pF	6.0V	38	52	66	78	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	C_L = 50 pF	2.0V	120	285	356	427	ns
		C_L = 150 pF	2.0V	130	325	406	488	ns
		C_L = 50 pF	4.5V	42	57	71	86	ns
		C_L = 150 pF	4.5V	50	65	81	97	ns
		C_L = 50 pF	6.0V	34	48	60	72	ns
		C_L = 150 pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	C_L = 50 pF	2.0V	120	300	375	450	ns
		C_L = 150 pF	2.0V	110	340	425	510	ns
		C_L = 50 pF	4.5V	45	60	75	90	ns
		C_L = 150 pF	4.5V	52	68	85	102	ns
		C_L = 50 pF	6.0V	36	51	64	77	ns
		C_L = 150 pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	50	125	156	188	ns
		C_L = 150 pF	2.0V	60	165	206	248	ns
		C_L = 50 pF	4.5V	18	25	31	38	ns
		C_L = 150 pF	4.5V	25	33	41	49	ns
		C_L = 50 pF	6.0V	15	21	26	32	ns
		C_L = 150 pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	68	165	206	248	ns
		C_L = 50 pF	4.5V	24	33	41	49	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Setup Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	6	50	60	75	ns
			4.5V	3	10	13	15	ns
			6.0V	3	10	13	15	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ or $\overline{DC}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	10	15	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

AC Electrical Characteristics MM54HC356/MM74HC356 (Continued)

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	C_L = 50 pF	2.0V	100	225	318	338	ns
		C_L = 150 pF	2.0V	110	295	369	442	ns
		C_L = 50 pF	4.5V	36	51	63	76	ns
		C_L = 150 pF	4.5V	42	59	73	90	ns
		C_L = 50 pF	6.0V	28	43	53	64	ns
		C_L = 150 pF	6.0V	34	50	63	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	C_L = 50 pF	2.0V	120	285	356	427	ns
		C_L = 150 pF	2.0V	130	325	406	488	ns
		C_L = 50 pF	4.5V	42	57	71	86	ns
		C_L = 150 pF	4.5V	50	65	81	97	ns
		C_L = 50 pF	6.0V	34	48	60	72	ns
		C_L = 150 pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	C_L = 50 pF	2.0V	120	300	375	450	ns
		C_L = 150 pF	2.0V	110	340	425	510	ns
		C_L = 50 pF	4.5V	45	60	75	90	ns
		C_L = 150 pF	4.5V	52	68	85	102	ns
		C_L = 50 pF	6.0V	36	51	64	77	ns
		C_L = 150 pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	50	125	156	188	ns
		C_L = 150 pF	2.0V	60	165	206	248	ns
		C_L = 50 pF	4.5V	18	25	31	38	ns
		C_L = 150 pF	4.5V	25	33	41	49	ns
		C_L = 50 pF	6.0V	15	21	26	32	ns
		C_L = 150 pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	68	165	206	248	ns
		C_L = 50 pF	4.5V	24	33	41	49	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Setup Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	6	50	60	75	ns
			4.5V	3	10	13	15	ns
			6.0V	3	10	13	15	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ to CLK		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	10	15	18	20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Function Table

Inputs								Outputs	
Select†			Data Control 'HC354	Clock 'HC356	Output Enables				
S1	S2	S0	$\overline{DC}$	CLK	$\overline{G}1$	$\overline{G}2$	G3	W	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D}0$	D0
L	L	L	H	H or L	L	L	H	$\overline{D}0_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D}1$	D1
L	L	H	H	H or L	L	L	H	$\overline{D}1_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D}2$	D2
L	H	L	H	H or L	L	L	H	$\overline{D}2_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D}3$	D3
L	H	H	H	H or L	L	L	H	$\overline{D}3_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D}4$	D4
H	L	L	H	H or L	L	L	H	$\overline{D}4_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D}5$	D5
H	L	H	H	H or L	L	L	H	$\overline{D}5_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D}6$	D6
H	H	L	H	H or L	L	L	H	$\overline{D}6_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D}7$	D7
H	H	H	H	H or L	L	L	H	$\overline{D}7_n$	$D7_n$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

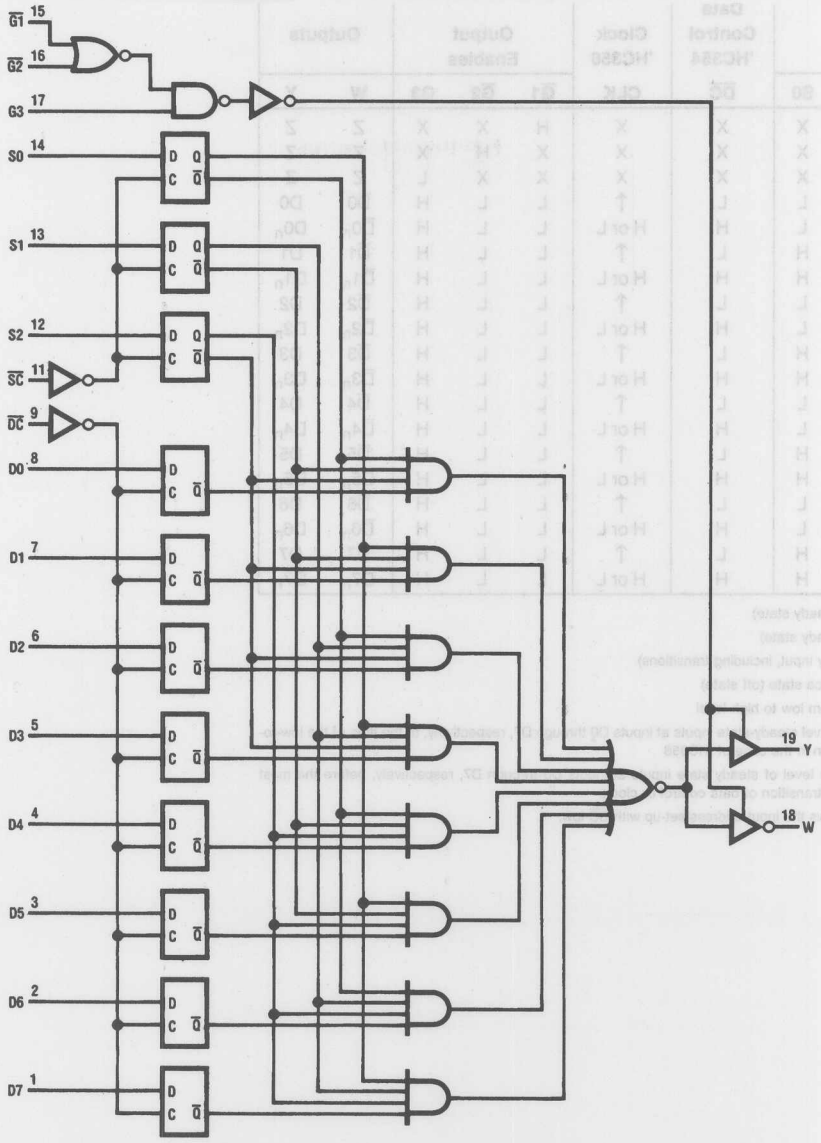
Z = high-impedance state (off state)

↑ = transition from low to high level

D0 . . . D7 = the level steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'HC356

$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock.

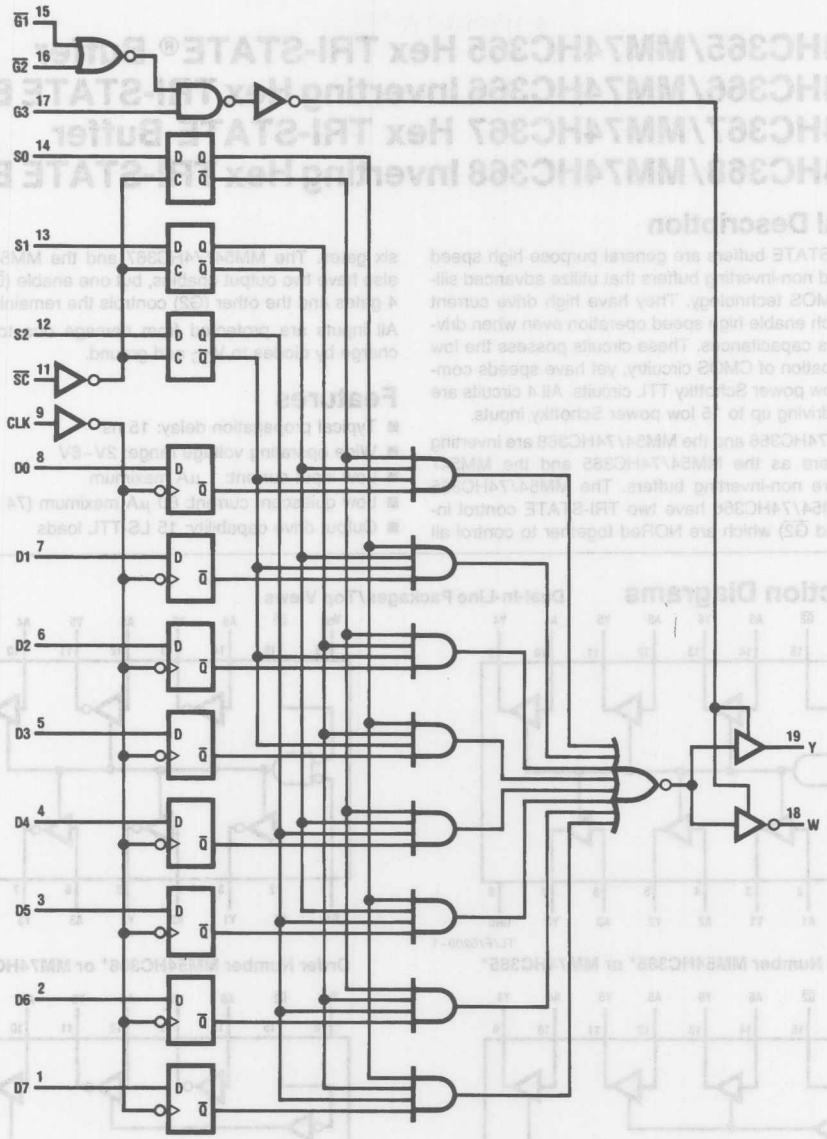
†This column shows the input address set-up with $\overline{SC}$ low.


G1 15
G2 16
G3 17
S0 14
S1 13
S2 12
SC 11
DC 9
D0 8
D1 7
D2 6
D3 5
D4 4
D5 3
D6 2
D7 1
D Q
C Q
19 Y
18 W

TL/F/5208–2

Logic Diagram

'HC356



TL/F/5208–3

National Semiconductor

MM54HC365/MM74HC365 Hex TRI-STATE® Buffer
MM54HC366/MM74HC366 Inverting Hex TRI-STATE Buffer
MM54HC367/MM74HC367 Hex TRI-STATE Buffer
MM54HC368/MM74HC368 Inverting Hex TRI-STATE Buffer

General Description

These TRI-STATE buffers are general purpose high speed inverting and non-inverting buffers that utilize advanced silicon-gate CMOS technology. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. All 4 circuits are capable of driving up to 15 low power Schottky inputs.

The MM54/74HC366 and the MM54/74HC368 are inverting buffers, where as the MM54/74HC365 and the MM54/74HC367 are non-inverting buffers. The MM54/74HC365 and the MM54/74HC366 have two TRI-STATE control inputs ($\overline{G1}$ and $\overline{G2}$) which are NORed together to control all six gates. The MM54/74HC367 and the MM54/74HC368 also have two output enables, but one enable ($\overline{G1}$) controls 4 gates and the other ($\overline{G2}$) controls the remaining 2 gates.

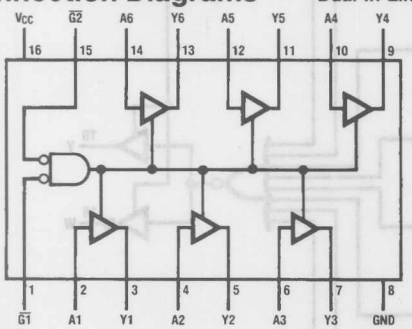
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

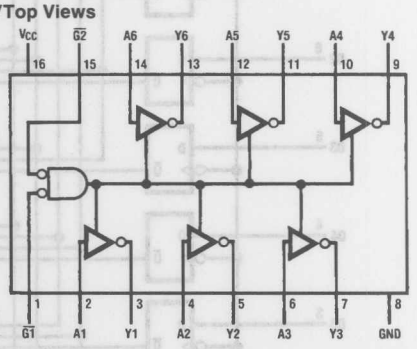
Connection Diagrams

Dual-In-Line Packages/Top Views



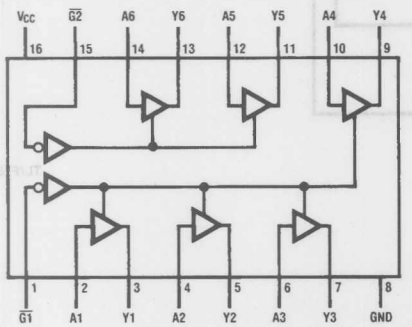
TL/F/5209–1

Order Number MM54HC365* or MM74HC365*



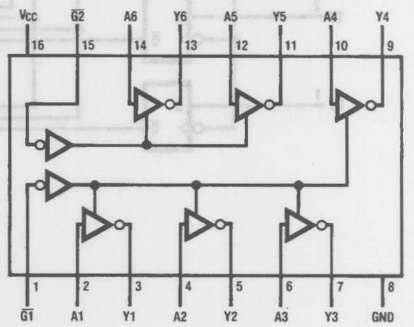
TL/F/5209–2

Order Number MM54HC366* or MM74HC366*



TL/F/5209–3

Order Number MM54HC367* or MM74HC367*



TL/F/5209–4

Order Number MM54HC368* or MM74HC368*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics MM54HC365/MM74HC365

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	15	22	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	36	ns

AC Electrical Characteristics MM54HC365/MM74HC365

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	35	105	130	150	ns
		$C_L=150$ pF	2.0V	45	135	168	205	ns
		$C_L=50$ pF	4.5V	14	24	30	36	ns
		$C_L=150$ pF	4.5V	17	29	36	45	ns
		$C_L=50$ pF	6.0V	11	19	24	28	ns
		$C_L=150$ pF	6.0V	15	24	30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	90	230	287	345	ns
		$C_L=150$ pF	2.0V	98	245	306	367	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	38	53	66	80	ns
		$C_L=50$ pF	6.0V	25	35	43	52	ns
		$C_L=150$ pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	58	175	218	260	ns
		$C_L=50$ pF	4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Truth Table

'HC365

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 45$ pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L = 1\ k\Omega$ $C_L = 45$ pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$ $C_L = 5$ pF	25	36	ns

AC Electrical Characteristics MM54HC366/MM74HC366

$V_{CC} = 2.0$–6.0V, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L = 50$ pF	2.0V	33	82	102	125	ns
		$C_L = 150$ pF	2.0V	43	107	134	160	ns
		$C_L = 50$ pF	4.5V	12	19	24	30	ns
		$C_L = 150$ pF	4.5V	16	26	32	39	ns
		$C_L = 50$ pF	6.0V	10	16	20	24	ns
		$C_L = 150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1\ k\Omega$						ns
		$C_L = 50$ pF	2.0V	90	230	287	345	ns
		$C_L = 150$ pF	2.0V	98	245	306	367	ns
		$C_L = 50$ pF	4.5V	31	44	55	66	ns
		$C_L = 150$ pF	4.5V	38	53	66	80	ns
		$C_L = 50$ pF	6.0V	25	35	43	52	ns
		$C_L = 150$ pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1\ k\Omega$ $C_L = 50$ pF	2.0V	58	175	218	260	ns
			4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Truth Table

'HC366

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

AC Electrical Characteristics (Continued) MM54HC367/MM74HC367

V_{CC} = 5V, T_A = 25°C, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	13	22	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	25	33	ns

AC Electrical Characteristics MM54HC367/MM74HC367

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C		54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	35	105	130	150	ns
		C_L = 150 pF	2.0V	45	135	168	205	ns
		C_L = 50 pF	4.5V	14	24	30	36	ns
		C_L = 150 pF	4.5V	17	29	36	45	ns
		C_L = 50 pF	6.0V	11	19	24	28	ns
		C_L = 150 pF	6.0V	15	24	30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						ns
		C_L = 50 pF	2.0V	69	172	216	250	ns
		C_L = 150 pF	2.0V	75	187	233	280	ns
		C_L = 50 pF	4.5V	24	38	47	57	ns
		C_L = 150 pF	4.5V	29	46	57	69	ns
		C_L = 50 pF	6.0V	22	35	43	52	ns
		C_L = 150 pF	6.0V	26	42	52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	47	117	146	220	ns
		C_L = 50 pF	4.5V	22	35	44	52	ns
			6.0V	19	31	39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table

'HC367

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

AC Electrical Characteristics (Continued) MM54HC368/MM74HC368

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	11	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	33	ns

AC Electrical Characteristics MM54HC368/MM74HC368

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	33	82	102	125	ns
		$C_L=150$ pF	2.0V	43	107	134	160	ns
		$C_L=50$ pF	4.5V	12	19	24	30	ns
		$C_L=150$ pF	4.5V	16	26	32	39	ns
		$C_L=50$ pF	6.0V	10	16	20	24	ns
		$C_L=150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	69	172	216	250	ns
		$C_L=150$ pF	2.0V	75	187	233	280	ns
		$C_L=50$ pF	4.5V	24	38	47	57	ns
		$C_L=150$ pF	4.5V	29	46	57	69	ns
		$C_L=50$ pF	6.0V	22	35	43	52	ns
		$C_L=150$ pF	6.0V	26	42	52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	117	146	220	ns
			4.5V	22	35	44	52	ns
			6.0V	19	31	39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Input Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

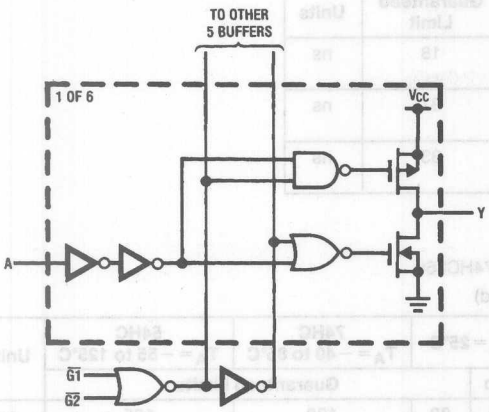
Truth Table

'HC368

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

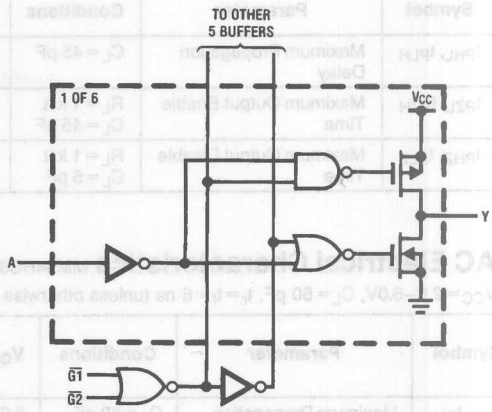
Logic Diagrams

MM54HC365/MM74HC365



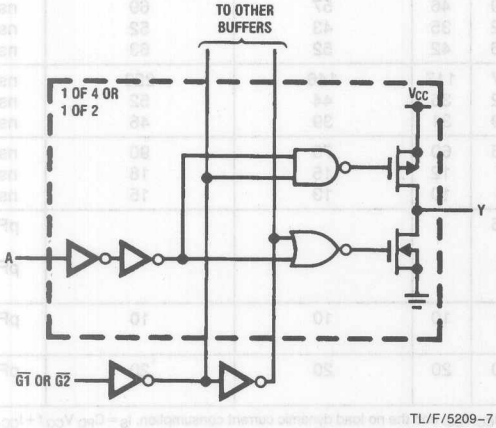
TL/F/5209–5

MM54HC366/MM74HC366



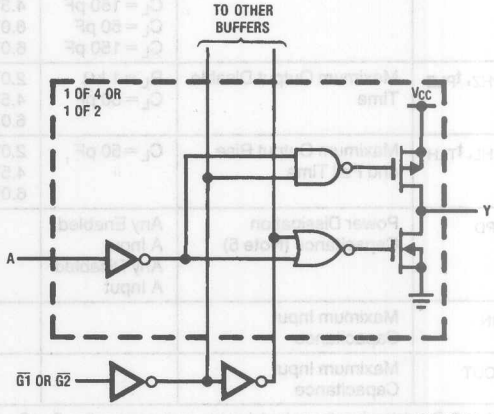
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MM54HC367/MM74HC367



TL/F/5209–7

MM54HC368/MM74HC368



TL/F/5209–8

MM54HC373/MM74HC373
TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

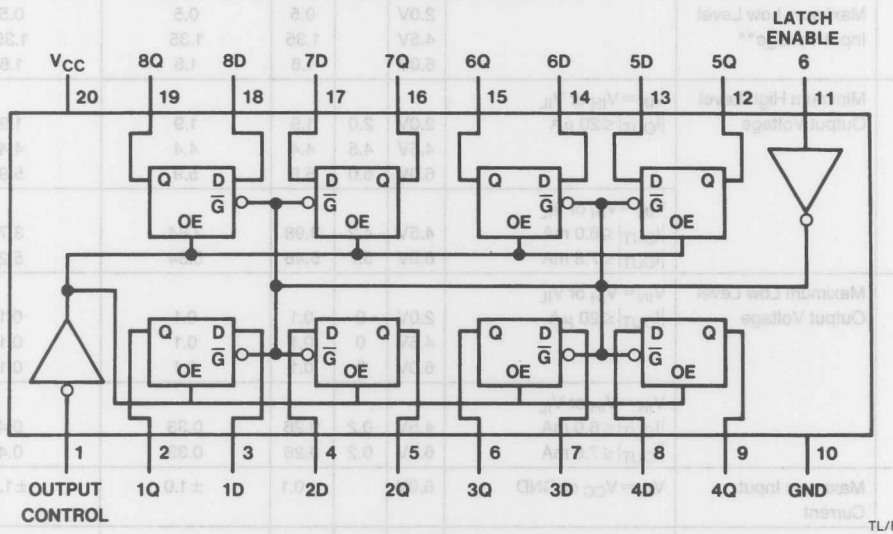
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5335–1

Top View

Order Number MM54HC373* or MM74HC373*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, OC = V_{IH} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V		50	60	75	ns
			4.5V		9	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch) OC = V_{CC}		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

MM54HC374/MM74HC374
TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed Octal D-Type Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

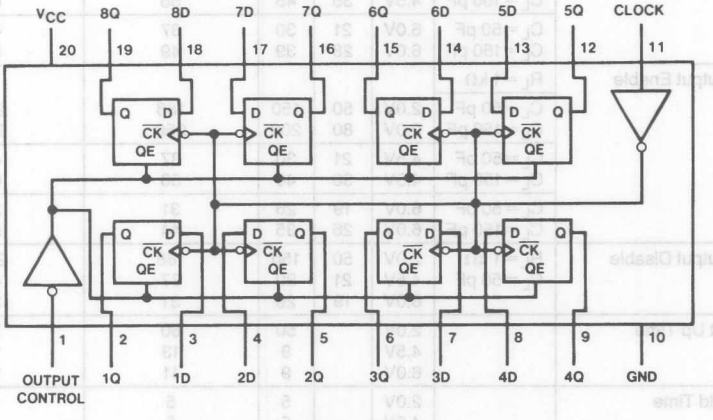
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5336–1

Top View

Order Number MM54HC374* or MM74HC374*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high Level, L = Low Level
X = don't Care
↑ = transition from low-to-high
Z = high impedance state
Q_0= the level of the output before steady state input conditions were established

DC Input Voltage (V_{IN})	-1.5 to $V_{CC}+1.5$V
DC Output Voltage (V_{OUT})	-0.5 to $V_{CC}+0.5$V
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA
DC Output Current, per pin (I_{OUT})	± 35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	± 70 mA
Storage Temperature Range (T_{STG})	-65°C to $+150$°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Temp. Range (T_A)				
MM74HC		-40	$+85$	°C
MM54HC		-55	$+125$	°C
Input Rise or Fall Times				
(t_r, t_f)	$V_{CC}=2.0$V		1000	ns
	$V_{CC}=4.5$V		500	ns
	$V_{CC}=6.0$V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	$T_A=25$°C	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20$ μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$, OC $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND	6.0V		± 0.5	± 5	± 10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0$ μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ± 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5$V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=$ kΩ $C_L=45$ pF	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=$ kΩ $C_L=5$ pF	17	25	ns
t_S	Minimum Setup Time			20	ns
t_H	Minimum Hold Time			5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	68	180	225	270	ns
		$C_L=150$ pF	2.0V	110	230	288	345	ns
		$C_L=50$ pF	4.5V	22	36	45	48	ns
		$C_L=150$ pF	4.5V	30	46	57	69	ns
		$C_L=50$ pF	6.0V	20	31	39	46	ns
		$C_L=150$ pF	6.0V	28	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	189	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Setup Time		2.0V		50	60	75	ns
			4.5V		9	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time		2.0V		5	30	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop) OC = V_{CC}		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC390/MM74HC390 Dual 4-Bit Decade Counter MM54HC393/MM74HC393 Dual 4-Bit Binary Counter

General Description

These counter circuits contain independent ripple carry counters and utilize advanced silicon-gate CMOS technology. The MM54HC390/MM74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter. The MM54HC393/MM74HC393 contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

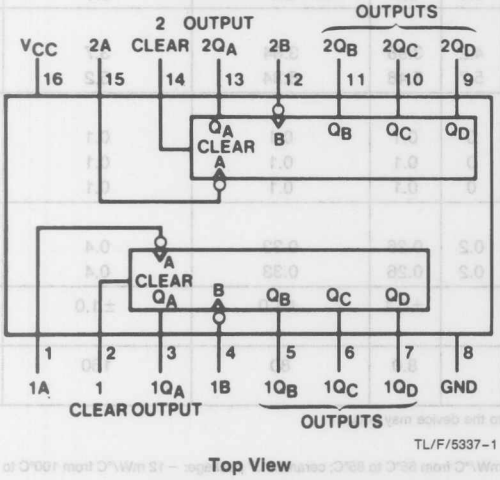
Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. These counters are functionally as well as pin equivalent to the 54LS390/74LS390 and the 54LS393/74LS393, respectively. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package



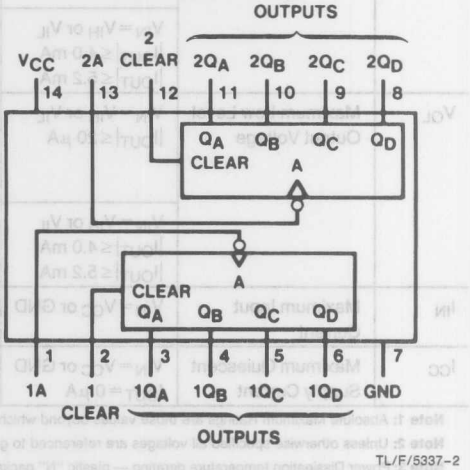
TL/F/5337–1

Top View

Order Number MM54HC390* or MM74HC390*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/5337–2

Top View

Order Number MM54HC393* or MM74HC393*

*Please look into Section 8, Appendix D for availability of various package types.

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency, Clock A or B		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A Connected to Clock B)		32	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		15	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		20	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Output		15	28	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_W	Minimum Pulse Width, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	3	MHz
			4.5V	27	21	18	MHz
			6.0V	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A Connected to Clock B)		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		2.0V	50	130	160	195	ns
			4.5V	16	26	33	39	ns
			6.0V	13	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		2.0V	60	185	230	280	ns
			4.5V	20	37	46	55	ns
			6.0V	17	32	40	48	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		2.0V	55	165	210	250	ns
			4.5V	17	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

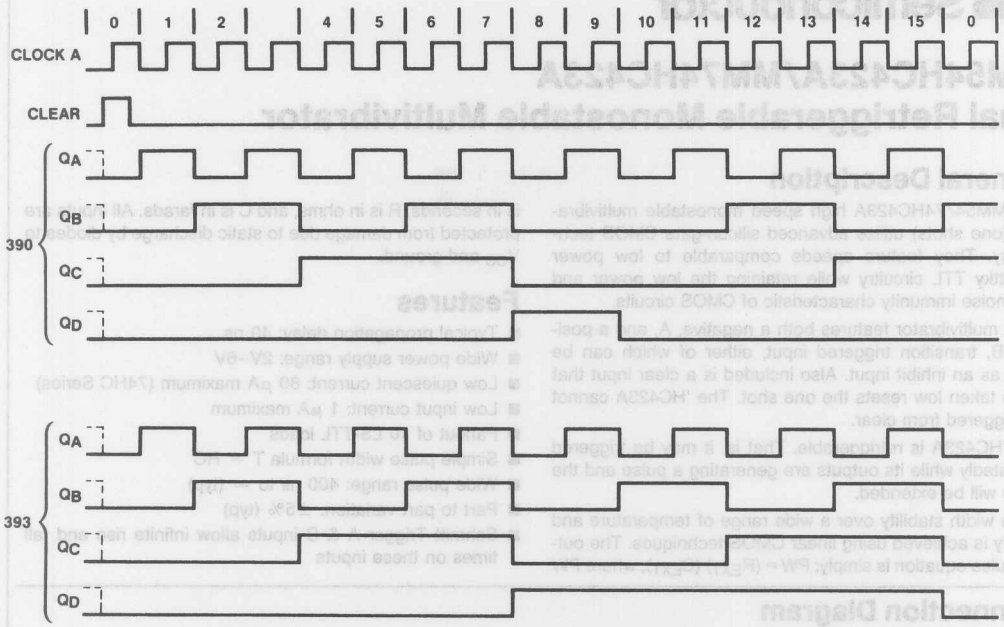
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_B		19	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C		23	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_D		27	50	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		15	28	ns
t_{REM}	Minimum Removal Time		−2	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_B		2.0V	68	190	240	285	ns
			4.5V	23	38	47	57	ns
			6.0V	20	32	40	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_C		2.0V	90	240	300	360	ns
			4.5V	30	48	60	72	ns
			6.0V	26	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_D		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}	Maximum Propagation Delay Clear to any Q		2.0V	54	165	210	250	ns
			4.5V	18	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Clear Removal Time		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		42				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Timing Waveforms



TL/F/5337–3

National Semiconductor

MM54HC423A/MM74HC423A
Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC423A high speed monostable multivibrators (one shots) utilize advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC423A cannot be triggered from clear.

The 'HC423A is retriggerable. That is, it may be triggered repeatedly while its outputs are generating a pulse and the pulse will be extended.

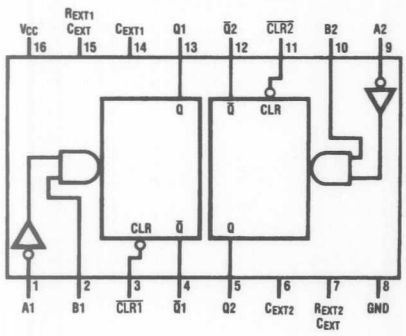
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs allow infinite rise and fall times on these inputs

Connection Diagram

Dual-In-Line Package



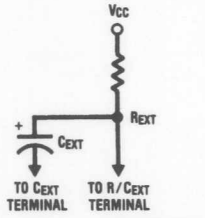
TL/F/5338–1

Top View

Order Number MM54HC423A* or MM74HC423A*

*Please look into Section 8, Appendix D for availability of various package types.

Timing Component



TL/F/5338–2

Note: Pin 6 and Pin 14 must be hard-wired to GND.

Truth Table

Inputs			Outputs	
$\overline{\text{Clear}}$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Maximum Input Rise and Fall Time (Clear Input)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}					V
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.96	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}					V
		$\|I_{OUT}\| \leq 4$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN} = V_{CC} or GND	5.0V		0.5	5.0	5.0	μA
I_{IN}	Maximum Input Current (all other pins)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (standby)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN} = V_{CC} or GND R/C_{EXT} = 0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

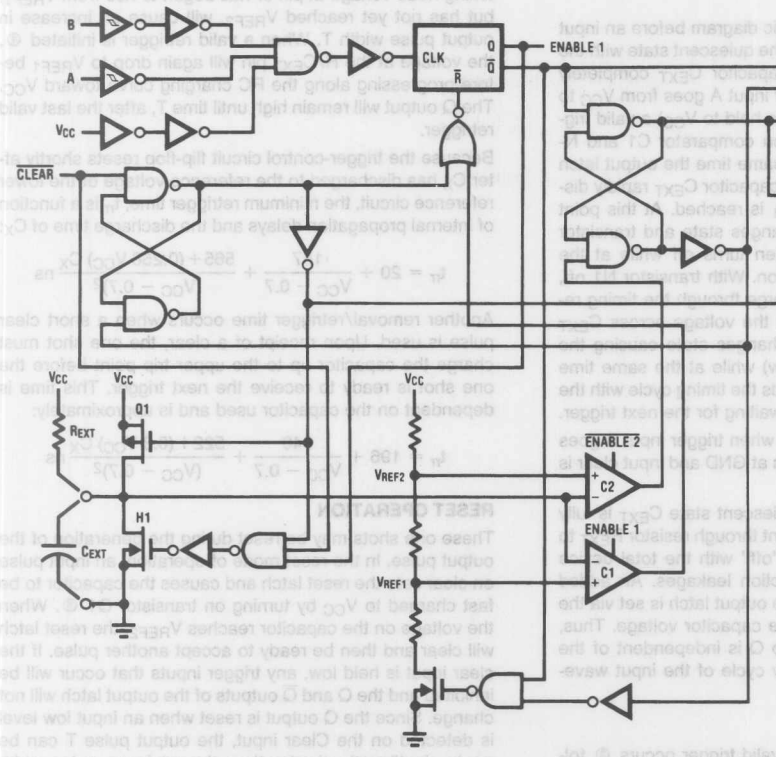
Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay, A, B to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT} = 28$ pF $R_{EXT} = 2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT} = 1000$ pF $R_{EXT} = 10$ kΩ	10		μs

AC Electrical Characteristics $C_L = 50$ pF $t_r = t_f = 6$ ns (Unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Trigger Propagation Delay, A or B to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	ns
				6.0V	21	32	39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay, A or B to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	ns
				6.0V	24	38	46	51	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	ns
				6.0V	19	28	33	36	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	ns
				6.0V	20	29	34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	ns
				6.0V	12	21	27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V	0	0	0	0	ns
				4.5V	0	0	0	0	ns
				6.0V	0	0	0	0	ns
t_{WQ}	Output Pulse Width	$C_{EXT} = 0.1$ μF $R_{EXT} = 10$ kΩ	Min	5.0V	1	0.9	0.86	0.85	ms
			Max	5.0V	1	1.1	1.14	1.15	ms
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)				83				pF
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (other inputs)				6	10	10	10	pF

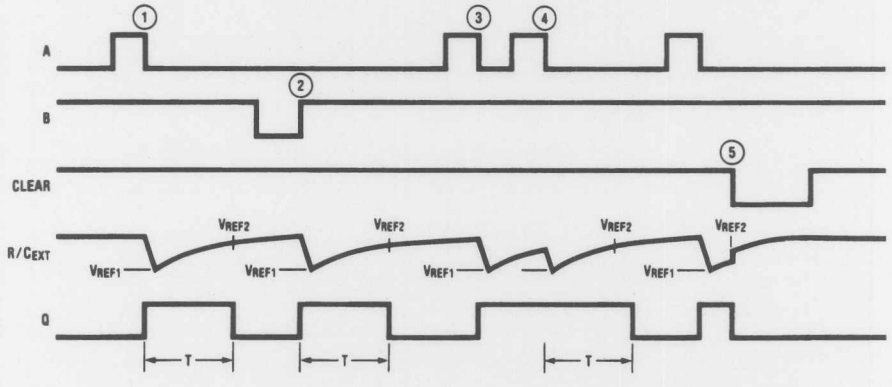
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5338–5

Theory of Operation



① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING

TL/F/5338–6

FIGURE 1

Theory of Operation (Continued)

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one-shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the one-shot in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC} ②.)

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC423A is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The 'HC423A is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

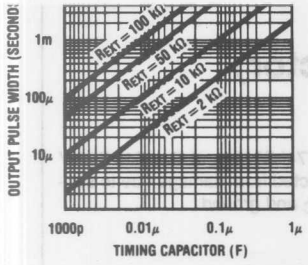
$$t_{rr} = 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256\ V_{CC})\ C_X}{(V_{CC} - 0.7)^2}\ \text{ns}$$

Another removal/retrigger time occurs when a short clear pulse is used. Upon receipt of a clear, the one shot must charge the capacitor up to the upper trip point before the one shot is ready to receive the next trigger. This time is dependent on the capacitor used and is approximately:

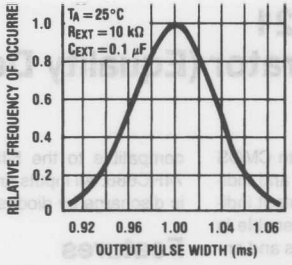
$$t_{rr} = 196 + \frac{640}{V_{CC} - 0.7} + \frac{522 + (0.3\ V_{CC})\ C_X}{(V_{CC} - 0.7)^2}\ \text{ns}$$

RESET OPERATION

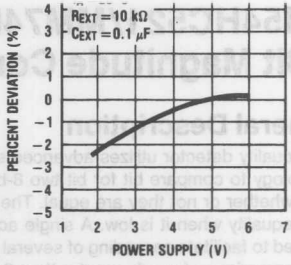
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.



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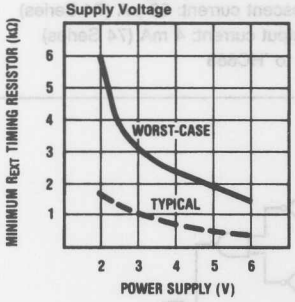


TL/F/5338–8



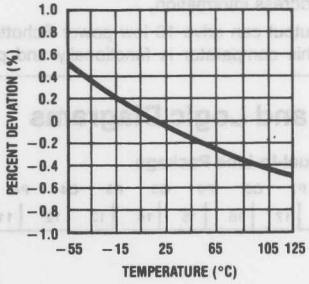
TL/F/5338–9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5338–10

Typical 1ms Pulse Width Variation vs. Temperature



TL/F/5338–11

Note: R and C are not subjected to temperature. The C is polypropylene.

MM54HC521/MM74HC521
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

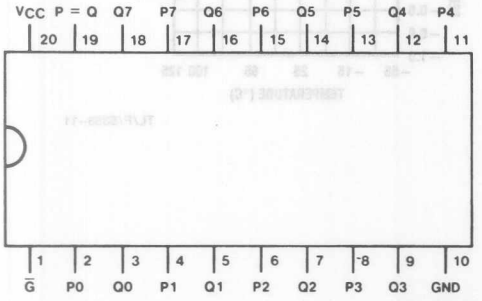
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 54LS688/74LS688 and the 54HC688/74HC688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 Series)
- Large output current: 4 mA (74 Series)
- Identical to 'HC688

Connection and Logic Diagrams

Dual-In-Line Package

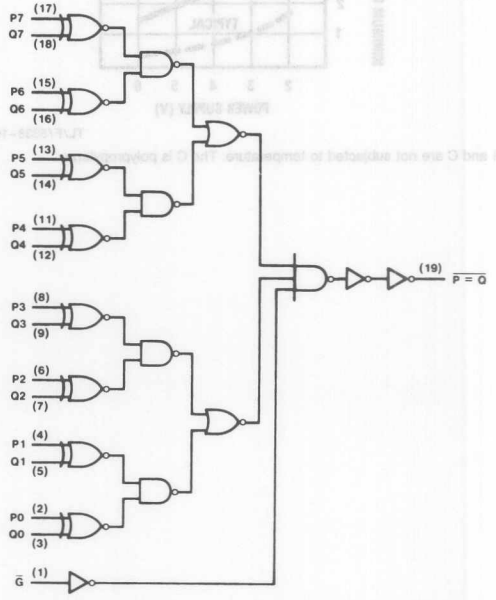


TL/F/6128–1

Top View

Order Number MM54HC521* or MM74HC521*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/6128–2

Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any P or Q to Output		21	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		14	20	ns

AC Electrical Characteristics

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, P or Q to Output		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Output		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

MM54HC533/MM74HC533 TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed OCTAL D-TYPE LATCHES utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the data present on the D inputs will appear inverted at the $\overline{Q}$ outputs. When the LATCH ENABLE goes low, the inverted data will be retained at the $\overline{Q}$ outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

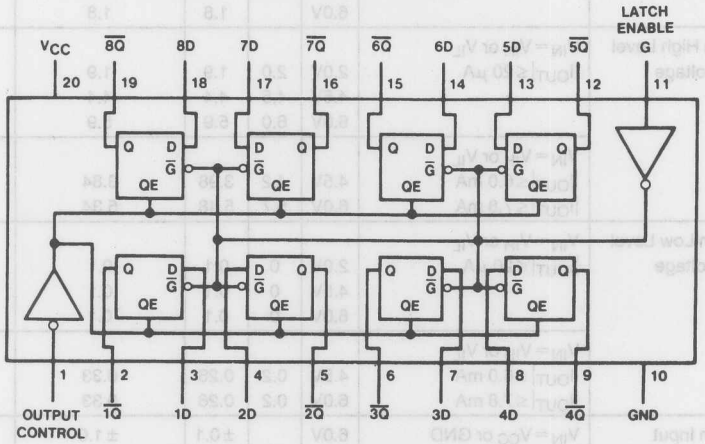
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA, maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5339–1

Top View

Order Number MM54HC533* or MM74HC533*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, OC = V_{IH} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V		50	60	75	ns
			4.5V		9	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time, Clock	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch) OC = V_{CC} OC = Gnd		30 50				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

MM54HC534/MM74HC534 TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These high speed Octal D-Type Flip-Flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

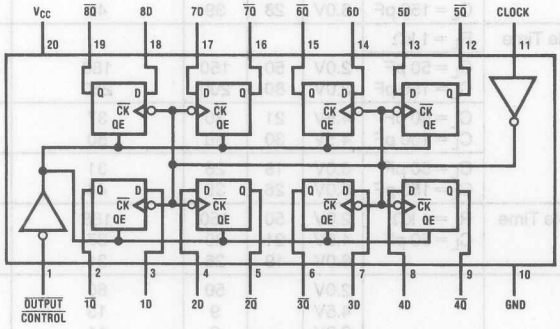
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 23 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5340–1

Top View

Order Number MM54HC534* or MM74HC534*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
$\overline{Q}_0$ = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} | I_{OUT} | ≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} | I_{OUT} | ≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		| I_{OUT} | ≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} | I_{OUT} | ≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} | I_{OUT} | ≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		| I_{OUT} | ≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to $\overline{Q}$	$C_L=45$ pF	23	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	21	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	25	ns
t_S	Minimum Setup Time		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	68	180	225	270	ns
		$C_L=150$ pF	2.0V	110	230	288	345	ns
		$C_L=50$ pF	4.5V	22	36	45	48	ns
		$C_L=150$ pF	4.5V	30	46	57	69	ns
		$C_L=50$ pF	6.0V	20	31	39	46	ns
		$C_L=150$ pF	6.0V	28	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	29	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	25	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	189	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Setup Time		2.0V		50	60	75	ns
			4.5V		9	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time Clock				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)						
		OC = V_{CC}		30				pF
		OC = Gnd		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

MM54HC540/MM74HC540 Inverting Octal TRI-STATE® Buffer MM54HC541/MM74HC541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Both devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC540/MM74HC540 is an inverting buffer and the MM54HC541/MM74HC541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

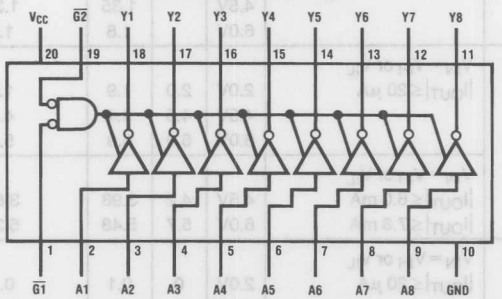
In order to enhance PC board layout, the 'HC540 and 'HC541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Output current: 6 mA

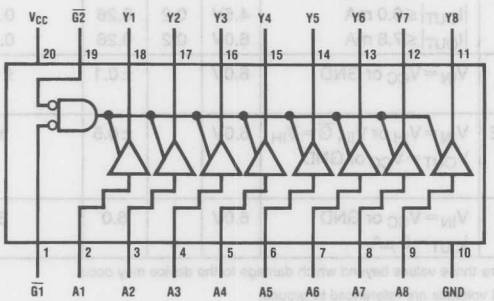
Connection Diagrams

Dual-In-Line Package



TL/F/5341–1

Top View
Order Number MM54HC540* or MM74HC540*



TL/F/5341–2

Top View
Order Number MM54HC541* or MM74HC541*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7 V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1 V
			4.5V	0	0.1	0.1	0.1 V
			6.0V	0	0.1	0.1	0.1 V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4 V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, $\overline{G}$ = V_{IH} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5	±10 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160 μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	$C_L=45$ pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	$C_L=45$ pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	83	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	18	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	11	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}=V_{IH}$		10				pF
		$\overline{G}=V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

MM54HC563/MM74HC563
TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE (LE) input is high, the data present on the D inputs will appear inverted at the $\overline{Q}$ outputs. When the LATCH ENABLE goes low, the inverted data will be retained at the $\overline{Q}$ outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

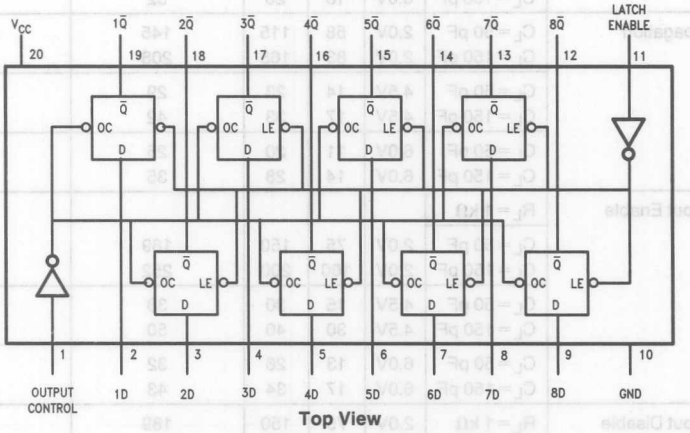
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- Functionally compatible with '580

Connection Diagram

Dual-In-Line Package



TL/F/5210–1

Top View

Order Number MM54HC563* or MM74HC563*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level

$\overline{Q}_0$ = level of output before steady-state input conditions were established

Z = high impedance

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CC})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA			8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to $\overline{Q}$	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time, Data to LE		10	15	ns
t_H	Minimum Hold Time, LE to Data		2	5	ns
t_W	Minimum Pulse Width, LE or Data		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	45	110	138	165	ns
		$C_L=150$ pF	2.0V	58	150	188	225	ns
		$C_L=50$ pF	4.5V	14	22	28	33	ns
		$C_L=150$ pF	4.5V	21	30	38	40	ns
		$C_L=50$ pF	6.0V	12	19	24	29	ns
		$C_L=150$ pF	6.0V	19	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to $\overline{Q}$	$C_L=50$ pF	2.0V	46	115	143	173	ns
		$C_L=150$ pF	2.0V	60	155	194	233	ns
		$C_L=50$ pF	4.5V	14	23	29	35	ns
		$C_L=150$ pF	4.5V	21	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	19	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	55	140	175	210	ns
		$C_L=150$ pF	2.0V	67	180	225	270	ns
		$C_L=50$ pF	4.5V	15	28	35	42	ns
		$C_L=150$ pF	4.5V	24	36	45	54	ns
		$C_L=50$ pF	6.0V	14	24	30	36	ns
		$C_L=150$ pF	6.0V	22	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	40	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	12	21	27	32	ns
t_S	Minimum Set Up Time Data to LE		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_H	Minimum Hold Time LE to Data		2.0V		25	31	38	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_W	Minimum Pulse Width, LE or Data		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC = V_{CC}		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC564/MM74HC564 TRI-STATE® Octal D-Type Edge-Triggered Flip-Flop with Inverted Outputs

General Description

These octal D-type flip-flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are inverted and transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

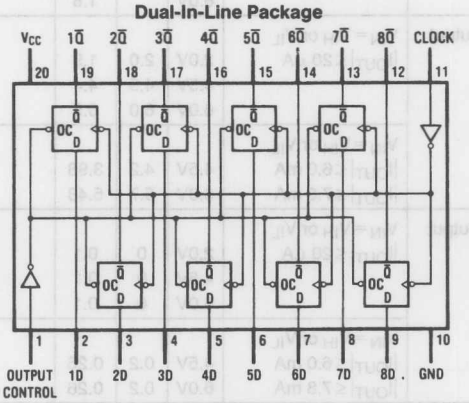
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- Functionally compatible with 54/74LS576

Connection Diagram

Dual-In-Line Package



TL/F/5211–1

Order Number MM54HC564* or MM74HC564*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High Impedance State
$\overline{Q}_0$ = The level of the output before steady state Input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V
			4.5V	3.15	3.15	3.15	V
			6.0V	4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V	0.5	0.5	0.5	V
			4.5V	1.35	1.35	1.35	V
			6.0V	1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

[illegible]	[illegible]	C_L = 45 pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	11	20	ns
t_S	Minimum Setup Time, Data to Clock		10	20	ns
t_H	Minimum Hold Time, Clock to Data		−3	0	ns
t_W	Minimum Clock Pulse Width		8	16	ns

AC Electrical Characteristics

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	C_L = 50 pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	C_L = 50 pF	2.0V	40	115	143	173	ns
		C_L = 150 pF	2.0V	51	155	194	233	ns
		C_L = 50 pF	4.5V	13	23	29	35	ns
		C_L = 150 pF	4.5V	19	31	47	47	ns
		C_L = 50 pF	6.0V	12	20	25	30	ns
		C_L = 150 pF	6.0V	18	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	45	140	175	210	ns
		C_L = 150 pF	2.0V	59	180	225	270	ns
		C_L = 50 pF	4.5V	14	28	35	42	ns
		C_L = 150 pF	4.5V	20	36	45	54	ns
		C_L = 50 pF	6.0V	12	24	30	36	ns
		C_L = 150 pF	6.0V	18	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	35	125	156	188	ns
			4.5V	12	25	31	38	ns
			6.0V	10	21	27	32	ns
t_S	Minimum Setup Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_W	Minimum Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	8	16	20	24	ns
			6.0V	7	14	18	20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC = VCC		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

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MM54HC573/MM74HC573 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE(LE) input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL OC input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

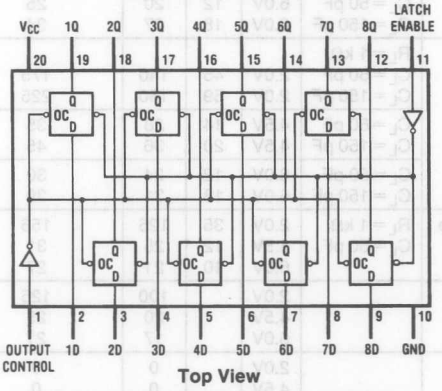
The 54HC/74HC logic family is speed, function and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



Top View

TL/F/5212–1

Order Number MM54HC573* or MM74HC573*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ		Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND OC=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L = 45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L = 45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ $C_L = 45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 5$ pF	11	20	ns
t_S	Minimum Set Up Time, Data to LE		10	15	ns
t_H	Minimum Hold Time, LE to Data		2	5	ns
t_W	Minimum Pulse Width, LE or Data		10	16	ns

AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Q	$C_L = 50$ pF	2.0V	45	110	138	165	ns
		$C_L = 150$ pF	2.0V	58	150	188	225	ns
		$C_L = 50$ pF	4.5V	14	22	28	33	ns
		$C_L = 150$ pF	4.5V	21	30	38	40	ns
		$C_L = 50$ pF	6.0V	12	19	24	29	ns
		$C_L = 150$ pF	6.0V	19	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Latch Enable to Q	$C_L = 50$ pF	2.0V	46	115	143	173	ns
		$C_L = 150$ pF	2.0V	60	155	194	233	ns
		$C_L = 50$ pF	4.5V	14	23	29	35	ns
		$C_L = 150$ pF	4.5V	21	31	47	47	ns
		$C_L = 50$ pF	6.0V	12	20	25	30	ns
		$C_L = 150$ pF	6.0V	19	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ						
		$C_L = 50$ pF	2.0V	55	140	175	210	ns
		$C_L = 150$ pF	2.0V	67	180	225	270	ns
		$C_L = 50$ pF	4.5V	15	28	35	42	ns
		$C_L = 150$ pF	4.5V	24	36	45	54	ns
		$C_L = 50$ pF	6.0V	14	24	30	36	ns
		$C_L = 150$ pF	6.0V	22	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ $C_L = 50$ pF	2.0V	40	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	12	21	27	32	ns
t_S	Minimum Set Up Time Data to LE		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_H	Minimum Hold Time LE to Data		2.0V		25	31	38	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_W	Minimum Pulse Width LE, or Data		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time, Clock	$C_L = 50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC = V_{CC}		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

MM54HC574/MM74HC574
TRI-STATE® Octal D-Type Edge-Triggered Flip-Flop

General Description

These high speed octal D-type flip-flops utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

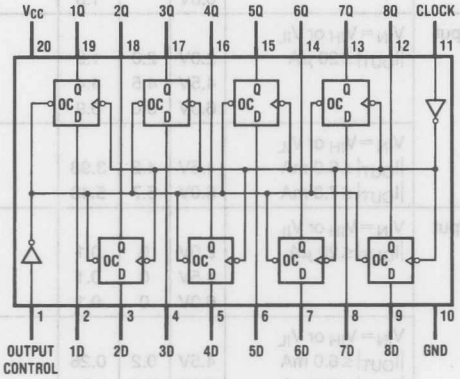
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5213–1

Top View

Order Number MM54HC574* or MM74HC574*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
X = don't care
↑ = transition from low-to-high
Z = high impedance state
Q_0 = the level of the output before steady state input conditions were established

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Setup Time, Data to Clock		10	20	ns
t_H	Minimum Hold Time, Clock to Data		−3	0	ns
t_W	Minimum Pulse Clock Width		8	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	6	5	4	MHz
			4.5V	30	24	20	MHz
			6.0V	35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	40	115	143	173	ns
		$C_L=150$ pF	2.0V	51	155	194	233	ns
		$C_L=50$ pF	4.5V	13	23	29	35	ns
		$C_L=150$ pF	4.5V	19	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	18	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	45	140	175	210	ns
		$C_L=150$ pF	2.0V	59	180	225	270	ns
		$C_L=50$ pF	4.5V	14	28	35	42	ns
		$C_L=150$ pF	4.5V	20	36	45	54	ns
		$C_L=50$ pF	6.0V	12	24	30	36	ns
		$C_L=150$ pF	6.0V	18	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	35	125	156	188	ns
			4.5V	12	25	31	38	ns
			6.0V	10	21	27	32	ns
t_S	Minimum Setup Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_W	Minimum Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC = VCC		30				pF
		OC = GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

MM54HC589/MM74HC589
8-Bit Shift Registers with Input Latches and TRI-STATE® Serial Output

General Description

This high speed shift register utilizes advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

The 'HC589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Data can also be entered serially the shift register through the SER pin. Both the storage register and shift register have positive-edge triggered clocks, RCK and SCK, respectively. $\overline{SLOAD}$ pin controls parallel LOAD or serial shift operations for the shift register. The shift register has a TRI-STATE output to enable the wire-ORing of multiple devices on a serial bus.

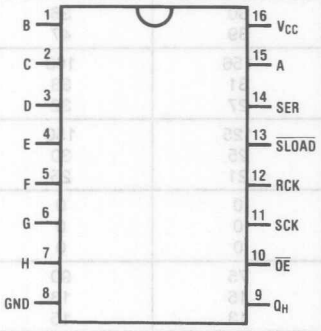
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load
- Guaranteed shift frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum (74HC Series)
- TRI-STATE output for 'Wire-OR'

Connection Diagram

Dual-In-Line Package



TL/F/5368–1

Top View

Order Number MM54HC589* or MM74HC589*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{OE}$	Function
X	X	X	H	Q_H in Hi-Z State
X	X	X	L	Q_H is enabled
↑	X	X	X	Data loaded into input latches
↑	X	L	X	Data loaded into shift register from pins
H or L	X	L	X	Data loaded from latches to shift register
X	↑	H	X	Shift register is shifted. Data on SER pin is shifted in.
↑	↑	H	X	Data is shifted in shift register, and data is loaded into latches

Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V		3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V		0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA
I_{OZ}	Maximum Three-State Leakage Current	Output in High Impedance State V_{IN} = V_{IL} or V_{IH} V_{OUT} = V_{CC} or GND $\overline{OE}$ = V_{IH}	6.0V		±0.5	±5.0	±10.0	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SLOAD}$ to $Q_{H'}$			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from LCK to $Q_{H'}$	$\overline{SLOAD}$ = logic '0'	25	45	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L=1$ kΩ, $C_L=5$ pF	19	25	ns
t_S	Minimum Setup Time from RCK to SCK		10	20	ns
t_S	Minimum Setup Time from SER to SCK		10	20	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$		8	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency for SCK		2.0V		6	4.8	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to Q_H		2.0V	62	175	220	265	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	37	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to Q_H	$C_L=150$ pF	2.0V	120	225	280	340	ns
			4.5V	31	45	56	68	ns
			6.0V	28	38	48	58	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_H		2.0V	80	210	265	315	ns
			4.5V	25	42	53	63	ns
			6.0V	21	36	45	54	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay RCK to Q_H	$C_L=150$ pF	2.0V	80	210	265	313	ns
			4.5V	25	52	66	77	ns
			6.0V	21	44	56	66	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L=1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_S	Minimum Setup Time from RCK to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_H	Minimum Hold Time		2.0V	−5	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	1	5	5	5	ns

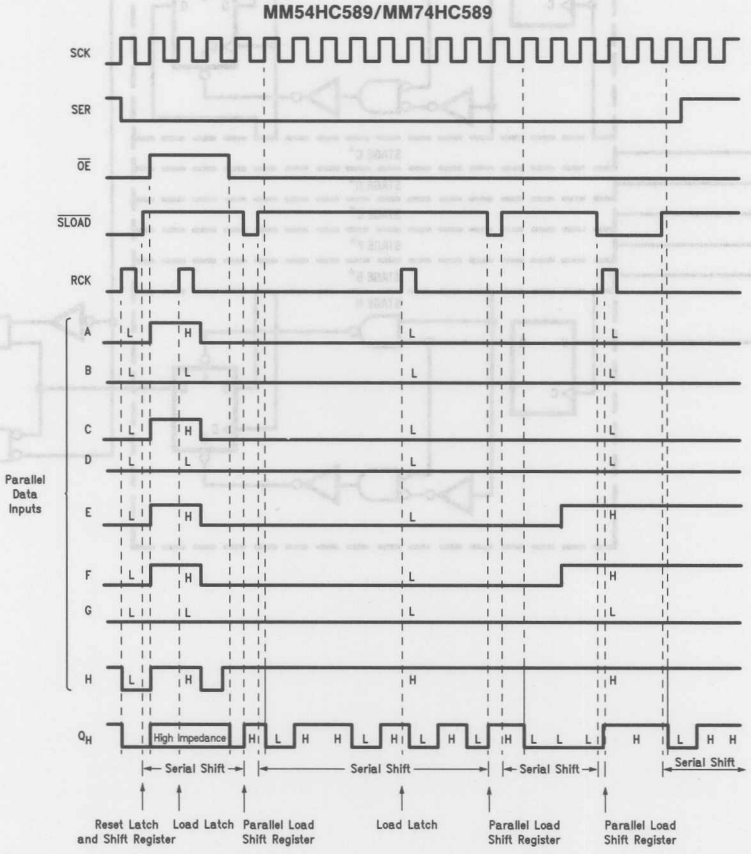
AC Electrical Characteristics (Continued)

V_{CC} = 2.0–6V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_W	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$, SLOAD		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1500	1500	1500	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	12	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			87				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

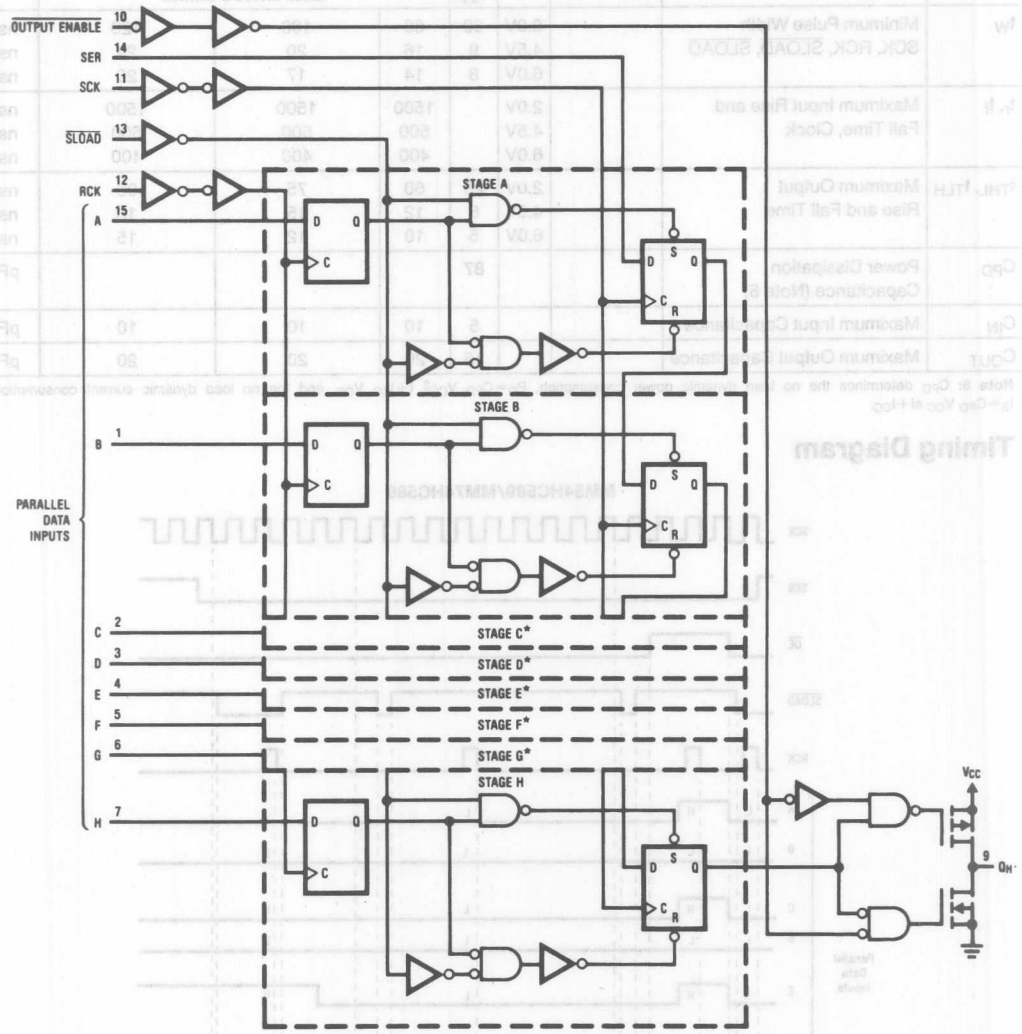
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ sf + I_{CC}$.

Timing Diagram



Functional Block Diagram (positive logic)

MM54HC589/MM74HC589



TL/F/5368–2

National Semiconductor

MM54HC595/MM74HC595
8-Bit Shift Registers with Output Latches

General Description

This high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 TRI-STATE® outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

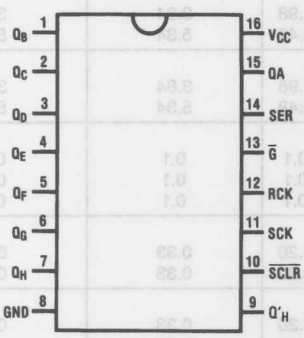
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

Connection Diagram

Dual-In-Line Package



TL/F/5342–1

Top View

Order Number MM54HC595* or MM74HC595*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Function
X	X	X	H	Q_A thru Q_H = TRI-STATE
X	X	L	L	Shift Register cleared $Q'_H = 0$
X	↑	H	L	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	L	Contents of Shift Register transferred to output latches

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	Q'_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	Q'_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to $Q_{H'}$	$C_L=45$ pF	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	$C_L=45$ pF	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q_H	$R_L=$ kΩ $C_L=5$ pF	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
t_S	Minimum Setup Time from $\overline{SCLR}$ to SCK			20	ns
t_S	Minimum Setup Time from SCK to RCK (See Note 5)			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

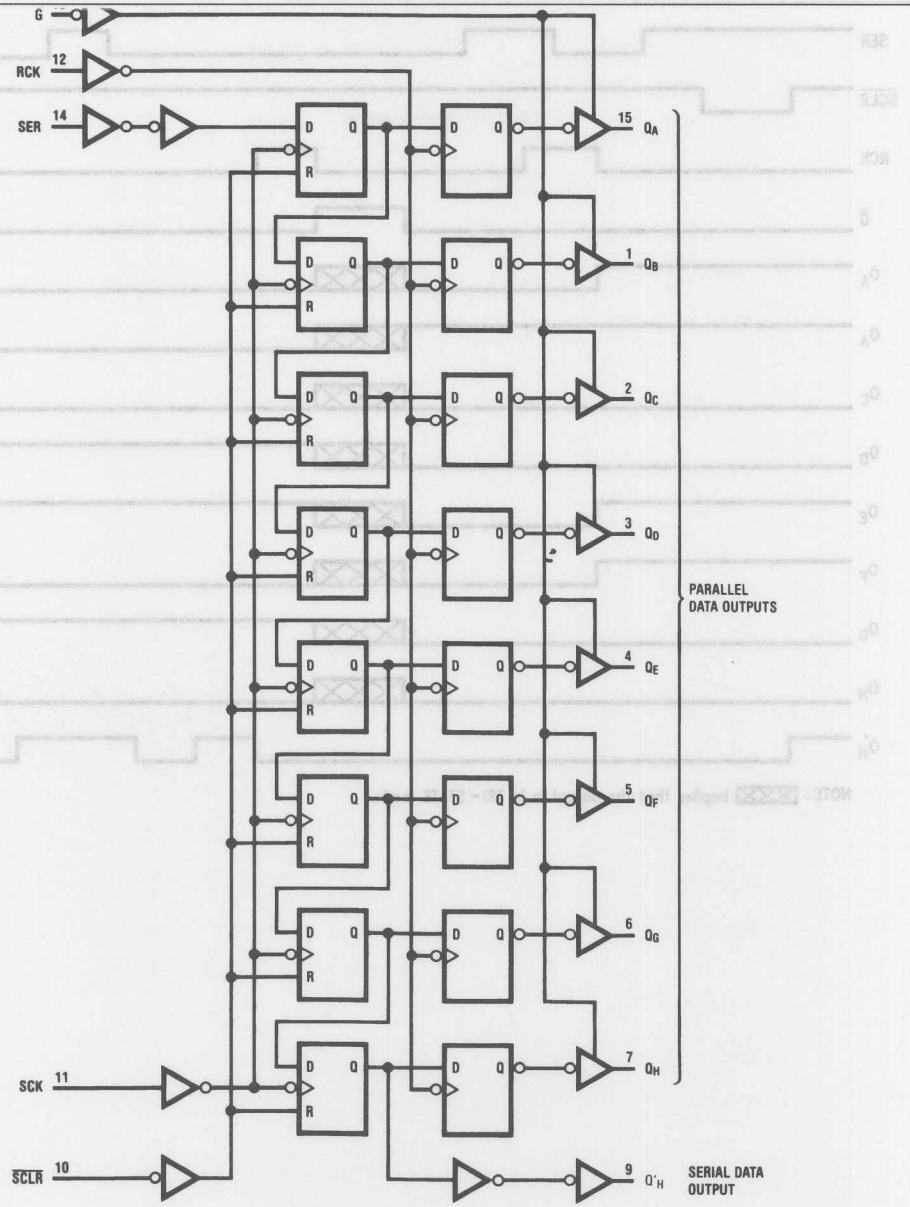
Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	10	6	4.8	4.0	MHz
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q'_H	$C_L=50$ pF	2.0V	58	210	265	315	ns
		$C_L=150$ pF	2.0V	83	294	367	441	ns
		$C_L=50$ pF	4.5V	14	42	53	63	ns
		$C_L=150$ pF	4.5V	17	58	74	88	ns
		$C_L=50$ pF	6.0V	10	36	45	54	ns
		$C_L=150$ pF	6.0V	14	50	63	76	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	$C_L=50$ pF	2.0V	70	175	220	265	ns
		$C_L=150$ pF	2.0V	105	245	306	368	ns
		$C_L=50$ pF	4.5V	21	35	44	53	ns
		$C_L=150$ pF	4.5V	28	49	61	74	ns
		$C_L=50$ pF	6.0V	18	30	37	45	ns
		$C_L=150$ pF	6.0V	26	42	53	63	ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SCLR}$ to Q'_H		2.0V		175	221	261	ns
			4.5V		35	44	52	ns
			6.0V		30	37	44	ns
t_{PZH}, t_{PZL}	Maximum Output Enable from $\overline{G}$ to Q_A thru Q_H	$R_L = 1\ k\Omega$						
		$C_L = 50$ pF	2.0V	75	175	220	265	ns
		$C_L = 150$ pF	2.0V	100	245	306	368	ns
		$C_L = 50$ pF	4.5V	15	35	44	53	ns
		$C_L = 150$ pF	4.5V	20	49	61	74	ns
		$C_L = 50$ pF	6.0V	13	30	37	45	ns
		$C_L = 150$ pF	6.0V	17	42	53	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q_H	$R_L = 1\ k\Omega$	2.0V	75	175	220	265	ns
		$C_L = 50$ pF	4.5V	15	35	44	53	ns
			6.0V	13	30	37	45	ns
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_R	Minimum Removal Time from $\overline{SCLR}$ to SCK		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_S	Minimum Setup Time from SCK to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	26	ns
t_H	Minimum Hold Time SER to SCK		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width of SCK or $\overline{SCLR}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	22	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time Q_A–Q_H		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time Q'_H		2.0V		75	95	110	ns
			4.5V		15	19	22	ns
			6.0V		13	16	19	ns
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G} = V_{CC}$		90				pF
		$\overline{G} = GND$		150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

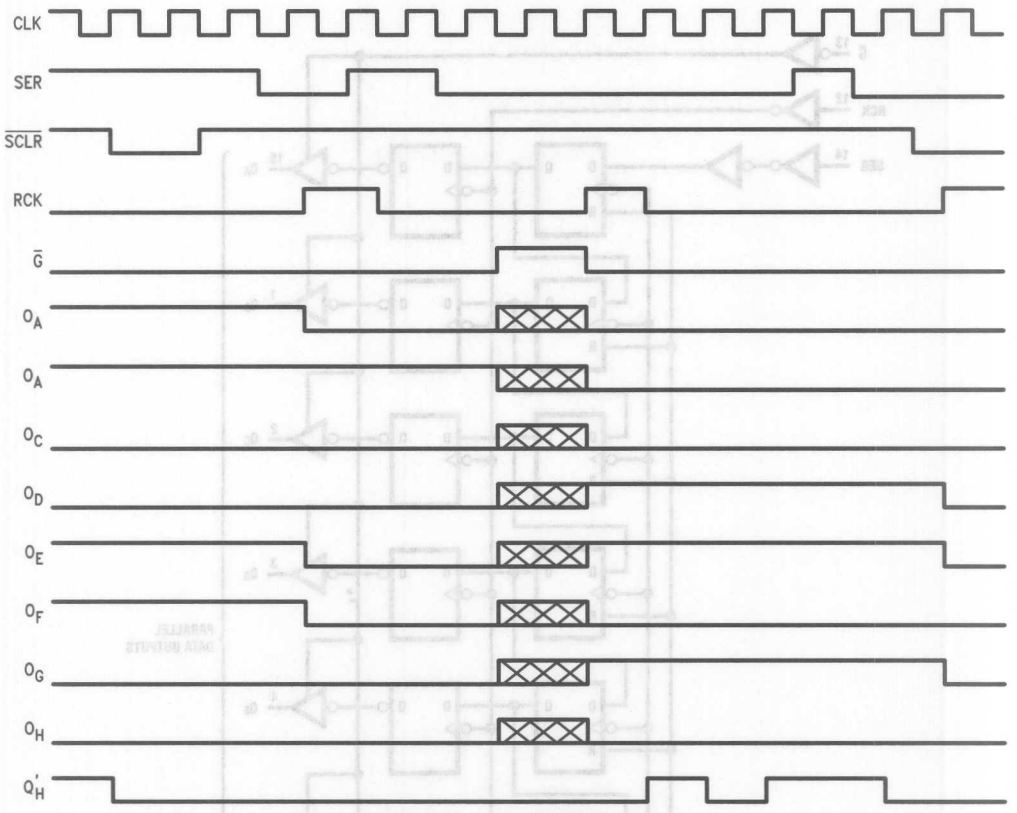
Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.


G
RCK
12
SER
14
SCK
11
SCLR
10
D
Q
R
15
Q_A
1
Q_B
2
Q_C
3
Q_D
4
Q_E
5
Q_F
6
Q_G
7
Q_H
9
Q'_H
PARALLEL DATA OUTPUTS
SERIAL DATA OUTPUT

TL/F/5342–3

Timing Diagram

MM54HC595/MM74HC595



NOTE: ⊠ Implies that the output is in TRI-STATE mode.

TL/F/5342–2

National Semiconductor

MM54HC597/MM74HC597
8-Bit Shift Registers with Input Latches

General Description

This high speed shift register utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The 'HC597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

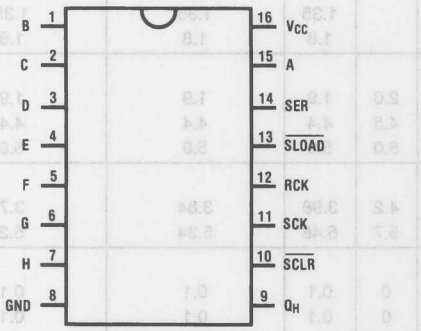
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5343–1

Top View

Order Number MM54HC597* or MM74HC597*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{SCLR}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked $Q_n = Q_{n-1}$, Q_0 = SER

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q_H		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SLOAD}$ to Q_H		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_H	$\overline{SLOAD}$ = logic'0'	25	45	ns
t_{PHL}	Maximum Propagation Delay from $\overline{SCLR}$ to Q_H		20	30	ns
t_{REM}	Minimum Removal Time, $\overline{SCLR}$ to SCK		10	20	ns
t_S	Minimum Setup Time from RCK to SCK		30	40	ns
t_S	Minimum Setup Time from SER to SCK		10	20	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$ $\overline{SLOAD}$		10	16	ns

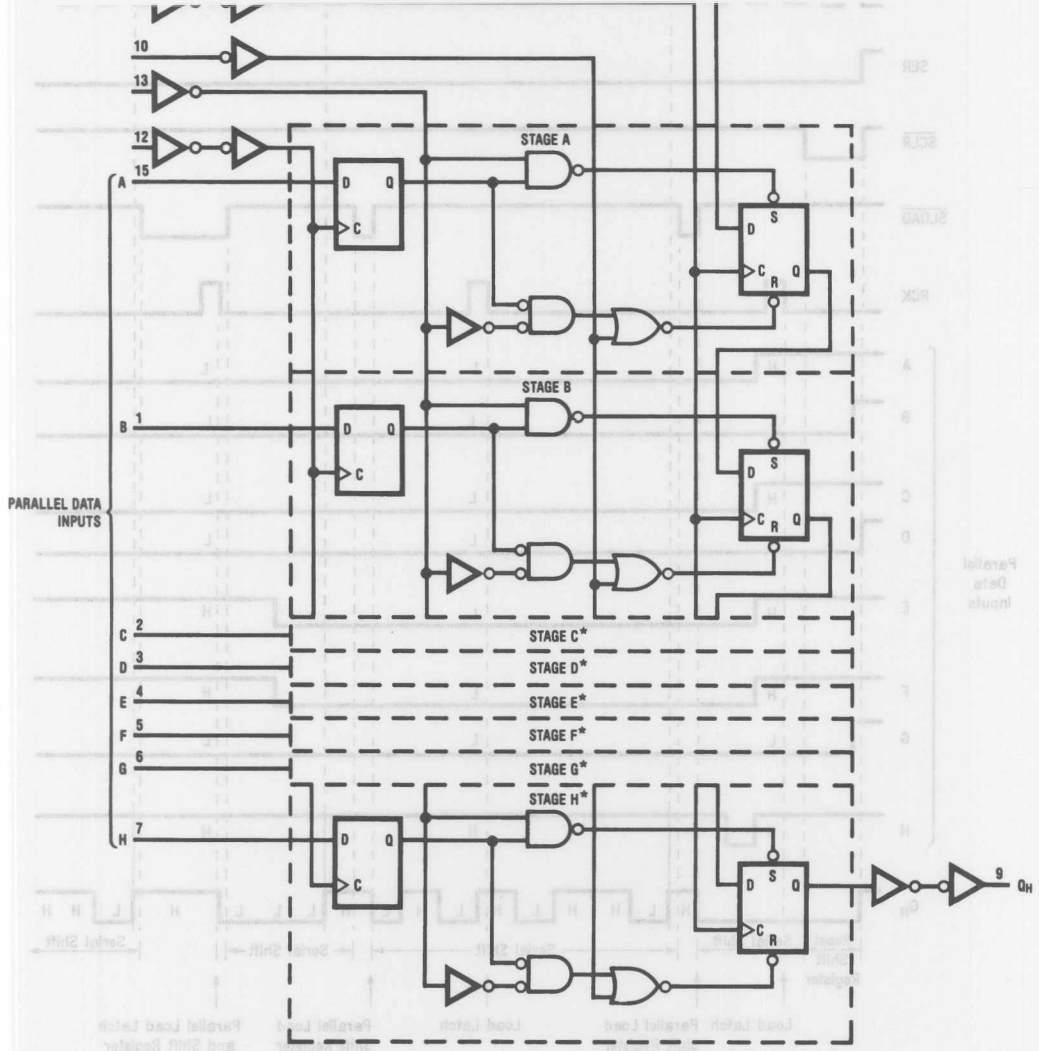
AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency for SCK		2.0V	10	6.0	4.8	4.0	MHz
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q_H		2.0V	62	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SLOAD}$ to Q_H		2.0V	65	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_H	$\overline{SLOAD}$ = Logic '0'	2.0V	120	205	255	310	ns
			4.5V	30	41	51	62	ns
			6.0V	28	35	43	53	ns
t_{PHL}	Maximum Propagation Delay from $\overline{SCLR}$ to Q_H		2.0V	66	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{REM}	Minimum Removal Time $\overline{SCLR}$ to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Setup Time from RCK to SCK		2.0V		200	250	300	ns
			4.5V		40	50	60	ns
			6.0V		34	42	50	ns
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns

AC Electrical Characteristics (Continued) $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_S	Minimum Setup Time from Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$, $\overline{SLOAD}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	8	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			87				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

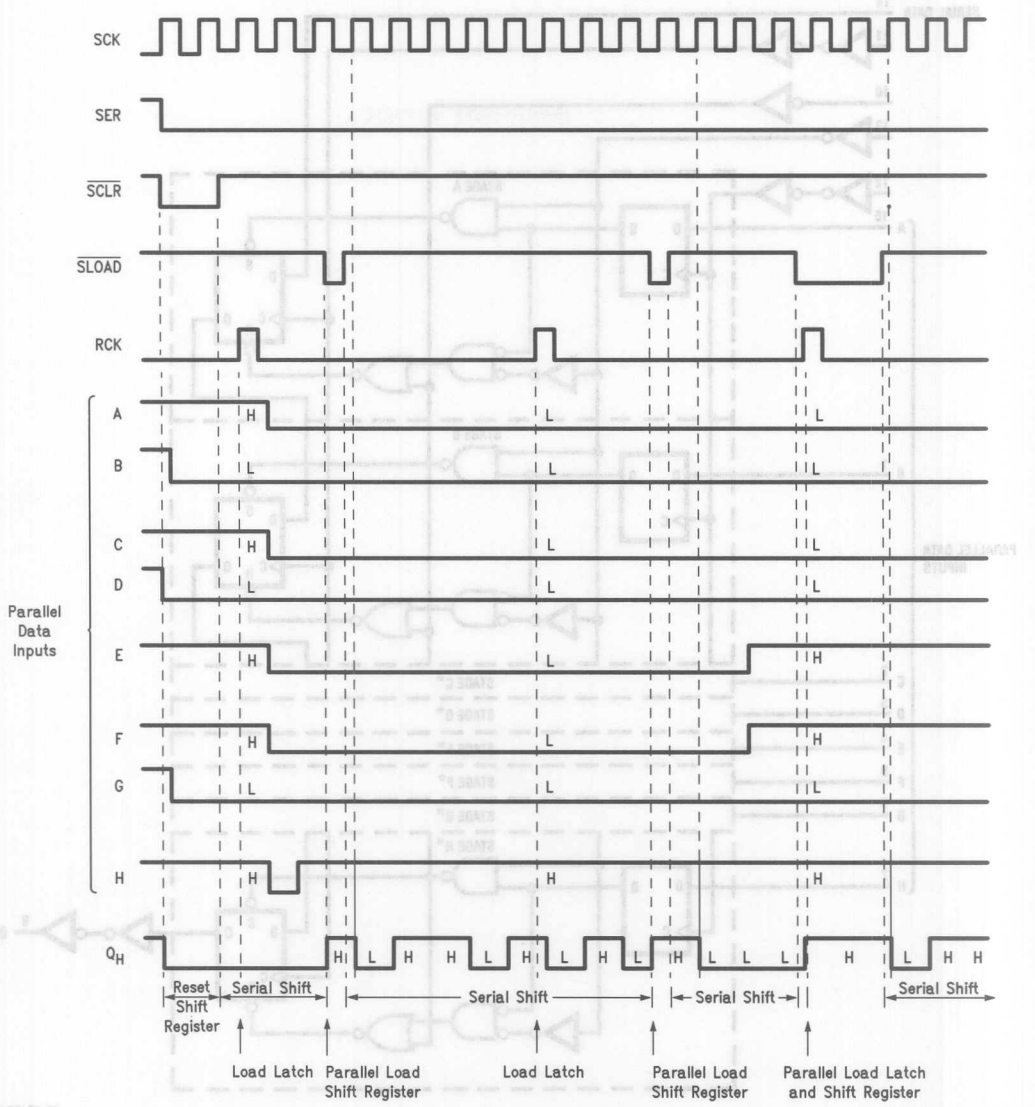
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.



TL/F/5343–3

* **NOTE:** Stages C thru G (not shown in detail) are identical to stages A and B above.

MM54HC597/MM74HC597 Timing Diagram



TL/F/5343–2

National Semiconductor

MM54HC620/MM74HC620 Inverting Octal TRI-STATE® Transceiver MM54HC623/MM74HC623 True Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize advanced silicon-gate CMOS technology and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. These devices allow data transmission from the A bus to the B bus or from the B bus to the A bus depending on the logic levels at the enable inputs. Both buses can be isolated from each other with proper logic levels at the enable inputs. When GAB is taken high and GBA is taken low, these devices store the states presently appearing at the data inputs. The 8-bit codes appearing on the two sets of buses will be indentical for the 623 option or complimentary for the 620 option.

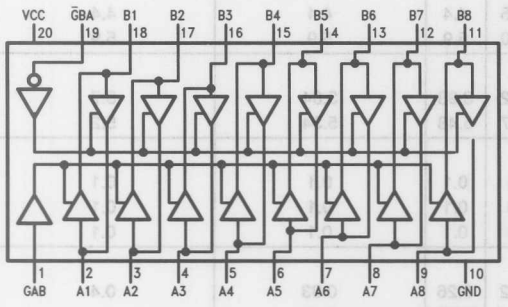
These devices can drive up to 15 LS-TTL loads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delays: 13 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum (74HC series)
- TRI-STATE outputs for connection to system buses
- High output drive: 6 mA (minimum)

Connection Diagrams

Dual-In-Line Package



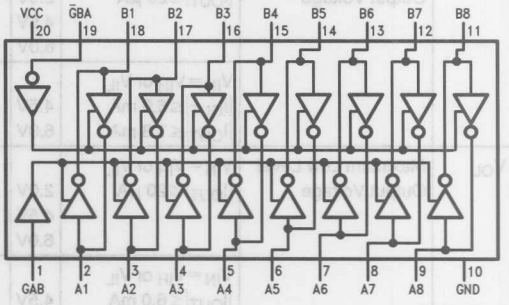
TL/F/9393–1

Top View

Order Number MM54HC623* or MM74HC623*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/9393–2

Top View

Order Number MM54HC620* or MM74HC620*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Enable Inputs		Operation	
$\overline{GBA}$	GAB		
L	L	$\overline{B}$ data to A bus	B data to A bus
H	H	$\overline{A}$ data to B bus	A data to B bus
H	L	Isolation	Isolation
L	L	$\overline{B}$ data to A bus, $\overline{A}$ data to B bus	B data to A bus, A data to B bus

3

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to +85°C	54HC T_A = −55°C to +125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF		15	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF		31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF		18	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to +85°C	54HC T_A = −55°C to +125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V		85	105	130	ns
		C_L = 150 pF	2.0V		105	130	160	ns
		C_L = 50 pF	4.5V		17	21	26	ns
		C_L = 150 pF	4.5V		21	26	32	ns
		C_L = 50 pF	6.0V		14	18	22	ns
		C_L = 150 pF	6.0V		18	22	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	R_L = 1 kΩ						
		C_L = 50 pF	2.0V		170	215	255	ns
		C_L = 150 pF	2.0V		195	245	295	ns
		C_L = 50 pF	4.5V		34	43	51	ns
		C_L = 150 pF	4.5V		39	49	59	ns
		C_L = 50 pF	6.0V		29	37	43	ns
		C_L = 150 pF	6.0V		33	42	50	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V		130	165	195	ns
			4.5V		26	33	39	ns
			6.0V		22	28	33	ns
t_{THL}, t_{TLH}	Output Rise and Fall Time	C_L = 50 pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}BA$, GAB = V_{IL}		120				pF
		$\overline{G}BA$ = V_{IH}, GAB = V_{IL}		12				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

National Semiconductor

MM54HC640/MM74HC640 Inverting Octal TRI-STATE® Transceiver MM54HC643/MM74HC643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize advanced silicon-gate CMOS technology, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

Each device has an active low enable $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC640/MM74HC640 transfers inverted data from one bus to other and the MM54HC643/MM74HC643 transfers inverted data from the A bus to the B bus and true data from the B bus to the A bus.

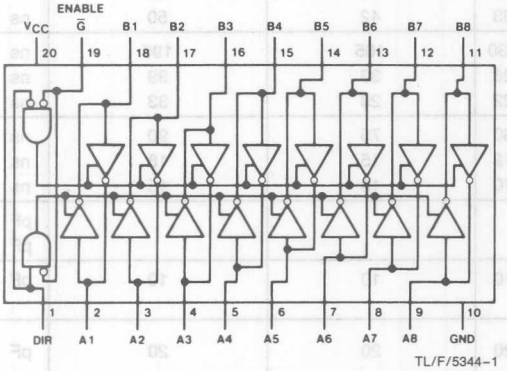
These devices can drive up to 15 LS-TTL Loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- TRI-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (min)

Connection Diagrams

Dual-In-Line Package



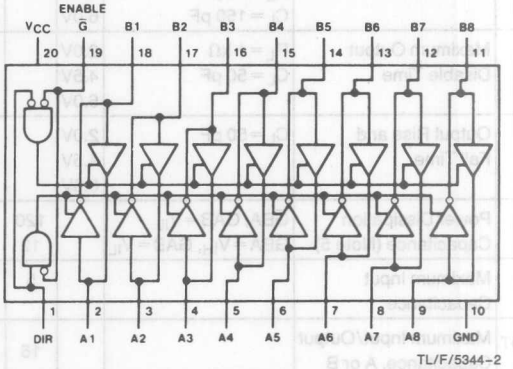
TL/F/5344–1

Top View

Order Number MM54HC640* or MM74HC640*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/5344–2

Top View

Order Number MM54HC643* or MM74HC643*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	32	42	ns

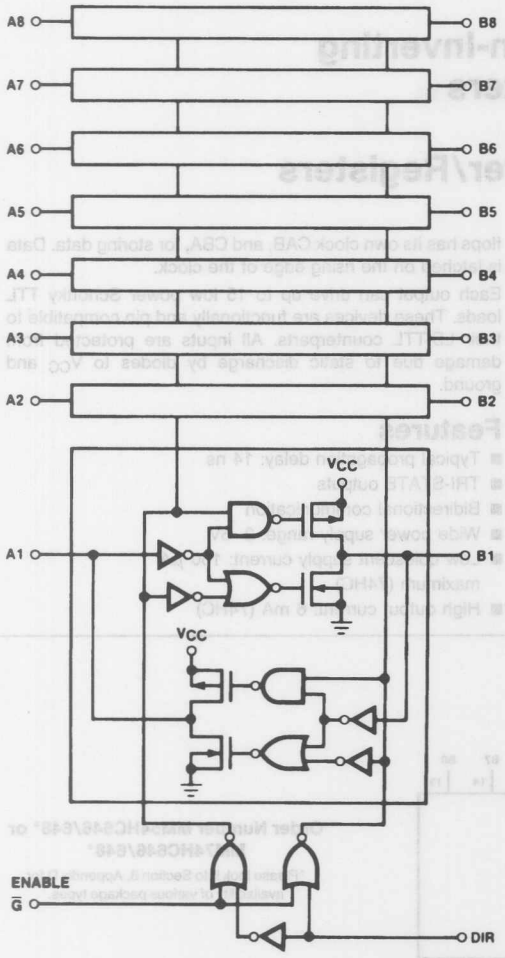
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	29	72	88	96	ns
		$C_L=150$ pF	2.0V	38	96	116	128	ns
		$C_L=50$ pF	4.5V	14	18	22	24	ns
		$C_L=150$ pF	4.5V	18	24	29	32	ns
		$C_L=50$ pF	6.0V	14	18	22	24	ns
		$C_L=150$ pF	6.0V	18	24	29	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	70	184	224	240	ns
		$C_L=150$ pF	2.0V	80	216	260	284	ns
		$C_L=50$ pF	4.5V	35	46	56	60	ns
		$C_L=150$ pF	4.5V	41	54	65	71	ns
		$C_L=50$ pF	6.0V	31	41	50	54	ns
		$C_L=150$ pF	6.0V	36	47	57	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	172	208	224	ns
			4.5V	33	43	52	56	ns
			6.0V	31	41	50	54	ns
t_{THL}, t_{TLH}	Output Rise and Fall Time	$C_L=50$ pF	2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}=V_{IL}$		120				pF
		$\overline{G}=V_{IH}$		12				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

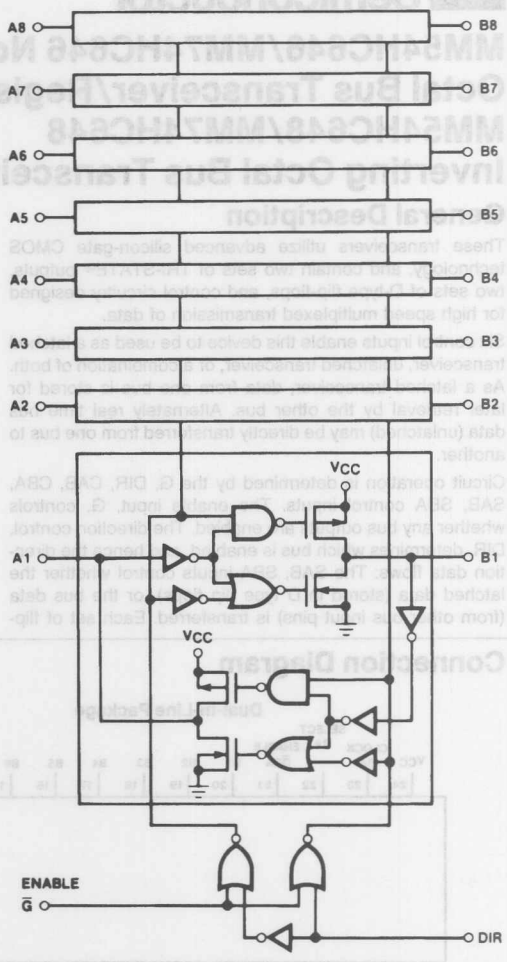
Logic Diagrams

'HC640



TL/F/5344–5

'HC643



TL/F/5344–6

National Semiconductor

MM54HC646/MM74HC646 Non-Inverting Octal Bus Transceiver/Registers
MM54HC648/MM74HC648 Inverting Octal Bus Transceiver/Registers

General Description

These transceivers utilize advanced silicon-gate CMOS technology, and contain two sets of TRI-STATE® outputs, two sets of D-type flip-flops, and control circuitry designed for high speed multiplexed transmission of data.

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver, or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the G, DIR, CAB, CBA, SAB, SBA control inputs. The enable input, G, controls whether any bus outputs are enabled. The direction control, DIR, determines which bus is enabled, and hence the direction data flows: The SAB, SBA inputs control whether the latched data (stored in D type flip flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock CAB, and CBA, for storing data. Data is latched on the rising edge of the clock.

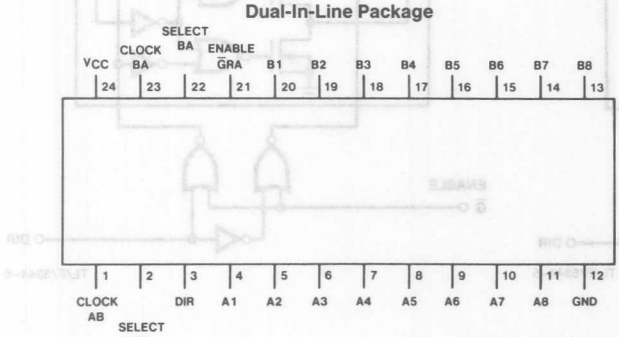
Each output can drive up to 15 low power Schottky TTL loads. These devices are functionally and pin compatible to their LS-TTL counterparts. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- TRI-STATE outputs
- Bidirectional communication
- Wide power supply range: 2–6V
- Low quiescent supply current: 160 μA maximum (74HC)
- High output current: 6 mA (74HC)

Connection Diagram

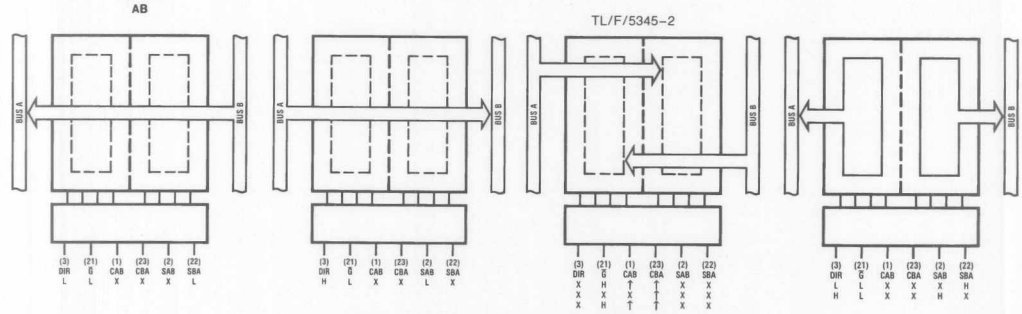
Dual-In-Line Package



Order Number MM54HC646/648* or MM74HC646/648*

*Please look into Section 8, Appendix D for availability of various package types.

TL/F/5345–2



TL/F/5345–1

Real-Time Transfer Bus B to Bus A | **Real-Time Transfer Bus A to Bus B** | **Storage from A, B, or A and B** | **Transfer Stored Data to A or B**

Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA $\lvert I_{OUT}\rvert \le 7.8$ mA	4.5V	4.2	3.96	3.84	3.7	V
			6.0V	5.7	5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA $\lvert I_{OUT}\rvert \le 7.8$ mA	4.5V	0.2	0.26	0.33	0.4	V
			6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Truth Table

Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data Isolation, hold storage	Store A and B Data Isolation, hold storage
H	X	H or L	H or L	X	X				

Truth Table (Continued)

Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = High Level L = Low Level X = Irrelevant ↑ = low-to-high level transition

The data output functions i.e., data at the bus pins may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled.

The data output functions i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

AC Electrical Characteristics MM54HC646/MM74HC646, MM54HC648/MM74HC648

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=45$ pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=45$ pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=45$ pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=45$ pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=5$ pF	17	30	ns

AC Electrical Characteristics MM54HC646/MM74HC646, MM54HC648/MM74HC648

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	2.0V	60	180	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	31	39	ns
		$C_L=150$ pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	2.0V	110	220	275	330	ns
		$C_L=150$ pF	2.0V	150	270	338	405	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	40	54	68	81	ns
		$C_L=50$ pF	6.0V	28	38	47	57	ns
		$C_L=150$ pF	6.0V	34	47	59	71	ns

AC Electrical Characteristics MM54HC646/MM74HC646, MM54HC648/MM74HC648 (Continued)

$V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

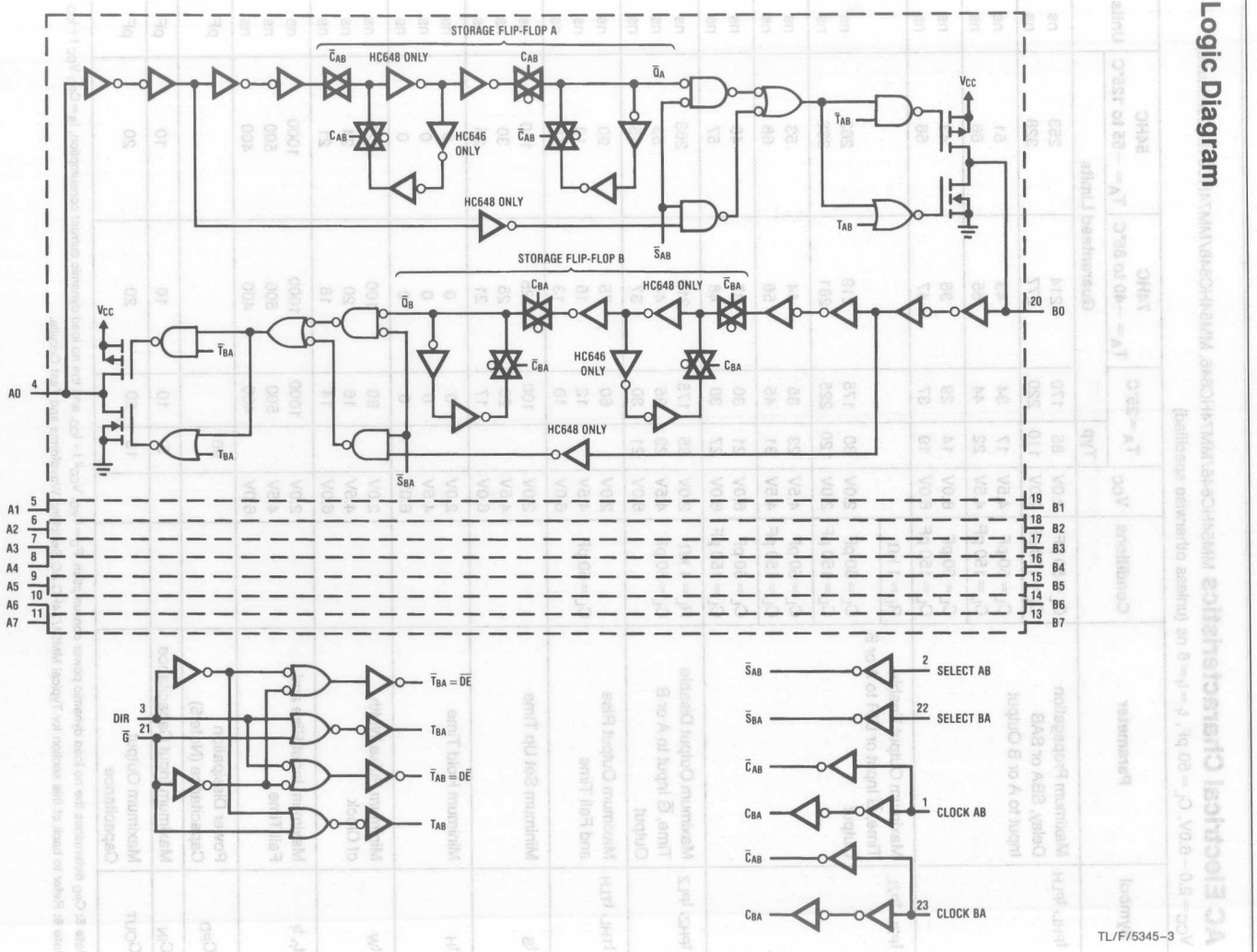
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output	$C_L=50$ pF	2.0V	85	170	214	253	ns
		$C_L=150$ pF	2.0V	110	220	277	328	ns
		$C_L=50$ pF	4.5V	17	34	43	51	ns
		$C_L=150$ pF	4.5V	22	44	55	66	ns
		$C_L=50$ pF	6.0V	14	29	36	43	ns
		$C_L=150$ pF	6.0V	19	37	47	56	ns
t_{PZL}, t_{PZL}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	80	175	219	263	ns
		$C_L=150$ pF	2.0V	120	225	281	338	ns
		$C_L=50$ pF	4.5V	23	35	44	53	ns
		$C_L=150$ pF	4.5V	31	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	$R_L=1$ kΩ, $C_L=50$ pF	2.0V	85	175	219	263	ns
			4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}$, V_{CC}^2 f + I_{CC}, and the no load dynamic current consumption, $I_S=C_{PD}$ V_{CC} f + I_{CC}.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

3

Logic Diagram



National Semiconductor

MM54HC688/MM74HC688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

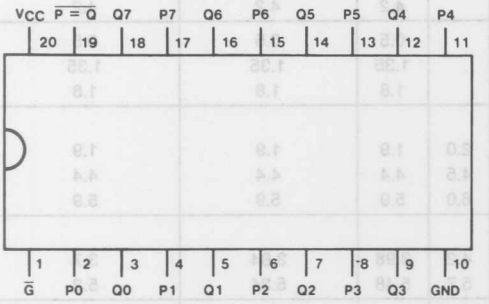
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 Series)
- Large output current: 4 mA (74 Series)
- Same as 'HC521

Connection and Logic Diagrams

Dual-In-Line Package

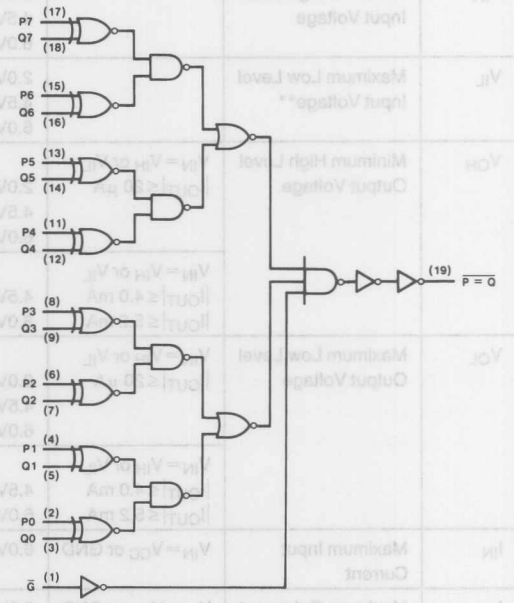


TL/F/5018–1

Top View

Order Number MM54HC688* or MM74HC688*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5018–2

Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

3

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

				Limit	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any P or Q to Output		21	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		14	20	ns

AC Electrical Characteristics

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, P or Q to Output		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Output		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HC4002/MM74HC4002 Dual 4-Input NOR Gate

General Description

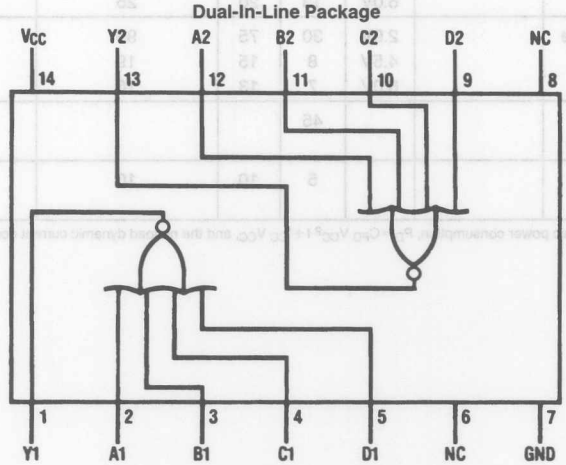
These NOR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4002/74HC4002 is functionally equivalent and pin-out compatible with the CD4002B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5154–1

$Y = \overline{A + B + C + D}$

Order Number MM54HC4002* or MM74HC4002*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}						V
		$\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	40	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

MM54HC4016/MM74HC4016 Quad Analog Switch

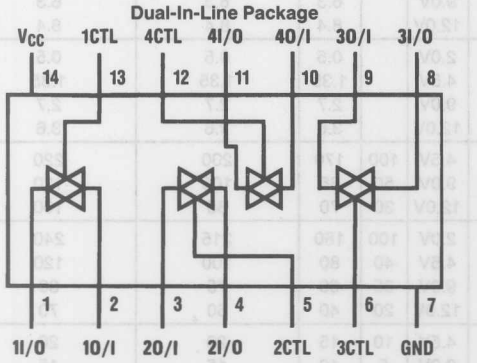
General Description

These devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. The '4016 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 50Ω typ.
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram



Top View

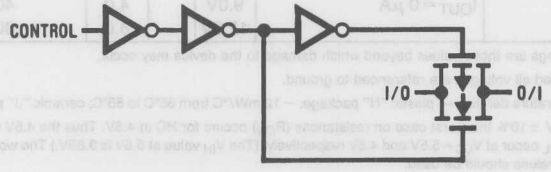
Order Number MM54HC4016* or MM74HC4016*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Input	Switch
CTL	I/O-O/I
L	"OFF"
H	"ON"

Schematic Diagram



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Switch I/O Voltage (V_{IO})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	6.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			9.0V		2.7	2.7	2.7	V
			12.0V		3.6	3.6	3.6	V
R_{ON}	Maximum 'ON' Resistance (See Note 5)	V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	120	Ω
			12.0V	30	70	85	100	Ω
		V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} or GND (Figure 1)	2.0V	100	180	215	240	Ω
			4.5V	40	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum 'ON' Resistance Matching	V_{CTL} = V_{IH} V_{IS} = V_{CC} to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch 'OFF' Leakage Current	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{CTL} = V_{IL} (Figure 2)	6.0V		±60	±600	±600	nA
			9.0V		±80	±800	±800	nA
			12.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch 'ON' Leakage Current	V_{IS} = V_{CC} to GND V_{CTL} = V_{IH}, V_{OH} = OPEN (Figure 3)	6.0V		±40	±150	±150	nA
			9.0V		±50	±200	±200	nA
			12.0V		±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA
			9.0V		4.0	40	80	μA
			12.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so these values should be used.

Note 5: At supply voltages (V_{CC}–GND) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

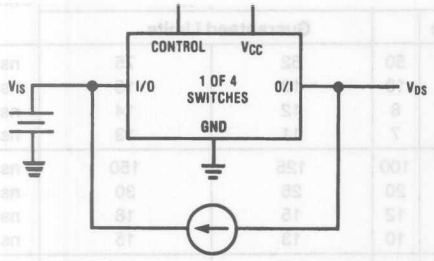
AC Electrical Characteristics V_{CC} = 2.0V–12.0V, C_L = 50 pF (unless otherwise specified), (Notes 6 and 7)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50	62	75	ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	12	14	ns
			12.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	$R_L = 1\ k\Omega$	2.0V	32	100	125	150	ns
			4.5V	8	20	25	30	ns
			9.0V	6	12	15	18	ns
			12.0V	5	10	13	15	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	$R_L = 1\ k\Omega$	2.0V	45	168	210	252	ns
			4.5V	15	36	45	54	ns
			9.0V	10	32	40	48	ns
			12.0V	8	30	38	45	ns
	Minimum Frequency Response (Figure 7) 20 log (V_{OS}/V_{IS}) = −3 dB	$R_L = 600\Omega$, $V_{IS} = 2V_{PP}$ at ($V_{CC}/2$) (Notes 6 & 7)	4.5V	40				MHz
			9.0V	100				MHz
	Control to Switch Feedthrough Noise (Figure 8)	$R_L = 600\Omega$, F = 1 MHz C_L = 50 pF (Notes 7 & 8)	4.5V	100				mV
			9.0V	250				mV
	Crosstalk Between any Two Switches (Figure 9)	$R_L = 600\Omega$, F = 1 MHz	4.5V	−52				dB
			9.0V	−50				dB
	Switch OFF Signal Feedthrough Isolation (Figure 10)	$R_L = 600\Omega$, F = 1 MHz $V_{CTL} = V_{IL}$ (Notes 7 & 8)	4.5V	−42				dB
			9.0V	−44				dB
THD	Sinewave Harmonic Distortion (Figure 11)	$R_L = 10\ k\Omega$, C_L = 50 pF, F = 1 kHz $V_{IS} = 4V_{PP}$	4.5V	0.013				%
		$V_{IS} = 8V_{PP}$	9.0V	0.008				%
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		5				pF
C_{PD}	Power Dissipation Capacitance	(per switch)		15				pF

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/R_{ON} Attenuation)

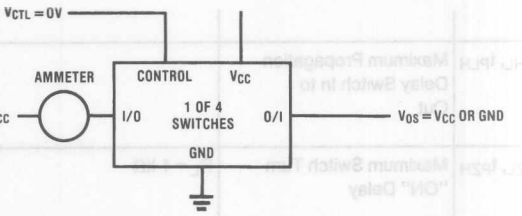
Note 7: V_{IS} is centered at $V_{CC}/2$

Note 8: Adjust input for 0 dBm



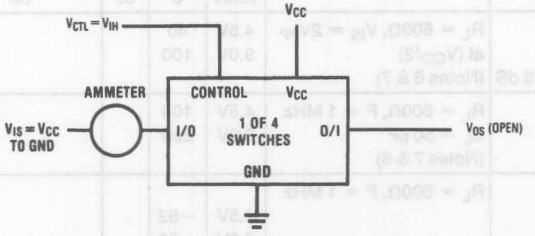
TL/F/5350–3

FIGURE 1. "ON" Resistance



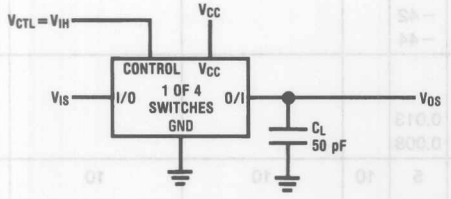
TL/F/5350–4

FIGURE 2. "OFF" Channel Leakage Current

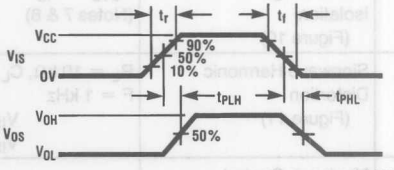


TL/F/5350–5

FIGURE 3. "ON" Channel Leakage Current

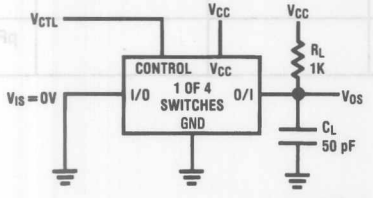


TL/F/5350–6

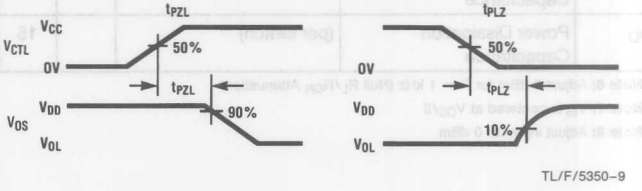


TL/F/5350–7

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



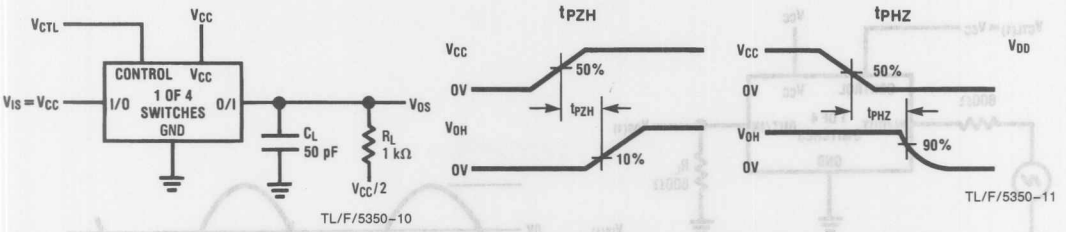
TL/F/5350–8



TL/F/5350–9

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

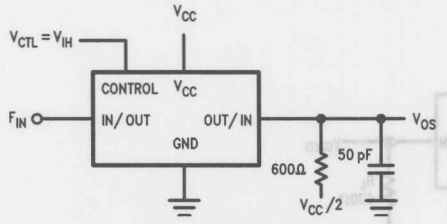
AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5350–10

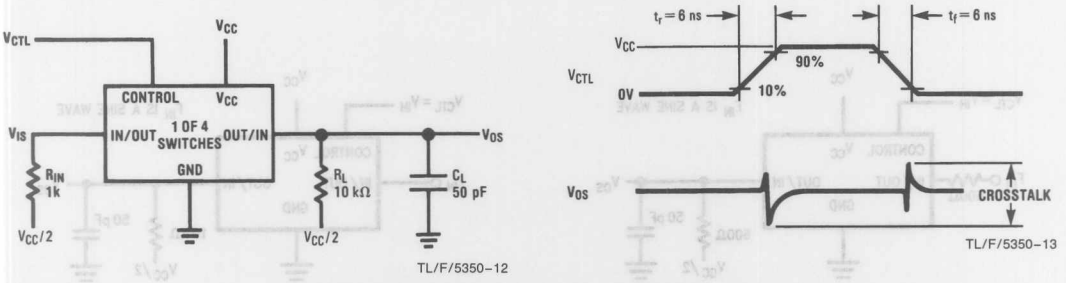
TL/F/5350–11

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5350–20

FIGURE 7. Frequency Response



TL/F/5350–12

TL/F/5350–13

FIGURE 8. Crosstalk: Control Input to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

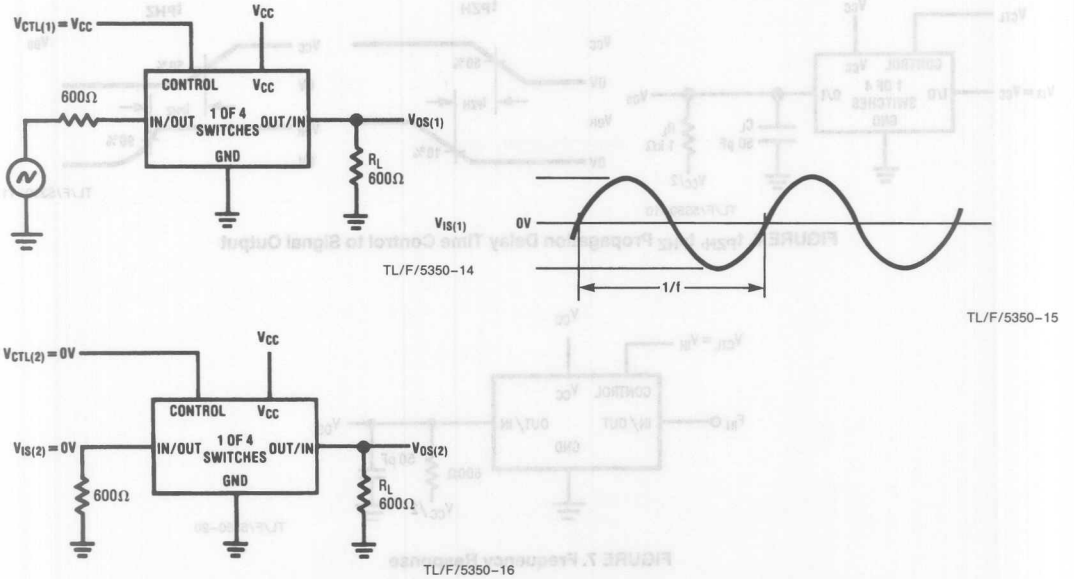


FIGURE 9. Crosstalk Between Any Two Switches

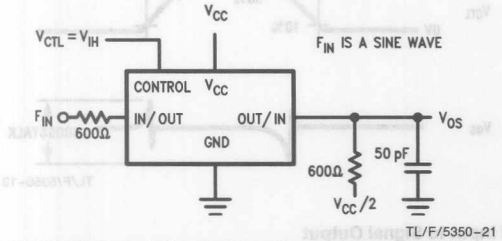


FIGURE 10. Switch OFF Signal Feedthrough Isolation

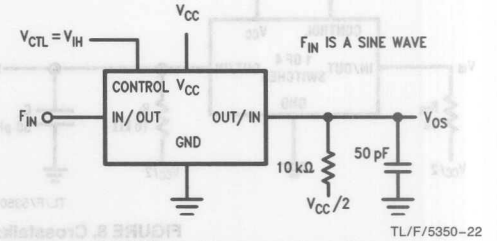
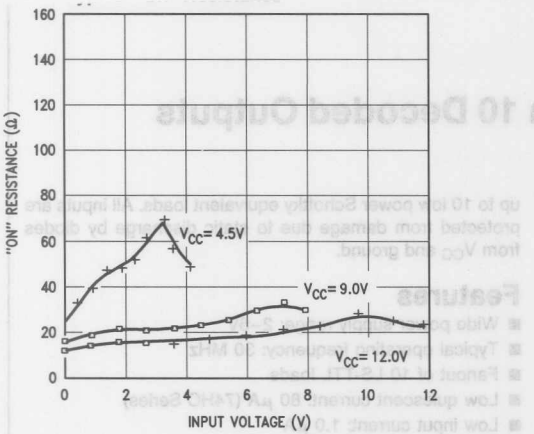
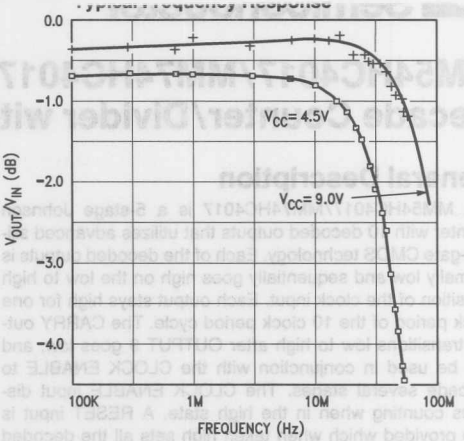


FIGURE 11. Sinewave Distortion

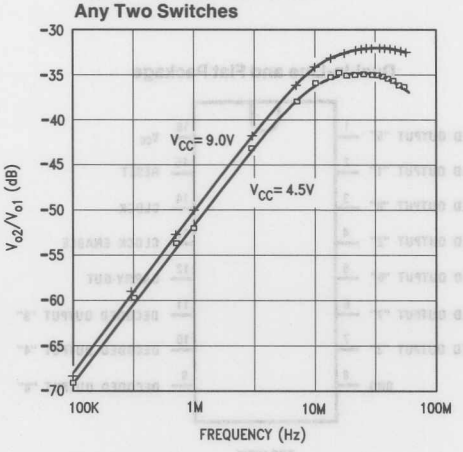


TL/F/5350–19



TL/F/5350–23

Typical Crosstalk Between Any Two Switches



TL/F/5350–24

Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

3

National Semiconductor

MM54HC4017/MM74HC4017
Decade Counter/Divider with 10 Decoded Outputs

General Description

The MM54HC4017/MM74HC4017 is a 5-stage Johnson counter with 10 decoded outputs that utilizes advanced silicon-gate CMOS technology. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output transitions low to high after OUTPUT 9 goes low, and can be used in conjunction with the CLOCK ENABLE to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET input is also provided which when taken high sets all the decoded outputs low except output 0.

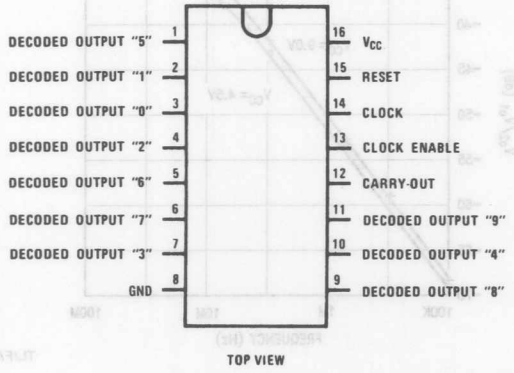
The MM54HC4017/MM74HC4017 is functionally and pinout equivalent to the CD4017BM/CD4017BC. It can drive up to 10 low power Schottky equivalent loads. All inputs are protected from damage due to static discharge by diodes from V_{CC} and ground.

Features

- Wide power supply range: 2–6V
- Typical operating frequency: 30 MHz
- Fanout of 10 LS-TTL loads
- Low quiescent current: 80 μA (74HC Series)
- Low input current: 1.0 μA

Connection Diagram

Dual-In-Line and Flat Package



TL/F/5351–1

Order Number MM54HC4017* or MM74HC4017*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		26	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable Decode-Out Lines		27	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		23	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		23	40	ns
t_S	Minimum Clock Inhibit to Clock Set-Up Time		12	20	ns
t_W	Minimum Clock or Reset Pulse Width		8	16	ns
t_{REM}	Minimum Reset Removal Time		20	10	ns

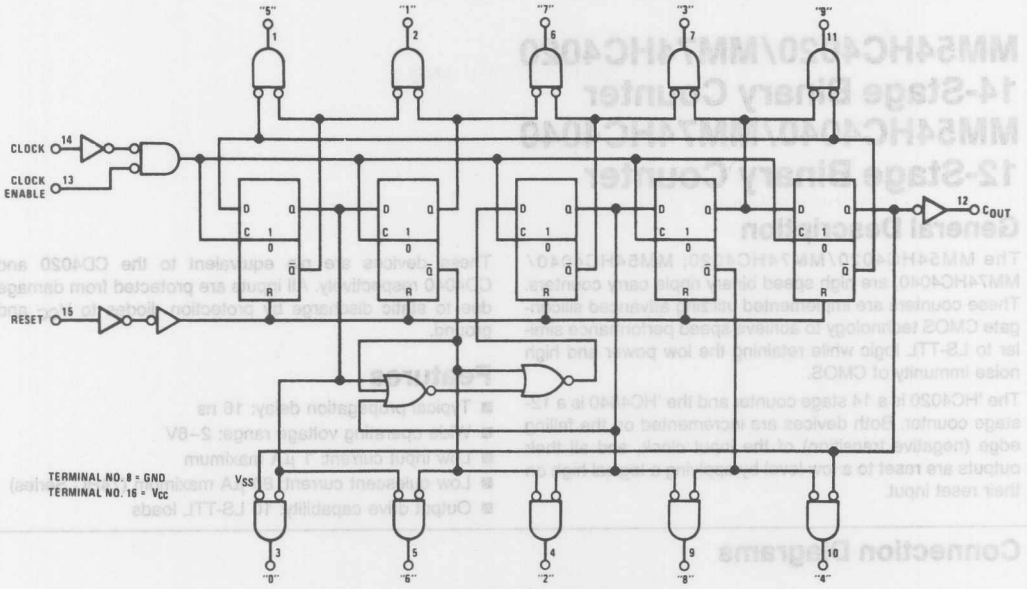
AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	2.0V	6	5	4	MHz
			4.5V	30	24	20	MHz
			6.0V	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		2.0V	89	250	312	375	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Decode Out Line		2.0V	90	250	312	375	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		2.0V	82	230	288	345	ns
			4.5V	22	46	58	69	ns
			6.0V	18	39	49	59	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		2.0V	82	230	288	345	ns
			4.5V	22	46	58	69	ns
			6.0V	18	39	49	59	ns
t_W	Minimum Reset, Clock, or Clock Enable Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	21	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S, t_H	Minimum Clock Inhibit to Clock Set-Up or Hold Time		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Minimum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

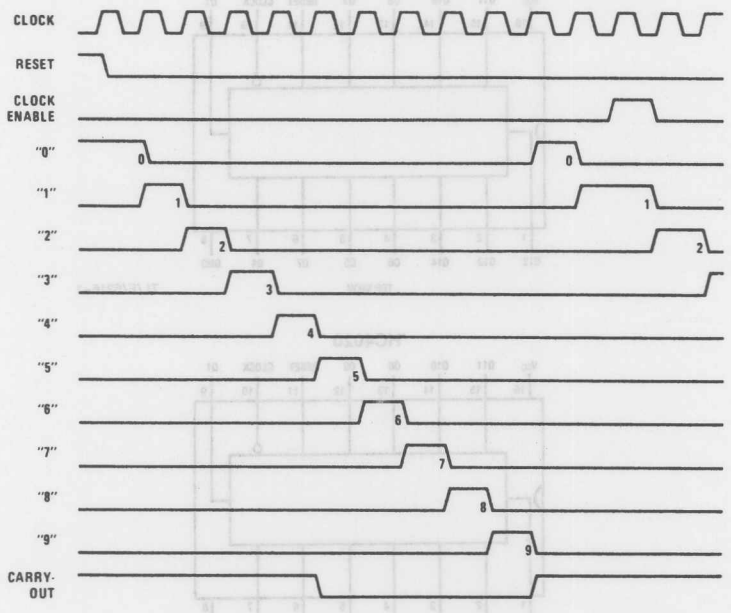
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic and Timing Diagrams

MM54HC4017/MM74HC4017



TL/F/5351–2



TL/F/5351–3

National Semiconductor

MM54HC4020/MM74HC4020 14-Stage Binary Counter MM54HC4040/MM74HC4040 12-Stage Binary Counter

General Description

The MM54HC4020/MM74HC4020, MM54HC4040/MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4020 is a 14 stage counter and the 'HC4040 is a 12-stage counter. Both devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

These devices are pin equivalent to the CD4020 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

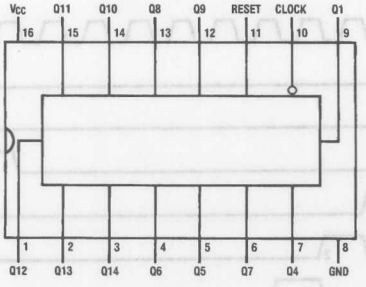
Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagrams

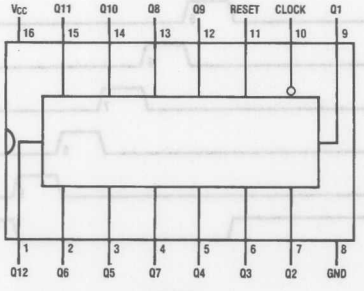
Dual-In-Line Packages

'HC4040



TOP VIEW TL/F/5216–1

'HC4020



TOP VIEW TL/F/5216–3

Order Number MM54HC4020/4040* or MM74HC4020/4040*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	(Note 5)	17	35	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

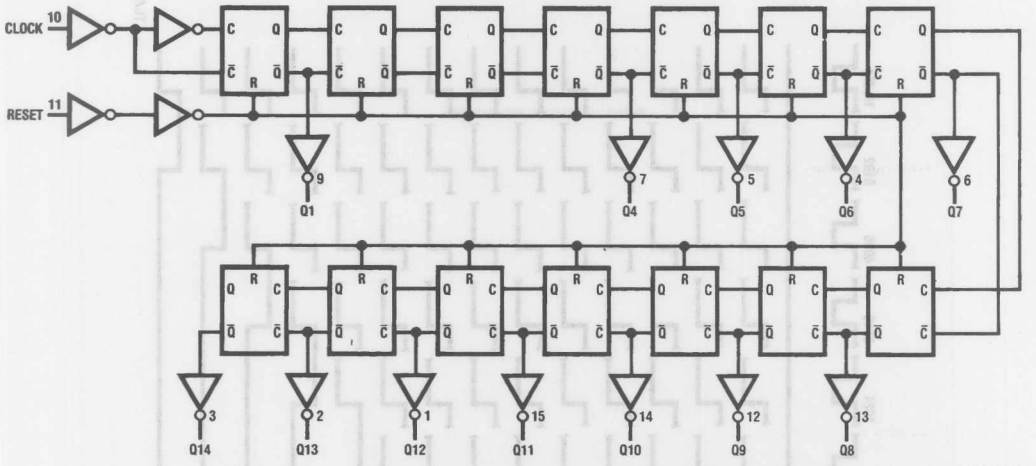
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	40	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_1		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
T_{PHL}, t_{PLH}	Maximum Propagation Delay Between Stages from Q_n to Q_{n+1}		2.0V	80	125	156	188	ns
			4.5V	18	25	31	38	ns
			6.0V	15	21	26	31	ns
t_{PHL}	Maximum Propagation Delay Reset to Q ('4024 only)		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q ('4020 and '4040)		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	126	149	ns
			4.5V		20	25	50	ns
			6.0V		16	21	25	ns
t_W	Minimum Pulse Width		2.0V		90	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: Typical Propagation delay time to any output can be calculated using: $t_P=17+12(N-1)$ ns; where N is the number of the output, Q_W, at $V_{CC}=5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

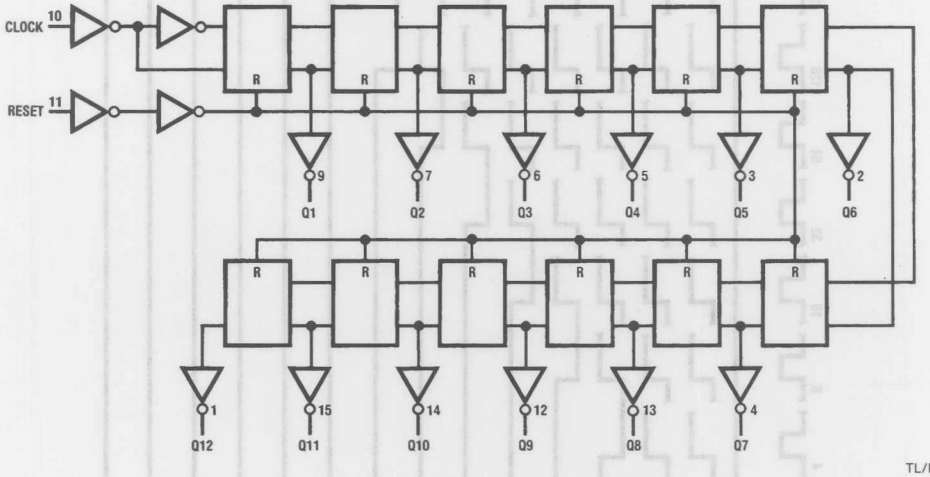
Logic Diagrams

MM54HC4020/MM74HC4020



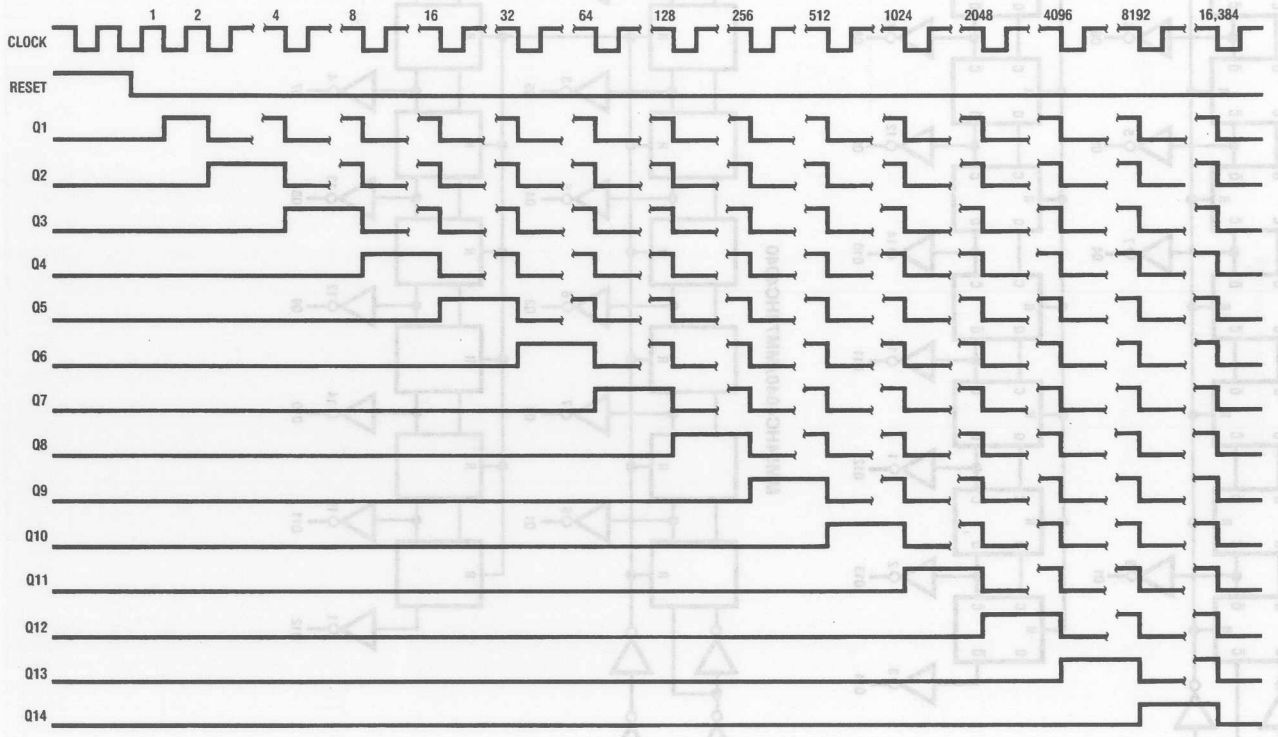
TL/F/5216–5

MM54HC4040/MM74HC4040



TL/F/5216–7

Timing Diagram



TL/F/5216–11

National Semiconductor

MM54HC4046/MM74HC4046 CMOS Phase Lock Loop

General Description

The MM54HC4046/MM74HC4046 is a low power phase lock loop utilizing advanced silicon-gate CMOS technology to obtain high frequency operation both in the phase comparator and VCO sections. This device contains a low power linear voltage controlled oscillator (VCO), a source follower, and three phase comparators. The three phase comparators have a common signal input and a common comparator input. The signal input has a self biasing amplifier allowing signals to be either capacitively coupled to the phase comparators with a small signal or directly coupled with standard input logic levels. This device is similar to the CD4046 except that the Zener diode of the metal gate CMOS device has been replaced with a third phase comparator.

Phase Comparator I is an exclusive OR (XOR) gate. It provides a digital error signal that maintains a 90 phase shift between the VCO's center frequency and the input signal (50% duty cycle input waveforms). This phase detector is more susceptible to locking onto harmonics of the input frequency than phase comparator I, but provides better noise rejection.

Phase comparator III is an SR flip-flop gate. It can be used to provide the phase comparator functions and is similar to the first comparator in performance.

Phase comparator II is an edge sensitive digital sequential network. Two signal outputs are provided, a comparator output and a phase pulse output. The comparator output is a TRI-STATE® output that provides a signal that locks the VCO output signal to the input signal with 0 phase shift between them. This comparator is more susceptible to noise throwing the loop out of lock, but is less likely to lock onto harmonics than the other two comparators.

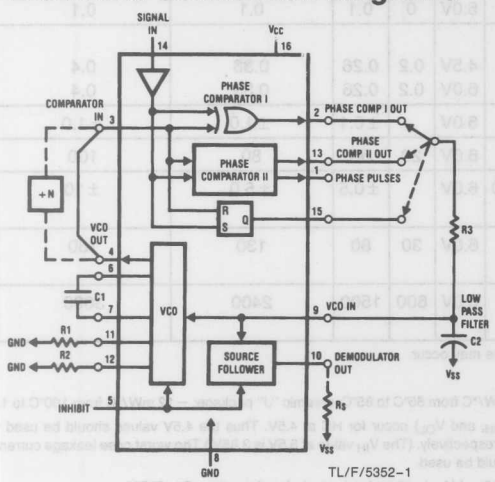
In a typical application any one of the three comparators feed an external filter network which in turn feeds the VCO input. This input is a very high impedance CMOS input which also drives the source follower. The VCO's operating frequency is set by three external components connected to the C1A, C1B, R1 and R2 pins. An inhibit pin is provided to disable the VCO and the source follower, providing a method of putting the IC in a low power state.

The source follower is a MOS transistor whose gate is connected to the VCO input and whose drain connects the Demodulator output. This output normally is used by tying a resistor from pin 10 to ground, and provides a means of looking at the VCO input without loading down modifying the characteristics of the PLL filter.

Features

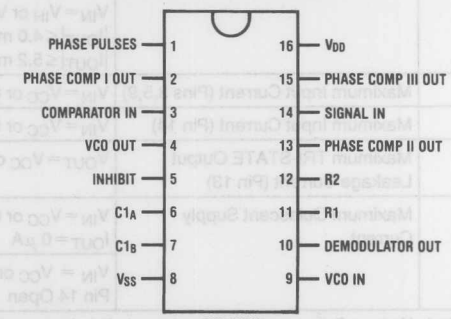
- Low dynamic power consumption (V_{CC} = 4.5V)
- Maximum VCO operating frequency: 12 MHz (V_{CC} = 4.5V)
- Fast comparator response time (V_{CC} = 4.5V)
  - Comparator I: 25 ns
  - Comparator II: 30 ns
  - Comparator III: 25 ns
- VCO has high linearity and high temperature stability

Block and Connection Diagrams



TL/F/5352–1

Dual-In-Line Package



TOP VIEW

TL/F/5352–2

Order Number MM54HC4046* or MM74HC4046*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to + 7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 3,5,9)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IN}	Maximum Input Current (Pin 14)	V_{IN} = V_{CC} or GND	6.0V	20	50	80	100	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current (Pin 13)	V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V	30	80	130	160	μA
		V_{IN} = V_{CC} or GND Pin 14 Open	6.0V	600	1500	2400	3000	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

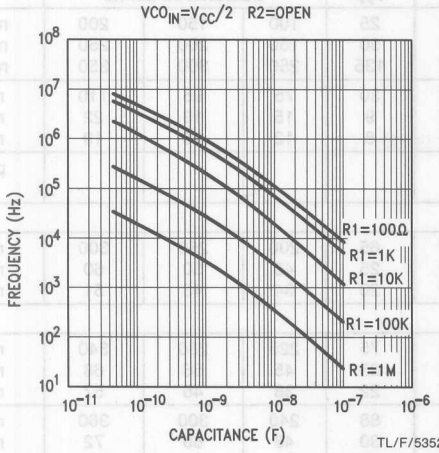
AC Electrical Characteristics V_{CC} = 2.0 to 6.0V, CL = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified.)

Symbol	Parameters	Conditions	V_{CC}	T = 25C	74HC	54HC	Units
				Typ	Guaranteed Limits		
	AC Coupled Input Sensitivity, Signal In	C (series) = 100 pF f_{IN} = 500 kHz	2.0V 4.5V 6.0V	25 50 135	100 150 250	150 200 300	200 250 350	mV mV mV
t_r, t_f	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 9 8	75 15 12	95 19 15	110 22 19	ns ns ns
C_{IN}	Maximum Input Capacitance		7					pF
Phase Comparator I								
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	65 25 20	200 40 34	250 50 43	300 60 51	ns ns ns
Phase Comparator II								
t_{PZL}	Maximum TRI-STATE Enable Time		2.0V 4.5V 6.0V	75 25 22	225 45 38	280 56 48	340 68 57	ns ns ns
t_{PZH}, t_{PHZ}	Maximum TRI-STATE Enable Time		2.0V 4.5V 6.0V	88 30 25	240 48 41	300 60 51	360 72 61	ns ns ns
t_{PLZ}	Maximum TRI-STATE Disable Time		2.0V 4.5V 6.0V	90 32 28	240 48 41	300 60 51	360 72 61	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay High to Low to Phase Pulses		2.0V 4.5V 6.0V	100 34 27	250 50 43	310 63 53	380 75 64	ns ns ns
Phase Comparator III								
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	75 25 22	200 40 34	250 50 43	300 60 51	ns ns ns
C_{PD}	Maximum Power Dissipation Capacitance	All Comparators $V_{IN} = V_{CC}$ and GND		130				pF
Voltage Controlled Oscillator (Specified to operate from V_{CC} = 3.0V to 6.0V)								
f_{MAX}	Maximum Operating Frequency	C1 = 50 pF R1 = 100Ω R2 = ∞ $VCO_{in} = V_{CC}$	4.5V 6.0V	7 11	4.5 7			MHz MHz
		C1 = 0 pF R1 = 100Ω $VCO_{in} = V_{CC}$	4.5V 6.0	12 14				MHz MHz
	Duty Cycle			50				%
Demodulator Output								
	Offset Voltage $VCO_{in}-V_{dem}$	R_s = 20 kΩ	4.5V	0.75	1.3	1.5	1.6	V
	Offset Variation	R_s = 20 kΩ VCO_{in} = 1.75V 2.25V 2.75V	4.5V	 0.65 0.1 0.75				V

Typical Performance Characteristics

Typical Center Frequency vs R1, C1 V_{CC} = 4.5V

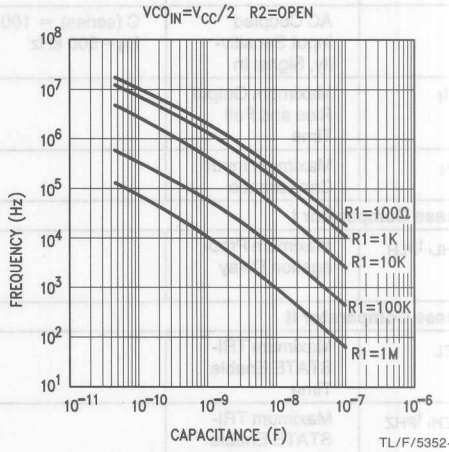
$VCO_{IN}=V_{CC}/2$ R2=OPEN



TL/F/5352–15

Typical Center Frequency vs R1, C1 V_{CC} = 6V

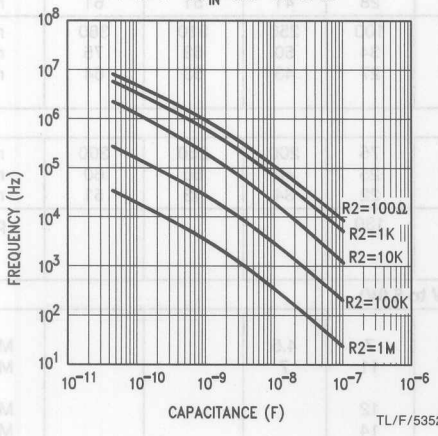
$VCO_{IN}=V_{CC}/2$ R2=OPEN



TL/F/5352–16

Typical Offset Frequency vs R2, C1 V_{CC} = 4.5V

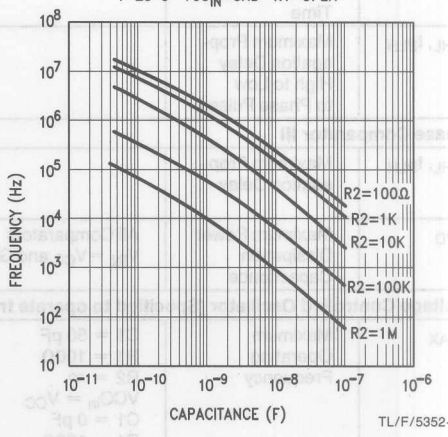
T=25°C VCO_{IN}=GND R1=OPEN



TL/F/5352–17

Typical Offset Frequency vs R2, C1 V_{CC} = 6V

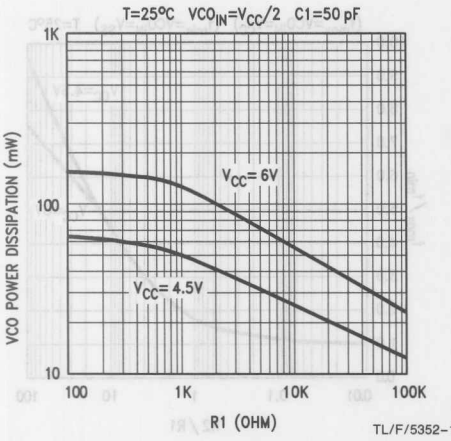
T=25°C VCO_{IN}=GND R1=OPEN



TL/F/5352–18

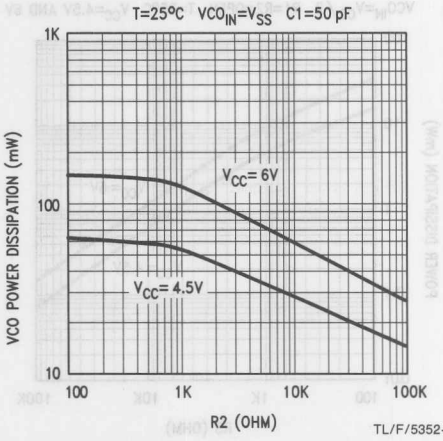
Typical Performance Characteristics (Continued)

HC4046 Typical VCO Power Dissipation @ Center Frequency vs R1



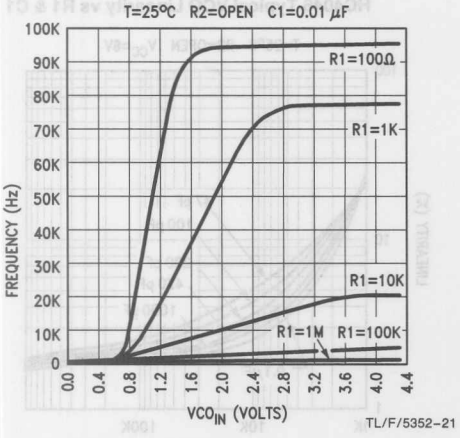
TL/F/5352-19

HC4046 Typical VCO Power Dissipation @ f_{min} vs R2



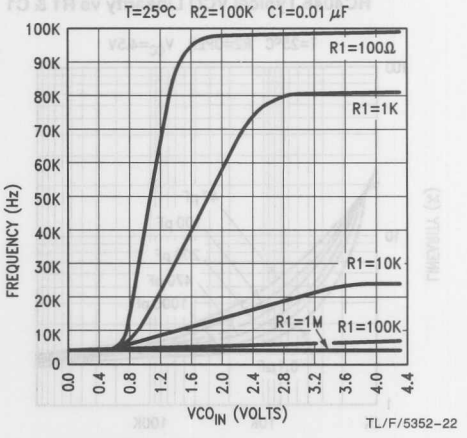
TL/F/5352-20

HC4046 VCO_{in} vs f_{out} V_{CC} = 4.5V



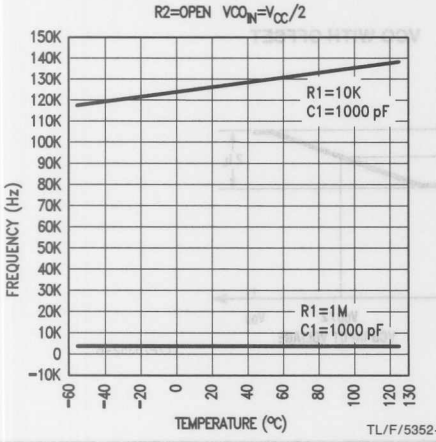
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HC4046 VCO_{in} vs f_{out} V_{CC} = 4.5V



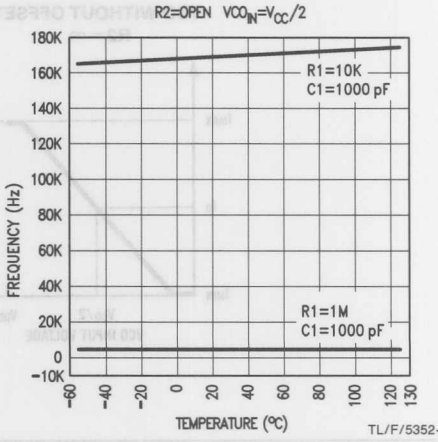
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HC4046 VCO_{out} vs Temperature V_{CC} = 4.5V

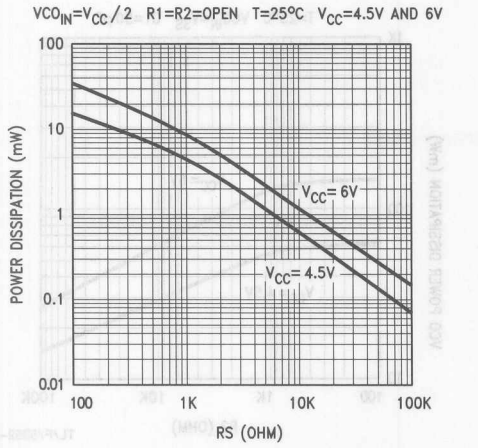


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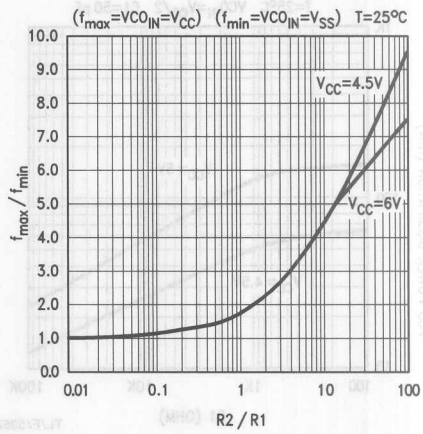
HC4046 VCO_{out} vs Temperature V_{CC} = 6V



TL/F/5352-24

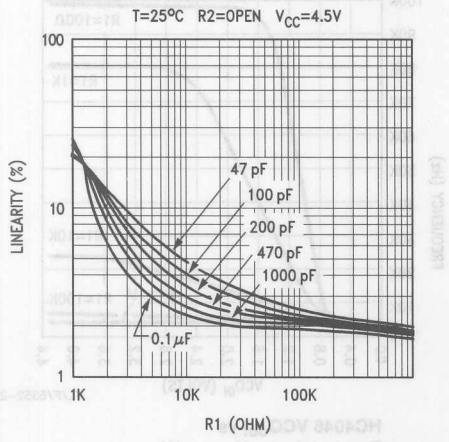


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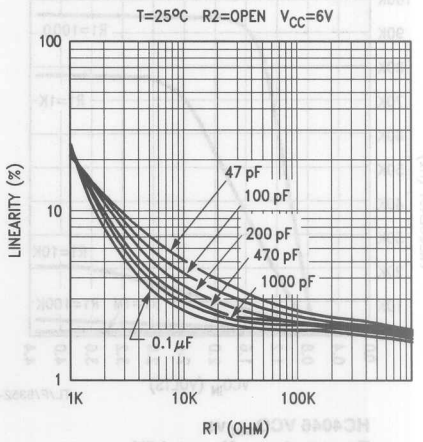
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HC4046 Typical VCO Linearity vs R1 & C1



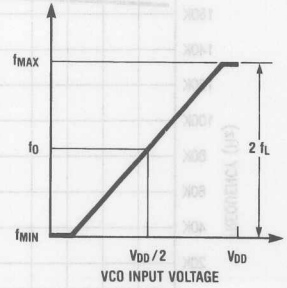
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HC4046 Typical VCO Linearity vs R1 & C1

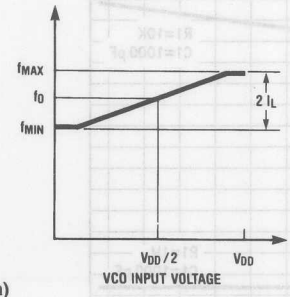


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VCO WITHOUT OFFSET
R2 = ∞



VCO WITH OFFSET



(a)

TL/F/5352–6

FIGURE 1

center frequency vs R1, C to determine R1 and C1	equation $f_{min} = f_o - f_L$ – Use f_{min} with curve titled offset frequency vs R2, C to determine R2 and C1 – Calculate f_{max}/f_{min} from the equation $f_{max}/f_{min} = f_o + f_L/f_o - f_L$ – Use f_{max}/f_{min} with curve titled f_{max}/f_{min} vs R2/R1 to determine ratio R2/R1 to obtain R1	equation $f_o = f_{max}/2$ – Use f_0 with curve titled center frequency vs R1, C to determine R1 and C1	offset frequency vs R2, C to determine R2 and C1 – Calculate f_{max}/f_{min} – Use f_{max}/f_{min} with curve titled f_{max}/f_{min} vs R2/R1 to determine ratio R2/R1 to obtain R1

(b)

FIGURE 1 (Continued)

Detailed Circuit Description

VOLTAGE CONTROLLED OSCILLATOR/SOURCE FOLLOWER

The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor R1 and capacitor C1 are selected to determine the center frequency of the VCO. R1 controls the lock range. As R1's resistance decreases the range of f_{min} to f_{max} increases. Thus the VCO's gain decreases. As C1 is changed the offset (if used) of R2, and the center frequency is changed. (See typical performance curves) R2 can be used to set the offset frequency with 0V at VCO input. If R2 is omitted the VCO range is from 0Hz. As R2 is decreased the offset frequency is increased. The effect of R2 is shown in the design information table and typical performance curves. By increasing the value of R2 the lock range of the PLL is offset above 0Hz and the gain (Volts/rad.) does not change. In general, when offset is desired, R2 and C1 should be chosen first, and then R1 should be chosen to obtain the proper center frequency.

Internally the resistors set a current in a current mirror as shown in *Figure 1*. The mirrored current drives one side of

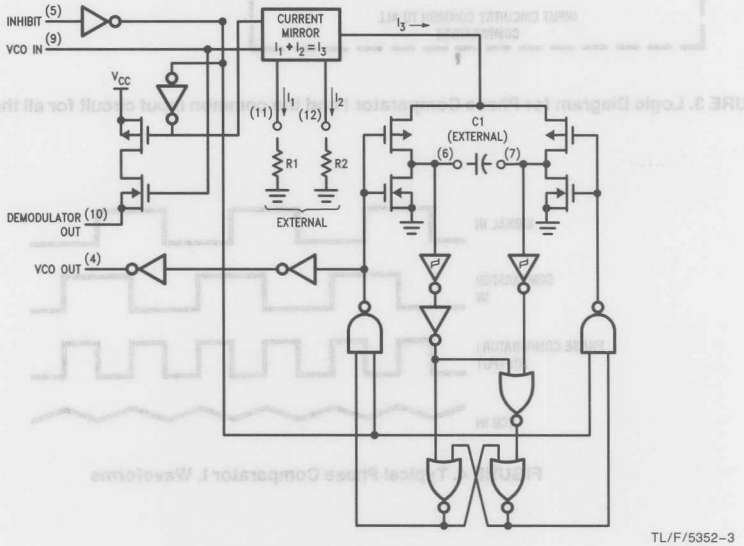


FIGURE 2. Logic Diagram for VCO

Detailed Circuit Description (Continued)

the capacitor once the capacitor charges up to the threshold of the schmitt trigger the oscillator logic flips the capacitor over and causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to pin 4.

The input to the VCO is a very high impedance CMOS input and so it will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance a source follower transistor is provided. This transistor can be used by connecting a resistor to ground and its drain output will follow the VCO input signal.

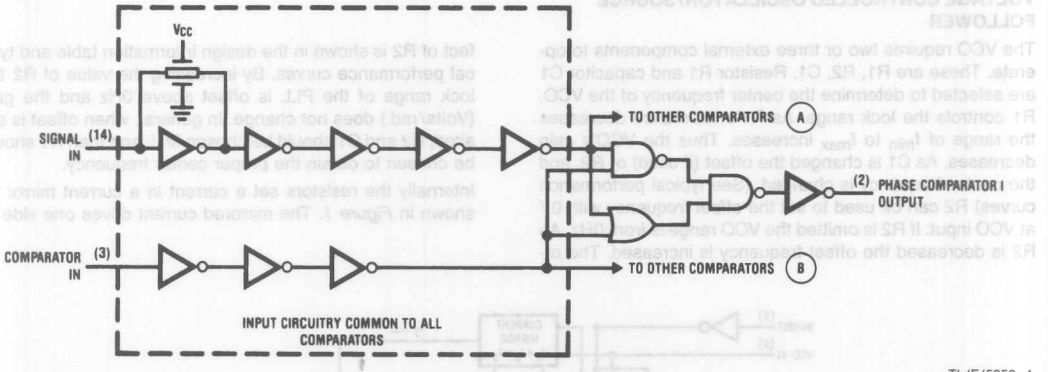
An inhibit signal is provided to allow disabling of the VCO and the source follower. This is useful if the internal VCO is not being used. A logic high on inhibit disables the VCO and source follower.

The output of the VCO is a standard high speed CMOS output with an equivalent LSTTL fanout of 10. The VCO output is approximately a square wave. This output can either directly feed the comparator input of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

PHASE COMPARATORS

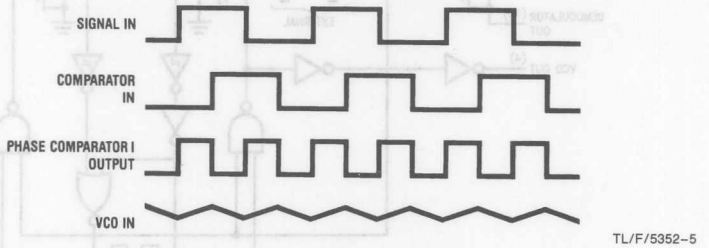
All three phase comparators share two inputs, Signal In and Comparator In. The Signal In has a special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled then this input requires logic levels the same as standard 54HC/74HC. The Comparator input is a standard digital input. Both input structures are shown in *Figure 3*.

The outputs of these comparators are essentially standard 54HC/74HC voltage outputs. (Comparator II is TRI-STATE.)



TL/F/5352–4

FIGURE 3. Logic Diagram for Phase Comparator I and the common input circuit for all three comparators



TL/F/5352–5

FIGURE 4. Typical Phase Comparator I. Waveforms

Detailed Circuit Description (Continued)

Thus in normal operation V_{CC} and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current output to the loop filter and this should be considered in the design. (The CD4046 also provides a voltage.)

Figure 5 shows the state tables for all three comparators.

PHASE COMPARATOR I

This comparator is a simple XOR gate similar to the 54/74HC86, and its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in *Figure 4*. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector I is dependent on the loop filter employed. The capture range can be as large as the lock range which is equal to the VCO frequency range.

To see how the detector operates refer to *Figure 4*. When two square wave inputs are applied to this comparator, an output waveform whose duty cycle is dependent on the phase difference between the two signals results. As the phase difference increases the output duty cycle increases and the voltage after the loop filter increases. Thus in order to achieve lock, when the PLL input frequency increases the VCO input voltage must increase and the phase difference between comparator in and signal in will increase. At an input frequency equal f_{min}, the VCO input is at 0V and this requires the phase detector output to be ground hence the two input signals must be in phase. When the input frequency is f_{max} then the VCO input must be V_{CC} and the phase detector inputs must be 180° out of phase.

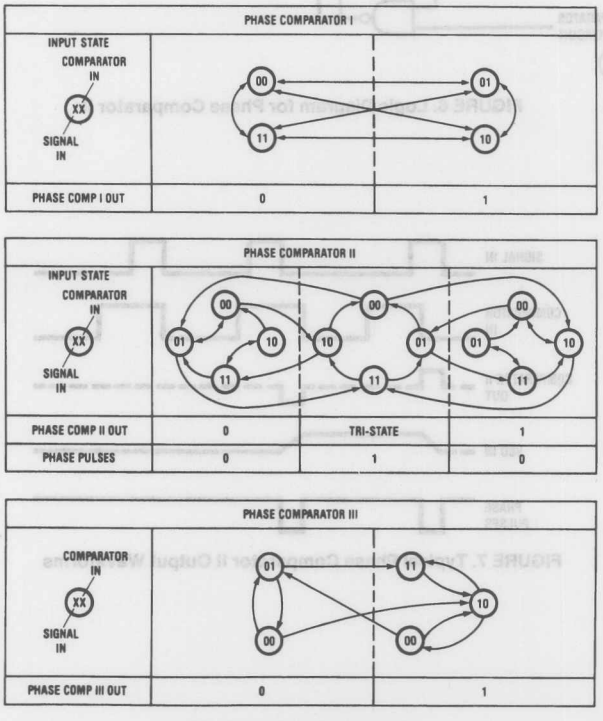
The XOR is more susceptible to locking onto harmonics of the signal input than the digital phase detector II. This can be seen by noticing that a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and the VCO range should be designed to prevent locking on to harmonics.

PHASE COMPARATOR II

This detector is a digital memory network. It consists of four flip-flops and some gating logic, a three state output and a phase pulse output as shown in *Figure 6*. This comparator acts only on the positive edges of the input signals and is thus independent of signal duty cycle.

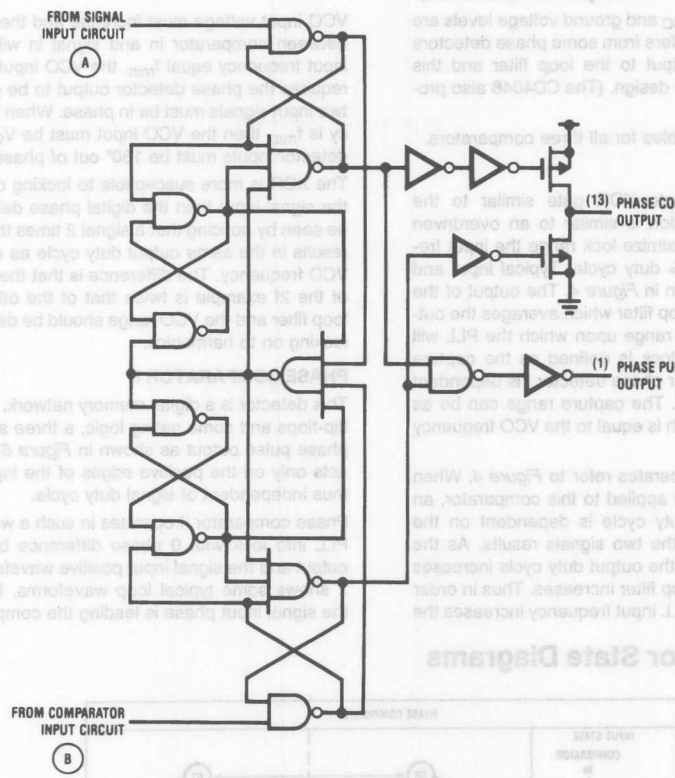
Phase comparator II operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. *Figure 7* shows some typical loop waveforms. First assume that the signal input phase is leading the comparator input. This

Phase Comparator State Diagrams



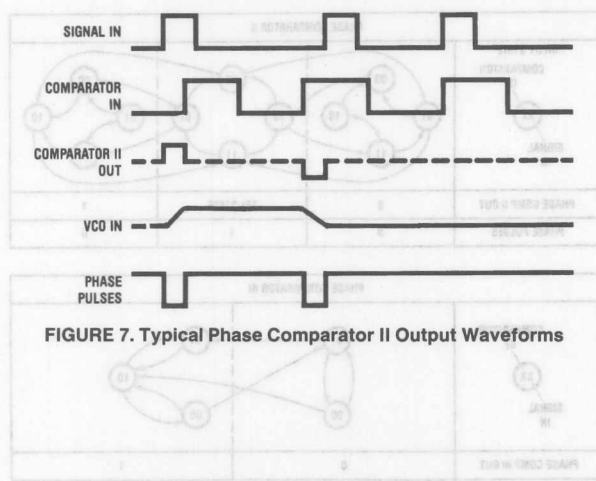
TL/F/5352–10

FIGURE 5. PLL State Tables



TL/F/5352–14

FIGURE 6. Logic Diagram for Phase Comparator II



TL/F/5352–13

FIGURE 7. Typical Phase Comparator II Output Waveforms

Detailed Circuit Description (Continued)

means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector II output is set high. This will cause the loop filter to charge up the VCO input increasing the VCO frequency. Once the leading edge of the comparator input is detected the output goes TRI-STATE holding the VCO input at the loop filter voltage. If the VCO still lags the signal then the phase detector will again charge up to VCO input for the time between the leading edges of both waveforms.

If the VCO leads the signal then when the leading edge of the VCO is seen the output of the phase comparator goes low. This discharges the loop filter until the leading edge of the signal is detected at which time the output TRI-STATE itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveform coincident.

When the PLL is out of lock the VCO will be running either slower or faster than the signal input. If it is running slower the phase detector will see more signal rising edges and so the output of the phase comparator will be high a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the signal the output of the detector will be low most of the time and the VCO's output frequency will be decreased.

As one can see when the PLL is locked the output of phase comparator II will be almost always TRI-STATE except for minor corrections at the leading edge of the waveforms. When the detector is TRI-STATE the phase pulse output is high. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the comparator input and the signal input. The lock range of the PLL is the same as the capture range. Minimal power is consumed in the loop filter since in lock the detector output is a high impedance. Also when no signal is present the detector will see only VCO leading edges, and so the comparator output will stay low forcing the VCO to f_{min} operating frequency.

Phase comparator II is more susceptible to noise causing the phase lock loop to unlock. If a noise pulse is seen on the signal input, the comparator treats it as another positive edge of the signal and will cause the output to go high until the VCO leading edge is seen, potentially for a whole signal input period. This would cause the VCO to speed up during that time. When using the phase comparator I the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

PHASE COMPARATOR III

This comparator is a simple S-R Flip-Flop which can function as a phase comparator *Figure 8*. It has some similar characteristics to the edge sensitive comparator. To see how this detector works assume input pulses are applied to the signal and comparator inputs as shown in *Figure 9*. When the signal input leads the comparator input the flop is set. This will charge up the loop filter and cause the VCO to speed up, bringing the comparator into phase with the signal input. When using short pulses as input this comparator behaves very similar to the second comparator. But one can see that if the signal input is a long pulse, the output of the comparator will be forced to a one no matter how many comparator input pulses are received. Also if the VCO input is a square wave (as it is) and the signal input is pulse then the VCO will force the comparator output low much of the time. Therefore it is ideal to condition the signal and comparator input to short pulses. This is most easily done by using a series capacitor.

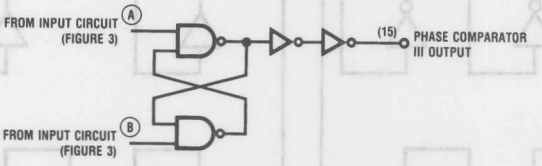


FIGURE 8. Phase Comparator III Logic Diagram

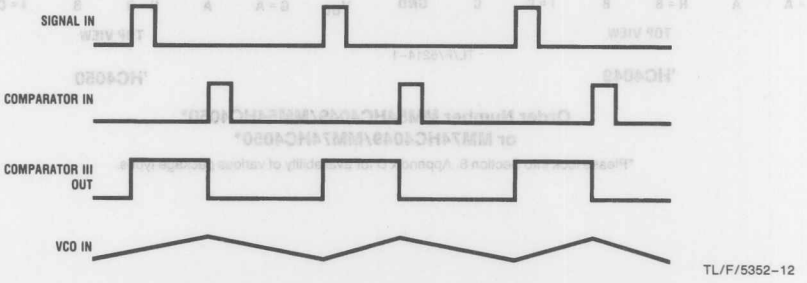


FIGURE 9. Typical Waveforms for Phase Comparator III

National Semiconductor

MM54HC4049/MM74HC4049 Hex Inverting Logic Level Down Converter
MM54HC4050/MM74HC4050 Hex Logic Level Down Converter

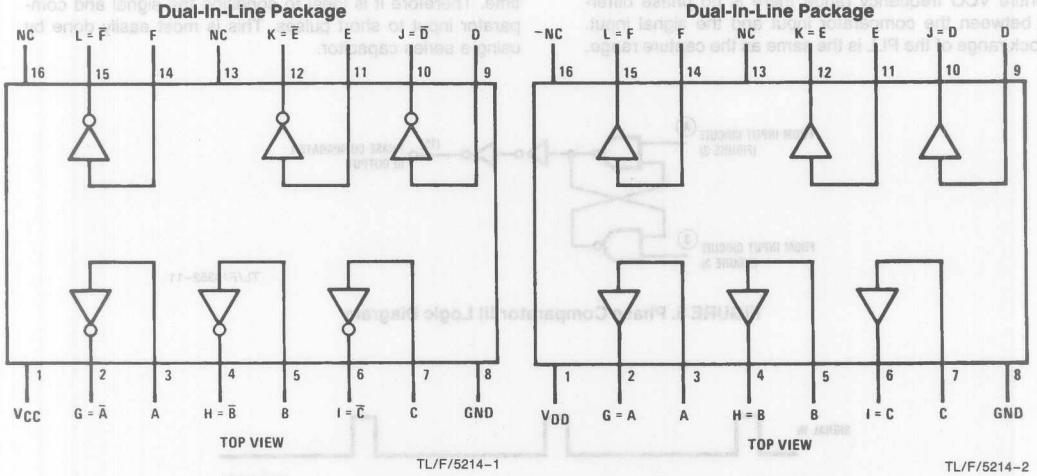
General Description

The MM54HC4049/MM74HC4049 and the MM54HC4050/MM74HC4050 utilize advanced silicon-gate CMOS technology, and have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC}, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a simple buffer or inverter without level translation. The MM54HC4049/MM74HC4049 is pin and functionally compatible to the CD4049BM/CD4049BC and the MM54HC4050/MM74HC4050 is compatible to the CD4050BM/CD4050BC

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 20 μA maximum (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagrams



Order Number MM54HC4049/MM54HC4050*
or MM74HC4049/MM74HC4050*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to +18V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{ZK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temp. Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input Voltage (V_{IN})		0	15	V
DC Output Voltage (V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to 85°C	54HC T_A = −55°C to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7 V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2 V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4 V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4 V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0 μA
		V_{IN} = 15V	2.0V		±0.5	±5	±5 μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND	6.0V		2.0	20	40 μA
		I_{OUT} = 0 μA					

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40°$ to 85°C	54HC $T_A = -55°$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	85	100	130	ns
			4.5V	10	17	20	26	ns
			6.0V	9	15	18	22	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HC4051/MM74HC4051 8-Channel Analog Multiplexer
MM54HC4052/MM74HC4052 Dual 4-Channel Analog Multiplexer
MM54HC4053/MM74HC4053 Triple 2-Channel Analog Multiplexer

General Description

These multiplexers are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, ground, and V_{EE}. This enables the connection of 0–5V logic signals when $V_{CC}=5V$ and an analog input range of ±5V when $V_{EE}=5V$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is "on", and connects one of the eight inputs to the common output.

MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4-channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.

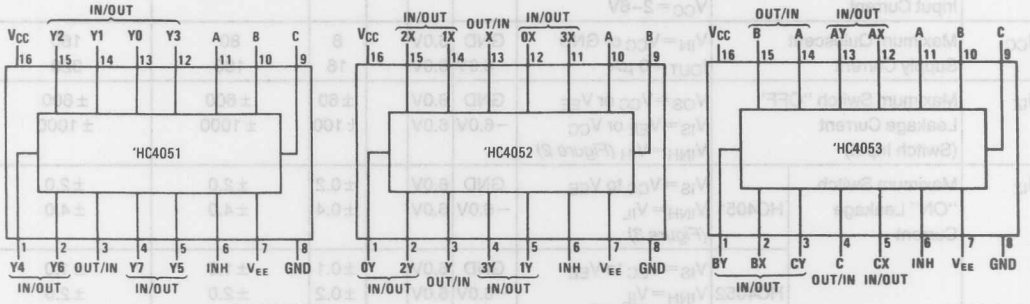
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum (74HC)
- Matched Switch characteristic

Connection Diagrams

Dual-In-Line Packages



TL/F/5353–1 TL/F/5353–2 TL/F/5353–3

Top View **Top View** **Top View**

Order Number MM54HC4051*, MM74HC4051*, MM54HC4052*, MM74HC4052*, MM54HC4053* or MM74HC4053*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V	1000		ns
V_{CC} = 4.5V	500		ns
V_{CC} = 6.0V	400		ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
						Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage				2.0V		1.5	1.5	1.5	V
					4.5V		3.15	3.15	3.15	V
					6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**				2.0V		0.5	0.5	0.5	V
					4.5V		1.35	1.35	1.35	V
					6.0V		1.8	1.8	1.8	V
R_{ON}	Maximum "ON" Resistance (Note 5)		V_{INH} = V_{IL}, I_S = 2.0 mA V_{IS} = V_{CC} to V_{EE} *(Figure 1)*	GND	4.5V	40	160	200	240	Ω
				−4.5V	4.5V	30	120	150	170	Ω
				−6.0V	6.0V	20	100	125	140	Ω
			V_{INH} = V_{IL}, I_S = 2.0 mA V_{IS} = V_{CC} or V_{EE} *(Figure 1)*	GND	2.0V	100	230	280	320	Ω
				GND	4.5V	40	110	140	170	Ω
				−4.5V	4.5V	20	90	120	140	Ω
				−6.0V	6.0V	15	80	100	115	Ω
R_{ON}	Maximum "ON" Resistance Matching		V_{CTL} = V_{IL} V_{IS} = V_{CC} to GND	GND	4.5V	10	20	25	25	Ω
				−4.5V	4.5V	5	10	15	15	Ω
				−6.0V	6.0V	5	10	12	15	Ω
I_{IN}	Maximum Control Input Current		V_{IN} = V_{CC} or GND V_{CC} = 2–6V				±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current		V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	GND	6.0V		8	80	160	μA
				−6.0V	6.0V		16	160	320	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current (Switch Input)		V_{OS} = V_{CC} or V_{EE} V_{IS} = V_{EE} or V_{CC} V_{INH} = V_{IH} *(Figure 2)*	GND	6.0V		±60	±600	±600	nA
				−6.0V	6.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	HC4051	V_{IS} = V_{CC} to V_{EE} V_{INH} = V_{IL} *(Figure 3)*	GND	6.0V		±0.2	±2.0	±2.0	μA
				−6.0V	6.0V		±0.4	±4.0	±4.0	μA
		HC4052	V_{IS} = V_{CC} to V_{EE} V_{INH} = V_{IL} *(Figure 3)*	GND	6.0V		±0.1	±1.0	±1.0	μA
				−6.0V	6.0V		±0.2	±2.0	±2.0	μA
		HC4053	V_{IS} = V_{CC} to V_{EE} V_{INH} = V_{IL} *(Figure 3)*	GND	6.0V		±0.1	±1.0	±1.0	μA
				−6.0V	6.0V		±0.1	±1.0	±1.0	μA

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits		
I_{IZ}	Maximum Switch "OFF" Leakage Current (Common Pin)	HC4051	$V_{OS} = V_{CC}$ or V_{EE} $V_{IS} = V_{EE}$ or V_{CC} $V_{INH} = V_{IH}$	GND	6.0V		±0.2	±2.0	±2.0	μA
				−6.0V	6.0V		±0.4	±4.0	±4.0	μA
		HC4052	$V_{OS} = V_{CC}$ or V_{EE} $V_{IS} = V_{EE}$ or V_{CC} $V_{INH} = V_{IH}$	GND	6.0V		±0.1	±1.0	±1.0	μA
				−6.0V	6.0V		±0.2	±2.0	±2.0	μA
		HC4053	$V_{OS} = V_{CC}$ or V_{EE} $V_{IS} = V_{EE}$ or V_{CC} $V_{INH} = V_{IH}$	GND	6.0V		±0.1	±1.0	±1.0	μA
				−6.0V	6.0V		±0.1	±1.0	±1.0	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages ($V_{CC}-V_{EE}$) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

Note 6: Adjust 0 dB for f = 1 kHz (Null R1/R_{ON} Attenuation).

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 2.0V-6.0V$, $V_{EE} = 0V-6V$, $C_L = 50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions		V_{EE}	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$		54HC $T_A = -55$ to $125°C$		Units
						Typ	Guaranteed Limits				
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out			GND	2.0V	25	60	75		90	ns
				GND	4.5V	5	12	15		18	ns
				−4.5V	4.5V	4	8	12		14	ns
				−6.0V	6.0V	3	7	11		13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	$R_L = 1$ kΩ		GND	2.0V	92	355	435		515	ns
				GND	4.5V		69	87		103	ns
				−4.5V	4.5V	16	46	58		69	ns
				−6.0V	6.0V	15	41	51		62	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay			GND	2.0V	65	290	365		435	ns
				GND	4.5V	28	58	73		87	ns
				−4.5V	4.5V	18	37	46		56	ns
				−6.0V	6.0V	16	32	41		48	ns
f_{MAX}	Minimum Switch Frequency Response 20 log (V_I/V_O) = 3 dB			GND	4.5V	30					MHz
				−4.5V	4.5V	35					MHz
	Control to Switch Feedthrough Noise	$R_L = 600\Omega$, f = 1 MHz, $C_L = 50$ pF	V_{IS} = 4 V_{PP}	0V	4.5V	1080					mV
			V_{IS} = 8 V_{PP}	−4.5V	4.5V	250					mV
	Crosstalk between any Two Switches	$R_L = 600\Omega$, f = 1 MHz	V_{IS} = 4 V_{PP}	0V	4.5	−52					dB
			V_{IS} = 8 V_{PP}	−4.5V	4.5V	−50					dB
	Switch OFF Signal Feedthrough Isolation	$R_L = 600\Omega$, f = 1 MHz, $V_{CTL} = V_{IL}$	V_{IS} = 4 V_{PP}	0V	4.5V	−42					dB
			V_{IS} = 8 V_{PP}	−4.5V	4.5V	−44					dB
THD	Sinewave Harmonic Distortion	$R_L = 10$ kΩ, $C_L = 50$ pF, f = 1 kHz	V_{IS} = 4 V_{PP}	0V	4.5V	0.013					%
			V_{IS} = 8 V_{PP}	−4.5V	4.5V	0.008					%

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified) (Continued)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits			
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input 4051 Common 4052 Common 4053 Common			15 90 45 30				pF
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Truth Tables

'4051

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

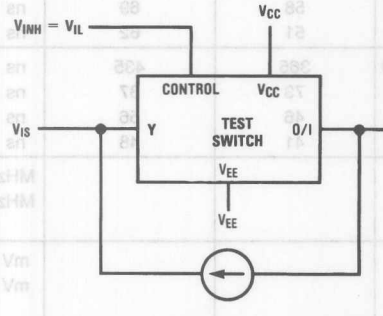
'4052

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

'4053

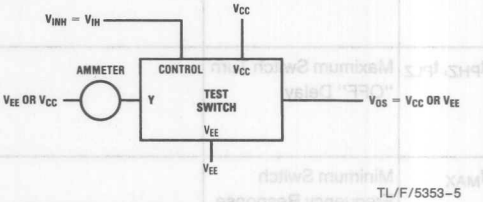
Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AX
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AX
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AX
L	H	H	H	CY	BY	AY

AC Test Circuits and Switching Time Waveforms



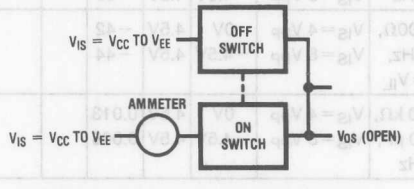
TL/F/5353–4

FIGURE 1. "ON" Resistance



TL/F/5353–5

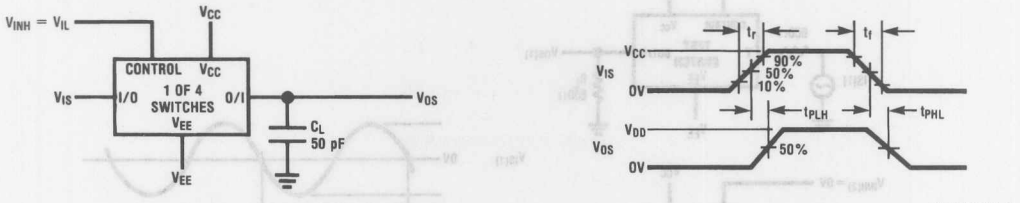
FIGURE 2. "OFF" Channel Leakage Current



TL/F/5353–6

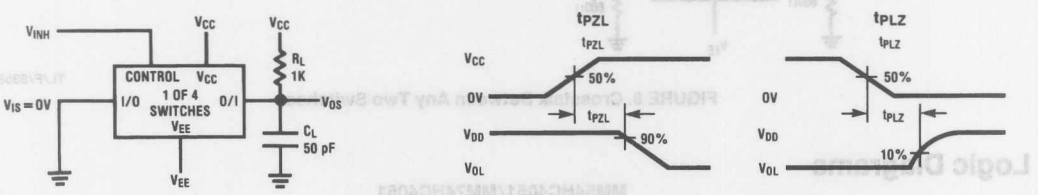
FIGURE 3. "ON" Channel Leakage Current

AC Test Circuits and Switching Time Waveforms (Continued)



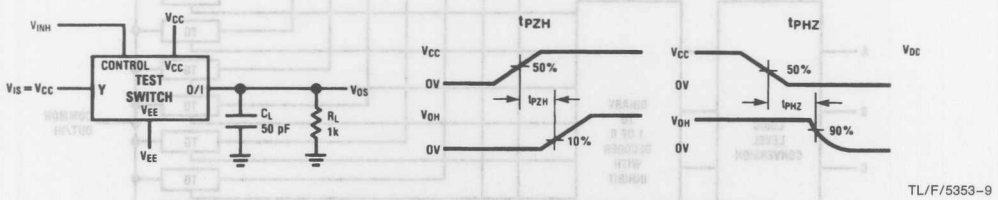
TL/F/5353–7

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



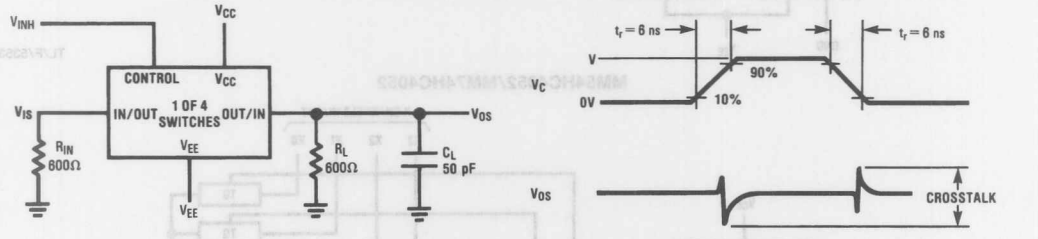
TL/F/5353–8

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output



TL/F/5353–9

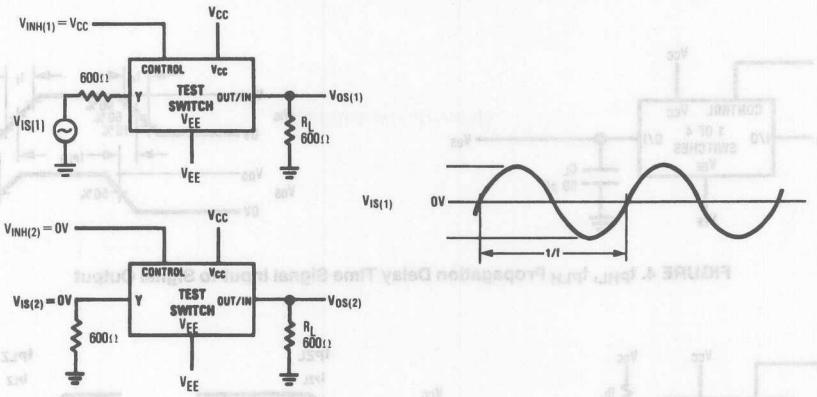
FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5353–10

FIGURE 7. Crosstalk: Control Input to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

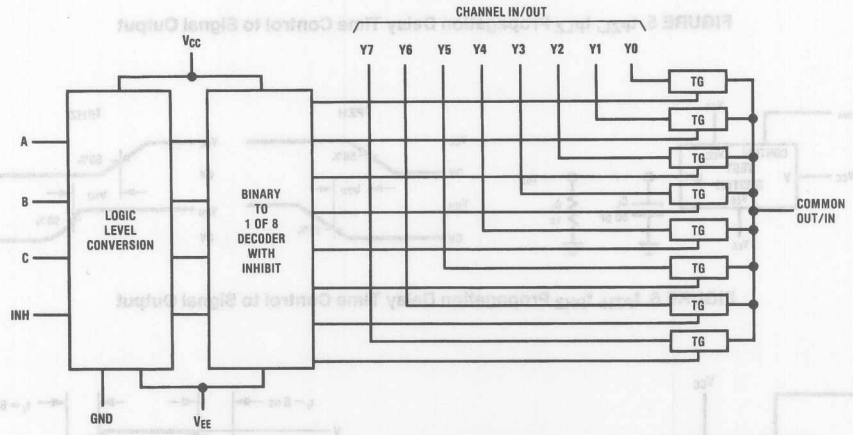


TL/F/5353–11

FIGURE 8. Crosstalk Between Any Two Switches

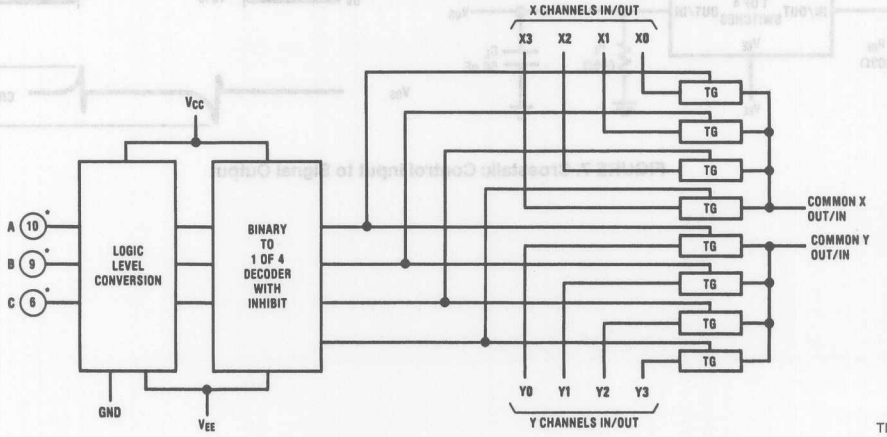
Logic Diagrams

MM54HC4051/MM74HC4051



TL/F/5353–19

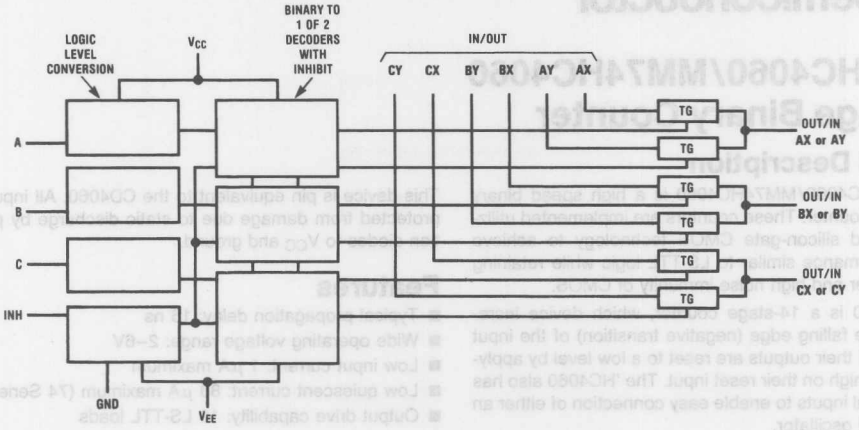
MM54HC4052/MM74HC4052



TL/F/5353–20

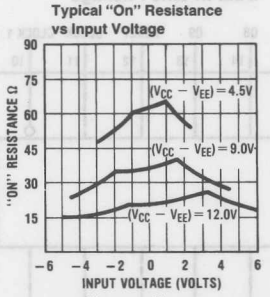
Logic Diagrams (Continued)

MM54HC4053/MM74HC4053



TL/F/5353–21

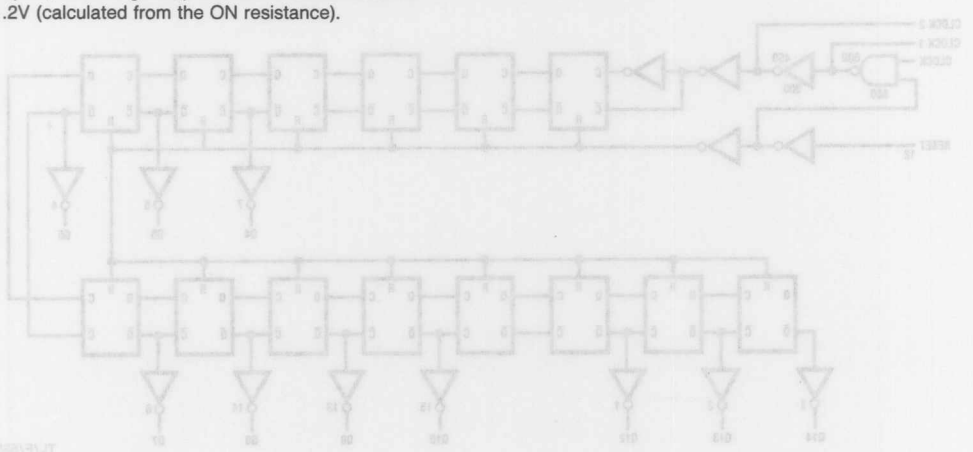
Typical Performance Characteristics



TL/F/5353–18

Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch pins, the voltage drop across the switch must not exceed 1.2V (calculated from the ON resistance).



National Semiconductor

MM54HC4060/MM74HC4060
14 Stage Binary Counter

General Description

The MM54HC4060/MM74HC4060 is a high speed binary ripple carry counter. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4060 is a 14-stage counter, which device increments on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input. The 'HC4060 also has two additional inputs to enable easy connection of either an RC or crystal oscillator.

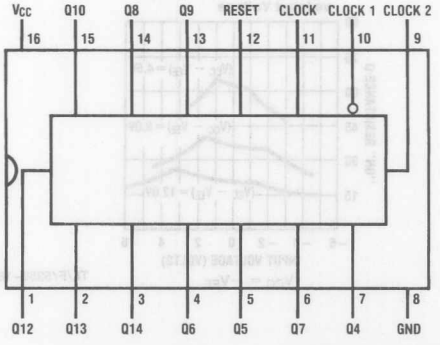
This device is pin equivalent to the CD4060. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads

Connection and Logic Diagrams

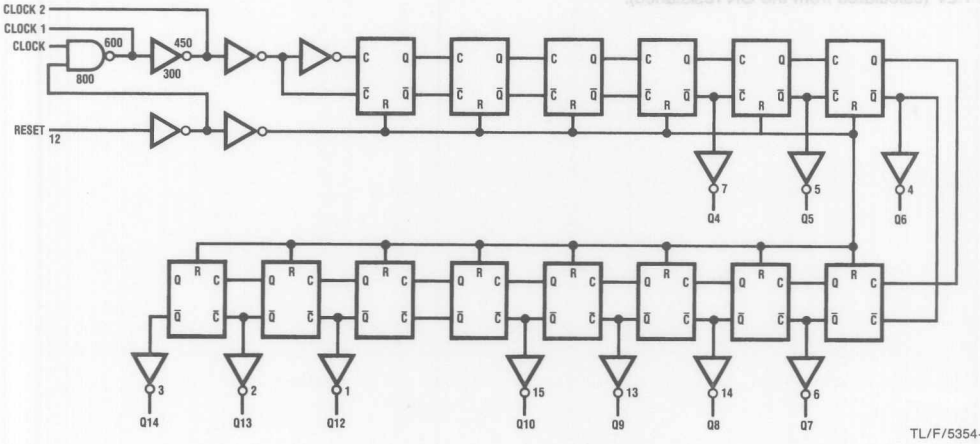
Dual-In-Line Package



Top View

Order Number MM54HC4060* or MM74HC4060*

*Please look into Section 8, Appendix D for availability of various package types.



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC Vcc or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Voltage (Not Applicable to Pins 9 & 10)		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage ** (Not Applicable to Pins 9 & 10)		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	Except Pins 9 & 10	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		| I_{OUT} | ≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
	Pins 9 & 10	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | = 0.4 mA			3.98	3.84	3.7	V
		| I_{OUT} | = 0.52 mA			5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	Except Pins 9 & 10	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | ≤ 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		| I_{OUT} | ≤ 5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
	Pins 9 & 10	V_{IN} = V_{IH} or V_{IL} | I_{OUT} | = 0.4 mA			0.26	0.33	0.4	V
		| I_{OUT} | = 0.52 mA			0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.
Note 2: Unless otherwise specified all voltages are referenced to ground.
Note 3: Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C ceramic "J" package: −12 mW/°C from 100°C to 125°C
Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.
** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency			30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Q_4	(Note 5)	40	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay to any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

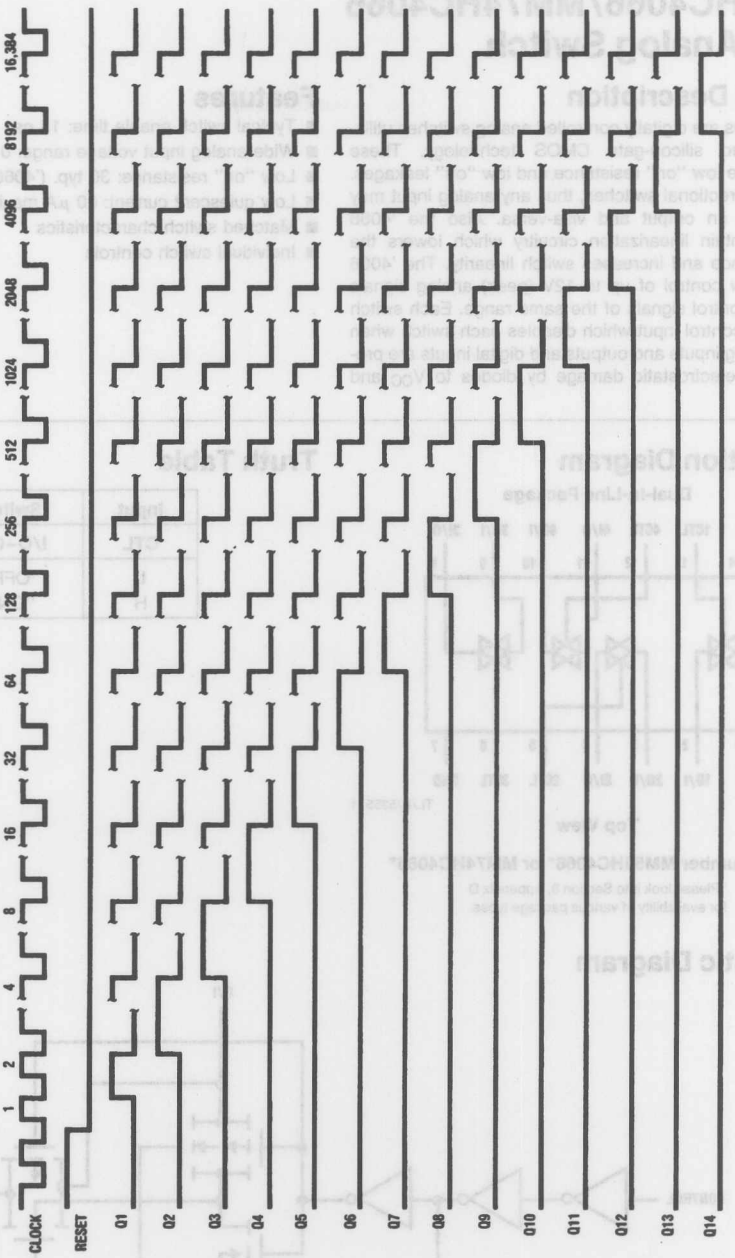
AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A74HC T_A = −40 to 85°C	T_A54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		6	5	4	MHz
			4.5V0		30	24	20	MHz
			6.0V		35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_4		2.0V	120	380	475	171	ns
			4.5V	42	76	95	114	ns
			6.0V	35	65	81	97	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Between Stages Q_n to Q_{n+1}		2.0V		125	156	188	ns
			4.5V		25	31	38	ns
			6.0V		21	26	31	ns
t_{REM}	Mimimum Reset Removal Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_W	Mimimum Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: Typical Propagation delay time to any output can be calculated using: $t_P = 17 + 12(N-1)$ ns; where N is the number of the output, Q_W, at V_{CC} = 5V.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Timing Diagram



National Semiconductor

MM54HC4066/MM74HC4066 Quad Analog Switch

General Description

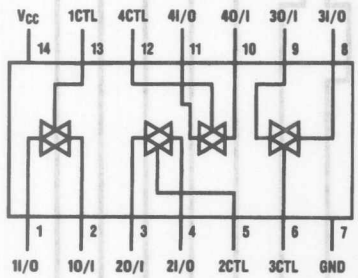
These devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the '4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The '4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line Package



TL/F/5355–1

Top View

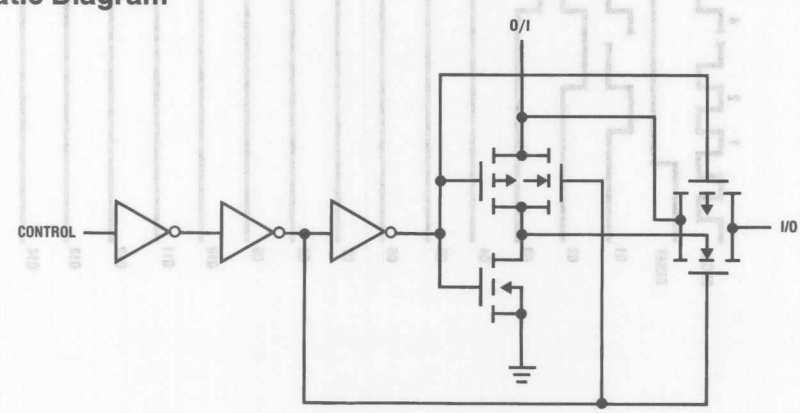
Order Number MM54HC4066* or MM74HC4066*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Schematic Diagram



TL/F/5355–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE} −0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 9.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	5.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			9.0V		2.7	2.7	2.7	V
			12.0V		3.6	3.6	3.6	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	110	Ω
			12.0	30	70	85	90	Ω
		V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} or GND (Figure 1)	2.0V	120	180	215	240	Ω
			4.5V	50	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL} = V_{IH} V_{IS} = V_{CC} to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{CTL} = V_{IL} (Figure 2)	6.0V	10	±60	±600	±600	nA
			9.0V	15	±80	±800	±800	nA
			12.0V	20	±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{IS} = V_{CC} to GND V_{CTL} = V_{IH} (Figure 3) V_{OS} = OPEN	6.0V	10	±40	±150	±150	nA
			9.0V	15	±50	±200	±200	nA
			12.0V	20	±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA
			9.0V		4.0	40	80	μA
			12.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–GND) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–12V, C_L = 50 pF (unless otherwise specified)

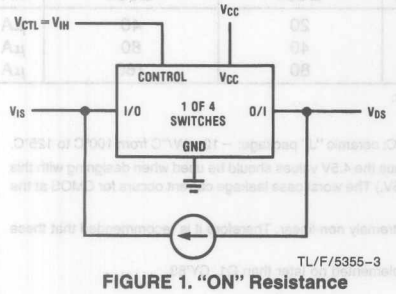
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50	30	75	ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	10	12	ns
			12.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			9.0V	6	12	15	18	ns
			12.0V	5	10	13	15	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L = 1 kΩ	2.0V	60	168	210	252	ns
			4.5V	25	36	45	54	ns
			9.0V	20	32	40	48	ns
			12.0V	15	30	38	45	
	Minimum Frequency Response (Figure 7) 20 log(V_O/V_I) = −3 dB	R_L = 600Ω V_{IS} = 2 V_{PP} at (V_{CC}/2) (Notes 6 & 7)	4.5V	40				MHz
			9.0V	100				MHz
	Crosstalk Between any Two Switches (Figure 8)	R_L = 600Ω, F = 1 MHz (Notes 7 & 8)	4.5V	−52				dB
			9.0V	−50				dB
	Peak Control to Switch Feedthrough Noise (Figure 9)	R_L = 600Ω, F = 1 MHz C_L = 50 pF	4.5V	100				mV
			9.0V	250				mV
	Switch OFF Signal Feedthrough Isolation (Figure 10)	R_L = 600Ω, F = 1 MHz $V_{(CT)}$ V_{IL} (Notes 7 & 8)	4.5V	−42				dB
			9.0V	−44				dB
THD	Total Harmonic Distortion (Figure 11)	R_L = 10 kΩ, C_L = 50 pF, F = 1 kHz V_{IS} = 4 V_{PP}	4.5V	.013				%
		V_{IS} = 8 V_{PP}	9.0V	.008				%
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			20				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		0.5				pF
C_{PD}	Power Dissipation Capacitance			15				pF

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/R_{ON} Attenuation).

Note 7: V_{IS} is centered at V_{CC}/2.

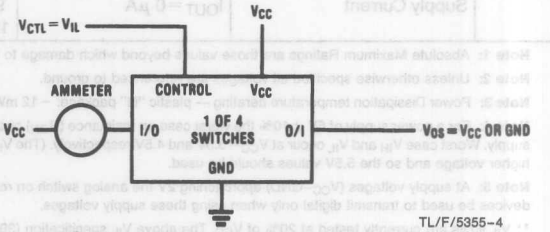
Note 8: Adjust input for 0 dBm.

AC Test Circuits and Switching Time Waveforms



TL/F/5355–3

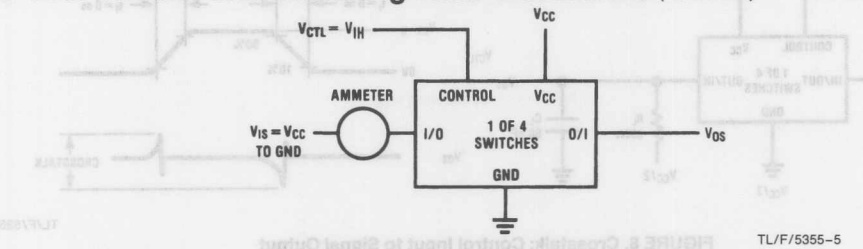
FIGURE 1. "ON" Resistance



TL/F/5355–4

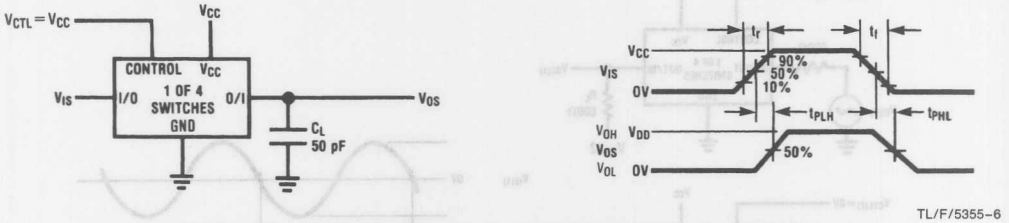
FIGURE 2. "OFF" Channel Leakage Current

AC Test Circuits and Switching Time Waveforms (Continued)



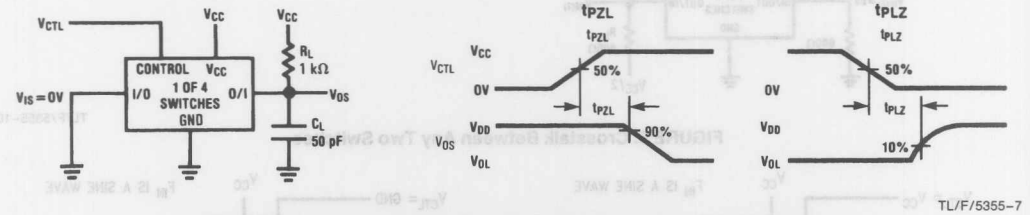
TL/F/5355–5

FIGURE 3. "ON" Channel Leakage Current



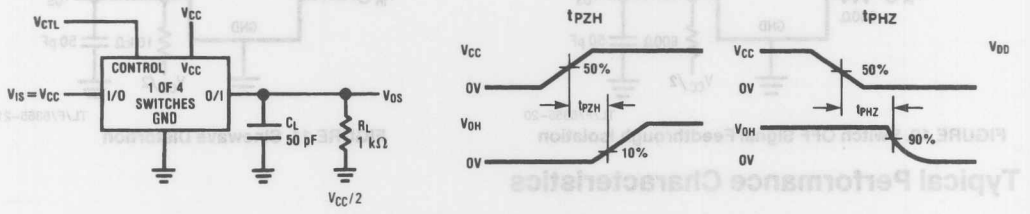
TL/F/5355–6

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



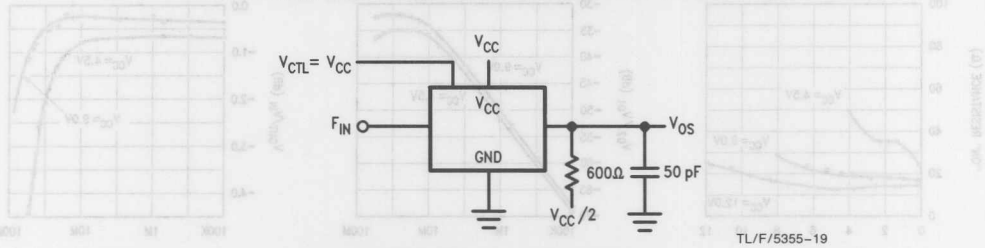
TL/F/5355–7

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output



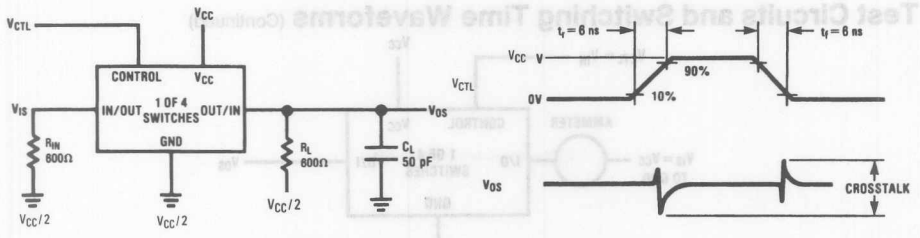
TL/F/5355–8

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



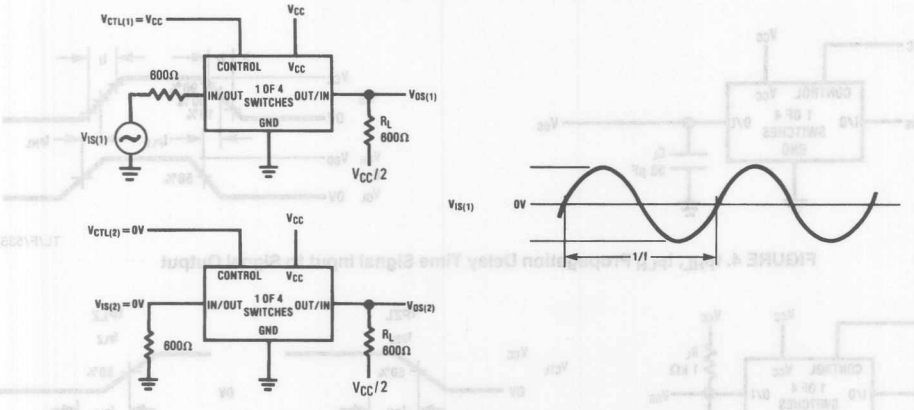
TL/F/5355–19

FIGURE 7. Frequency Response



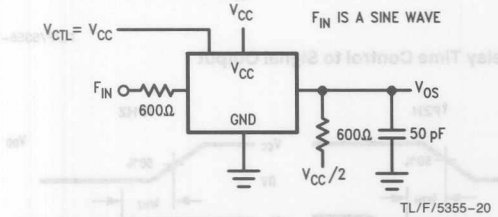
TL/F/5355–9

FIGURE 8. Crosstalk: Control Input to Signal Output



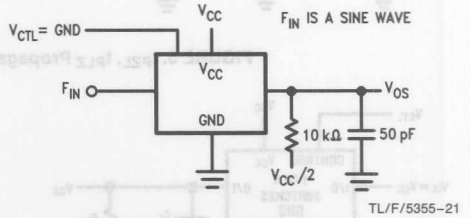
TL/F/5355–10

FIGURE 9. Crosstalk Between Any Two Switches



TL/F/5355–20

FIGURE 10. Switch OFF Signal Feedthrough Isolation

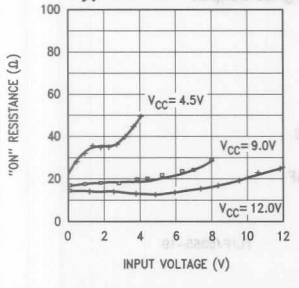


TL/F/5355–21

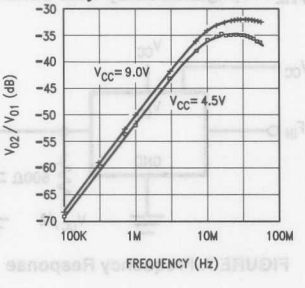
FIGURE 11. Sinewave Distortion

Typical Performance Characteristics

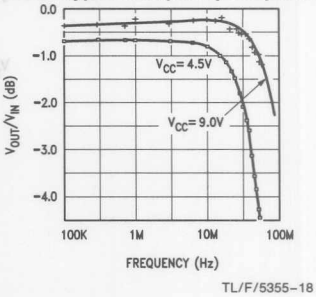
Typical "ON" Resistance



Typical Crosstalk Between Any Two Switches



Typical Frequency Response



TL/F/5355–18

Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

National Semiconductor

MM54HC4075/MM74HC4075 Triple 3-Input OR Gate

General Description

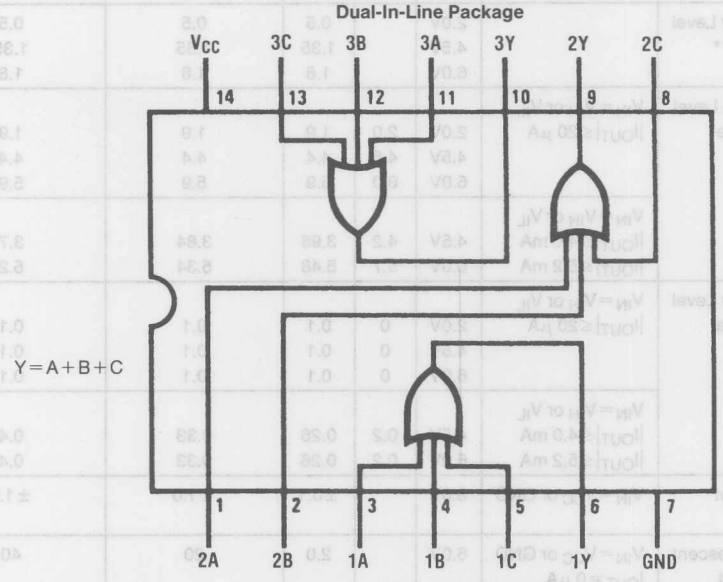
These OR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4075/74HC4075 is functionally equivalent and pin-out compatible with the CD4075B and MC14075B metal gate CMOS devices. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 11 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



Top View

Order Number MM54HC4075* or MM74HC4075*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	40	115	145	171	ns
			4.5V	12	23	29	34	ns
			6.0V	10	20	25	29	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		30				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC4078/MM74HC4078 8-Input NOR/OR Gate

General Description

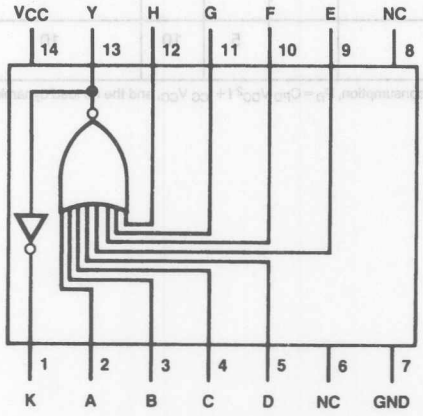
These NOR gates utilize advanced silicon-gate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. Both outputs are buffered, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC4078/74HC4078 is functionally equivalent and pin-out compatible with the CD4078B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5135–1

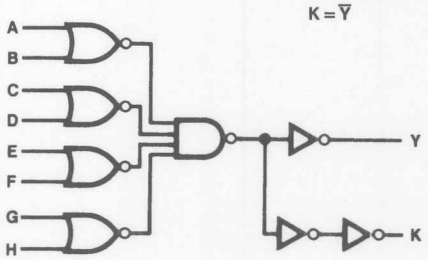
Top View

Order Number MM54HC4078* or MM74HC4078*

*Please look into Section 8, Appendix D for availability of various package types.

$$Y = \overline{A + B + C + D + E + F + G + H}$$

$$K = \overline{Y}$$



TL/F/5135–2

Absolute Maximum Ratings

(Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics MM54HC4078/74HC4078

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y Output		14	22	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K Output		16	24	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y Output		2.0V	47	130	160	195	ns
			4.5V	17	26	33	39	ns
			6.0V	14	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K Output		2.0V	50	140	175	210	ns
			4.5V	20	28	35	42	ns
			6.0V	17	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HC4316/MM74HC4316
Quad Analog Switch with Level Translator

General Description

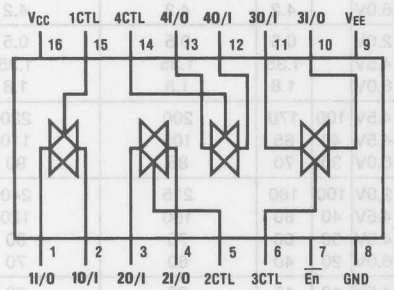
These devices are digitally controlled analog switches implemented in advanced silicon-gate CMOS technology. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the '4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels. The '4316 also has a common enable input in addition to each switch's control which when low will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls plus a common enable

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5369–1

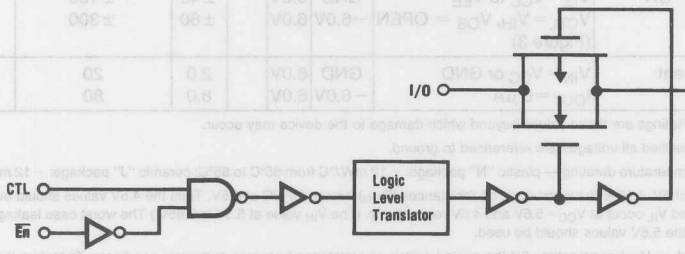
Top View

Order Number MM54HC4316* or MM74HC4316*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"



TL/F/5369–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE} −0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns
V_{CC} = 12.0V		250	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**			2.0V		0.5	0.5	0.5	V
				4.5V		1.35	1.35	1.35	V
				6.0V		1.8	1.8	1.8	V
R_{ON}	Minimum "ON" Resistance (See Note 5)	V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} to V_{EE} (Figure 1)	GND	4.5V	100	170	200	220	Ω
			−4.5V	4.5V	40	85	105	110	Ω
			−6.0V	6.0V	30	70	85	90	Ω
		V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} or V_{EE} (Figure 1)	GND	2.0V	100	180	215	240	Ω
			GND	4.5V	40	80	100	120	Ω
			−4.5V	4.5V	50	60	75	80	Ω
			−6.0V	6.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL} = V_{IH} V_{IS} = V_{CC} to V_{EE}	GND	4.5V	10	15	20	20	Ω
			−4.5V	4.5V	5	10	15	15	Ω
			−6.0V	6.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND	GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS} = V_{CC} or V_{EE} V_{IS} = V_{EE} or V_{CC} V_{CTL} = V_{IL} (Fig 2)	GND	6.0V		±60	±600	±600	nA
			−6.0V	6.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{IS} = V_{CC} to V_{EE} V_{CTL} = V_{IH}, V_{OS} = OPEN (Figure 3)	GND	6.0V		±40	±150	±150	nA
			−6.0V	6.0V		±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	GND	6.0V		2.0	20	40	μA
			−6.0V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V, V_{EE} = 0V–6V, C_L = 50 pF (unless otherwise specified)

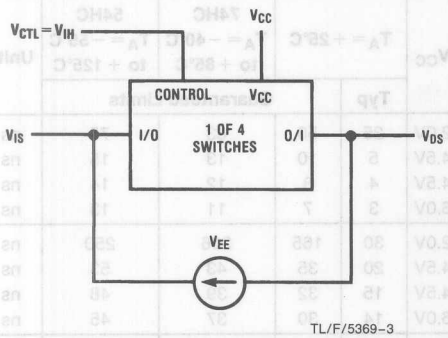
Symbol	Parameter	Conditions	V_{EE}	V_{CC}	$T_A = +25°C$		74HC $T_A = -40°C$ to $+85°C$	54HC $T_A = -55°C$ to $+125°C$	Units
					Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	50	63	75	ns
			GND	4.5V	5	10	13	15	ns
			−4.5V	4.5V	4	8	12	14	ns
			−6.0V	6.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Control)	$R_L = 1\ k\Omega$	GND	2.0V	30	165	206	250	ns
			GND	4.5V	20	35	43	53	ns
			−4.5V	4.5V	15	32	39	48	ns
			−6.0V	6.0V	14	30	37	45	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay (Control)	$R_L = 1\ k\Omega$	GND	2.0V	45	250	312	375	ns
			GND	4.5V	25	50	63	75	ns
			−4.5V	4.5V	20	44	55	66	ns
			−6.0V	6.0V	20	44	55	66	
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Enable)		GND	2.0V	35	205	256	308	ns
			GND	4.5V	20	41	52	62	ns
			−4.5V	4.5V	19	38	48	57	ns
			−6.0V	6.0V	18	36	45	54	ns
t_{PLZ}, t_{PHZ}	Maximum Switch Turn "OFF" Delay (Enable)		GND	2.0V	58	265	330	400	ns
			GND	4.5V	28	53	67	79	ns
			−4.5V	4.5V	23	47	59	70	ns
			−6.0V	6.0V	21	47	59	70	ns
	Minimum Frequency Response (*Figure 7*) 20 log (V_{OS}/V_{IS}) = −3 dB	$R_L = 600\Omega$, $V_{IS} = 2V_{PP}$ at ($V_{CC}-V_{EE}/2$) (Notes 6, 7)	0V	4.5	40				MHz
			−4.5V	4.5V	100				MHz
	Control to Switch Feedthrough Noise (*Figure 8*)	$R_L = 600\Omega$, F = 1 MHz C_L = 50 pF (Notes 7, 8)	0V	4.5V	100				mV
			−4.5V	4.5V	250				mV
	Crosstalk Between any Two Switches (*Figure 9*)	$R_L = 600\Omega$, F = 1 MHz	0V	4.5V	−52				dB
			−4.5V	4.5V	−50				dB
	Switch OFF Signal Feedthrough Isolation (*Figure 10*)	$R_L = 600\Omega$, F = 1 MHz $V_{CTL} = V_{IL}$, (Notes 7, 8)	0V	4.5V	−42				dB
			−4.5V	4.5V	−44				dB
THD	Sinewave Harmonic Distortion (Figure 11)	$R_L = 10\ K\Omega$, C_L = 50 pF, F = 1 KHz $V_{IS} = 4V_{PP}$	0V	4.5V	0.013				%
		$V_{IS} = 8V_{PP}$	−4.5V	4.5V	0.008				%
C_{IN}	Maximum Control Input Capacitance				5				pF
C_{IN}	Maximum Switch Input Capacitance				35				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND			0.5				pF
C_{PD}	Power Dissipation Capacitance				15				pF

Note 6: Adjust 0 dBm for F = 1 KHz (Null R_L/Ron Attenuation).

Note 7: V_{IS} is centered at $V_{CC}-V_{EE}/2$.

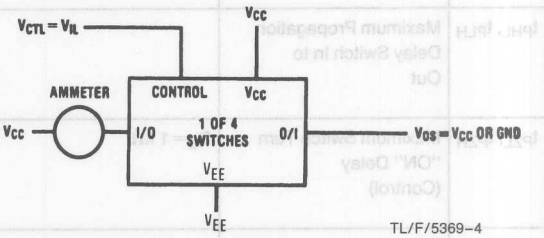
Note 8: Adjust for 0 dBm.

AC Test Circuits and Switching Time Waveforms



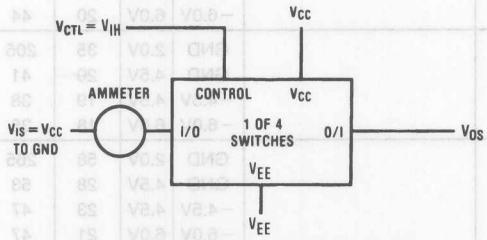
TL/F/5369–3

FIGURE 1. "ON" Resistance



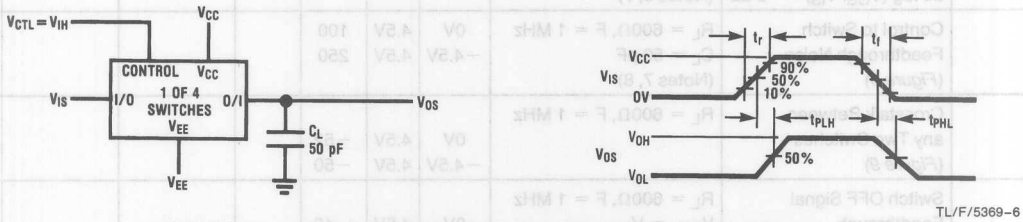
TL/F/5369–4

FIGURE 2. "OFF" Channel Leakage Current



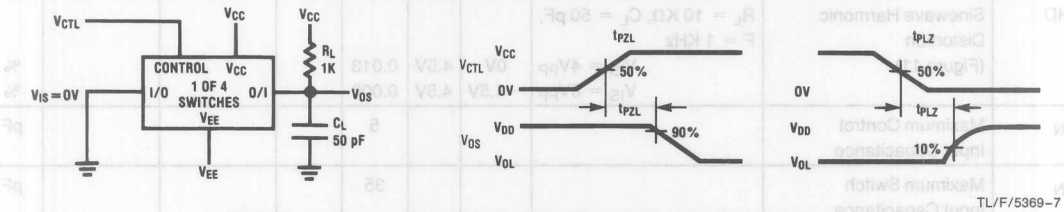
TL/F/5369–5

FIGURE 3. "ON" Channel Leakage Current



TL/F/5369–6

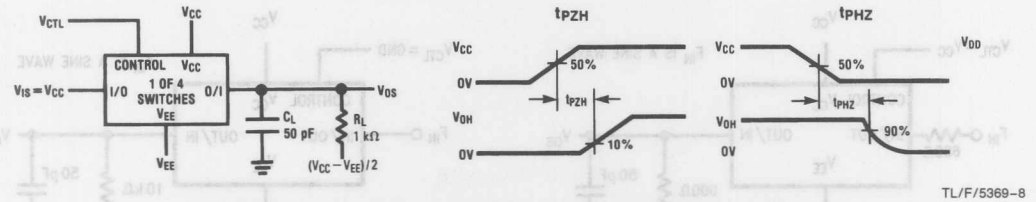
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/F/5369–7

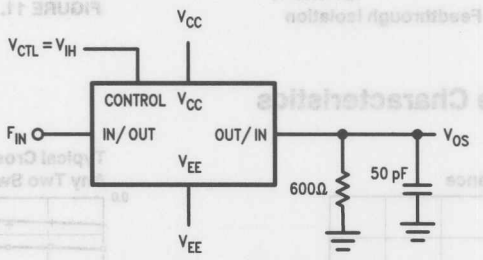
FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



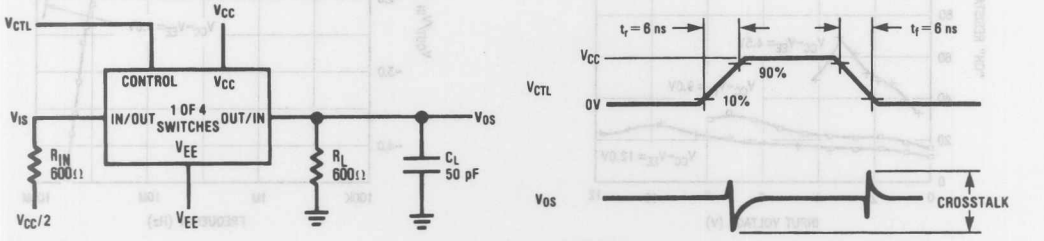
TL/F/5369–8

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



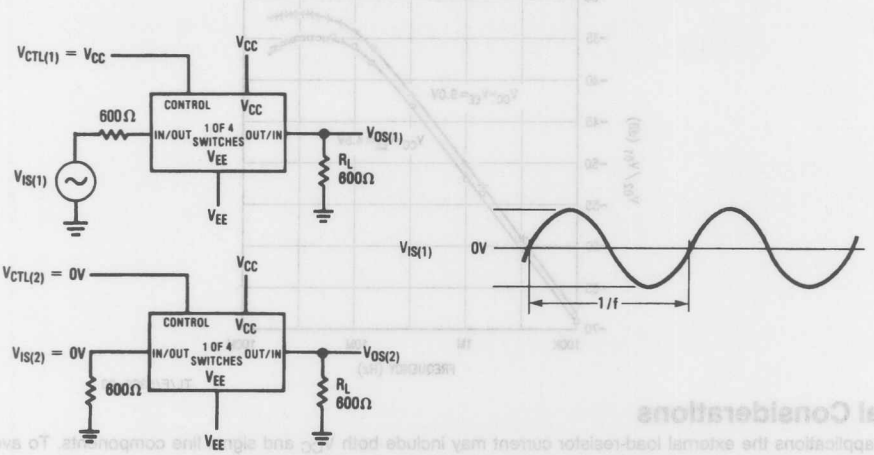
TL/F/5369–18

FIGURE 7. Frequency Response



TL/F/5369–9

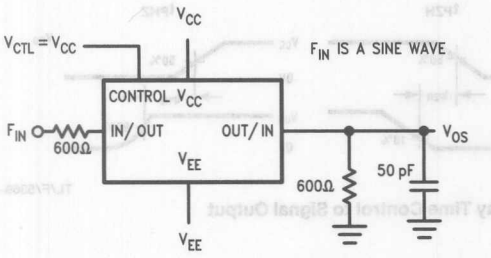
FIGURE 8. Crosstalk: Control Input to Signal Output



TL/F/5369–10

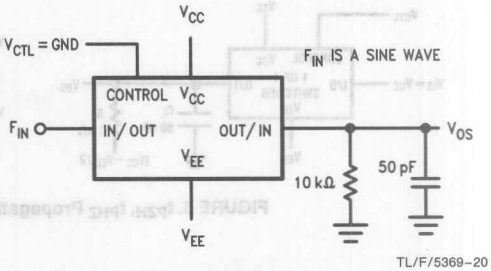
FIGURE 9: Crosstalk Between Any Two Switches

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5369–19

FIGURE 10. Switch OFF Signal Feedthrough Isolation

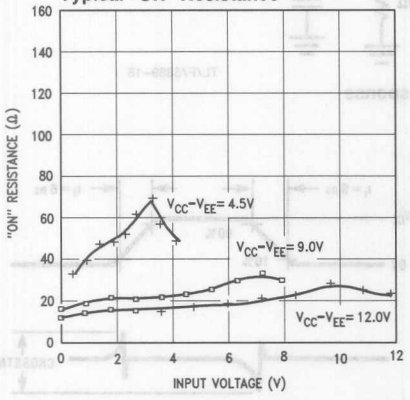


TL/F/5369–20

FIGURE 11. Sinewave Distortion

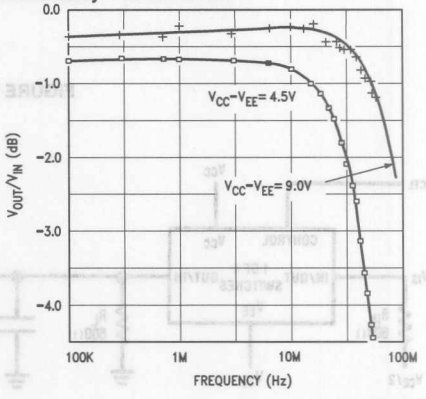
Typical Performance Characteristics

Typical "ON" Resistance



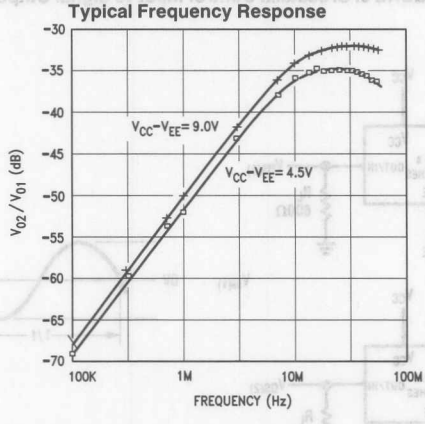
TL/F/5369–21

Typical Crosstalk Between Any Two Switches



TL/F/5369–22

Typical Frequency Response



TL/F/5369–23

Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

National Semiconductor

MM54HC4511/MM74HC4511 BCD-to-7 Segment Latch/Decoder/Driver

General Description

This high speed latch/decoder/driver utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

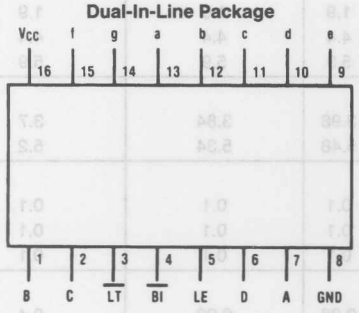
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Latch storage of input data
- Blanking input
- Lamp test input
- Low power consumption characteristics of CMOS devices
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum over full temperature range (74 Series)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5373–1

Order Number MM54HC4511* or MM74HC4511*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
x	x	L	x	x	x	x	H	H	H	H	H	H	H	8
x	L	H	x	x	x	x	L	L	L	L	L	L	L	
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	
L	H	H	H	L	H	H	L	L	L	L	L	L	L	
L	H	H	H	H	L	L	L	L	L	L	L	L	L	
L	H	H	H	H	L	H	L	L	L	L	L	L	L	
L	H	H	H	H	H	L	L	L	L	L	L	L	L	
L	H	H	H	H	H	H	L	L	L	L	L	L	L	
H	H	H	x	x	x	x	*							*

x = Don't care

* = Depends upon the BCD code applied during the 0 to 1 transition of LE.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Inputs A thru D to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{BI}$ to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{LT}$ to any Output		60	120	ns
t_S	Minimum Setup Time Inputs A thru D to LE		10	20	ns
t_H	Minimum Hold Time Inputs A thru D to LE		−3	0	ns
t_W	Minimum Pulse Width for LE			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Inputs A thru D to any Output	LE = 0V $\overline{LT}=V_{CC}$ $\overline{BI}=V_{CC}$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{BI}$ to any Output	$\overline{LT}=V_{CC}$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{LT}$ to any Output	$\overline{BI}=0V$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_S	Minimum Setup Time Inputs A thru D to LE		2.0V 4.5V 6.0V		100 20 17	126 25 21	149 30 25	ns ns ns
t_H	Minimum Hold Time Inputs A thru D to LE		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width for LE		2.0V 4.5V 6.0V		80 16 14	100 20 17	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

INPUTS

A, B, C, D (Pins 7, 1, 2, 6)—BCD data inputs. A (pin 7) is the least-significant data bit and D (pin 6) is the most significant bit. Hexadecimal data A–F at these inputs will cause the outputs to assume a logic low, offering an alternate method of blanking the display.

OUTPUTS

a–g—Decoded, buffered outputs. These outputs, unlike the 4511, have CMOS drivers, which will produce typical CMOS output voltage levels.

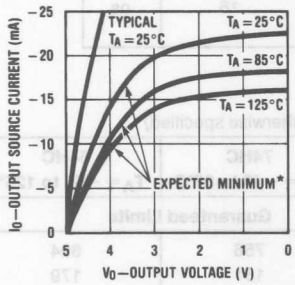
CONTROLS

$\overline{BI}$ (Pin 4)—Active-low display blanking input. A logic low on this input will cause all outputs to be held at a logic low, thereby blanking the display. LT is the only input that will override the BI input.

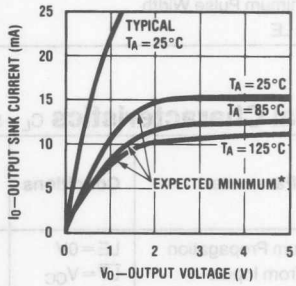
$\overline{LT}$ (Pin 3)—Active-low lamp test. A low logic level on this input causes all outputs to assume a logic high. This input allows the user to test all segments of a display, with a single control input. This input is independent of all other inputs.

LE (Pin 5)—Latch enable input. This input controls the 4-bit transparent latch. A logic high on this input latches the data present at the A, B, C and D inputs; a logic low allows the data to be transmitted through the latch to the decoder.

Output Characteristics (V_{CC} = 5V)



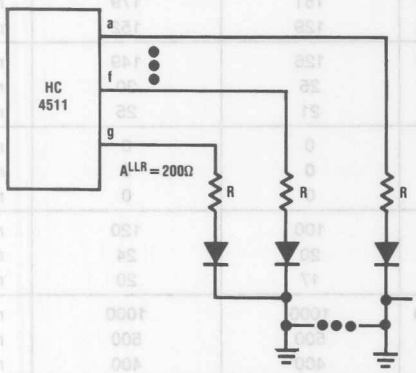
TL/F/5373–2



TL/F/5373–3

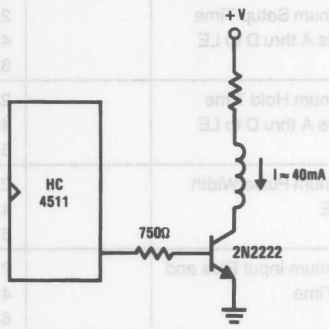
*The expected minimum curves are not guarantees, but are design aids.

Typical Applications



TL/F/5373–4

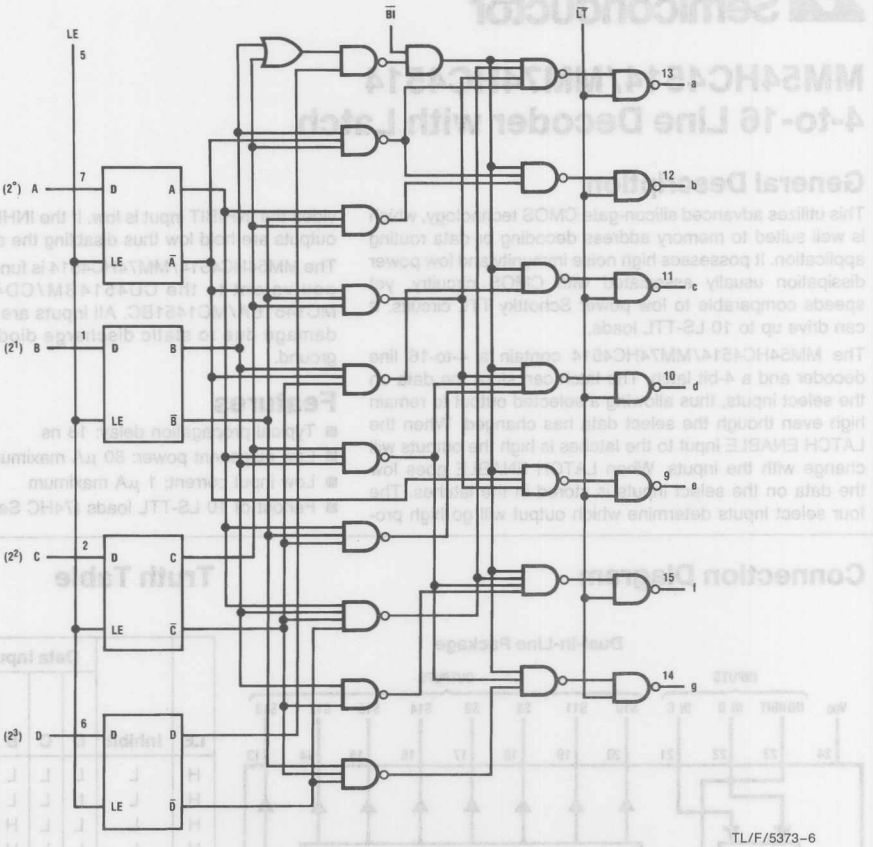
Typical Common Cathode LED Connection



TL/F/5373–5

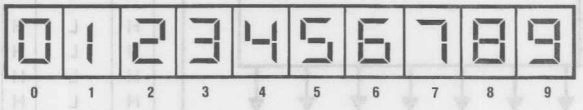
Incandescent Bulb Driving Circuit

Logic Diagram



TL/F/5373–6

Display



TL/F/5373–7

Segment Identification



TL/F/5373–8

National Semiconductor

MM54HC4514/MM74HC4514
4-to-16 Line Decoder with Latch

General Description

This utilizes advanced silicon-gate CMOS technology, which is well suited to memory address decoding or data routing application. It possesses high noise immunity and low power dissipation usually associated with CMOS circuitry, yet speeds comparable to low power Schottky TTL circuits. It can drive up to 10 LS-TTL loads.

The MM54HC4514/MM74HC4514 contain a 4-to-16 line decoder and a 4-bit latch. The latch can store the data on the select inputs, thus allowing a selected output to remain high even though the select data has changed. When the LATCH ENABLE input to the latches is high the outputs will change with the inputs. When LATCH ENABLE goes low the data on the select inputs is stored in the latches. The four select inputs determine which output will go high provided the INHIBIT input is low. If the INHIBIT input is high all outputs are held low thus disabling the decoder.

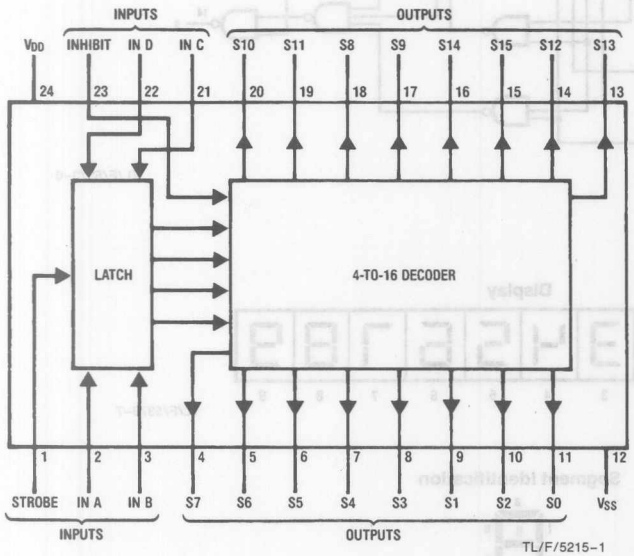
The MM54HC4514/MM74HC4514 is functionally and pinout equivalent to the CD4514BM/CD4514BC and the MC1451BA/MC1451BC. All inputs are protected against damage due to static discharge diodes from V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Low quiescent power: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC Series)

Connection Diagram

Dual-In-Line Package



Top View

Order Number MM54HC4514* or MM74HC4514*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

LE	Inhibit	Data Inputs D	C	B	A	Selected Output High
H	L	L	L	L	L	S0
H	L	L	L	L	H	S1
H	L	L	L	H	L	S2
H	L	L	L	H	H	S3
H	L	L	H	L	L	S4
H	L	L	H	L	H	S5
H	L	L	H	H	L	S6
H	L	L	H	H	H	S7
H	L	H	L	L	L	S8
H	L	H	L	L	H	S9
H	L	H	L	H	L	S10
H	L	H	L	H	H	S11
H	L	H	H	L	L	S12
H	L	H	H	L	H	S13
H	L	H	H	H	L	S14
H	L	H	H	H	H	S15
X	H	X	X	X	X	All Outputs = 0
L	L	X	X	X	X	Latched Data

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	V
			4.5V		1.35	1.35	V
			6.0V		1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

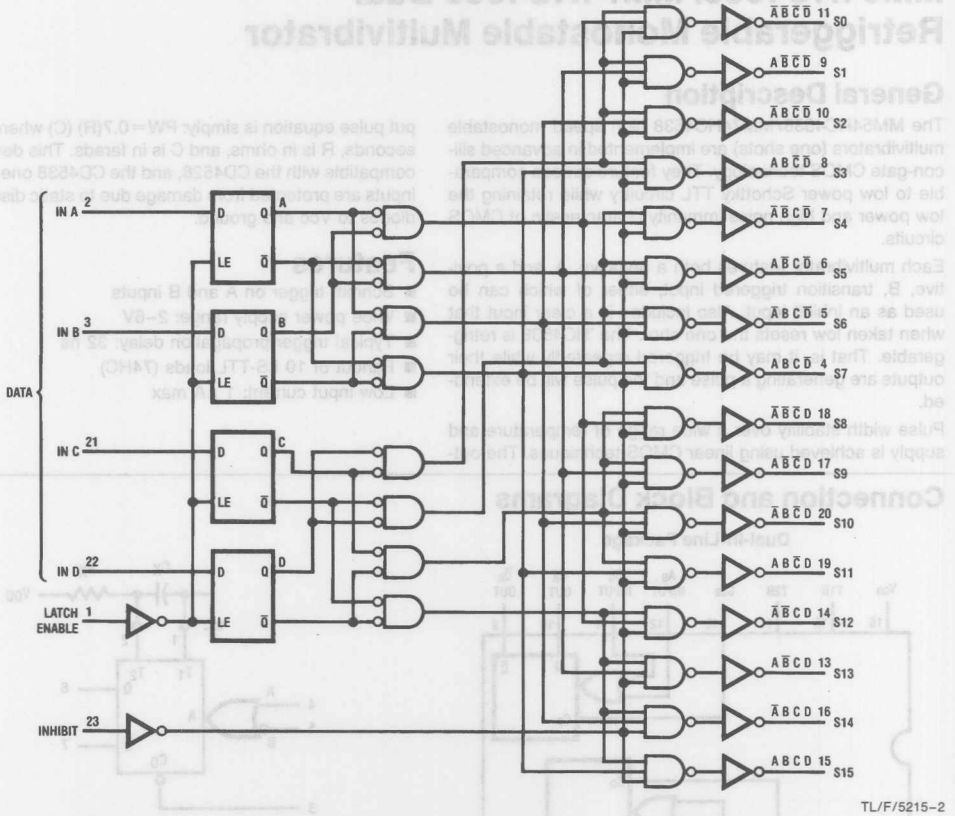
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	30	ns
t_{PHL}	Maximum Propagation Delay LE to Output		18	30	ns
t_{PLH}	Maximum Propagation Delay LE to Output		24	40	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		16	30	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		24	40	ns
t_s	Minimum Setup Time, Date to LE			20	ns
t_H	Minimum Hold Time, LE to Data			5	ns
t_W	Minimum Pulse Width, Latch Enable			16	ns

AC Electrical Characteristics $V_{CC}=2.0V-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		2.0V	80	175	220	263	ns
			4.5V	18	35	44	53	ns
			6.0V	16	30	38	45	ns
t_{PHL}	Maximum Propagation Delay LE to Output		2.0V	80	175	220	263	ns
			4.5V	19	35	44	53	ns
			6.0V	17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay LE to Output		2.0V	120	230	290	343	ns
			4.5V	27	46	58	69	ns
			6.0V	22	39	49	58	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		2.0V	70	175	220	263	ns
			4.5V	18	35	44	53	ns
			6.0V	16	30	38	45	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		2.0V	120	230	290	343	ns
			4.5V	27	46	58	69	ns
			6.0V	22	39	49	58	ns
t_s	Minimum Setup Time, Data to LE		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time, LE to Data		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width, Latch Enable		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance			290				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5215–2

3

National Semiconductor

MM54HC4538/MM74HC4538 Dual Retriggerable Monostable Multivibrator

General Description

The MM54HC4538/MM74HC4538 high speed monostable multivibrators (one shots) are implemented in advanced silicon-gate CMOS technology. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC4538 is retriggerable. That is, it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

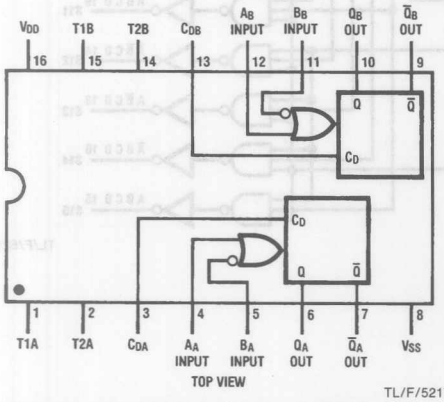
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: PW = 0.7(R) (C) where PW is in seconds, R is in ohms, and C is in farads. This device is pin compatible with the CD4528, and the CD4538 one shots. All inputs are protected from damage due to static discharge by diodes to Vcc and ground.

Features

- Schmitt trigger on A and B inputs
- Wide power supply range: 2–6V
- Typical trigger propagation delay: 32 ns
- Fanout of 10 LS-TTL loads (74HC)
- Low input current: 1 μA max

Connection and Block Diagrams

Dual-In-Line Package

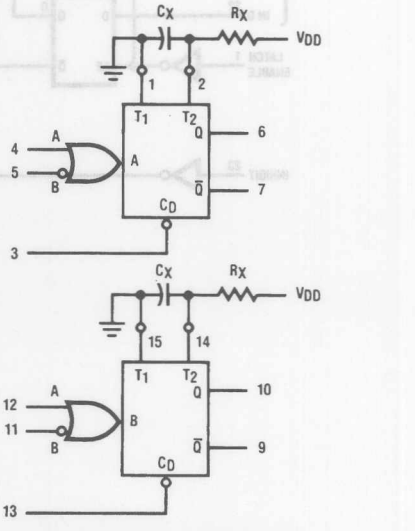


TOP VIEW

TL/F/5217–1

Order Number MM54HC4538* or MM74HC4538*

*Please look into Section 8, Appendix D for availability of various package types.



RX AND CX ARE EXTERNAL COMPONENTS

TL/F/5217–2

Note: Pin 1 and Pin 15 must be hard-wired to GND.

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to Vcc+1.5V
DC Output Voltage (V_{OUT})	−0.5 to Vcc+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Reset only)			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL}						
		$\|I_{OUT}\| \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
I_{IN}	Maximum Input Current (Pins 2, 14) (Note 6)	$V_{IN} = V_{CC}$ or GND	6.0V	±0.1	±1.0	±1.0	μA
I_{IN}	Maximum Input Current (all other pins)	$V_{IN} = V_{CC}$ or GND	6.0V	±0.1	±1.0	±1.0	μA
I_{CC} Active	Maximum Active Supply Current	Pins 2, 14 = 0.5 V_{CC} Q1, Q2 = High $V_{IN} = V_{CC}$ or GND	6.0V	150	250	400	μA
I_{CC} Quiescent	Maximum Quiescent Supply Current	Pins 2, 14 = OPEN Q1, Q2 = Low $V_{IN} = V_{CC}$ or GND	6.0V	130	220	350	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Note 6: The device must be set up with 3 steps **before** measuring I_{IN}:

	Clear	A	B
1.	H	L	H
2.	H	H	H
3.	H	L	H

** V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Propagation Delay A, or B to Q		23	45	ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$		26	50	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		23	45	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		26	50	ns
t_W	Minimum Pulse Width A, B or Clear		10	16	ns

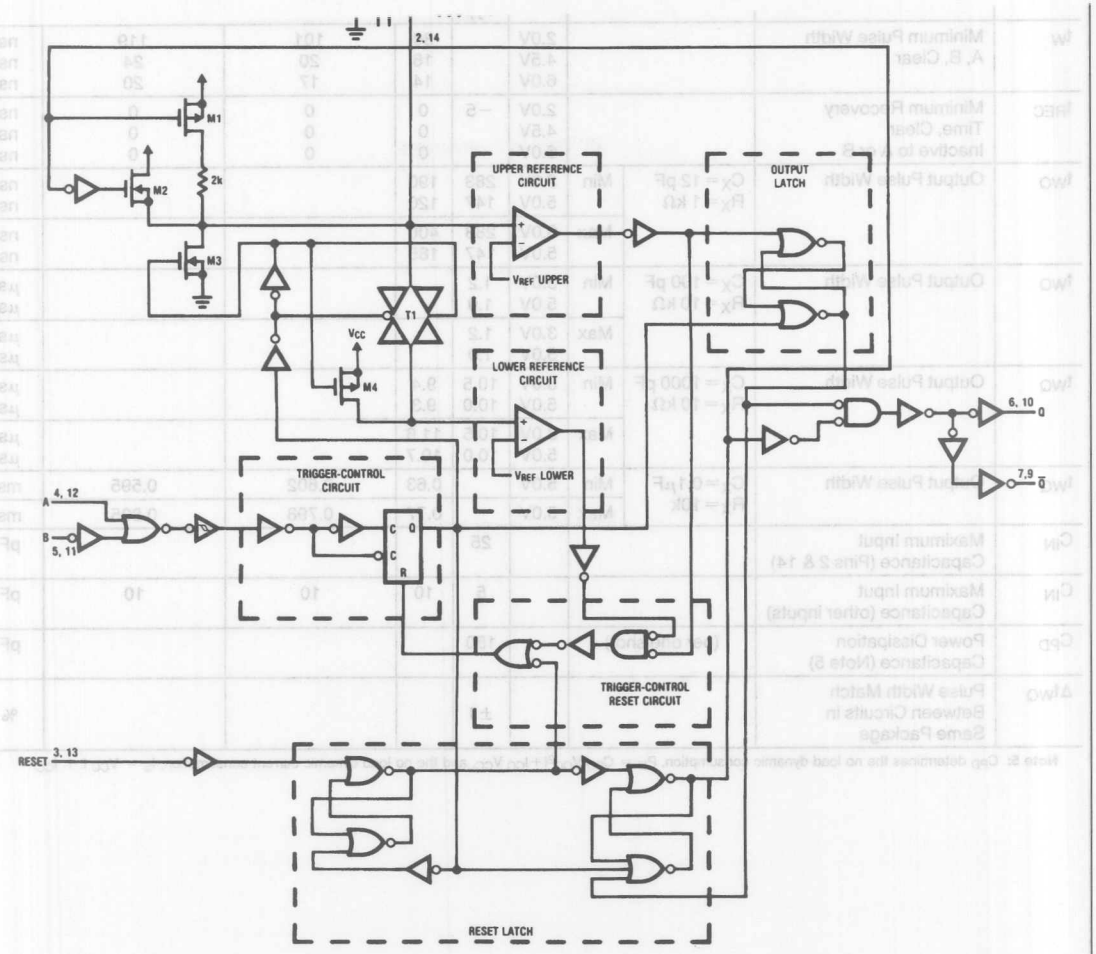
AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay A, or B to Q		2.0V 4.5V 6.0V	100 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$		2.0V 4.5V 6.0V	110 28 23	275 55 47	347 69 59	410 82 70	ns ns ns
t_{PHL}	Maximum Propagation Delay Clear to Q		2.0V 4.5V 6.0V	100 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		2.0V 4.5V 6.0V	110 28 23	275 55 47	347 69 59	410 82 70	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 10 8	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time (Reset only)		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns

AC Electrical Characteristics $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified) (Continued)

Symbol	Parameter	Conditions		V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_W	Minimum Pulse Width A, B, Clear			2.0V		80	101	119	ns
				4.5V		16	20	24	ns
				6.0V		14	17	20	ns
t_{REC}	Minimum Recovery Time, Clear Inactive to A or B			2.0V	−5	0	0	0	ns
				4.5V		0	0	0	ns
				6.0V		0	0	0	ns
t_{WQ}	Output Pulse Width	$C_X = 12$ pF $R_X = 1$ kΩ	Min	3.0V	283	190			ns
				5.0V	147	120			ns
			Max	3.0V	283	400			ns
				5.0V	147	185			ns
t_{WQ}	Output Pulse Width	$C_X = 100$ pF $R_X = 10$ kΩ	Min	3.0V	1.2				μs
				5.0V	1.0				μs
			Max	3.0V	1.2				μs
				5.0V	1.0				μs
t_{WQ}	Output Pulse Width	$C_X = 1000$ pF $R_X = 10$ kΩ	Min	3.0V	10.5	9.4			μs
				5.0V	10.0	9.3			μs
			Max	3.0V	10.5	11.6			μs
				5.0V	10.0	10.7			μs
t_{WQ}	Output Pulse Width	$C_X = 0.1$ μF $R_X = 10$k	Min	5.0V		0.63	0.602	0.595	ms
			Max	5.0V		0.77	0.798	0.805	ms
C_{IN}	Maximum Input Capacitance (Pins 2 & 14)				25				pF
C_{IN}	Maximum Input Capacitance (other inputs)				5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per one shot)			150				pF
Δt_{WQ}	Pulse Width Match Between Circuits in Same Package				±1				%

Note 5: C_{PD} determines the no load dynamic consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = V_{CC} f + I_{CC}$.



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Circuit Operation

The 'HC4538 operates as follows (refer to logic diagram). In the quiescent state, the external timing capacitor, C_X, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{REF} Lower = ⅓ V_{CC}). C_X then charges, through R_X, back up to the upper reference voltage (V_{REF} Upper = ⅔ V_{CC}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic diagram and the timing diagram.

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in logic diagram).

Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, timing diagram).

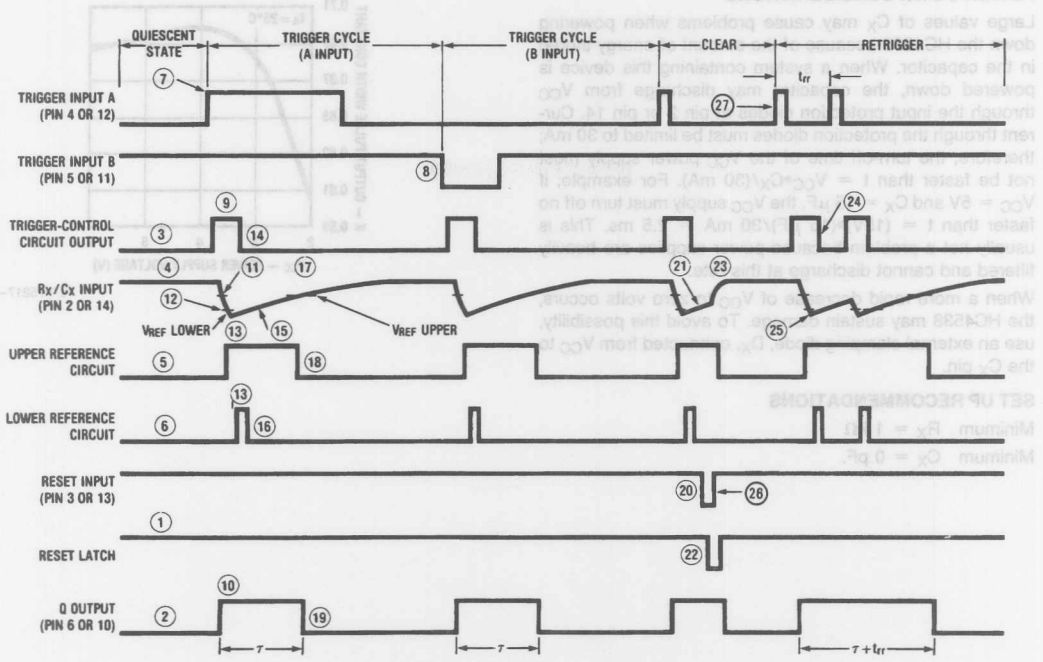
The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{CC} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{CC} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The 'HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Truth Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

Timing Diagram



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Circuit Operation (Continued)

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the 'HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator.) Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 'HC4538 to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the 'HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

Recovery time is the required delay after reset goes inactive to a new trigger rising edge. On the diagram it is shown as (#26) to (#27).

RETRIGGER OPERATION

In the retriggerable mode, the 'HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

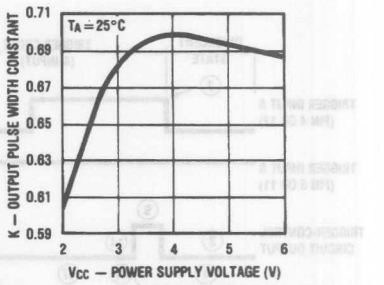
$$t_{rr}(ns) \cong 72 + \frac{V_{CC}(volts) \bullet C_X(pF)}{30.5}, \text{ at room temperature}$$

Circuit Operation (Continued)

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \bullet C_X/(30\ mA)$. For example, if $V_{CC} = 5V$ and $C_X = 15\ \mu F$, the V_{CC} supply must turn off no faster than $t = (15V) \bullet (15\ \mu F)/30\ mA = 2.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected from V_{CC} to the C_X pin.



TL/F/5217–5

SET UP RECOMMENDATIONS

Minimum $R_X = 1\ k\Omega$

Minimum $C_X = 0$ pF.

National Semiconductor

MM54HC4543/MM74HC4543 BCD-to-7 Segment Latch/Decoder/Driver for Liquid Crystal Displays

General Description

The MM54HC4543/MM74HC4543 BCD-to-7 segment latch/decoder/driver utilize advanced silicon-gate CMOS technology, and can be used either as a high speed decoder or as a display driver. This circuit contains a 4-bit latch, BCD-to-7 segment decoder, and 7 output drivers. Data on the input pins flow through to the output when the LATCH ENABLE (LE) is high and is latched on the high to low transition of the LE input. The PHASE input (PH) controls the polarity of the 7 segment outputs. When PH is low the outputs are true 7 segment, and when PH is high the outputs are inverted 7 segment. When the PHASE input is driven by a liquid crystal display (LCD) backplane waveform the segment pins output the correct segment waveform for proper LCD AC drive voltages.

In addition a BLANKING INPUT (BI) is provided, which will blank the display.

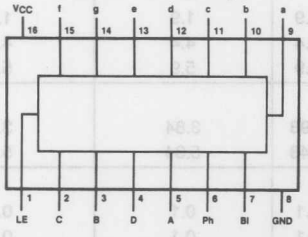
The MM54HC4543/MM74HC4543 are functionally and pin-out equivalent to the CD4543BC/CD4543BM and the MC14543BA/MC14543BC. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 60 ns
- Supply voltage range: 2–6V
- Maximum input current: 1 μA
- Maximum quiescent supply current: 80 μA (74HC)
- Display blanking
- Low dynamic power consumption

Connection Diagram

Dual-In-Line Package



TL/F/5128–1

Top View

Order Number MM54HC4543* or MM74HC4543*

*Please look into Section 8, Appendix D for availability of various package types.

Display Format



TL/F/5128–2

Truth Table

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

X — don't care

† = same as above combinations

* = for liquid crystal readouts, apply a square wave to Ph.

** = depends upon the BCD code previously applied when LE—H

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 0.4$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 0.52$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 0.4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 0.52$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, BI, Ph to Output		60	100	ns
t_s	Minimum Setup Time LE to Data			20	ns
t_H	Minimum Hold Time Data to LE			10	ns
t_W	Minimum LE Pulse Width			16	ns

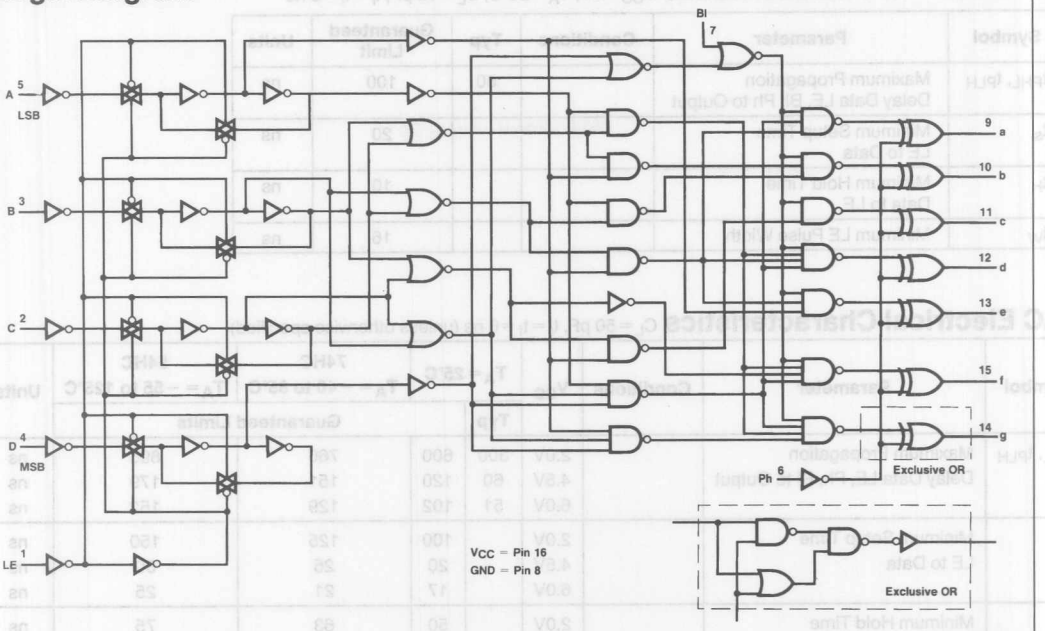
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, Ph, BI to Output		2.0V	300	600	760	895	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_s	Minimum Setup Time LE to Data		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data to LE		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_W	Minimum LE Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

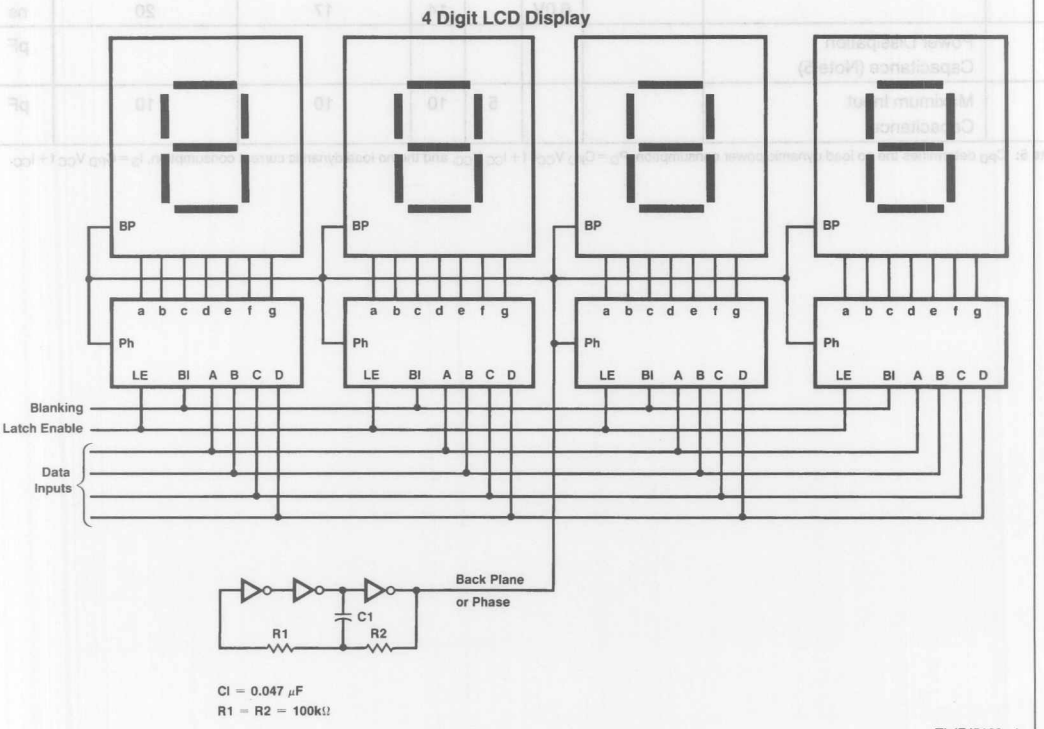
3

Logic Diagram



TL/F/5128–3

Typical Applications



TL/F/5128–4

National Semiconductor

MM54HC7266/MM74HC7266 Quad 2-Input Exclusive NOR Gate

General Description

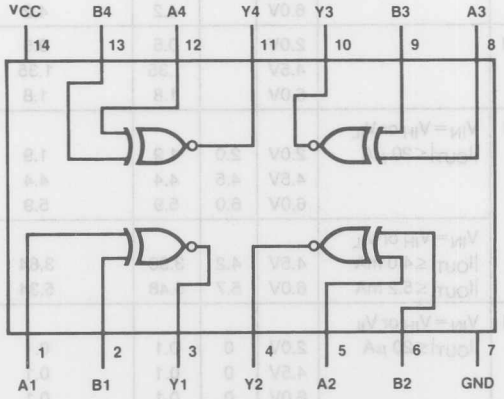
This exclusive NOR gate utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/MM74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. However, unlike the 'LS266, which is an open collector gate, the 'HC266 has standard CMOS push-pull outputs. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads
- Push-pull output

Connection Diagram

Dual-In-Line Package



TL/F/8437–1

Top View

Order Number MM54HC7266* or MM74HC7266*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40°C to 85°C	54HC T_A = −55°C to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage**		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**V_{IL} limits are currently tested at 20% of V_{CC}. The above V_{IL} specification (30% of V_{CC}) will be implemented no later than Q1, CY'89.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40°C$ to 85°C	54HC $T_A=-55°C$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

MM74HC942 300 Baud Modem

General Description

The MM74HC942 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC942 utilizes advanced silicon-gate CMOS technology. Switched capacitor techniques are used to perform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two-to-four-wire conversion and drive the line at a maximum of 0 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

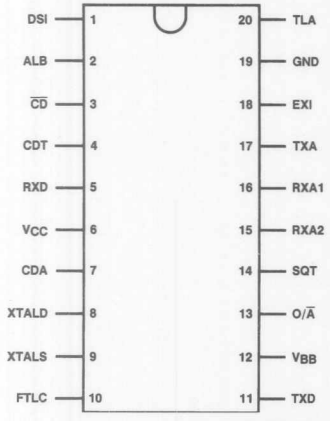
- Drives 600Ω at 0 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- ±5V supplies
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signalling systems
- Remote process control

Connection and Block Diagrams

Dual-In-Line Package

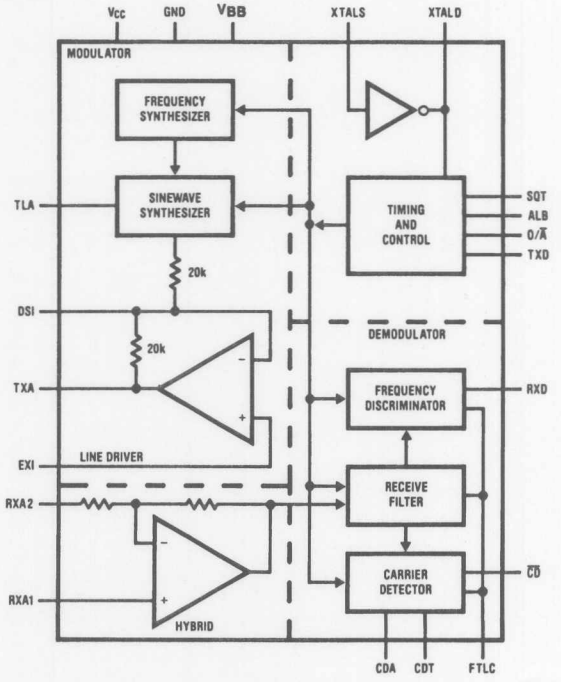


TL/F/5348–1

Top View

Order Number MM54HC942* or MM74HC942*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5348–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
Supply Voltage (V_{BB})	+0.5 to −7.0V
DC Input Voltage (V_{IN})	V_{BB} −1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	V_{BB} −0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Supply Voltage (V_{BB})	−4.5	−5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics

Symbol	Parameter	Conditions	T = 25°C	74HC T = −40 to 85°C		Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}				
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		3.98	3.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}				
		$\|I_{OUT}\|$ = 20 μA		0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		0.26	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	μA
I_{OZ}	Output TRI-STATE® Leakage Current RXD and $\overline{CD}$ Outputs	ALB = SQT = V_{CC}			±5	μA
I_{CC}, I_{BB}	Maximum Quiescent Supply Current	V_{IH} = V_{CC}, V_{IL} = GND ALB or SQT = GND Transmit Level = −9 dBm	8.0	12.0	12.0	mA
I_{CC}, I_{BB}	Power Down Supply Current	ALB = SQT = V_{CC} V_{IH} = V_{CC}, V_{IL} = GND			300	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

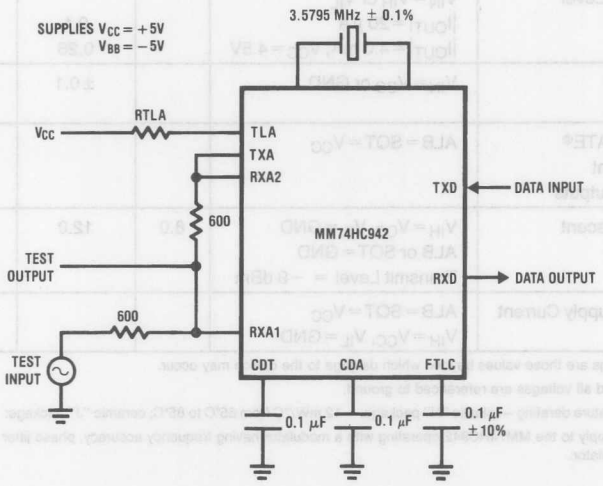
*The demodulator specifications apply to the MM74HC942 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC942 modulator.

AC Electrical Characteristics

Unless otherwise specified, all specifications apply to the MM74HC942 over the range −40°C to +85°C using a V_{CC} = +5V ±10%, a V_{BB} = −5V ±10% and a 3.579MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error					4	Hz
	Power Output	V_{CC} = 5.0V	R_{TLA} = 0Ω	−3	−1.5	0	dBm
		R_L = 1.2 kΩ	R_{TLA} = 5.49 kΩ	−12	−10.5	−9	dBm
	2nd Harmonic Energy		R_{TLA} = 0Ω		−62	−56	dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			5	10	50	kΩ
	Adjacent Channel Rejection	RXA2 = GND TXA = GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−9	dBm
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100	200	μS
	Bit Bias	Alternating 1-0 Pattern			5	10	%
	Carrier Detect Trip Points	CDA = 1.2V	Off to On	−45	−42	−40	dBm
		V_{CC} = 5.0V	On to Off	−47	−45	−42	dBm
	Carrier Detect Hysteresis	V_{CC} = 5V		2	3	4	dB

AC Specification Circuit



TL/F/5348–3

Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system, XTALD can be driven.
9	XTALS	Crystal Sense: Refer to Pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receive filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	V_{BB}	Negative Supply: The recommended supply is −5V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded.
19	GND	Ground: This defines the chip 0V.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC942 uses frequency shift keying (FSK) of an audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC942 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC942 is capable of transmitting and receiving data simultaneously.

The tone allocation by the MM74HC942 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I. BELL 103 Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switched capacitor nine-pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60 Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques. The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter. The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source impedances.

The transmit level is programmable by placing a resistor from TLA to VCC. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC942 will interface to most telephones. This arrangement is called the "permissive arrangement." The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

SNR can be maximized by adjusting the transmit level until the level at the exchange reaches −12 dBm. This must be done with the cooperation of the telephone company. The programming resistor used is specific for a given installation and is often included in the telephone jack at the installation. The modem is thus programmable and can be used with any jack correctly wired. This arrangement is called the universal registered jack arrangement and is possible with the MM74HC942. The values of resistors required to program the MM74HC942 follow the most common code in use; the universal service order code. The required resistors are given in Table II.

TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ohms)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490
4	−8	3,610
5	−7	2,520
6	−6	1,780
7	−5	1,240
8	−4	866
9	−3	562
10	−2	336
11	−1	150
12	0	0

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used;

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on Pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$T_{\overline{CDL}} \cong 6.4 \times C_{CDT}$ for $\overline{CD}$ going low

$T_{\overline{CDH}} \cong 0.54 \times C_{CDT}$ for $\overline{CD}$ going high

Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

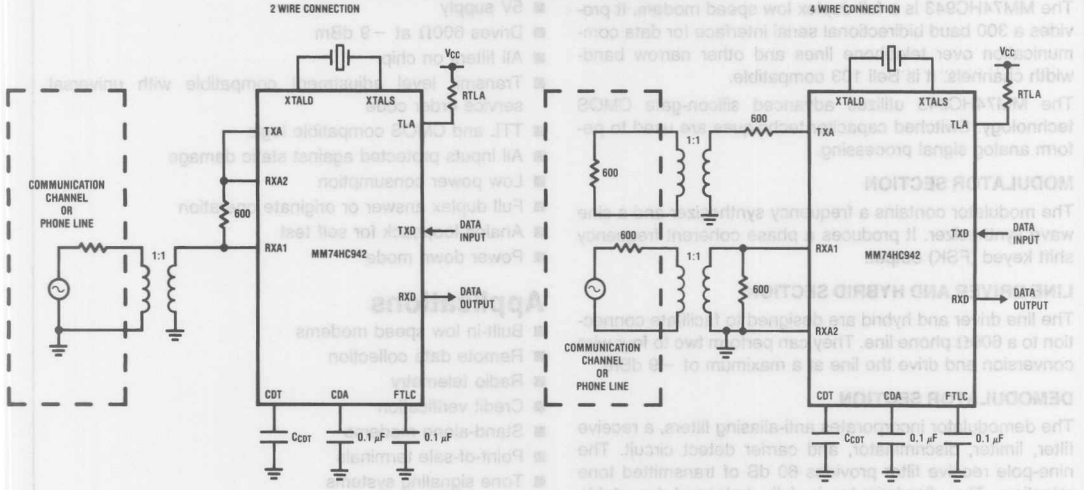
Applications Information (Continued)

DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC942 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

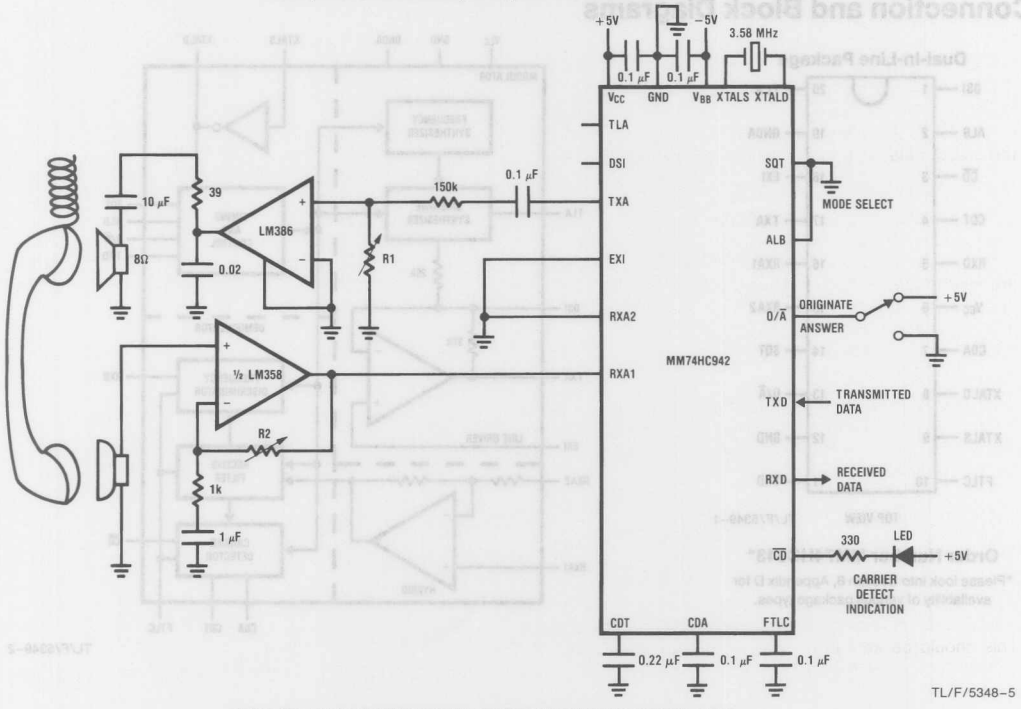
Interface Circuits for MM74HC942 300 Baud Modem



TL/F/5348–4

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



TL/F/5348–5

Note: The efficiency of the acoustic coupling will set the valves of R1 and R2.

National Semiconductor

PRELIMINARY

MM74HC943 300 Baud Modem

General Description

The MM74HC943 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC943 utilizes advanced silicon-gate CMOS technology. Switched capacitor techniques are used to peform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two to four wire conversion and drive the line at a maximum of −9 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine-pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

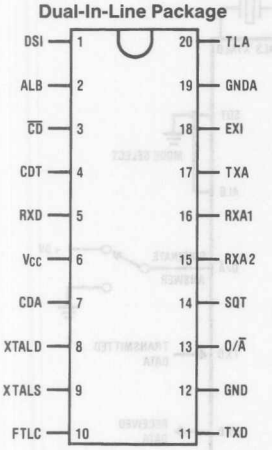
- 5V supply
- Drives 600Ω at −9 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signaling systems
- Remote process control

Connection and Block Diagrams

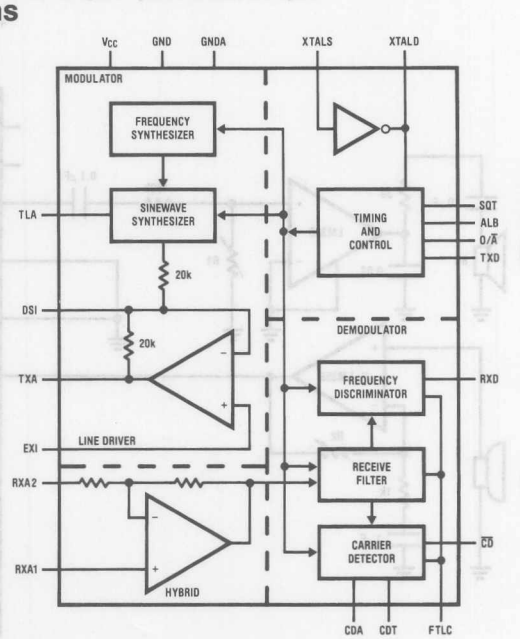
Dual-In-Line Package



TOP VIEW TL/F/5349–1

Order Number MM74HC943*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5349–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HC T_A = −40 to 85°C		Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	V_{CC} −0.05	V_{CC} −0.1 3.84	V_{CC} −0.1 3.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		0.1 0.33	0.1 0.4	V V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	μA
I_{OZ}	Output TRI-STATE® Leakage Current, RXD and $\overline{CD}$ Outputs	ALB = SQT = V_{CC}			±5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IH} = V_{CC}, V_{IL} = GND ALB or SQT = GND Transmit Level = −9 dBm	8.0	10.0	10.0	mA
I_{GNDA}	Analog Ground Current		1.0	2.0	2.0	mA
I_{CC}	Power Down Supply Current	ALB = SQT = V_{CC} V_{IH} = V_{CC}, V_{IL} = GND			300	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

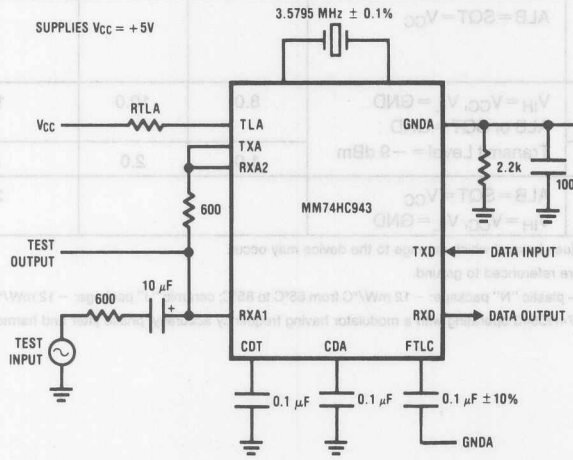
*The demodulator specifications apply to the MM74HC943 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC943 modulator.

AC Electrical Characteristics

Unless otherwise specified, all specifications apply to the MM74HC943 over the range −40°C to +85°C using a V_{CC} of +5V ±10%, and a 3.579 MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error					4	Hz
	Power Output	V_{CC} = 5.0V R_L = 1.2 kΩ	R_{TLA} = 5490Ω	−12	−10.5	−9	dBm
	2nd Harmonic Energy		R_{TLA} = 5490Ω		−62	−56	dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			5	10	50	kΩ
	Adjacent Channel Rejection	RXA2 = GNDA, TXD = GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−12	dBm
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100	200	μS
	Bit Bias	Alternating 1–0 Pattern			5	10	%
	Carrier Detect Trip Points	CDA = 1.2V	Off to On	−45	−42	−40	dBm
		V_{CC} = 5.0V	On to Off	−47	−45	−42	dBm
	Carrier Detect Hystereisis	V_{CC} = 5.0V		2	3	4	dB

AC Specification Circuit



TL/F/5349–3

Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This input may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system. XTALD can be driven.
9	XTALS	Crystal Sense: Refer to pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receiver filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	GND	Ground: This defines the chip 0V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded to GNDA.
19	GNDA	Analog Ground: Analog signals within the chip are referred to this pin.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC943 uses frequency shift keying (FSK) of audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC943 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC943 is capable of transmitting and receiving data simultaneously.

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TABLE I. Bell 103 Tone Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switch capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency synthesizer produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter.

The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source inpedances.

The transmit level is programmable by placing a resistor from TLA to V_{CC}. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC943 will interface to most telephones. This arrangement is called the "permissive arrangement." The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ω)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used:

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on Pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$$T_{\overline{CDL}} \cong 6.4 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going low}$$

$$T_{\overline{CDH}} \cong 0.54 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going high}$$

Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

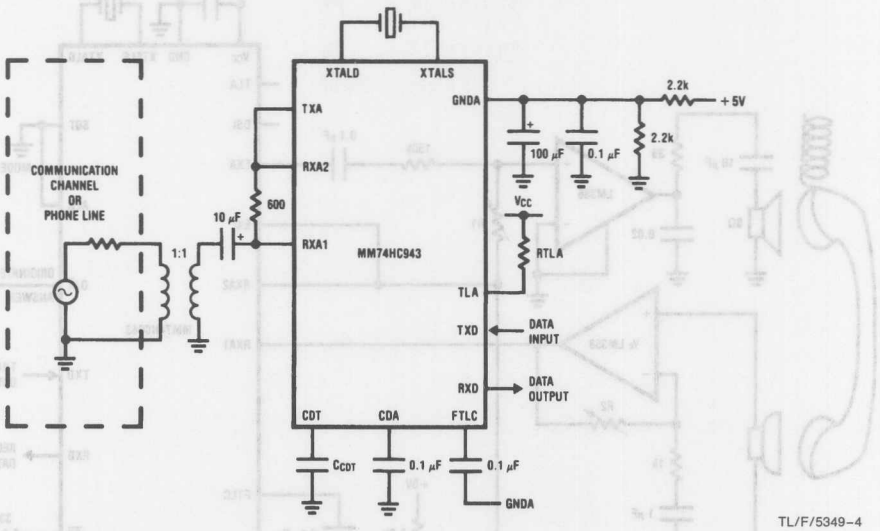
DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC943 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

Applications Information (Continued)

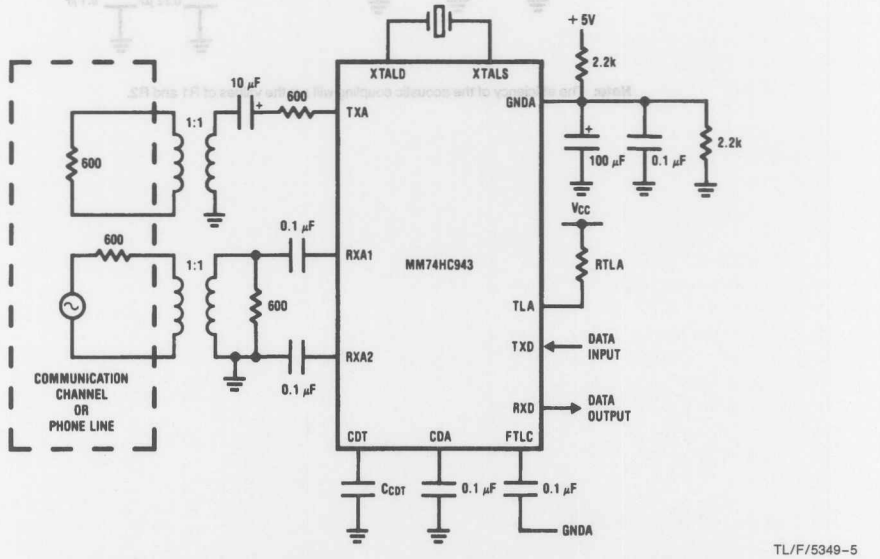
Interface Circuits for MM74HC943 300 Baud Modem

2 Wire Connection



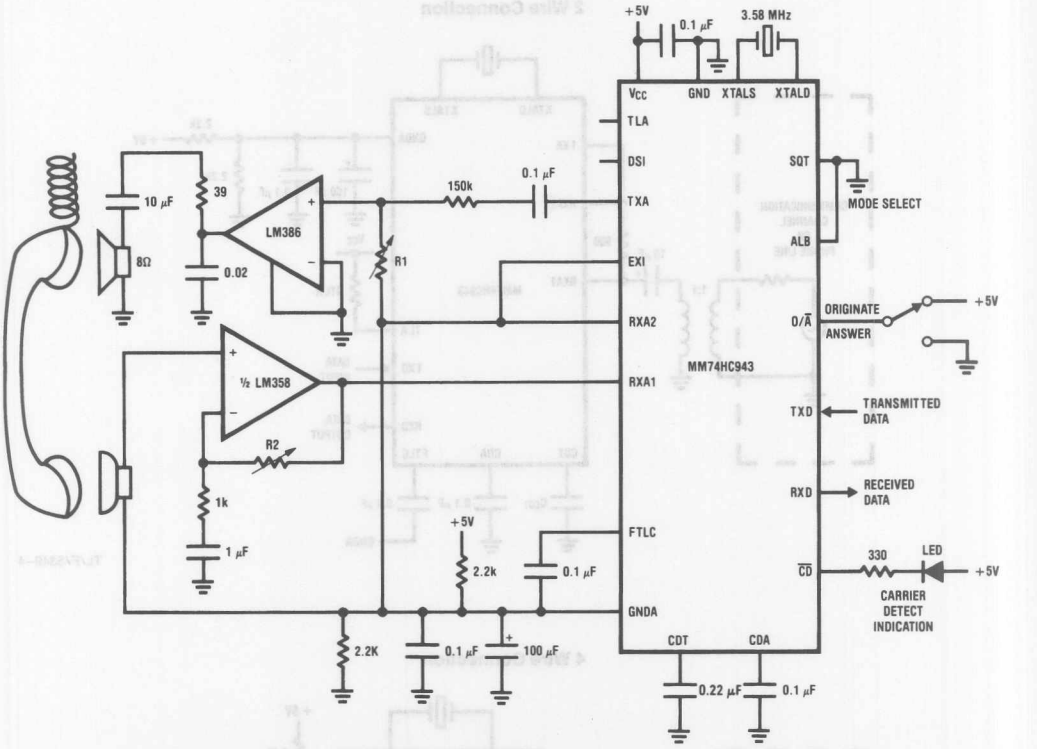
TL/F/5349–4

4 Wire Connection



TL/F/5349–5

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.



TL/F/5349–6

Note: The efficiency of the acoustic coupling will set the values of R1 and R2.

Section 4
MM54HCT/MM74HCT

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National Semiconductor

MM54HCT00/MM74HCT00 Quad 2 Input NAND Gate

General Description

The MM54HCT00/MM74HCT00 are NAND gates fabricated using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pin-out compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

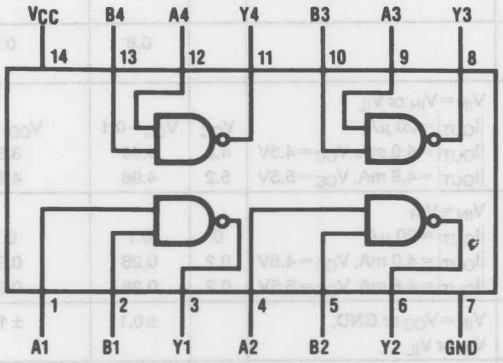
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 14 ns (typ)
- Low power: 10 μW at DC
- High fan out, 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



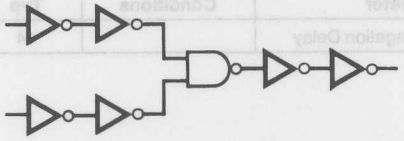
TL/F/5356–1

Top View

Order Number MM54HCT00* or MM74HCT00*

*Please look into Section 8, Appendix D for availability of various package types.

(1 of 4 gates)



TL/F/5356–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)	0.18	0.3	0.4	0.5	mA

AC Electrical Characteristics V_{CC}=5.0V, t_r=t_f=6 ns, C_L=15 pF, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	18	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns, $C_L = 50$ pF (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$		54HCT $T_A = -55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		18	23	29	35	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	30				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

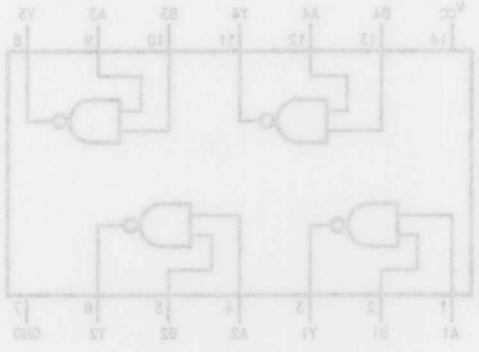
Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

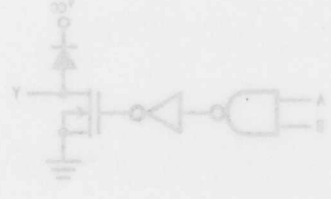
Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.





National Semiconductor

MM54HCT03/MM74HCT03
Quad 2-Input NAND Gate (Open Drain)

General Description

The MM54HCT03/MM74HCT03 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

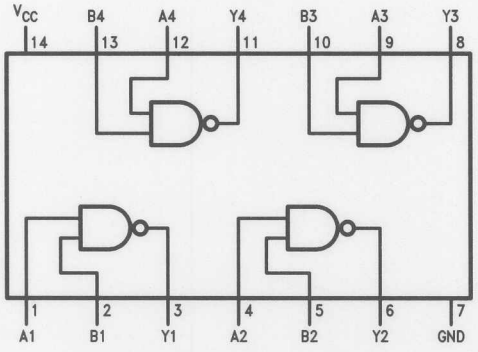
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 12 ns (typ)
- Low power: 10 μW at DC
- High fan-out, 10 LS-TTL loads

Connection and Logic Diagrams

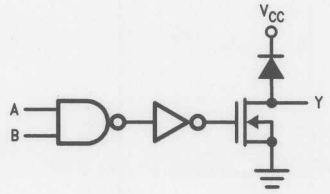
Dual-In-Line Package



TL/F/9395–1

Order Number MM54HCT03* or MM74HCT03*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/9395–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC}		0.5	5.0	10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package; −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

t_{PLZ}	Maximum Propagation Delay	R_L = 1 kΩ	10		ns

AC Electrical Characteristics V_{CC} = 5.0V ±10%, C_L = 50 pF, t_r = t_f = 6 ns, unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
t_{PZL}	Maximum Propagation Delay	R_L = 1 kΩ	10	20	25	30	ns
t_{PLZ}	Maximum Propagation Delay	R_L = 1 kΩ	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) R_L = ∞		14			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HCT04/MM74HCT04 Hex Inverter

General Description

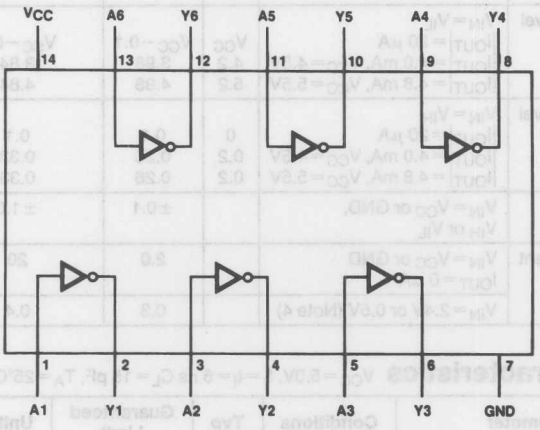
The MM54HCT04/MM74HCT04 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS - low quiescent power and wide power supply range. These devices are input and output characteristic as well as pin-out compatible with standard DM54LS/74LS logic families. The MM54HCT04/MM74HCT04, triple buffered, hex inverters, feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 12 ns (typ)
- Low power: 10 μW at DC, 3.7 mW at 5 MHz
- High fanout: ≥ 10 LS loads
- Inverting, triple buffered

Connection Diagram



TL/F/5357–1

Top View

Order Number MM54HCT04* or MM74HCT04*

*Please look into Section 8, Appendix D for availability of various package types.

4

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

AC Electrical Characteristics V_{CC} = 5.0V, t_r = t_f = 6 ns C_L = 15 pF, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics V_{CC} = 5.0V ±10%, t_r = t_f = 6 ns, C_L = 50 pF (unless otherwise noted)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C		54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HCT05/MM74HCT05 Hex Inverter (Open Drain)

General Description

The MM54HCT05/MM74HCT05 are logic functions fabricated by using advanced silicon-gate CMOS technology, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are also input and output characteristic and pinout compatible with standard DM54LS/DM74LS logic families. The MM54HCT05/MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

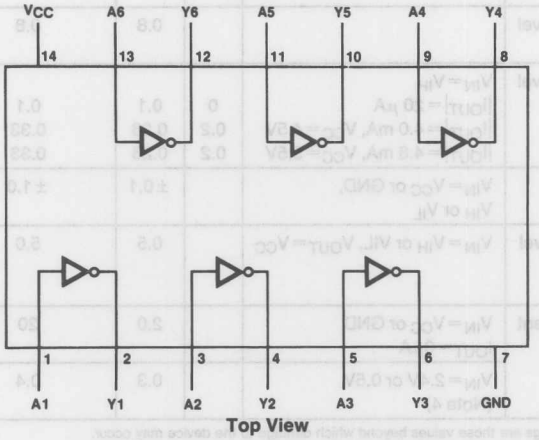
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fanout of 10 LS-TTL loads
- Typical propagation delays:
  t_{PLH} (with 1 kΩ resistor) 10 ns
  t_{PHL} (with 1 kΩ resistor) 8 ns

Connection Diagram

Dual-In-Line Package



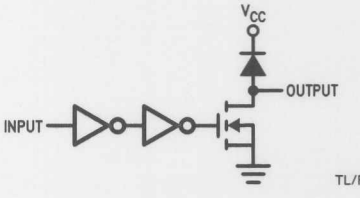
TL/F/5358–1

Top View

Order Number MM54HCT05* or MM74HCT05*

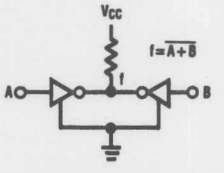
*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



TL/F/5358–2

Typical Application



TL/F/5358–3

Note: Can be extended to more than 2 inputs.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC} = 5V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN} = V_{IH} or VIL, V_{OUT} = V_{CC}		0.5	5.0	10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

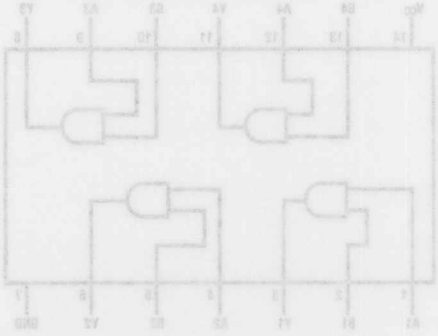
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns unless otherwise noted.

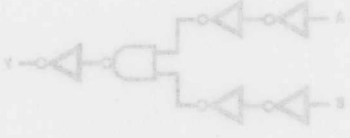
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PZL}	Maximum Propagation Delay	$R_L=1\ k\Omega$	8	15	ns
t_{PLZ}	Maximum Propagation Delay	$R_L=1\ k\Omega$	9	16	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits		
t_{PZL}	Maximum Propagation Delay	$R_L=1\ k\Omega$	10	22	28	33	ns
t_{PLZ}	Maximum Propagation Delay	$R_L=1\ k\Omega$	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) $R_L=\infty$		20			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.





National Semiconductor

MM54HCT08/MM74HCT08 Quad 2-Input AND Gate

General Description

The MM54HCT08/MM74HCT08 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

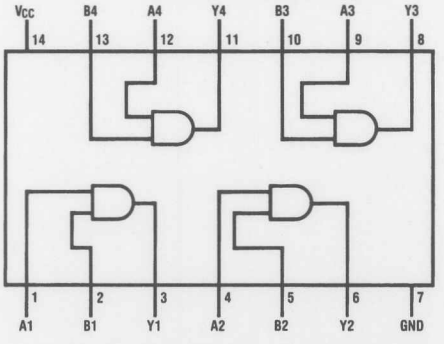
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 12 ns (typ)
- Low power: 10 μW at DC
- High fan-out, 10 LS-TTL loads

Connection and Logic Diagrams

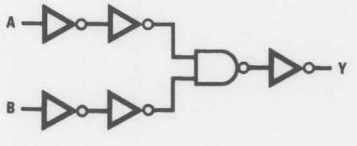
Dual-In-Line Package



TL/F/5754–1

Order Number MM54HCT08* or MM74HCT08*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5754–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package −12 mW/°C from 65°C to 85°C: ceramic "J" package 12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		9	15	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$		54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		11	18	23	27	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		7	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	38				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption. $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$ and the no load dynamic current consumption. $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

MM54HCT32/MM74HCT32 Quad 2-Input OR Gate

General Description

The MM54HCT32/MM74HCT32 are logic functions fabricated by using advanced silicon-gate CMOS technology, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pin-out compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

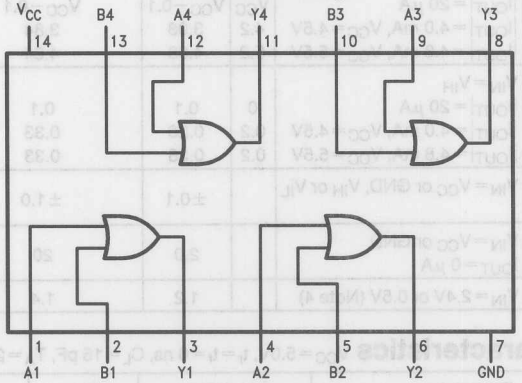
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 10 ns (typ)
- Low power: 10 μW at DC
- High fan-out, 10 LS-TTL loads

Connection and Logic Diagrams

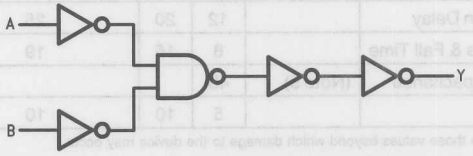
Dual-In-Line Package



TL/F/9396–1

Order Number MM54HCT32* or MM74HCT32*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/9396–2

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.2	1.4	1.5	mA

AC Electrical Characteristics V_{CC} = 5.0V, t_r = t_f = 6 ns, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10		ns

AC Electrical Characteristics V_{CC} = 5.0V ±10%, t_r = t_f = 6 ns, C_L = 50 pF (unless otherwise noted)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay		12	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	48				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HCT34/MM74HCT34 Non-Inverter

General Description

The MM54HCT34/74HCT34 are logic functions fabricated by using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS - low quiescent power and wide power supply range. These devices are input and output characteristic as well as pin-out compatible with standard DM54LS/74LS logic families. The MM54HCT34/MM74HCT34 feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

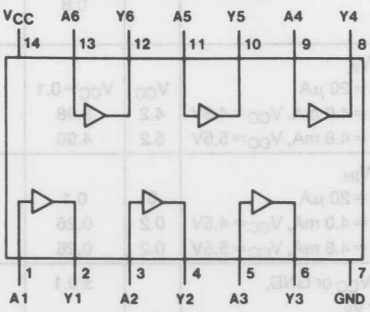
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 10 ns (typ)
- Low power: 10 μW at DC, 3.7 mW at 5 MHz
- High fanout: 10 LS loads

Connection Diagram

Dual-In-Line Package



TL/F/5359–1

Top View

Order Number MM54HCT34* or MM74HCT34*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$ (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	20	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	22	29	33	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	30				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

National Semiconductor

MM54HCT74/MM74HCT74
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HCT74/MM74HCT74 utilizes advanced silicon-gate CMOS technology to achieve operation speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

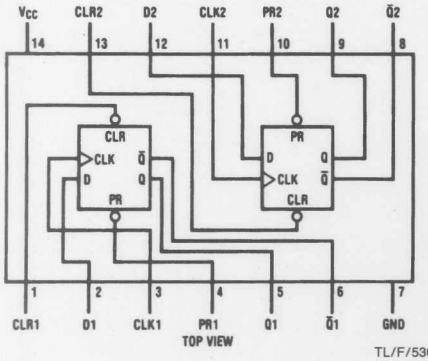
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Meta-stable hardened

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5360–1

Order Number MM54HCT74* or MM74HCT74*

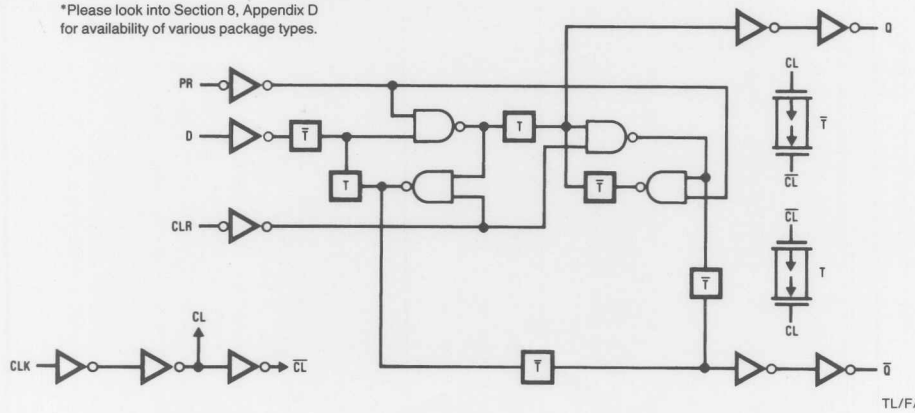
*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



TL/F/5360–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND					
		I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per pin. All other inputs are held at V_{CC} Ground.

f_{MAX}	Maximum Operating Frequency from Clock to Q or $\overline{Q}$		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Setup Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$	54HCT $T_A = -55$ to $125°C$	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		21	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		21	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		9	16	20	24	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)	10				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HCT76/MM74HCT76/ MM54HCT112/MM74HCT112 Dual J-K Flip-Flops with Preset and Clear

General Description

These flip-flops utilize advanced silicon-gate CMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These flip-flops have independent J, K, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The flip-flops are edge-triggered and change state on the negative-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

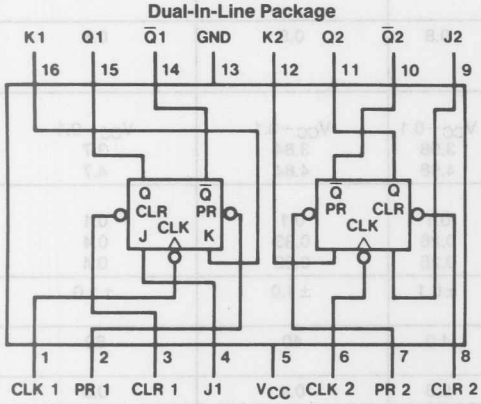
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

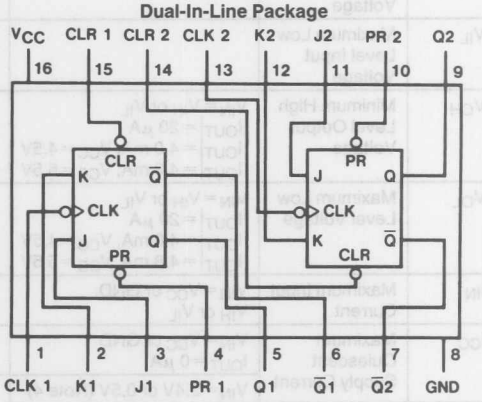
Connection Diagram

'HCT76
Dual-In-Line Package



TL/F/5762–1

'HCT112
Dual-In-Line Package



TL/F/5762–3

Order Number MM54HCT76/T112* or MM74HCT76/T112*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

4

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V±10% unless otherwise specified

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40°C to 85°C	54HCT T_A=−55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	$V_{IN}=V_{IH}$ or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics V_{CC}=5V, T_A=25°C, C_L=15 pF, t_r=t_f=6 ns

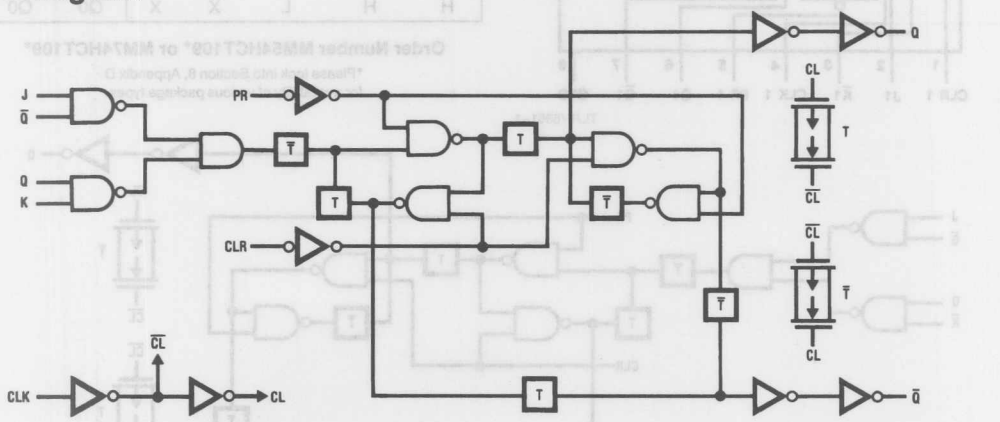
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set-Up Time J or K Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40°C$ to $85°C$	54HCT $T_A = -55°C$ to $125°C$	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Setup Time J or K to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)	35				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5762–2

National Semiconductor

MM54HCT109/MM74HCT109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These high speed J-$\overline{K}$ FLIP-FLOPS utilize advanced silicon-gate CMOS technology. They possess the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

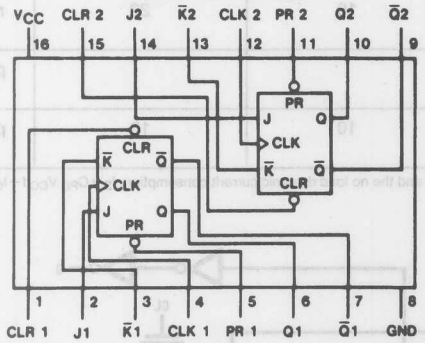
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HCT Series)
- Output drive capability: 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



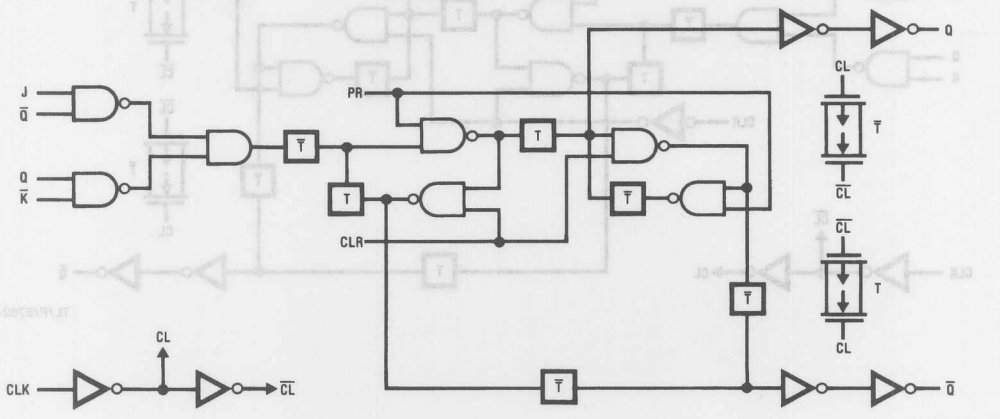
TL/F/5361–1

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

Order Number MM54HCT109* or MM74HCT109*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5361–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		4.0	40	80	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Setup Time J or $\overline{K}$ Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $V_{CC}=5.0V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40°$ to 85°C	54HCT $T_A=-55°$ to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Setup Time J or $\overline{K}$ to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)	35				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HCT138/MM74HCT138 3-to-8 Line Decoder

General Description

This decoder utilizes advanced silicon-gate CMOS technology, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM54HCT138/MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, G2A and G2B) are provided to ease the cascading decoders.

The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

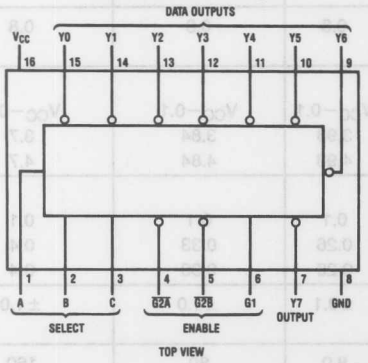
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

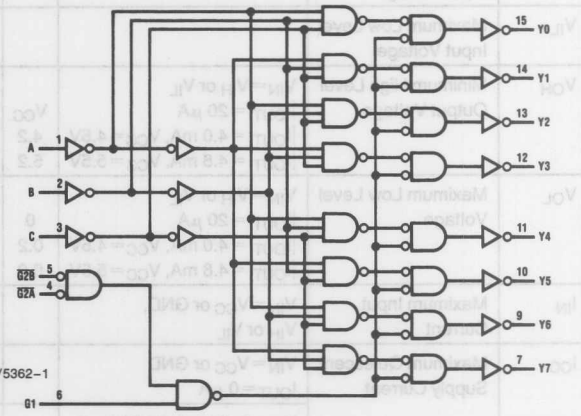


TL/F/5362–1

Order Number MM54HCT138* or MM74HCT138*

*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



TL/F/5362–2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2}$ = $\overline{G2A}$ + $\overline{G2B}$ H = high level L = low level X = don't care

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

(V_{IN}, V_{OUT})			
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input pin. All other inputs are held at V_{CC} or ground.

				Limit	
t_{PHL}	Maximum Propagation Delay, A, B, or C to Output		20	35	ns
t_{PLH}	Maximum Propagation Delay, A, B, or C to Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, G1 to Y Output		14	25	ns
t_{PLH}	Maximum Propagation Delay, G1 to Y Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		17	30	ns
t_{PLH}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		13	25	ns

AC Electrical Characteristics $V_{CC}=5V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$		54HCT $T=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay A, B, or C to Output		24	40	50	60	ns
t_{PLH}	Maximum Propagation Delay A, B, or C to Output		18	30	38	45	ns
t_{PHL}	Maximum Propagation Delay G1 to Y Output		17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay G1 to Y Output		20	30	38	45	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		23	35	43	52	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{IN}	Input Capacitance			5	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)	55				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HCT139/MM74HCT139 Dual 2-To-4 Line Decoder

General Description

The MM54HCT139/MM74HCT139 is a high speed silicon-gate CMOS decoder that is well suited to memory address decoding or data routing applications. It possesses an input threshold and output drive similar to LS-TTL and the low standby power of CMOS logic.

The device is comprised of two independent one-of-four decoders each with a single active low enable input (G1 or G2). Data on the select inputs (A1, B1 or A2, B2) cause one of the four normally high outputs to go low.

All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground. The device is capable of driving 10 low power Schottky TTL equivalent loads.

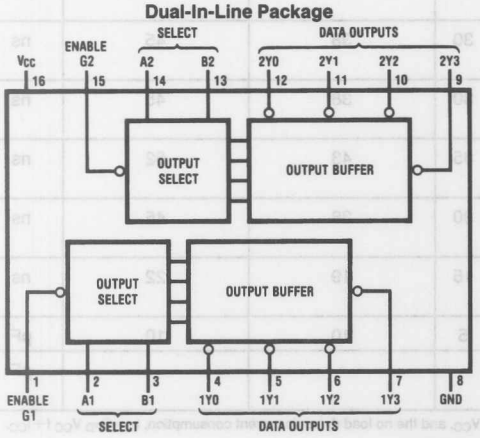
The MM54HCT139/MM74HCT139 is functionally and pin equivalent to the 54LS139/74LS139 and can be used as a plug-in replacement to reduce system power consumption in existing systems.

Features

- Typical propagation delays: 20 ns
- Low quiescent current: 40 μA maximum (74HCT Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5363–1

Top View
Order Number MM54HCT139* or MM74HCT139*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

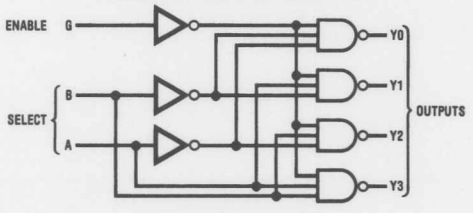
'HCT139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

MM54HCT139/MM74HCT139



TL/F/5363–2

(1 of 2 Gates)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	20 mA
DC Output Current, per Pin (I_{OUT})	25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	C
MM54HCT	−55	+125	C
Input Rise/Fall Time (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	Typ	Guaranteed Limits			Units
				T = 25°C	T = 25°C	74HCT T = −40 to 85°C	54HCT T = −55 to 125°C	
V_{IH}	Minimum High Level Input Voltage							V
					2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V
								V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA		V_{CC}	V_{CC} −.1	V_{CC} −.1	V_{CC} −.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V			3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V			4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA			0.10	0.10	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V			0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V			0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{IN} = V_{IH} or V_{IL}			±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA (Note 4)			4	40	80	μA
		V_{IN} = 2.4V or 0.5V I_{OUT} = 0 μA (Note 4)			0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs at V_{CC} or GND.

AC Electrical Characteristics (V_{CC}, temperature and loading of LS-TTL)

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Binary Select to any Output		18	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		18	30	ns

AC Electrical Characteristics

(Full range of V_{CC} and temperature) $V_{CC}=5V \pm 10\%$, $C_L=50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits			Units
			$T_A=25°C$	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Binary Select to any Output		20	35	44	51	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		21	35	44	51	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		9	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	Note 5	36				pF
C_{IN}	Minimum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=(C_{PD}\ V_{CC}{}^2)\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

National Semiconductor

PRELIMINARY

MM54HCT147/MM74HCT147 10-to-4 Line Priority Encoder

General Description

This priority encoder utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority encoder accepts 9 input request lines 1–9 and outputs 4 line BCD. The priority encoding ensures that only the highest order data line is encoded. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at low logic level.

All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

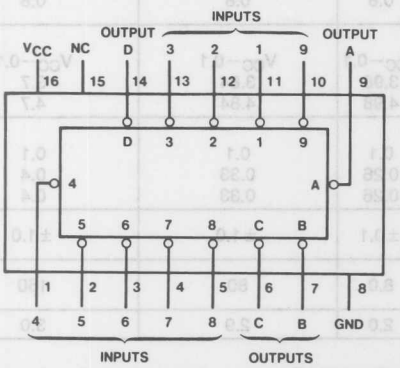
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power comsumption in existing designs.

Features

- Low quiescent power consumption: 40 μW maximum at 25°C
- High speed: 13 ns propagation delay (typical)
- Very low input current: 10^{-5} μA typical

Connection and Logic Diagrams

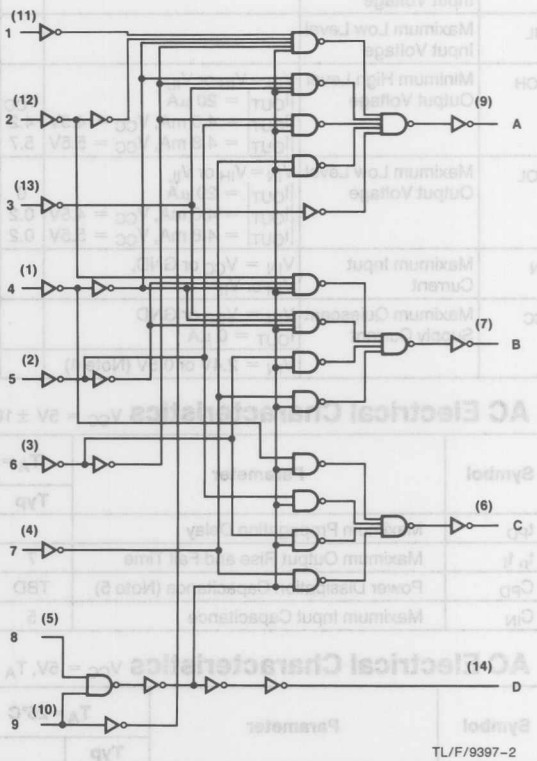
Dual-In-Line Package



TL/F/9397–1

Order Number MM54HCT147* or MM74HCT147*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/9397–2

Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±75 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		2.0	2.9	3.0	mA

AC Electrical Characteristics V_{CC} = 5V ±10%, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	T_A = 25°C	74HCT −40°C to +85°C	54HCT −55°C to +125°C	Units
		Typ	Guaranteed Limits		
t_{PD}	Maximum Propagation Delay		22	28	33	ns
t_r, t_f	Maximum Output Rise and Fall Time	7	11	14	17	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	TBD				pF
C_{IN}	Maximum Input Capacitance	5	10	10	10	pF

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameter	T_A = 25°C	74HCT −40°C to +85°C	54HCT −55°C to +125°C	Units
		Typ	Guaranteed Limits		
t_{PD}	Maximum Propagation Delay	11				ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

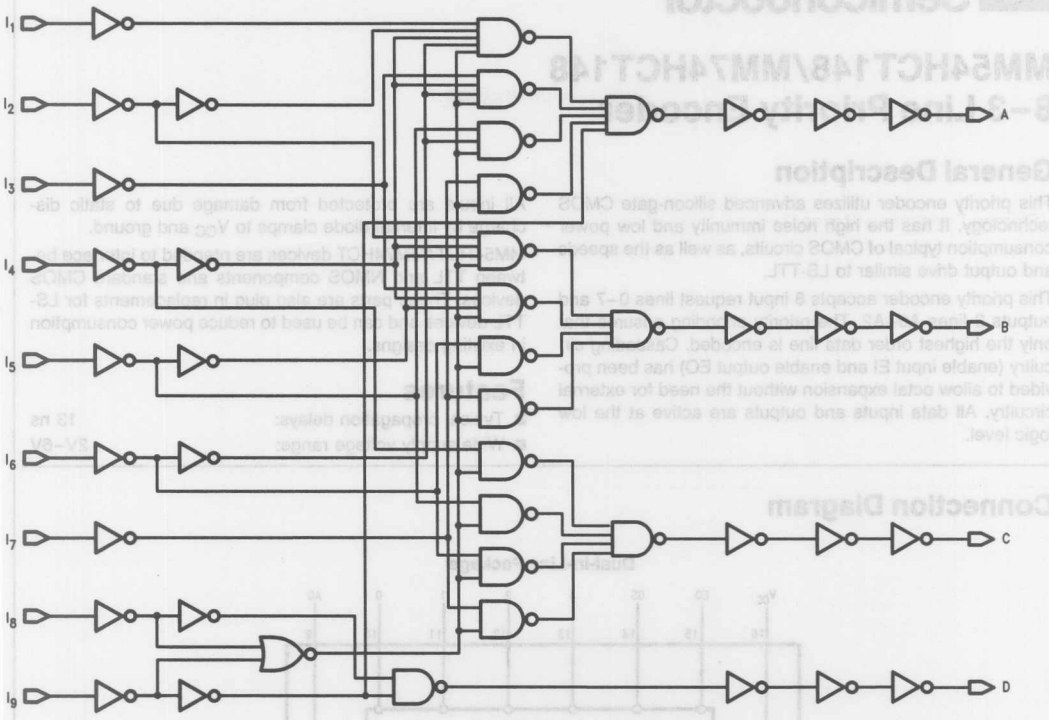
Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs held at V_{CC} or GND.

Note 5: C_{PD} determines the no load dynamic power consumption, and the no load dynamic current consumption.

Schematic Diagram



TL/F/9397–3

MM54HCT148/MM74HCT148
8–3 Line Priority Encoder

General Description

This priority encoder utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority encoder accepts 8 input request lines 0–7 and outputs 3 lines A0–A2. The priority encoding ensures that only the highest order data line is encoded. Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. All data inputs and outputs are active at the low logic level.

All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

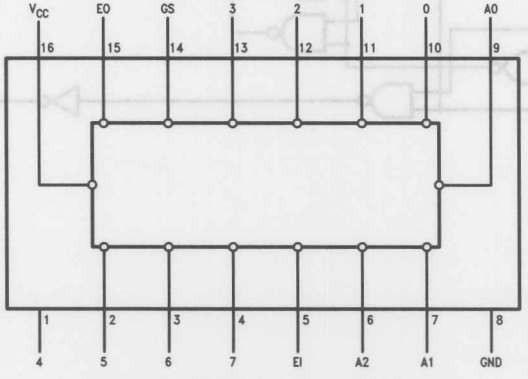
MM54HCT/MM74HCT devices are ntended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delays: 13 ns
- Wide supply voltage range: 2V–6V

Connection Diagram

Dual-in-Line Package



TL/F/9398–1

Order Number MM54HCT148* or MM74HCT148*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs									Outputs				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High, L = Low, X = Irrelevant

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package Only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 sec.)	260°C

DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operation Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.96	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		2.0	2.9	3.0	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating—plastic "N" package −12 mW/°C from 65°C to 85°C, ceramic "J" package 12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs held at V_{CC} or GND.

AC Electrical Characteristics MM54HCT148/MM74HCT148

V_{CC} = 5V ±10%, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
		Typ	Guaranteed Limits		
t_{pd}	Inputs 0–7 to A0, A1, A2	13	23	29	35	ns
t_{pd}	Inputs 0–7 to Output EO	12	22	28	33	ns
t_{pd}	Inputs 0–7 to Output GS	14	26	33	39	ns
t_{pd}	Inputs EI to A0, A1, A2	16	28	36	43	ns
t_{pd}	Input EI to Output GS	11	21	27	32	ns
t_{pd}	Input EI to Output EO	13	23	29	34	ns
t_r, t_f	Maximum Output Rise and Fall Times	7	11	14	17	ns
C_{pd}	Power Dissipation Capacitance (Note 5)	TBD				pF
C_{IN}	Maximum Input Capacitance	5	10	10	10	pF

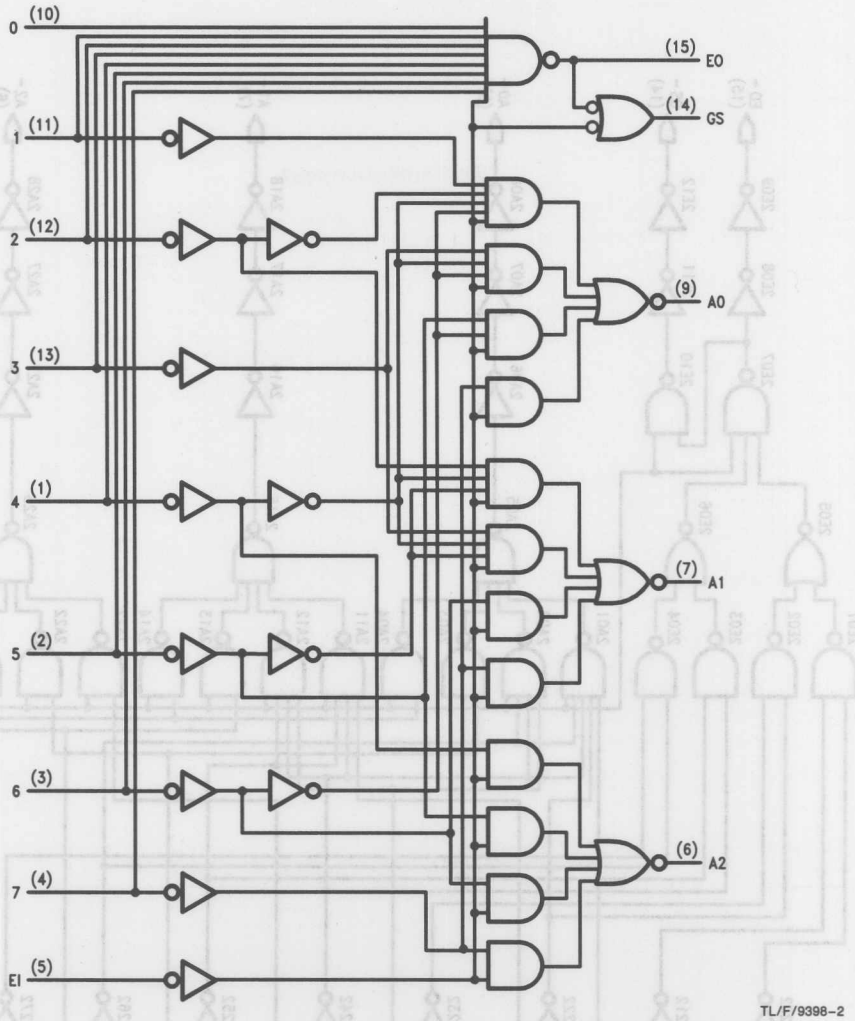
Note 5: C_{pd} determines the no load dynamic power consumption, and the no load dynamic current consumption.

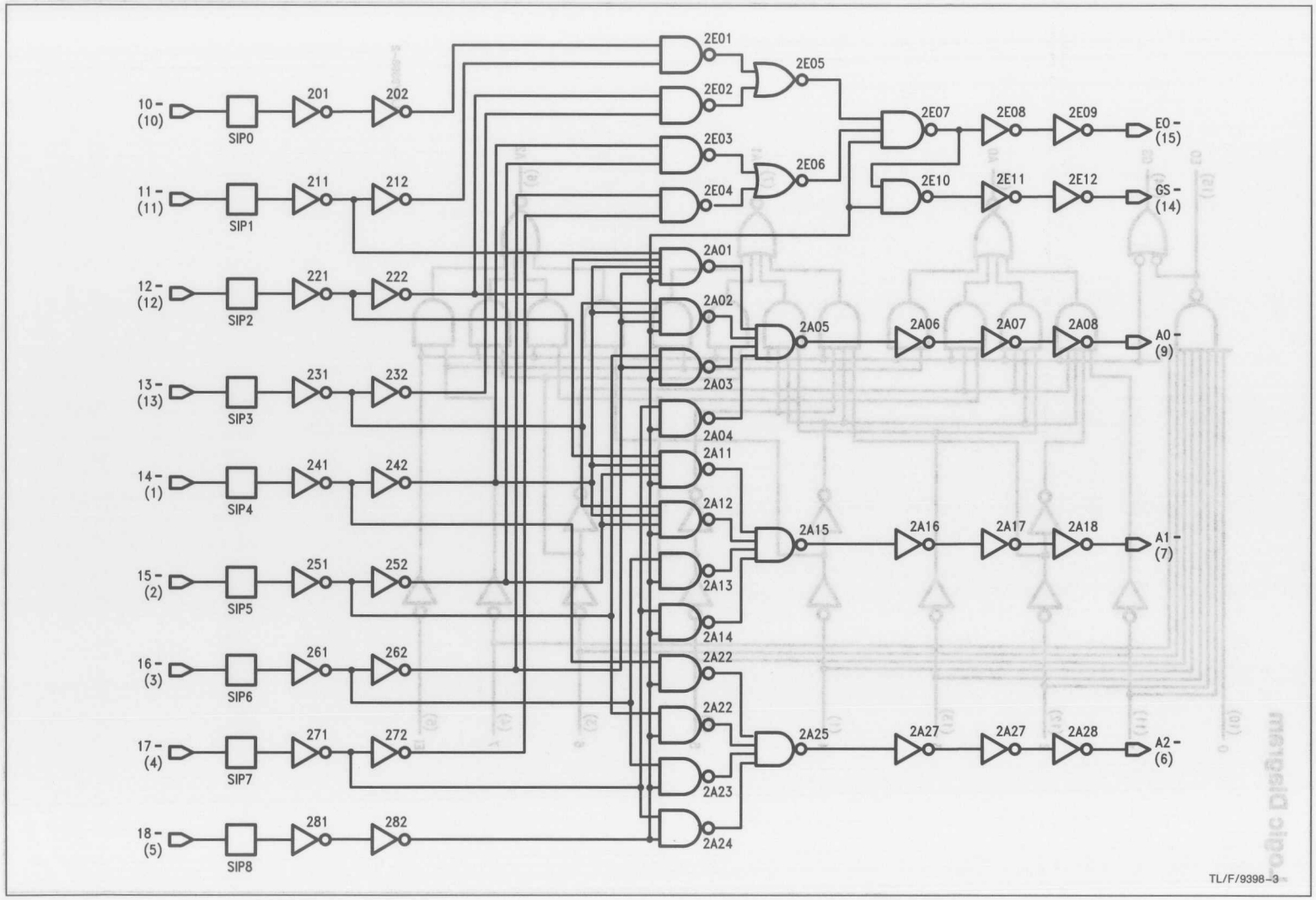
AC Electrical Characteristics MM54HCT148/MM74HCT148

V_{CC} = 5V, C_L = 15 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	T_A = 25°C		Units
		Typ	Guaranteed Limits	
t_{pd}	Inputs 0–7 to A0, A1, A2	12		ns
t_{pd}	Inputs 0–7 to Output EO	11		ns
t_{pd}	Inputs 0–7 to Output GS	13		ns
t_{pd}	Input EI to A0, A1, A2	15		ns
t_{pd}	Input EI to Output GS	11		ns
t_{pd}	Input EI to Output EO	12		ns
t_r, t_f	Maximum Output Rise and Fall Times	4		ns

Logic Diagram




10 - (10)
11 - (11)
12 - (12)
13 - (13)
14 - (1)
15 - (2)
16 - (3)
17 - (4)
18 - (5)
SIP0
SIP1
SIP2
SIP3
SIP4
SIP5
SIP6
SIP7
SIP8
201
202
211
212
221
222
231
232
241
242
251
252
261
262
271
272
281
282
2E01
2E02
2E03
2E04
2E05
2E06
2E07
2E08
2E09
2E10
2E11
2E12
EO - (15)
GS - (14)
2A01
2A02
2A03
2A04
2A05
2A06
2A07
2A08
A0 - (9)
2A11
2A12
2A13
2A14
2A15
2A16
2A17
2A18
A1 - (7)
2A22
2A22
2A23
2A24
2A25
2A27
2A27
2A28
A2 - (6)
TL/F/9398–3

National Semiconductor

MM54HCT149/MM74HCT149
8 Line to 8 Line Priority Encoder

General Description

This priority encoder is implemented in advanced silicon-gate CMOS technology. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority, encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. Only one request output can be low at a time. The output that is low is dependent on the highest priority request input that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is an enable input, $\overline{RQE}$, which, when high, forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RI}$ is active.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

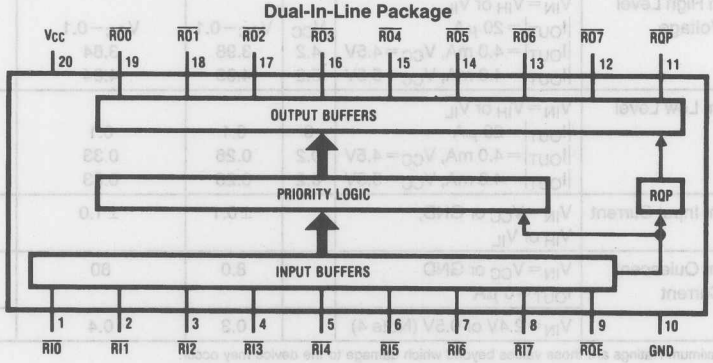
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Internal switched pull up resistors provided to reduce power consumption

Connection Diagram

Dual-In-Line Package



TL/F/5364–1

Top View

Order Number MM54HCT149* or MM74HCT149*

*Please look into Section 8, Appendix D for availability of various package types.

4

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs held at V_{CC} or GND.

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

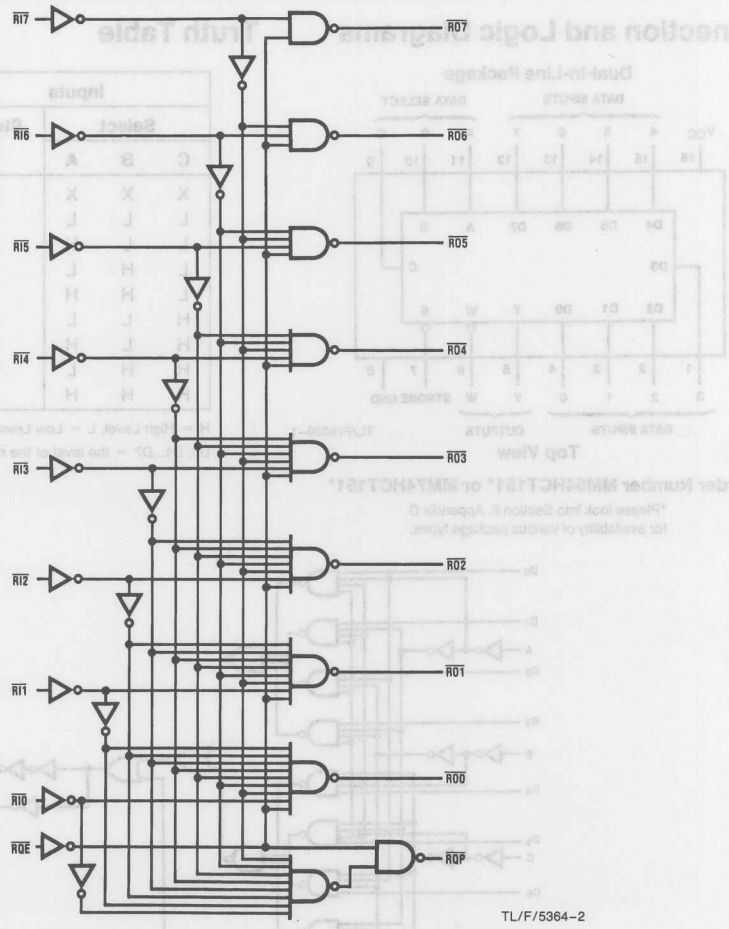
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any Input to $\overline{RQP}$		20	38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Any Input to Any Other Output		20	34	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pf $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any Input to $\overline{RQP}$		30	47	59	70	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Any Input To Any Other Output		26	43	54	65	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)		50			pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Simplified Logic Diagram



TL/F/5364–2

8-Channel Digital Multiplexer

General Description

This high speed Digital multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HCT151/MM74HCT151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

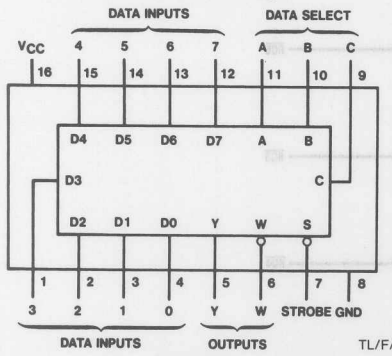
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent supply current: 40 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/9399–1

Top View

Order Number MM54HCT151* or MM74HCT151*

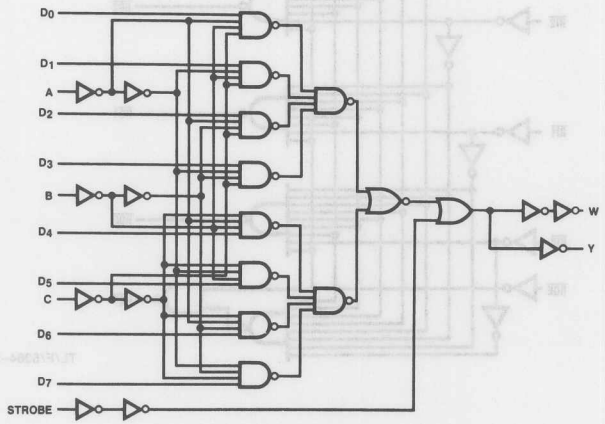
*Please look into Section 8. Appendix D for availability of various package types.

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1...D7 = the level of the respective D input



TL/F/9399–2

DC Input Voltage (V_{IN})	$-1.5V$ to $V_{CC}+1.5V$	Operating Temp. Range (T_A)			
DC Output Voltage (V_{OUT})	$-0.5V$ to $V_{CC}+0.5V$	MM74HCT	-40	$+85$	°C
Clamp Diode Current (I_{IK}, I_{OK})	± 20 mA	MM54HCT	-55	$+125$	°C
DC Output Current, per Pin (I_{OUT})	± 25 mA	Input Rise or Fall Times (t_r, t_f)		500	ns
DC V_{CC} or GND Current, per Pin (I_{CC})	± 50 mA				
Storage Temperature Range (T_{STG})	$-65°C$ to $+150°C$				
Power Dissipation (P_D) (Note 3)	600 mW				
S.O. Package only	500 mW				
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C				

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HCT	54HCT	Units
					$T_A = -40°C$ to $+85°C$	$T_A = -55°C$ to $+125°C$	
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}						
		$\lvert I_{OUT}\rvert \le 20\ \mu A$	4.5V		4.4	4.4	4.4	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 4.8$ mA	5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL}						
		$\lvert I_{OUT}\rvert = 20\ \mu A$		0	0.1	0.1	0.1	V
		$\lvert I_{OUT}\rvert = 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert = 4.8$ mA	5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND						
		$I_{OUT} = 0\ \mu A$			8.0	80	160	μA
		$V_{IN} = 2.4V$ or $0.5V$ (Note 4)		0.25	0.4	0.55	0.65	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C; ceramic "J" package: -12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V $\pm 10\%$ the worst case output voltages (V_{OH}, and V_{OL}) occur for HCT at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		17	23	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40°C$ to $+85°C$	54HCT $T_A=-55°C$ to $+125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		33	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		33	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to Y		27	39	49	59	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		27	39	49	59	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		21	28	35	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		21	28	35	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		8	15	19	23	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)	110				pF
C_{IN}	Maximum Input Capacitance		5	10			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HCT153/MM74HCT153 Dual 4-Input Multiplexer

General Description

This 4-to-1 line multiplexer utilizes advanced silicon-gate CMOS technology. It has the low power consumption of standard CMOS integrated circuits. This device is fully buffered, allowing it to drive 10 LS-TTL loads. Information on the data inputs of each multiplexer is selected by the address on the A and B inputs, and is presented on the Y outputs. Each multiplexer possesses a strobe input which enables it when taken to a low logic level. When a high logic level is applied to a strobe input, the output of its associated multiplexer is taken low.

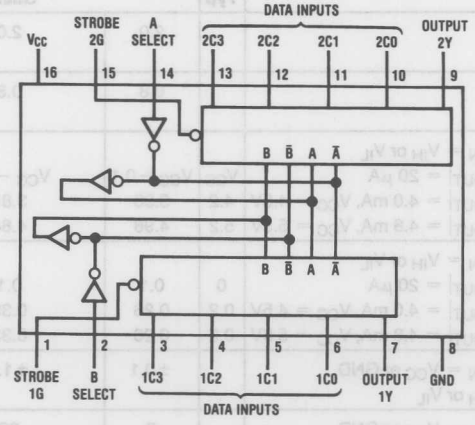
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- TTL Input Compatible

Connection Diagram

Dual-in-Line Package



TL/F/8436–1

Top View

Order Number MM54HCT153* or MM74HCT153*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Minimum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.6	0.8	1.0	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, t_r = t_f = 6 ns, C_L = 15 pF

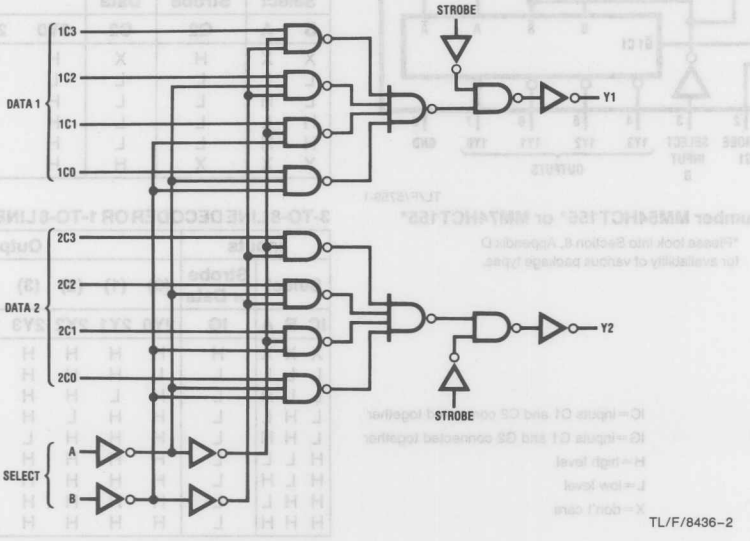
Symbol	Parameter	Conditions	Typ	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		12	ns

AC Electrical Characteristics C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C			74HC T_A = −40°C to 85°C		54HC T_A = −55°C to 125°C		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y			26	40		50		60	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y			24	35		44		53	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ		19	26		33		39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y			15	22		28		33	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			8	15		19		22	ns
C_{IN}	Maximum Input Capacitance			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)(per package) Outputs Enabled Outputs Disabled		 90 25						 pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/8436–2

National Semiconductor

MM54HCT155/MM74HCT155
Dual 2-to-4 Line Decoder/Demultiplexers

General Description

The MM54HCT155/MM74HCT155 is a high speed silicon gate CMOS decoder/demultiplexer. It features dual 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is "non-inverted" at its outputs. If the strobes (G1 and G2) are connected together and the Data Inputs are connected together, the device can be used as a 3-to-8 line decoder or a 1-to-8 line demultiplexer.

All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground. The device is capable of driving 10 low power Schottky TTL equivalent loads.

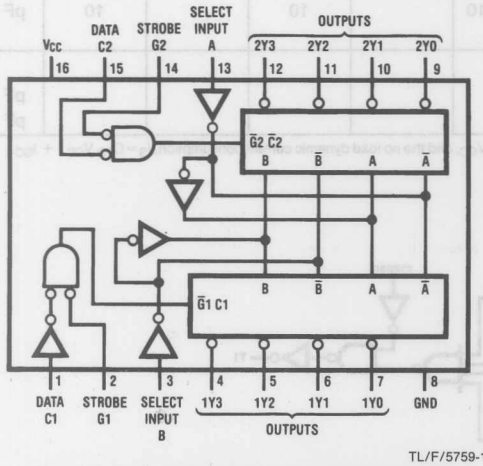
The MM54HCT155/MM74HCT155 is functionally and pin equivalent to the 54LS155/74LS155 and can be used as a plug-in replacement to reduce system power consumption in existing systems.

Features

- Applications:
  - Dual 2-to-4 line decoder
  - Dual 1-to-4 line demultiplexer
  - 3-to-8 line decoder
  - 1-to-8 line demultiplexer
- Typical propagation delay: 22 ns
- Low quiescent current: 80 μA maximum (74HCT Series)

Connection Diagram

Dual-In-Line Package



TL/F/5759-1

Order Number MM54HCT155* or MM74HCT155*

*Please look into Section 8, Appendix D for availability of various package types.

IC = inputs C1 and C2 connected together
IG = inputs G1 and G2 connected together
H = high level
L = low level
X = don't care

Truth Tables

2-TO-4 LINE DECODER OR 1-TO-4 LINE DEMULTIPLEXER

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-TO-8 LINE DECODER OR 1-TO-8 LINE DEMULTIPLEXER

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
IC	B	A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L)	
(Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise/Fall Time			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	Typ	Guaranteed Limits			Units
				T_A = 25°C	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V_{IL}	Maximum High Level Input Voltage				0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA	V_{CC}		V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V			3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V			4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA			0.10	0.10	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V			0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V			0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{IN} = V_{IH} or V_{IL}			±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0.0 μA (Note 4)			8	80	160	μA
		V_{IN} = 2.4V or 0.5V I_{OUT} = 0.0 μA (Note 4)			0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Power dissipation temperature deratings: plastic N package: −12 mW/°C from 65°C to 85°C; ceramic J package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs at V_{CC} or GND.

AC Electrical Characteristics

V_{CC}, temperature and loading of LS-TTL; $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output		19	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output		24	35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C1 to any Output		25	35	ns

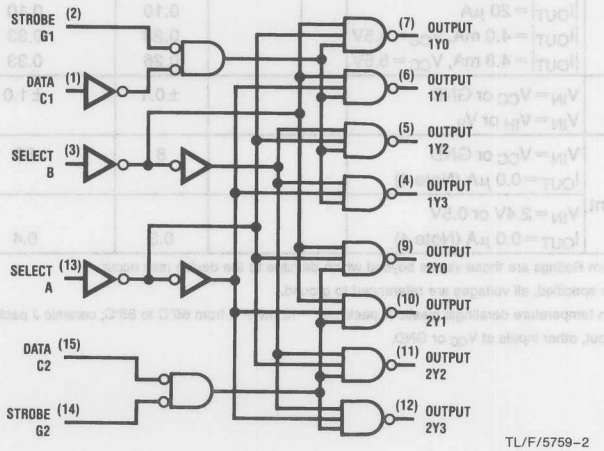
AC Electrical Characteristics

Full range of V_{CC} and temperature; $V_{CC}=5V\pm10\%$, $C_L=50$ pF unless otherwise specified

Symbol	Parameter	Conditions	Typ	Guaranteed Limits			Units
			T = 25°C	T = 25°C	74HCT T = −40°C to 85°C	54HCT T = −55°C to 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output		21	35	44	51	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output		26	40	50	60	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C1 to any Output		27	40	50	60	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance	Note 5	45				pF
C_{IN}	Minimum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5759–2

MM54HCT157/MM74HCT157 Quad 2-Input Multiplexer
MM54HCT158/MM74HCT158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed QUAD 2-to-1 line data selector/multiplexers utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and OUTPUT ENABLE inputs. On the MM54HCT157/MM74HCT157, when the OUTPUT ENABLE input is at logical "0" the four outputs assume the values as selected from the inputs. When the OUTPUT ENABLE input is at a logical "1" the outputs assume logical "0". The MM54HCT158/MM74HCT158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

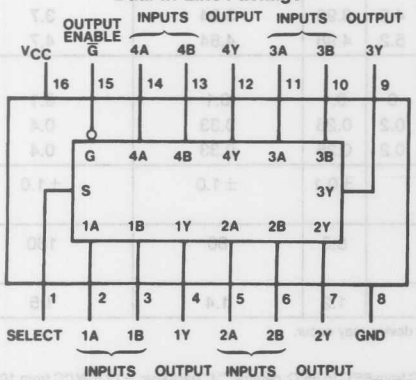
The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Power supply range: 5V ± 10%
- Low power supply quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Completely TTL compatible
- High output drive current: 60 mA minimum

Connection Diagrams

Dual-In-Line Package



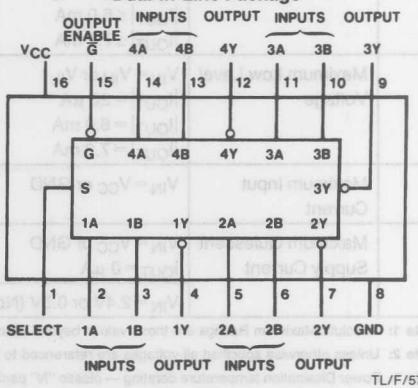
TL/F/5741–1

Top View

Order Number MM54HCT157/158* or MM74HCT157/158*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/5741–2

Top View

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HCT157	HCT158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

(V_{IN}, V_{OUT})			
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	4.5V	4.4	4.4	4.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.2$ mA	5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| = 20\ \mu A$		0	0.1	0.1	0.1	V
		$\|I_{OUT}\| = 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| = 7.2$ mA	5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND $I_{OUT} = 0\ \mu A$			8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)			1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HCT at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

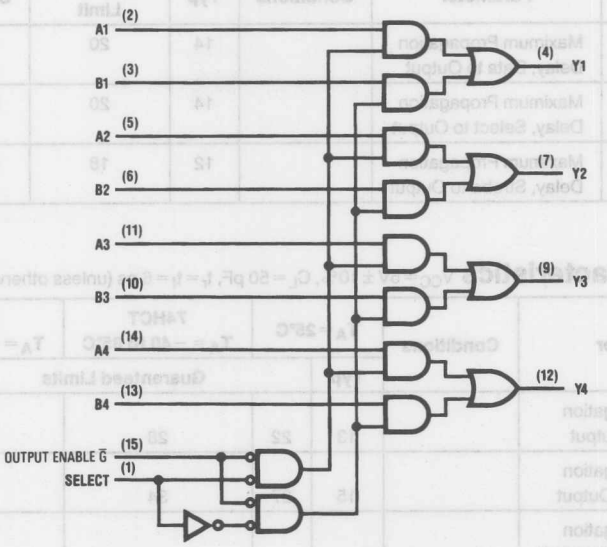
AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		13	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		15	27	34	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, OUTPUT ENABLE to Output		14	25	31	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)		48				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

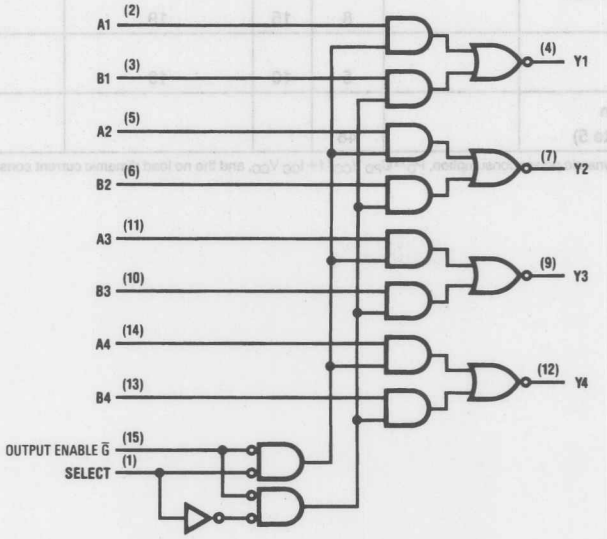
Logic Diagrams

'HCT157



TL/F/5741–3

'HCT158



TL/F/5741–4

National Semiconductor

MM54HCT164/MM74HCT164 8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HCT164/MM74HCT164 utilizes advanced silicon-gate CMOS technology. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

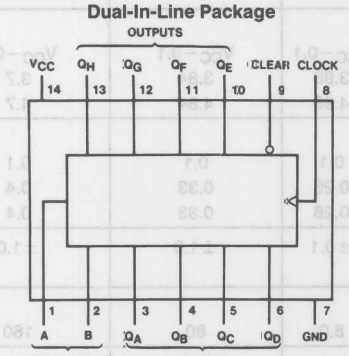
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

Connection Diagram

Dual-In-Line Package



TL/F/5765–1

Top View

Order Number MM54HCT164* or MM74HCT164*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

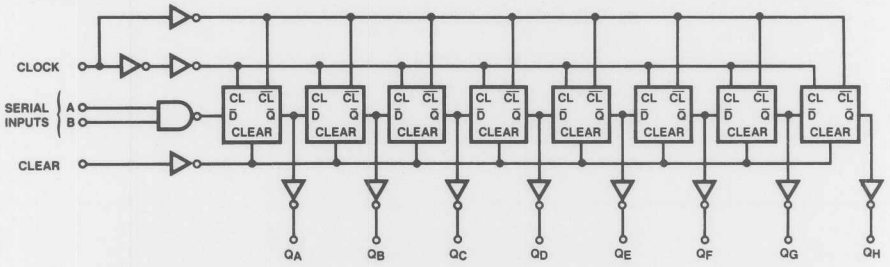
X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Logic Diagram



TL/F/5765–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package Only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

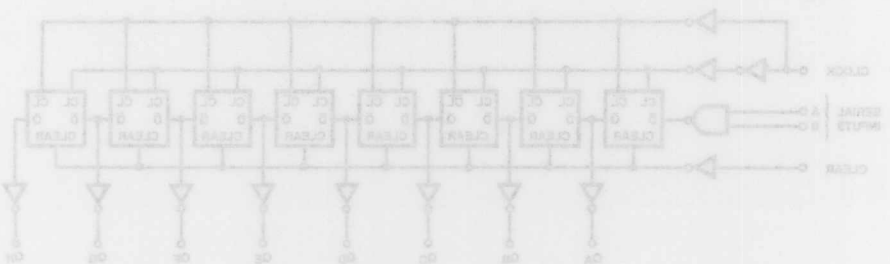
Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND					
		I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.4V (Note 4)		1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per pin. All other inputs are held at V_{CC} ground.



f_{MAX}	Maximum Operating Frequency from Clock to Q	50% Duty Cycle Clock	55	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q		17	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		23	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		3	6	ns
t_S	Minimum Set Up Time Data to Clock	$t_H \geq 20$ ns	6	13	ns
t_H	Minimum Hold Time Clock to Data	$t_S \geq 20$ ns	1.5	5	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		9	16	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to $85°C$		54HCT $T_A = -55°C$ to $125°C$		Units
			Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Operating Frequency	50% Duty Cycle Clock	45	30		25		22	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		20	30		38		45	ns
t_{PHL}	Maximum Propagation Delay from Clear to Q		26	41		51		61	ns
t_{REM}	Minimum Removal Time Clear to Clock		4	8		10		14	ns
t_S	Minimum Setup Time Data to Clock	$t_H \geq 20$ ns	7	15		19		23	ns
t_H	Minimum Hold Time Clock to Data	$t_S \geq 20$ ns	1.5	5		5		5	ns
t_W	Minimum Pulse Width Clock, or Clear		10	18		22		27	ns
t_r, t_f	Maximum Input Rise and Fall Time			500		500		500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15		19		22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)	160						pF
C_{IN}	Maximum Input Capacitance		5	10		10		10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of the section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

MM54HCT166/MM74HCT166
8-Bit Parallel In/Serial Out Shift Registers

General Description

The MM54HCT166/MM74HCT166 high speed 8-BIT PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes advanced silicon-gate CMOS technology. It has an input threshold and output drive similar to LS-TTL low standby power of CMOS.

These Parallel-In/Serial-In, Serial-Out shift registers feature gated CLOCK inputs and an overiding CLEAR input. The load mode is established by the SHIFT/LOAD input. When high, this input enables the SERIAL INPUT and couples the eight flip-flops for serial shifting with each clock pulse. When low, the PARALLEL INPUTS are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the CLOCK pulse through a 2-input NOR gate, permitting one input to be used as a clock enable or CLOCK INHIBIT function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The CLOCK INHIBIT input should be changed to the high level only while the clock input is high. A direct CLEAR input overrides all other inputs, including the CLOCK, and sets all flip-flops to zero.

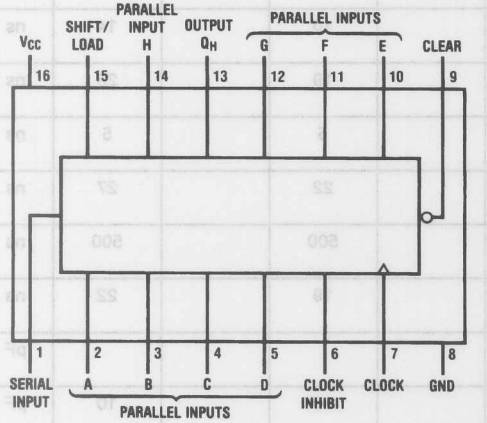
All inputs are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

The MM54HCT/MM74HCT logic family is intended to interface TTL and NMOS components to CMOS components. These parts can be used as plug-in relacement for LS-TTL devices to reduce system power consumption in existing designs.

Features

- TTL input compatible
- Low quiescent current: 80 μA max (74HCT series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram



TL/F/5751–1

Top View

Order Number MM54HCT166* or MM74HCT166*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock 1 Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady-state), L = low level (steady-state)

X = don't care (any input, including transitions)

↑ = transition from low-to-high level.

a . . . h = the level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = the level at Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input pin. All other inputs are held at V_{CC} or ground.

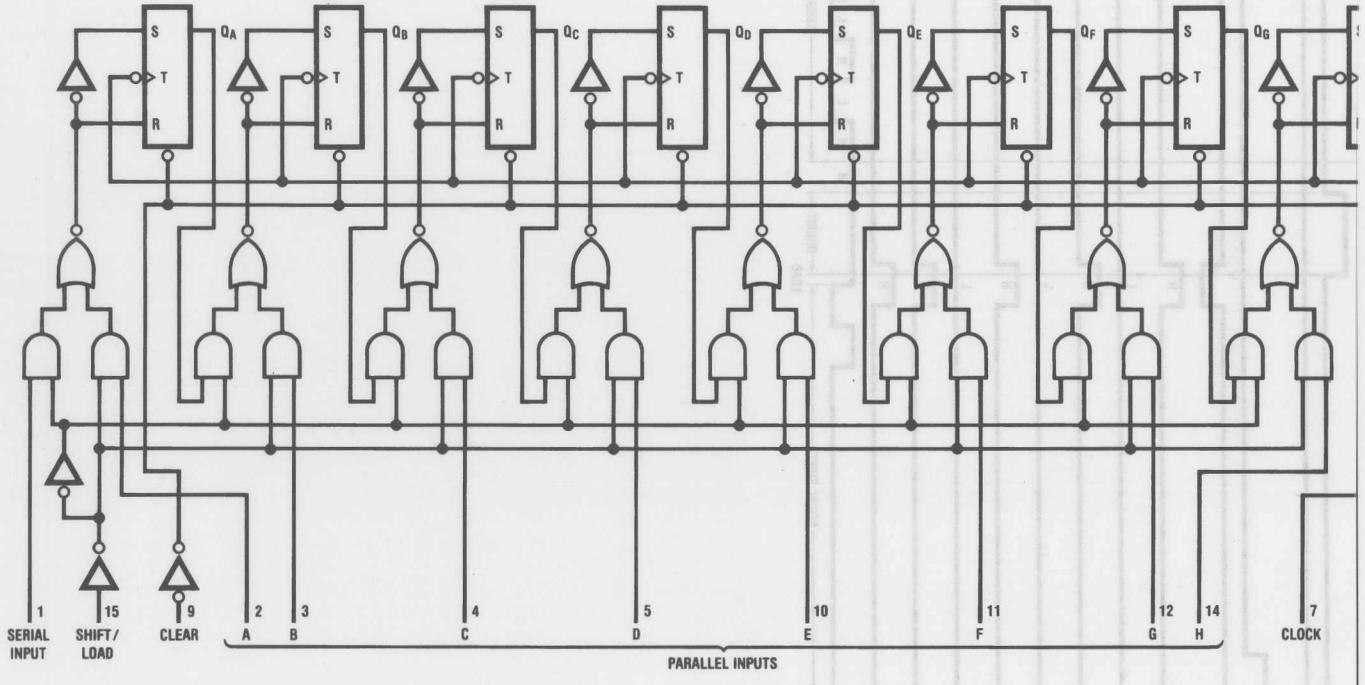
AC Electrical Characteristics V_{CC} = 5V, C_L = 15 pF, T_A = 25°C, t_r = t_f = 6 ns (unless otherwise noted)

Symbol	Parameter	Typical	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		31	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_H		16	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q_H		12	ns
t_{su}	Minimum Set-Up Time Shift/Load High to Clock		16	ns
t_{su}	Minimum Set-Up Time Data before Clock		16	ns
t_{REM}	Minimum Removal Time Clear to Clock		0	ns
t_H	Maximum Hold Time Data after Clock		0	ns
t_W	Minimum Pulse Width Clock or Clear		16	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise noted)

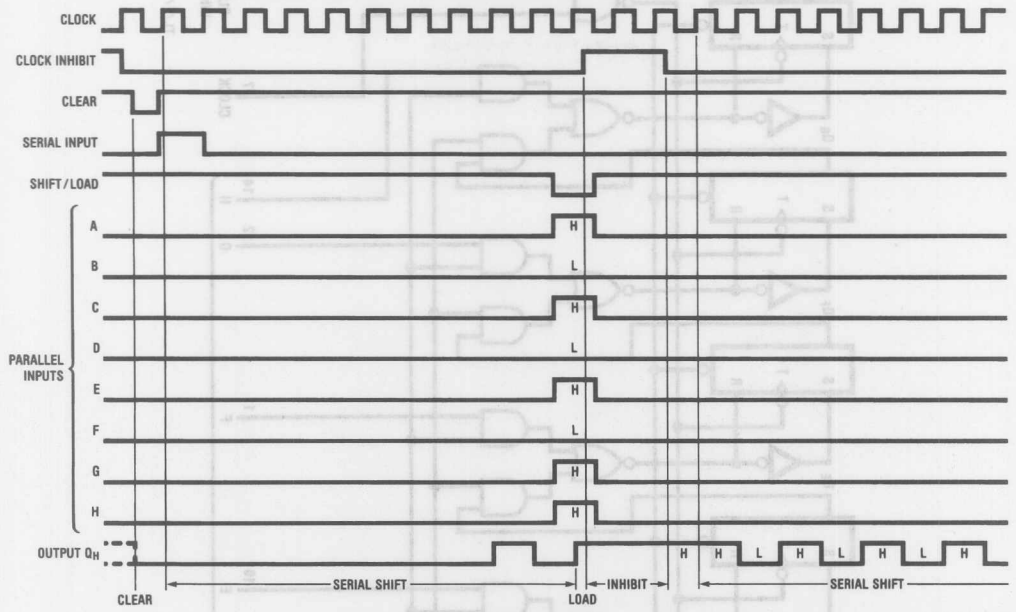
Symbol	Parameter	$T_A=25°C$	74HCT $T_A=-40°C$ to $+85°C$	54HCT $T_A=-55°C$ to $+125°C$	Units
		Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	31	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_H	25	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q_H	23	33	41	50	ns
t_{su}	Minimum Set-Up Time Shift/Load High to Clock	9	16	20	24	ns
t_{su}	Minimum Set-Up Time Data before Clock	9	16	20	24	ns
t_{REM}	Minimum Removal Time Clear to Clock		0	0	0	ns
t_H	Maximum Hold Time Data after Clock	−3	3	3	3	ns
t_r, t_f	Maximum Output Rise and Fall Time		15	19	22	ns
t_W	Minimum Pulse Width Clear or Clock		16	20	24	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		100			pF
C_{IN}	Maximum Input Capacitance	5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption P_D, and the no load dynamic current consumption, I_S.


S
T
R
Q_A
Q_B
Q_C
Q_D
Q_E
Q_F
Q_G
1
SERIAL INPUT
15
SHIFT/ LOAD
9
CLEAR
2
A
3
B
4
C
5
D
10
E
11
F
12
G
14
H
7
CLOCK
PARALLEL INPUTS

Timing Diagram

Typical Clear, Load, Inhibit, and Shift Sequences



TL/F/5751–3

National Semiconductor

MM54HCT190/MM74HCT190 Synchronous Decade Up/Down Counters with Mode Control. MM54HCT191/MM74HCT191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. These circuits are synchronous, reversible, up/down counters. The MM54HCT191/MM74HCT191 are 4-bit binary counters and the MM54HCT190/MM74HCT190 are BCD counters.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as divide by N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

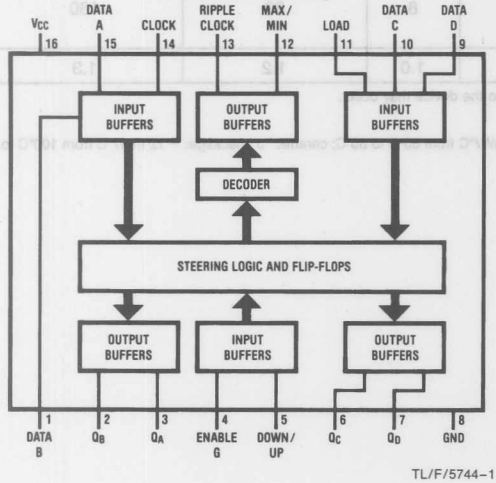
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices can be used to reduce power consumption in existing designs.

Features

- Level changes on Enable or Down/Up can be made regardless of the level of the clock.
- Low quiescent supply current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5744–1

Truth Table

Load	Enable G	Down/Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Order Number MM54HCT190/191* or MM74HCT190/191*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to + 150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.0	1.2	1.3	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

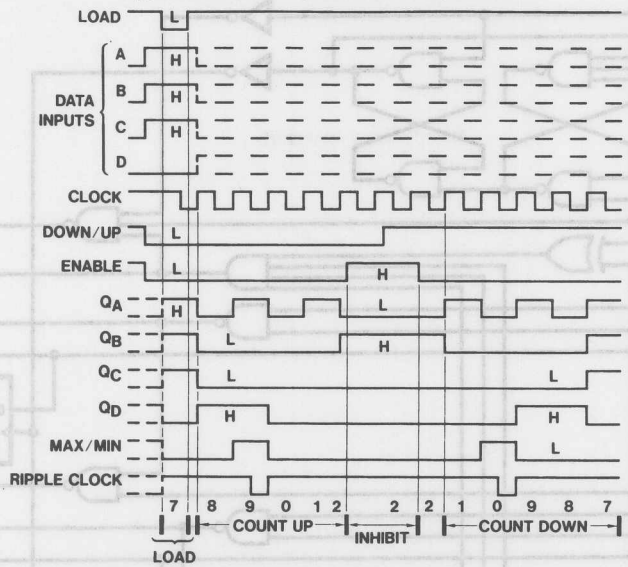
AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF unless otherwise specified

Symbol	Parameter	From Input	To Output	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Clock Frequency				40		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		27		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		16		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		24		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		29		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		22		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock		22		ns
t_W	Minimum Clock or Load Input Pulse Width				10		ns

					Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency				28	20	16	13	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		31	44	55	66	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		30	40	50	60	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		24	30	38	45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		32	43	54	65	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		45	55	69	83	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		42	50	63	75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		30	45	56	68	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		26	33	41	50	ns
t_W	Minimum Clock Pulse Width				15	25	31	38	ns
t_S	Minimum Set-Up Time	Data	Load		10	20	25	30	ns
t_H	Minimum Hold Time	Load	Data		−3	5	6	8	ns
t_S	Minimum Set-Up Time	Down/Up	Clock		23	30	38	45	ns
t_H	Minimum Hold Time	Clock	Down/Up		−7	0	0	0	ns
t_S	Minimum Set-Up Time	Enable	Clock		13	20	25	30	ns
t_H	Minimum Hold Time	Clock	Enable		−5	0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time				10	15	19	22	ns
C_{IN}	Maximum Input Capacitance				5				pF
C_{PD}	Power Dissipation Capacitance (Note 5)				35				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Typical Load, Count, and Inhibit Sequences

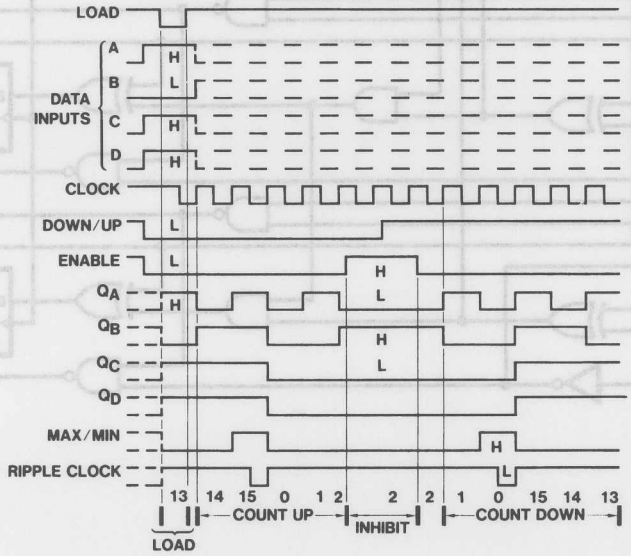


TL/F/5744–5

Sequence:

(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight and seven

'HCT191 Synchronous Binary Counters
Typical Load, Count, and Inhibit Sequence



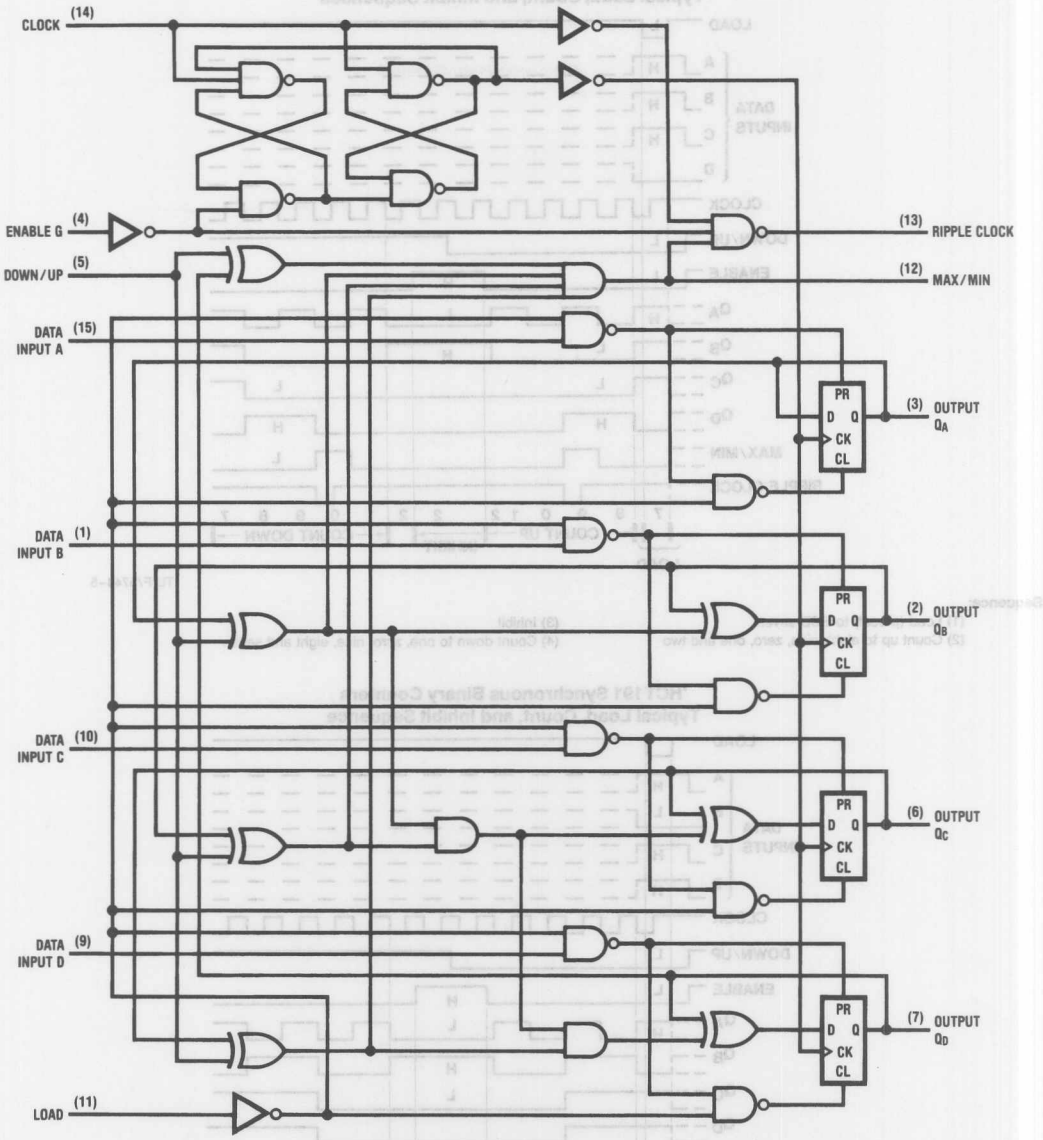
TL/F/5744–6

Sequence:

(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen and thirteen

Logic Diagram

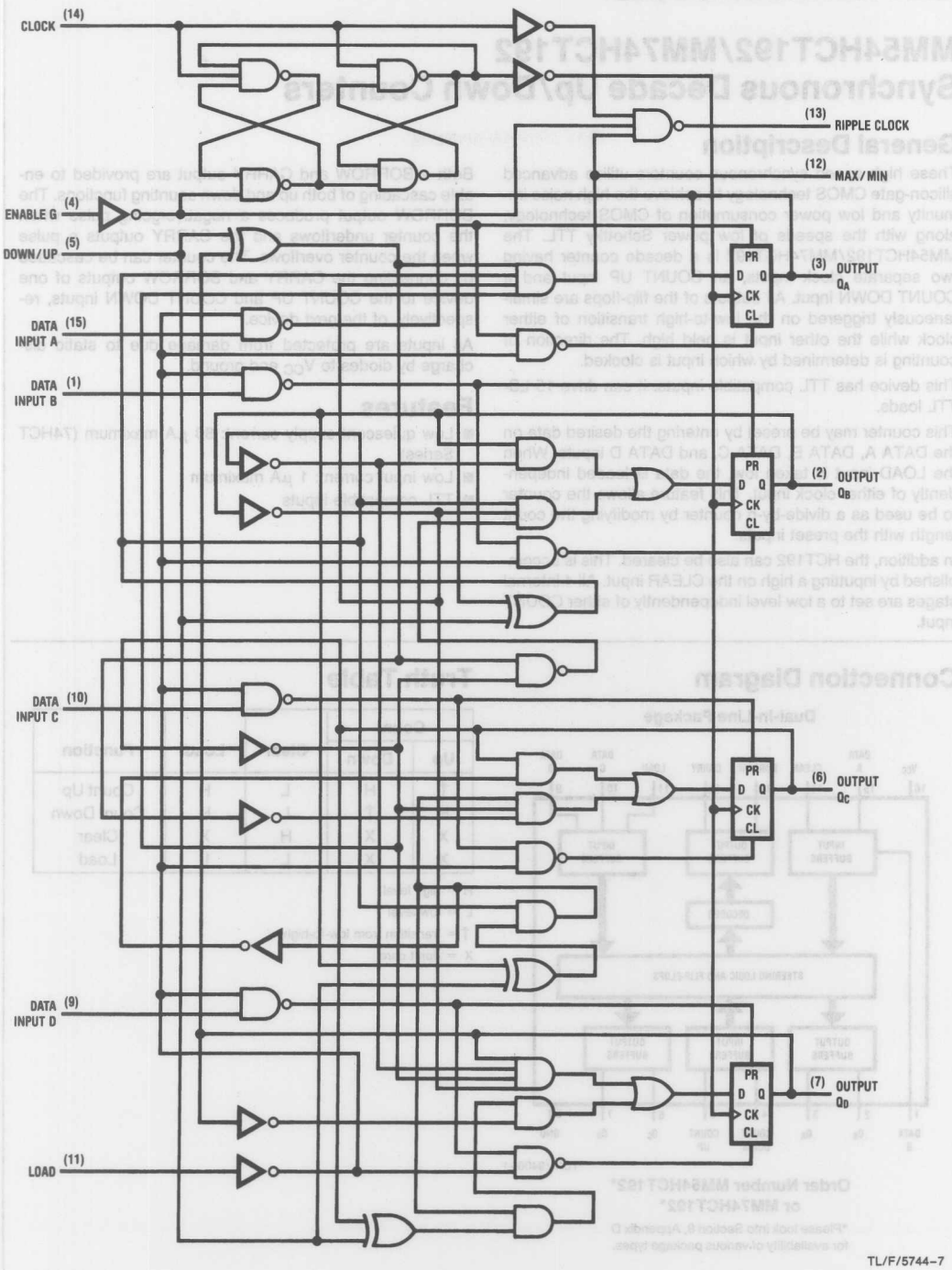
'HCT191



TL/F/5744–3

Logic Diagram (Continued)

'HCT190 Decade Counters



TL/F/5744–7

National Semiconductor

MM54HCT192/MM74HCT192 Synchronous Decade Up/Down Counters

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HCT192/MM74HCT192 is a decade counter having two separate clock inputs, an COUNT UP input and a COUNT DOWN input. All outputs of the flip-flops are simultaneously triggered on the low-to-high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

This device has TTL compatible inputs. It can drive 15 LS-TTL loads.

This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low, the data is loaded independently of either clock input. This feature allows the counter to be used as a divide-by-n counter by modifying the count length with the preset inputs.

In addition, the HCT192 can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative-going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

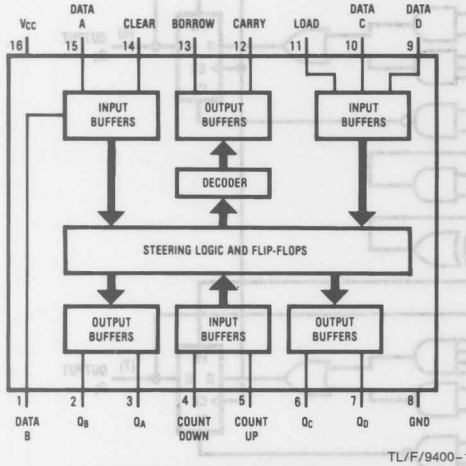
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Low quiescent supply current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/9400–1

Order Number MM54HCT192* or MM74HCT192*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level
L = low level
↑ = transition from low-to-high
X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin(I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	0.1	1.0	1.2	1.3	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: − 12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics

(Note 6) V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency				35		MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD		26		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A, B, C, D,	QA, QB, QC, QD		25		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB, QC, QD		26		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry		22		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Down	Borrow		22		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB, QC, QD		25		ns

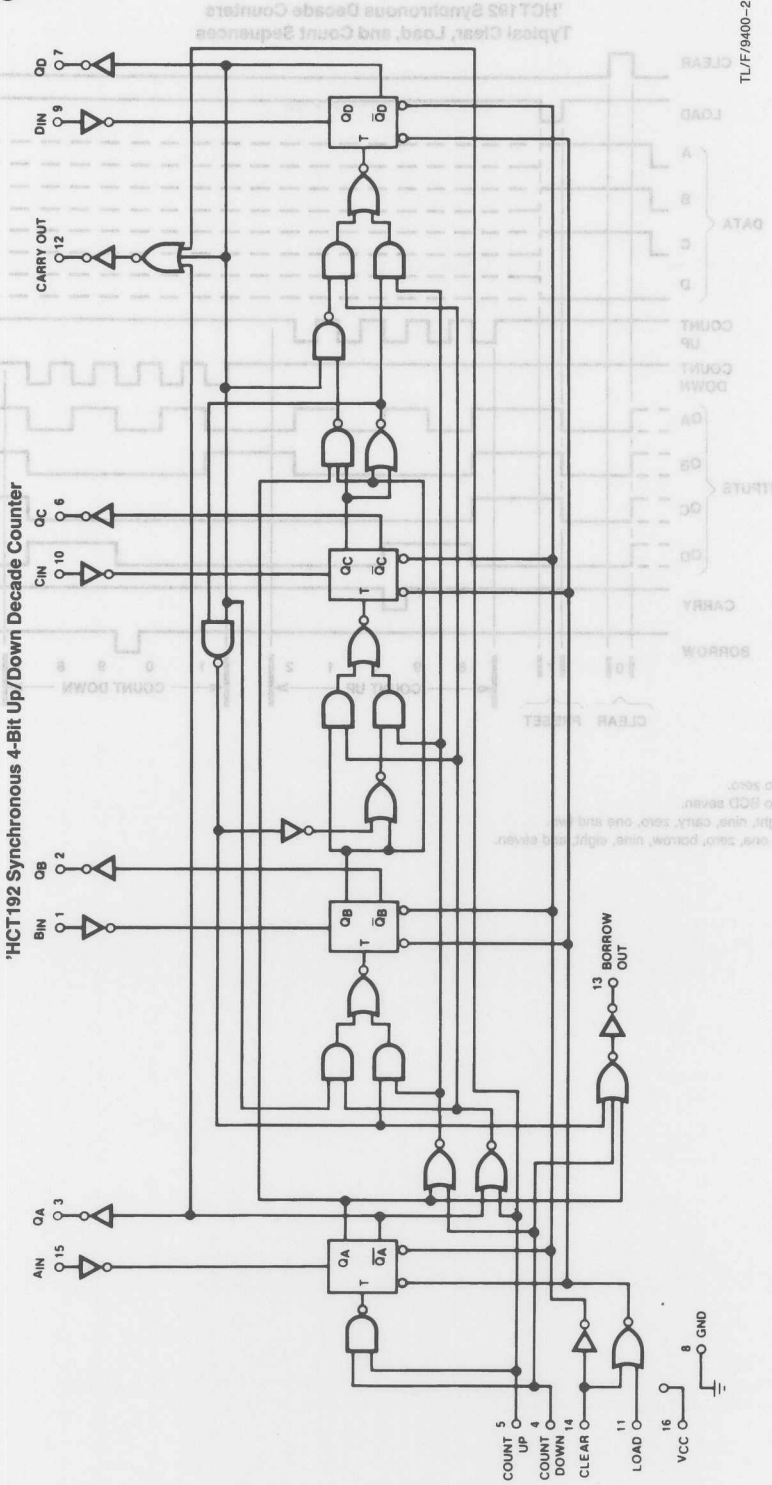
AC Electrical Characteristics (Note 6) V_{CC} = 5V ±10%, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	T = 25°C	T = 25°C	74HC T = −40°C to +85°C	54HC T = −55°C to +125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency			32	20	16	13	MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD	29	44	55	66	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A	QA, QB, QC, QD	28	40	50	60	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB QC, QD	30	43	54	65	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry	25	30	38	45	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Down	Borrow	25	30	38	45	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB QC, QD	28	35	44	53	ns
t_W	Minimum Clock Pulse Width			16	25	31	38	ns
t_S	Minimum Setup Time Data before Load-LH				20	25	30	ns
t_H	Minimum Hold Time Data after Load-LH			−3	5	6	8	ns
t_{REM}	Minimum Removal Time Load to Count			−2	5	6	8	ns
t_{REM}	Minimum Removal Time Clear to Count			2	5	6	8	ns
t_W	Minimum Load Pulse Width			18	20	25	30	ns
t_W	Minimum Clear Pulse Width			8	20	25	30	ns
$t_{TLH, THL}$	Output Rise or Fall Time			10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance			40				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

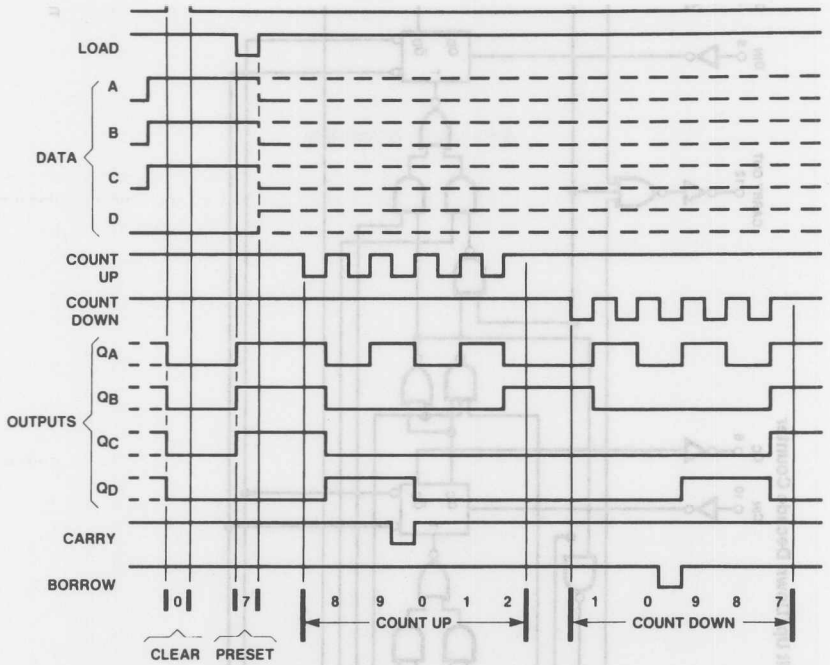
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ and the no load dynamic current consumption, $I_s = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switchforms and Test Circuits.

Logic Diagram



TL/F/9400–2



TL/F/9400–3

Sequences:
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

National Semiconductor

MM54HCT193/MM74HCT193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HCT193/MM74HCT193 is a binary counter having two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low-to-high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

This device has TTL compatible inputs. It can drive 15 LS-TTL loads.

This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low, the data is loaded independently of either clock input. This feature allows the counter to be used as a divide-by-n counter by modifying the count length with the preset inputs.

In addition, the HCT193 can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative-going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

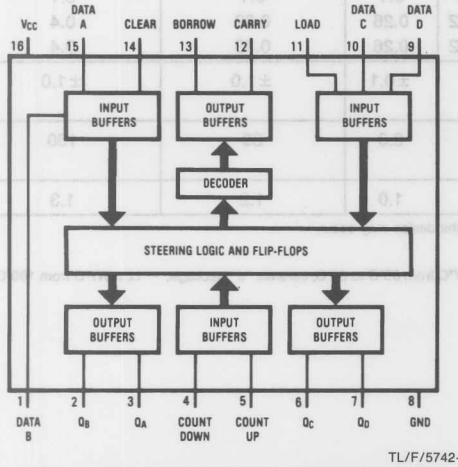
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Low quiescent supply current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5742–1

Order Number MM54HCT193* or MM74HCT193*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level
L = low level
↑ = transition from low-to-high
X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin(I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.0	1.2	1.3	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: − 12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics

(Note 6) V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency				35		MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD		26		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A, B, C, D,	QA, QB, QC, QD		25		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB, QC, QD		26		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry		22		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Dn	Borrow		22		ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB, QC, QD		25		ns

AC Electrical Characteristics (Note 6)

V_{CC} = 5V, ±10%, C_L = 50 pF (unless otherwise specified)

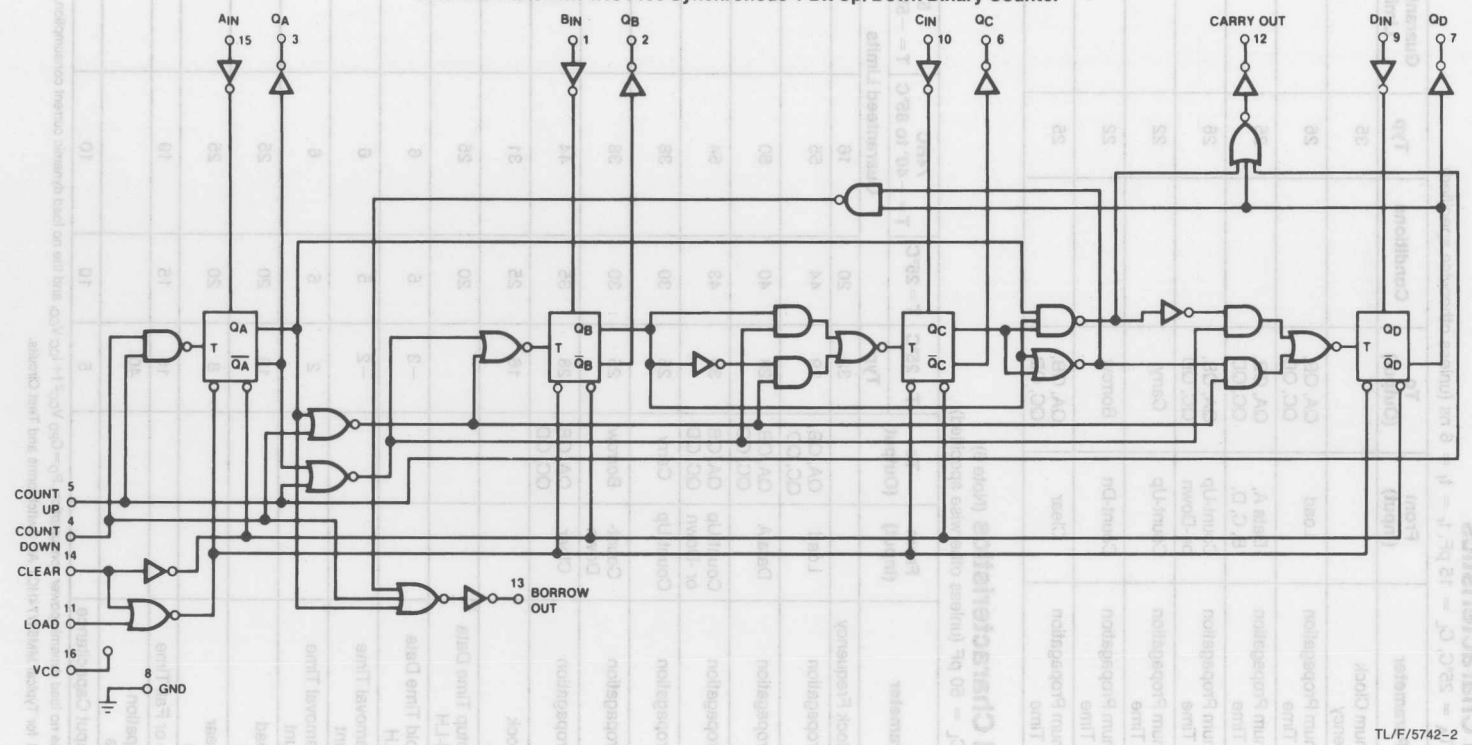
Symbol	Parameter	From (Input)	To (Output)	T = 25°C	T = 25°C	74HC T = −40° to 85°C	54HC T = −55° to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency			32	20	16	13	MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD	29	44	55	66	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A	QA, QB, QC, QD	28	40	50	60	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB QC, QD	30	43	54	65	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry	25	30	38	45	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Down	Borrow	25	30	38	45	ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB QC, QD	28	35	44	53	ns
t_W	Minimum Clock Pulse Width			16	25	31	38	ns
t_S	Minimum Setup Time Data before Load-LH				20	25	30	ns
t_H	Minimum Hold Time Data after Load-LH			−3	5	6	8	ns
t_{REM}	Minimum Removal Time Load to Count			−2	5	6	8	ns
t_{REM}	Minimum Removal Time Clear to Count			2	5	6	8	ns
t_W	Minimum Load Pulse Width			18	20	25	30	ns
t_W	Minimum Clear Pulse Width			8	20	25	30	ns
$t_{TLH, THL}$	Output Rise or Fall Time			10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance			40				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switchforms and Test Circuits.

4

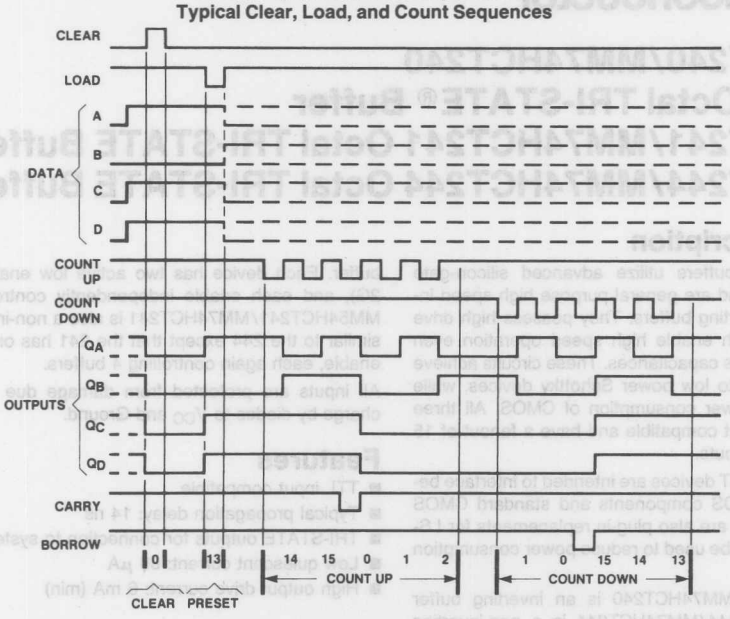
MM54HCT193/MM74HCT193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5742–2

Logic Waveforms

'HCT193 Synchronous Binary Counters
Typical Clear, Load, and Count Sequences



TL/F/5742–3

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

MM54HCT240/MM74HCT240 Inverting Octal TRI-STATE® Buffer
MM54HCT241/MM74HCT241 Octal TRI-STATE Buffer
MM54HCT244/MM74HCT244 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. All three devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT240/MM74HCT240 is an inverting buffer and the MM54HCT244/MM74HCT244 is a non-inverting buffer. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers. MM54HCT241/MM74HCT241 is also a non-inverting buffer similar to the 244 except that the 241 has one active high enable, each again controlling 4 buffers.

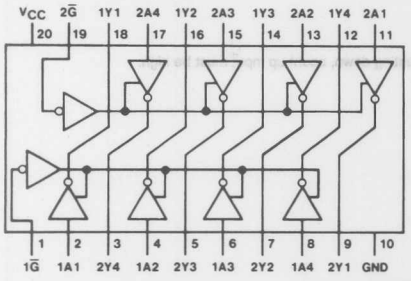
All inputs are protected from damage due to static discharge by diodes to V_{CC} and Ground.

Features

- TTL input compatible
- Typical propagation delay: 14 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- High output drive current: 6 mA (min)

Connection Diagrams

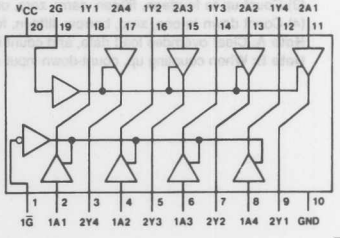
Dual-In-Line Packages



TL/F/5365–1

Top View

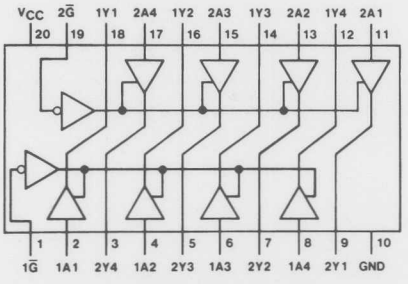
Order Number MM54HCT240* or MM74HCT240*



TL/F/5365–2

Top View

Order Number MM54HCT241* or MM74HCT241*



TL/F/5365–3

Top View

Order Number MM54HCT244* or MM74HCT244*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN-EE} = VIH or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, $\overline{G}$ = V_{IH}, G = V_{IL}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

Truth Tables

'HCT240

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

'HCT241

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

'HCT244

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

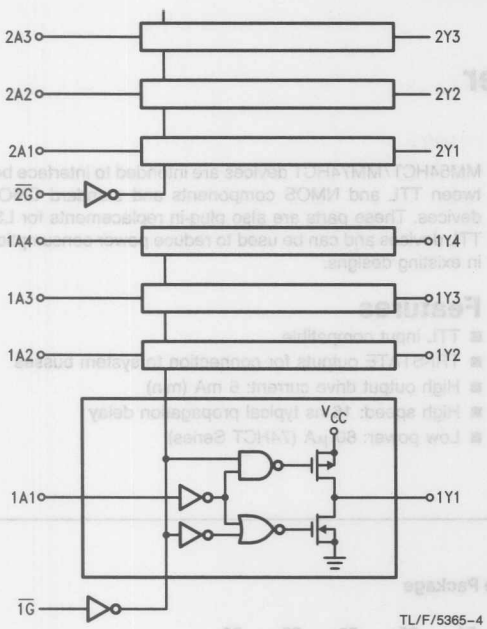
H = high level, L = low level, Z = high impedance

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 45$ pF	14	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L = 45$ pF, $R_L = 1$ kΩ	20	30	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	$C_L = 5$ pF, $R_L = 1$ kΩ	16	25	ns

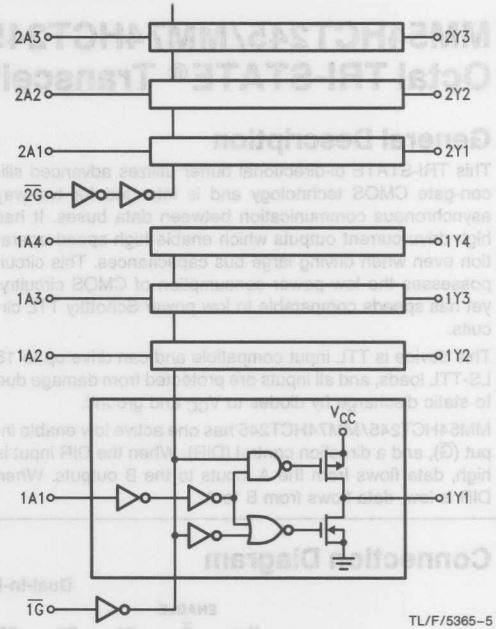
AC Electrical Characteristics MM54HCT240/MM74HCT240, MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244 $V_{CC} = 5.0V \pm 10\%$, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$	54HCT $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	$C_L = 50$ pF		14	20	25	30	ns
		$C_L = 150$ pF		20	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L = 1$ kΩ	$C_L = 50$ pF	21	30	38	45	ns
			$C_L = 150$ pF	26	42	53	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ, $C_L = 50$ pF		16	25	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L = 50$ pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G} = V_{CC}$, $G = GND$		5				pF
		$\overline{G} = GND$, $G = V_{CC}$		90				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

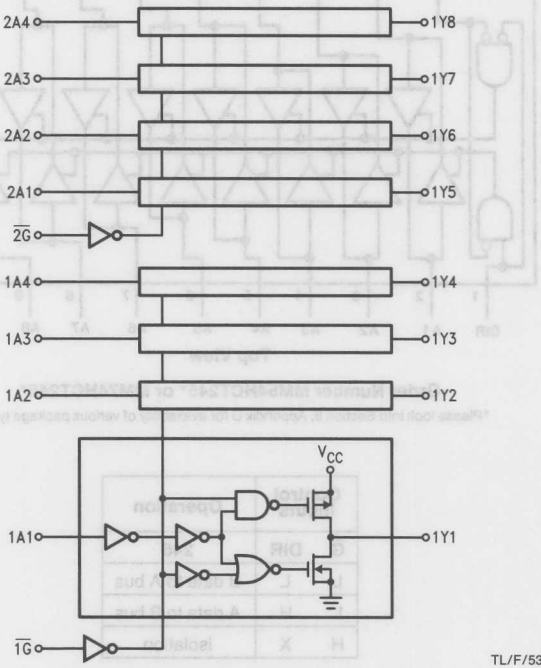


TL/F/5365–4



TL/F/5365–5

'HCT244



TL/F/5365–6

4

National Semiconductor

MM54HCT245/MM74HCT245 Octal TRI-STATE® Transceiver

General Description

This TRI-STATE bi-directional buffer utilizes advanced silicon-gate CMOS technology and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption of CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device is TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

MM54HCT245/MM74HCT245 has one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A.

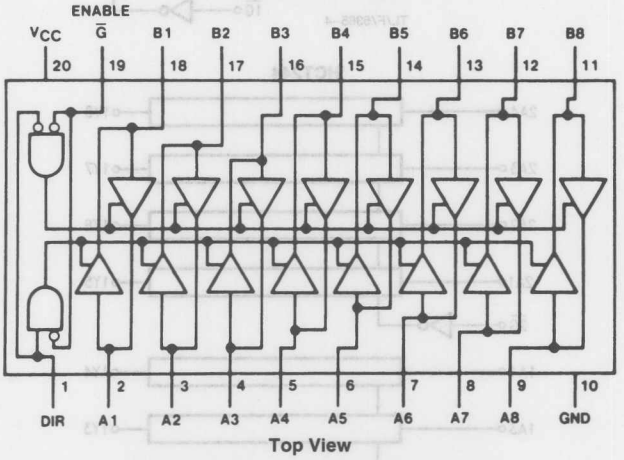
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- TRI-STATE outputs for connection to system busses
- High output drive current: 6 mA (min)
- High speed: 16 ns typical propagation delay
- Low power: 80 μA (74HCT Series)

Connection Diagram

Dual-In-Line Package



TL/F/5366–1

Top View

Order Number MM54HCT245* or MM74HCT245*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	245
L	L	B data to A bus
L	H	A data to B bus
H	X	isolation

H = high level L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC} = 5V ± 10%, unless otherwise specified.)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}, Pin 1 or 19		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or ground.

AC Electrical Characteristics MM54HCT245/MM74HCT245

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT245/MM74HCT245

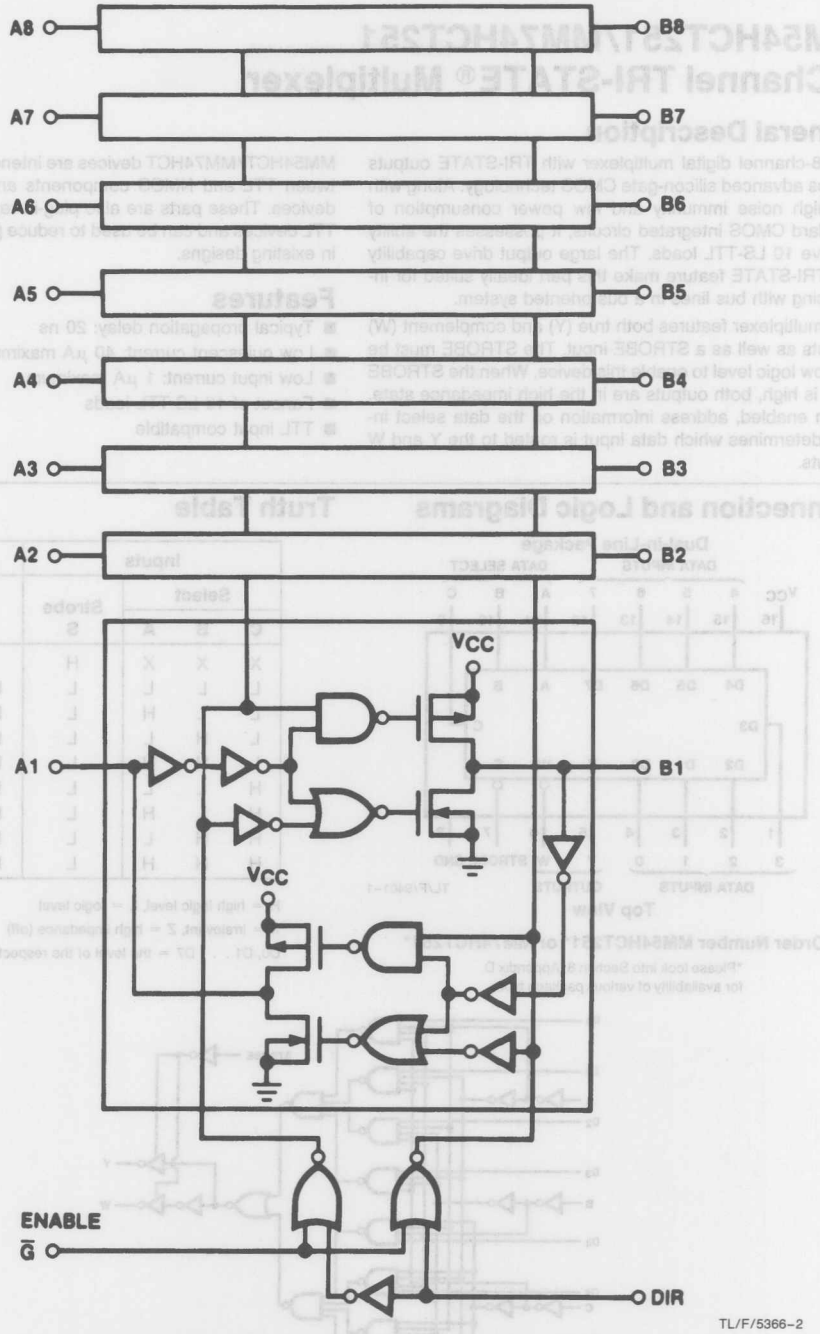
V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF	17	23	29	34	ns
		C_L = 150 pF	24	30	38	45	ns
t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 50 pF	31	42	53	63	ns
t_{PZH}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 50 pF	23	33	41	49	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output/Input Capacitance		20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance	(Note 5) $\overline{G}$ = V_{CC} GND $\overline{G}$ =	7 100				pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram

'HCT245



TL/F/5366–2

MM54HCT251/MM74HCT251
8-Channel TRI-STATE® Multiplexer

General Description

This 8-channel digital multiplexer with TRI-STATE outputs utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

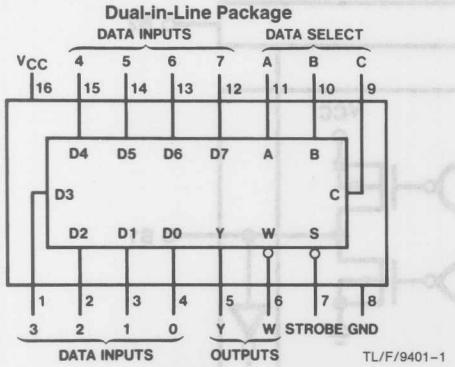
This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

Connection and Logic Diagrams



Top View

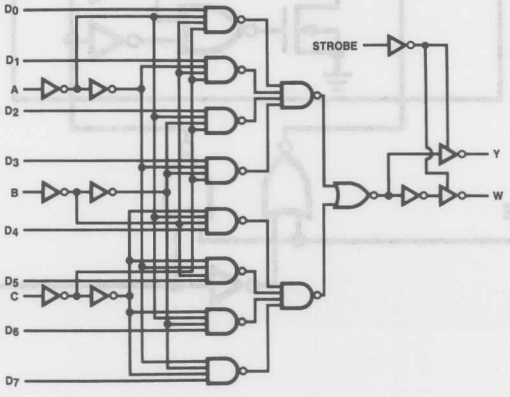
Order Number MM54HCT251* or MM74HCT251*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 4.5V		500	ns

DC Electrical Characteristics (Note 4) V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to +85°C	54HCT T_A = −55°C to +125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			0.9	0.9	0.9	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	4.5	4.4	4.4	4.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.8$ mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.8$ mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND STROBE = V_{CC}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V	0.25	0.4	0.55	0.65	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		22	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		24	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, W Output	$R_L=1$ kΩ $C_L=50$ pF	19	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, Y Output	$R_L=1$ kΩ $C_L=50$ pF	19	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1$ kΩ $C_L=5$ pF	26	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1$ kΩ $C_L=5$ pF	27	40	ns

AC Electrical Characteristics V_{CC} = 5.0V ±10%, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HC $T_A=-40°C$ to $+85°C$		54HC $T_A=-55°C$ to $+125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		33	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		33	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to Y		27	40	50	60	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to W		27	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time W Output	$R_L=1$ kΩ	21	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output	$R_L=1$ kΩ	21	30	38	45	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1$ kΩ	22	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1$ kΩ	23	40	50	60	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	23	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per Package)	110				pF
C_{IN}	Maximum Input Capacitance		5	10			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

MM54HCT253/MM74HCT253 Dual 4-Channel TRI-STATE® Multiplexer

General Description

The MM54HCT253/MM74HCT253 utilizes advanced silicon-gate CMOS technology to achieve the low power consumption of standard CMOS integrated circuits, along with the capability to drive 10 LS-TTL loads. The large output drive and TRI-STATE features of this device make it ideally suited for interfacing with bus lines in bus organized systems. When the output control input is taken high, the multiplexer outputs are sent into a high impedance state.

When the output control is held low, the associated multiplexer chooses the correct output channel for the given input signals determined by the select A and B inputs.

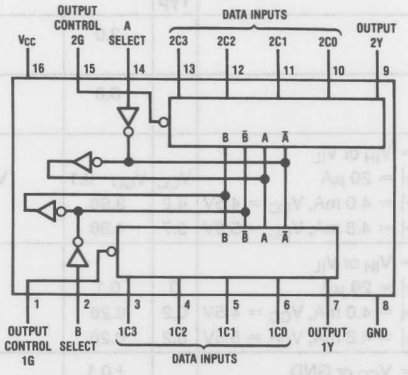
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

Connection Diagram

Dual-In-Line Package



TL/F/8434–1

Top View

Order Number MM54HCT253* or MM74HCT253*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable = V_{IH} or V_{IL}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.6	0.8	1.0	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, $t_r = t_f$ = 6 ns, C_L = 15 pF

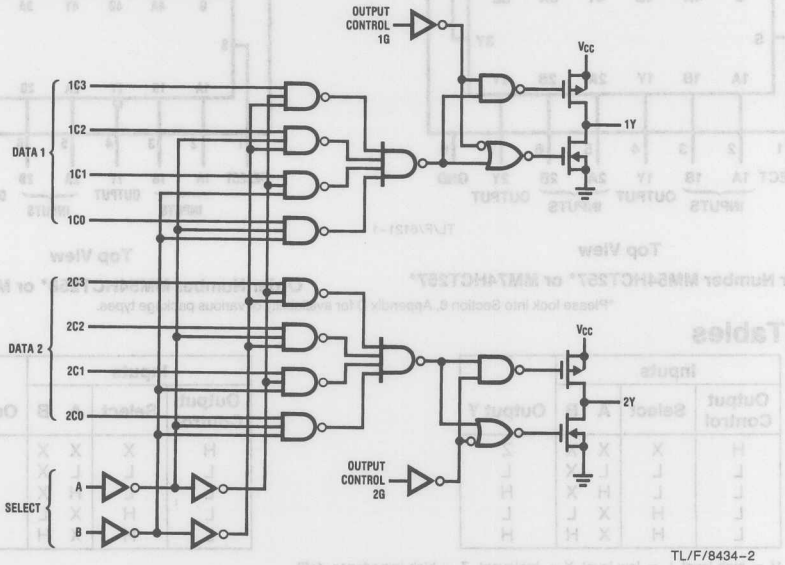
Symbol	Parameter	Conditions	Typ	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output to a Logic Level	R_L = 1k	15	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output to High Impedance State	R_L = 1k	11	ns

AC Electrical Characteristics C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C			74HC T_A = −40°C to 85°C		54HC T_A = 55°C to 125°C		Units
			Min	Typ	Max	Min	Max	Min	Max	
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y			26	40		50		60	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, and Data to Y			24	35		44		53	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ		19	26		33		39	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ		13	20		25		30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			8	15		19		22	ns
C_{IN}	Maximum Input Capacitance			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Output Enabled Outputs Disabled		90 25						pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/8434–2

National Semiconductor

MM54HCT257/MM74HCT257 Quad 2-Channel TRI-STATE® Multiplexer

MM54HCT258/MM74HCT258 Quad 2-Channel TRI-STATE® Multiplexer (Inverted Output)

General Description

These Quad 2-to-1 line date selector/multiplexers utilize advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, these possess the ability to drive LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make these devices ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, A or B data is selected for the HCT257 while $\overline{A}$ or $\overline{B}$ data is selected for the HCT258.

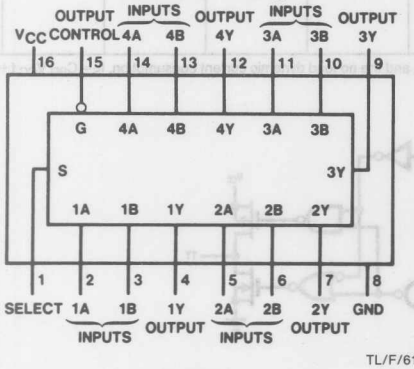
The 54HCT/74HCT logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Power supply range: 5V ±10%
- Low quiescent current: 80 μA maximum (74HC Series)
- Completely TTL compatible
- TRI-STATE outputs for connection to system buses
- Added circuitry allows data input levels to float during TRI-STATE with no additional power consumption
- High output drive current: 60 mA minimum

Connection Diagrams

Dual-In-Line Package

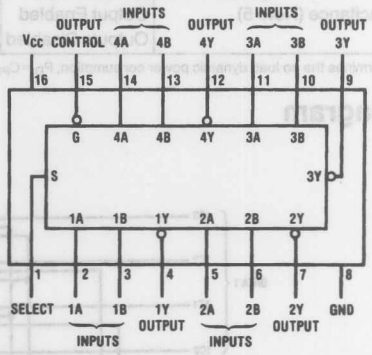


TL/F/6121–1

Top View

Order Number MM54HCT257* or MM74HCT257*

Dual-In-Line Package



TL/F/6121–2

Top View

Order Number MM54HCT258* or MM74HCT258*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering, 10 sec.)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 4.5V		500	ns

DC Electrical Characteristics (Note 4) V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			0.9	0.9	0.9	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	4.5	4.4	4.4	4.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA, V_{CC} = 4.5V $\|I_{OUT}\| \leq 7.2$ mA, V_{CC} = 5.5V	4.2	3.98 4.98	3.84 4.84	3.7 4.7	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA, V_{CC} = 4.5V $\|I_{OUT}\| \leq 7.2$ mA, V_{CC} = 5.5V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND OC = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.2	1.4	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

t_{PHL}, t_{PLH}	Maximum Propagation Select to any Output		16		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A or B to any Output		12		ns
t_{PZH}, t_{PZL}	Maximum Enable Time	$R_L = 1\ k\Omega$	23		ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time	$R_L = 1\ k\Omega$ $C_L = 5\ pF$	8		ns

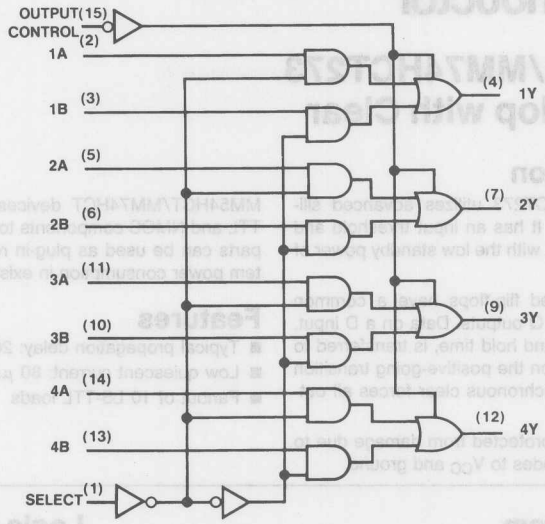
AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $t_r = t_f = 6$ ns, $C_L = 50$ pF (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40°C$ to $+85°C$	54HCT $T_A = -55°C$ to $+125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Output		18	24	30	36	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Output		15	20	25	30	ns
t_{PZH}, t_{PZL}	Maximum Enable to any Output	$R_L = 1k$ $C_L = 50$ pF		34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time	$R_L = 1k$ $C_L = 50$ pF	15	21	26	32	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Times			12	15	18	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		44				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

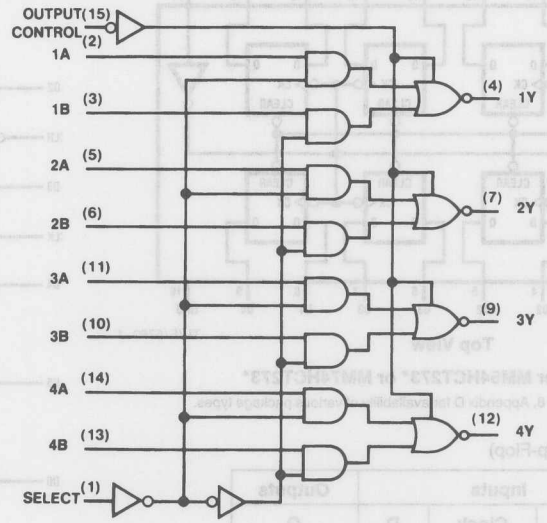
Logic Diagrams

'HCT257



TL/F/6121–3

'HCT258



TL/F/6121–4

4

National Semiconductor

MM54HCT273/MM74HCT273
Octal D Flip-Flop with Clear

General Description

The MM54HCT273/MM74HCT273 utilizes advanced silicon-gate CMOS technology. It has an input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These positive edge-triggered flip-flops have a common clock and clear-independent Q outputs. Data on a D input, having the specified set-up and hold time, is transferred to the corresponding Q output on the positive-going transition of the clock pulse. The asynchronous clear forces all outputs low when it is low.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

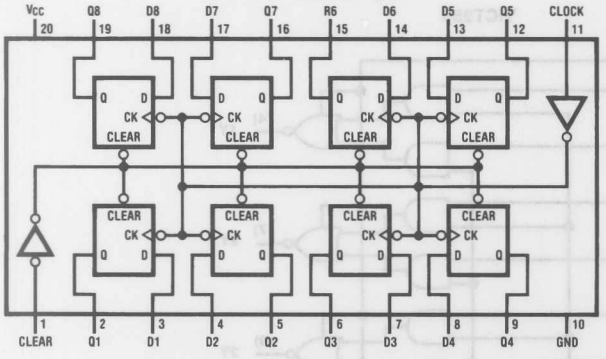
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. These parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



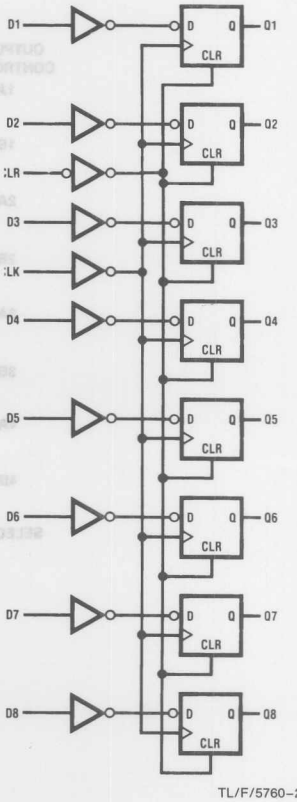
TL/F/5760–1

Top View

Order Number MM54HCT273* or MM74HCT273*

*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



TL/F/5760–2

Truth Table (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = high level (steady-state)

L = low level (steady-state)

X = don't care

↑ = transition from low to high level

Q0 = the level of Q before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to + 150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Minimum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.6	0.8	0.9	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		68	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		21	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−1	5	ns
t_S	Minimum Set-Up Time D to Clock		6	20	ns
t_H	Minimum Hold Time Clock to D		−3	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40°C$ to $85°C$	54HCT $T_A = -55°C$ to $125°C$	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		68	27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		22	37	46	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		25	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock		−1	5	6	7	ns
t_S	Minimum Set-Up Time D to Clock		6	20	25	30	ns
t_H	Minimum Hold Time Clock to D		−3	5	5	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	25	30	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		11	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)	50				pF
C_{IN}	Maximum Input Capacitance		6	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC}^2 f + I_{CC}$.

National Semiconductor

MM54HCT373/MM74HCT373 TRI-STATE® Octal D-Type Latch MM54HCT374/MM74HCT374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT373/MM74HCT373 octal D-type latches and MM54HCT374/MM74HCT374 Octal D-type flip flops advanced silicon-gate CMOS technology, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The TRI-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT373/MM74HCT373 LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT374/MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

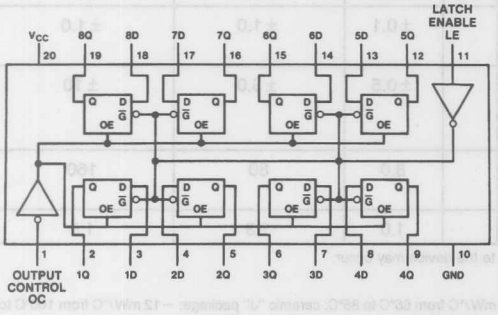
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package

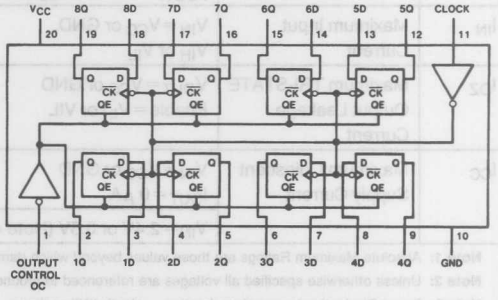


TL/F/5367–1

Top View

'HC373

Order Number MM54HCT373* or MM74HCT373*



TL/F/5367–2

Top View

'HC374

Order Number MM54HCT374* or MM74HCT374*

*Please look into Section 8, Appendix D for availability of various package types.

4

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable = V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT373/MM74HCT373

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 45 pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 45 pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 5 pF R_L = 1 kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT373/MM74HCT373

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 50 pF C_L = 150 pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 50 pF C_L = 150 pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF C_L = 150 pF R_L = 1 kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC = V_{CC} OC = GND		5 52			pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table

'373

Output Control	LE	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

'374

Output Control	Clock	Data	Output (374)
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level

X = Don't Care

↑ = Transition from low-to-high

Z = High impedance state

Q_0 = The level of the output before steady state input conditions were established.

AC Electrical Characteristics MM54HCT374/MM74HCT374

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	C_L = 45 pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 5 pF R_L = 1 kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT374/MM74HCT374

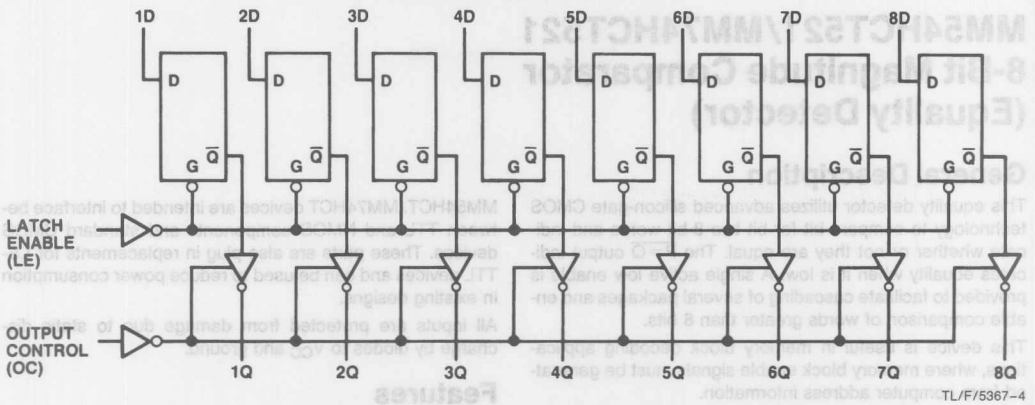
V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency		30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	C_L = 50 pF C_L = 150 pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF C_L = 150 pF R_L = 1 kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC = V_{CC} OC = GND		5 58			pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

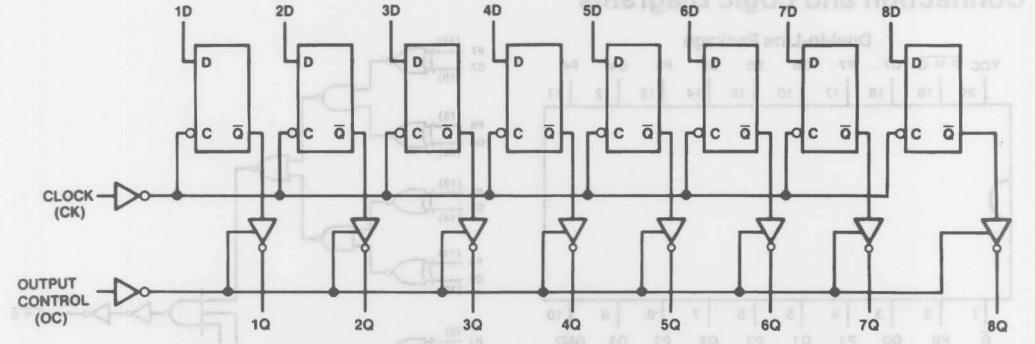
Logic Diagrams

MM54HCT373/MM74HCT373



TL/F/5367–4

MM54HCT374/MM74HCT374



TL/F/5367–5

4

MM54HCT521/MM74HCT521 8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicate whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator combines the low power consumption of CMOS, but inputs are compatible with TTL logic levels, and the output can drive 10 low power Schottky equivalent loads.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

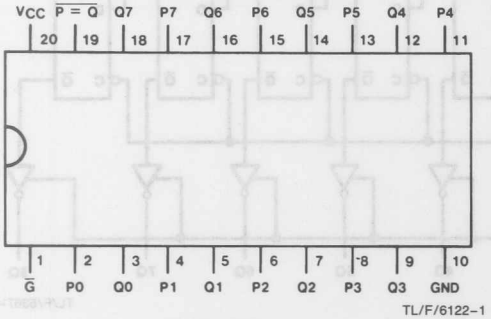
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Same as 'HCT688

Connection and Logic Diagrams

Dual-In-Line Package

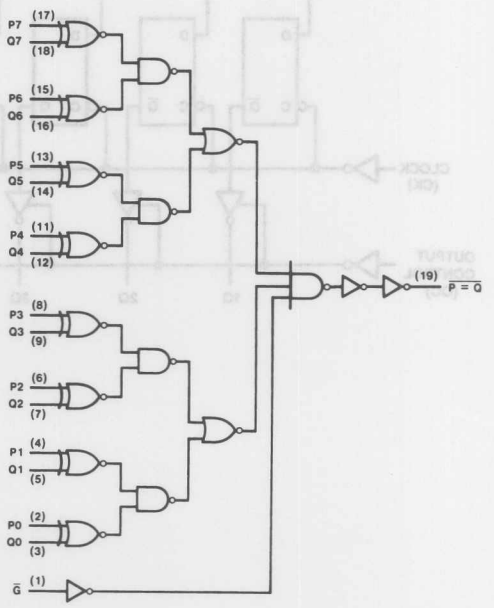


TL/F/6122–1

Top View

Order Number MM54HCT521* or MM74HCT521*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/6122–2

Truth Table

Inputs		$\overline{P=Q}$
Data P, Q	Enable $\overline{G}$	
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT688	−40	+85	°C
MM54HCT688	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = 0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.4V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25°C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay - P or Q to Output		19	30	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		13	22	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		13	20	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		10	18	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$	54HCT $T_A = -55$ to $125°C$	Units
			Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay - P or Q to Output		23	35	44	53	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		16	24	30	36	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		16	24	30	36	ns
t_{PLH}	Maximum Propagation Delay - Enable to Output		11	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		45				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} + I_{CC}$.

MM54HCT533/MM74HCT533 TRI-STATE® Octal D-Type Latch with Inverted Outputs MM54HCT534/MM74HCT534 TRI-STATE Octal D-Type Flip-Flop with Inverted Outputs

General Description

The MM54HCT533/MM74HCT533 octal D-type latches and MM54HCT534/MM74HCT534 Octal D-type flip-flops utilize advanced silicon-gate CMOS technology which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The TRI-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT533/MM74HCT533 LATCH ENABLE input is high, the data present on the D inputs will appear inverted at the QBar outputs. When the LATCH ENABLE goes low, the inverted data will be retained at the QBar outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT534/MM74HCT534 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are inverted and transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 18 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Truth Tables

'HCT533

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

'HCT534

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
$\overline{Q}_0$ = The level of the output before steady state Input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage		0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}				
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}				
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT533/MM74HCT533

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 45 pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 45 pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 5 pF R_L = 1 kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT533/MM74HCT533

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	C_L = 50 pF C_L = 150 pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	C_L = 50 pF C_L = 150 pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF C_L = 150 pF R_L = 1 kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC = V_{CC} OC = GND	5 55				pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

4

AC Electrical Characteristics MM54HCT534/MM74HCT534

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	C_L = 45 pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 5 pF R_L = 1 kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT534/MM74HCT534

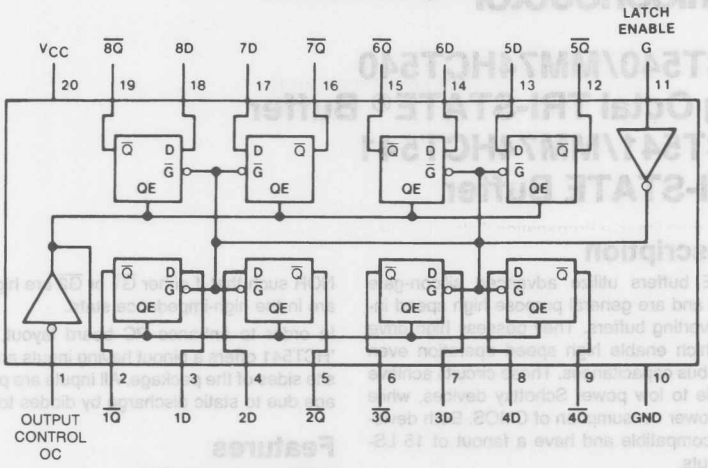
V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	C_L = 50 pF C_L = 150 pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF C_L = 150 pF R_L = 1 kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC = V_{CC} OC = GND	5 50				pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Connection Diagram

Dual-In-Line Package



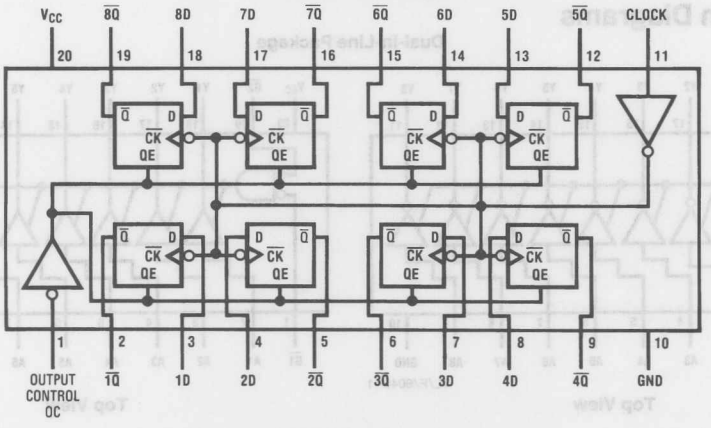
TL/F/6123–1

Top View

Order Number MM54HCT533* or MM74HCT533*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/6123–2

Top View

Order Number MM54HCT534* or MM74HCT534*

*Please look into Section 8, Appendix D for availability of various package types.

4

MM54HCT540/MM74HCT540 Inverting Octal TRI-STATE® Buffer MM54HCT541/MM74HCT541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize advanced silicon-gate CMOS technology and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. Both devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT540/MM74HCT540 is an inverting buffer and the MM54HCT541/MM74HCT541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

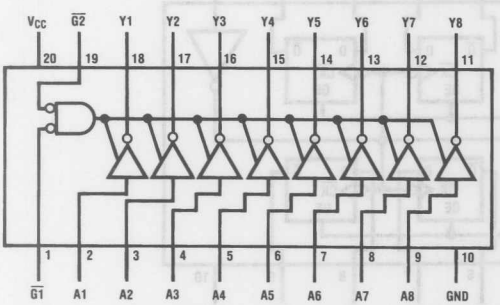
In order to enhance PC board layout, the 'HCT540 and 'HCT541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- Output current: 6 mA (min.)

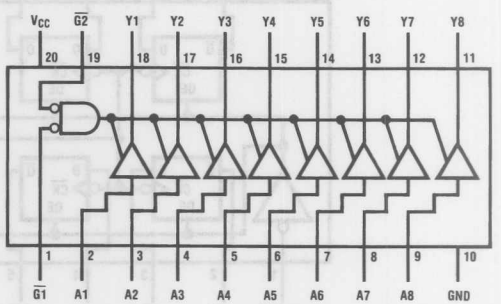
Connection Diagrams

Dual-In-Line Package



TL/F/6040–1

Top View



TL/F/6040–2

Top View

Order Number MM54HCT540* or MM74HCT540*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

AC Electrical Characteristics MM54HCT540/MM74HCT540

V_{CC} = 5.0V, t_r = t_f = 6 ns, T_A = 25°C, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	14	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	13	25	ns

AC Electrical Characteristics MM54HCT540/MM74HCT540

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		12	20	25	30	ns
		C_L = 150 pF		22	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	15	30	38	45	ns
			C_L = 150 pF	20	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$	12				pF
			$\overline{G}$ = GND	50				pF

AC Electrical Characteristics MM54HCT541/MM74HCT541

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	15	25	ns

AC Electrical Characteristics MM54HCT541/MM74HCT541

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		14	23	29	34	ns
		C_L = 150 pF		17	33	42	49	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	17	30	38	45	ns
			C_L = 150 pF	22	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		17	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$	12				pF
			$\overline{G}$ = GND	45				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

MM54HCT640/MM74HCT640 Inverting Octal TRI-STATE® Transceiver
MM54HCT643/MM74HCT643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional transceivers utilize advanced silicon-gate CMOS technology and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

All devices are TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Both the MM54HCT640/MM74HCT640 and the MM54HCT643/ MM74HCT643 have one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The MM54HCT640/MM74HCT640 transfers inverted data from one bus to the other. The MM54HCT643/MM74HCT643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus.

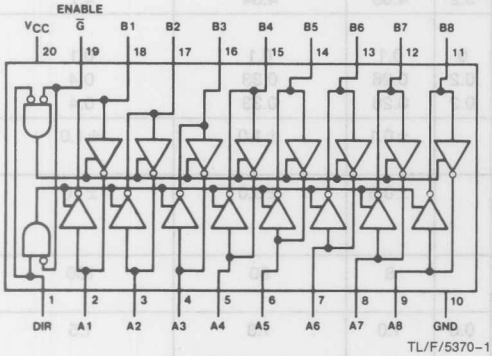
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typical
- High speed: 16 ns typical propagation delay
- Low power: 80 μA maximum (74HCT)

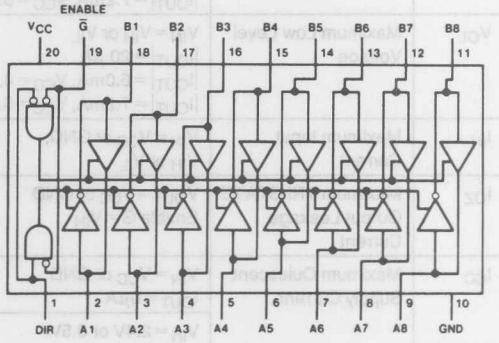
Connection Diagram

Dual-In-Line Packages



TL/F/5370–1

Top View
Order Number MM54HCT640* or MM74HCT640*



TL/F/5370–2

Top View
Order Number MM54HCT643* or MM74HCT643*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}-0.1	V_{CC}-0.1	V_{CC}-0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable $\overline{G}$=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC}=5.0V, t_r=t_f=6 ns, T_A=25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L=45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L=45 pF R_L=1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L=5 pF R_L=1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF	17	23	29	34	ns
		C_L = 150 pF	24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1kΩ, C_L = 50 pF	23	30	38	45	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1kΩ, C_L = 50 pF	21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output/ Input Capacitance		20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output) $\overline{G}$ = V_{CC}	7				pF
		$\overline{G}$ = GND	100				pF

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF, R_L = 1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF, R_L = 1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C		74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF	17	23	29	34	ns
		C_L = 150 pF	24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ, C_L = 50 pF	23	30	38	45	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ, C_L = 50 pF	21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	8	12	15	18	ns
C_{IN}	Maximum Input Capacitance		10	15	15	15	pF
C_{OUT}	Maximum Output/ Input Capacitance		20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output) $\overline{G}$ = V_{CC}	7				pF
		$\overline{G}$ = GND	100				pF

Note 5: C_{PD} determines the no load power consumption. $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. The no load dynamic current consumption, $I_S = C_{PD} V_{CC} + I_{CC}$.

National Semiconductor

MM54HCT688/MM74HCT688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes advanced silicon-gate CMOS technology to compare bit for bit two 8-bit words and indicate whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator combines the low power consumption of CMOS, but inputs are compatible with TTL logic levels, and the output can drive 10 low power Schottky equivalent loads.

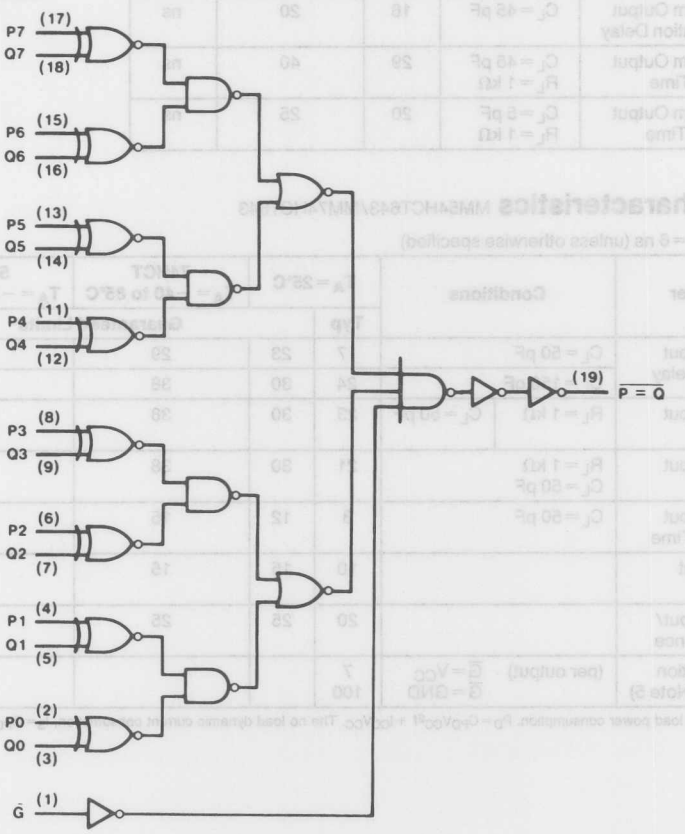
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Large output current: 4 mA
- Same as HCT521

Logic Diagrams



TL/F/5371–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT688	−40	+85	°C
MM54HCT688	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC} = 5V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = 0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All other inputs held at V_{CC} or ground.

t_{PHL}	Maximum Propagation Delay - P or Q to Output		19	30		ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		13	22		ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		13	20		ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		10	18		ns

AC Electrical Characteristics

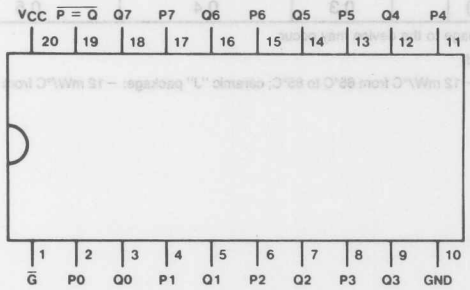
V_{CC} = 5V ±10%, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25°C$		74HCT $T_A = -40$ to 85°C	54HCT $T_A = -55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay - P or Q to Output		23	35	44	53	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		16	24	30	36	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		16	24	30	36	ns
t_{PLH}	Maximum Propagation Delay - Enable to Output		11	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		45				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} + I_{CC}$.

Connection Diagram

Dual-In-Line Package



TL/F/5371–1

Top View

Order Number MM54HCT688* or MM74HCT688*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs		
Data P, Q	Enable $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Section 5
CD4XXX

Section 5 Contents

CD4000M/CD4000C Dual 3-Input NOR Gate Plus Inverter 5-3
CD4001M/CD4001C Quad 2-Input NOR Gate 5-6
CD4011M/CD4011C Quad 2-Input NAND Gate 5-6
CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate 5-10
CD4011BM/CD4011BC Quad 2-Input NAND Gate 5-10
CD4002M/CD4002C Dual 4-Input NOR Gate 5-15
CD4012M/CD4012C Dual 4-Input NAND Gate 5-15
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CD4020BM/CD4020BC 14-Stage Ripple-Carry Binary Counter/Divider 5-70
CD4040BM/CD4040BC 12-Stage Ripple-Carry Binary Counter/Divider 5-70
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CD4021BM/CD4021BC 8-Stage Static Shift Register 5-75
CD4023M/CD4023C Triple 3-Input NOR Gate 5-80
CD4025M/CD4025C Triple 3-Input NAND Gate 5-80
CD4023BM/CD4023BC Triple 3-Input Buffered NAND Gate 5-84
CD4025BM/CD4025BC Triple 3-Input Buffered NOR Gate 5-84
CD4024BM/CD4024BC 7-Stage Ripple-Carry Binary Counter/Divider 5-88
CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset 5-92
CD4028BM/CD4028BC BCD-to-Decimal Decoder 5-97
CD4029BM/CD4029BC Presettable Binary/Decade Up/Down Counter 5-100
CD4030M/CD4030C Quad Exclusive-OR Gate 5-106
CD4031BM/CD4031BC 64-Stage Static Shift Register 5-109
CD4034BM/CD4034BC 8-Stage TRI-STATE Bidirectional Parallel/Serial Input/Output Bus Register 5-113
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CD4044BM/CD4044BC TRI-STATE NAND R/S Latches 5-137
CD4046BM/CD4046BC Micropower Phase-Locked Loop 5-141
CD4047BM/CD4047BC Low Power Monostable/Astable Multivibrator 5-149
CD4048BM/CD4048BC TRI-STATE Expandable 8-Function 8-Input Gate 5-154
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CD4050BM/CD4050BC Hex Non-Inverting Buffer 5-161

Section 5 Contents (Continued)

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CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate 5-188
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate 5-188
CD4072BM/CD4072BC Dual 4-Input OR Buffered B Series Gate 5-194
CD4082BM/CD4082BC Dual 4-Input AND Buffered B Series Gate 5-194
CD4073BM/CD4073BC Double Buffered Triple 3-Input AND Gate 5-197
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CD4089BM/CD4089BC Binary Rate Multiplier 5-206
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CD4093BM/CD4093BC Quad 2-Input NAND Schmitt Trigger 5-214
CD4094BM/CD4094BC 8-Bit Shift Register/Latch with TRI-STATE Outputs 5-219
CD4099BM/CD4099BC 8-Bit Addressable Latches 5-224
CD40106BM/CD40106BC Hex Schmitt Trigger 5-229
CD40160BM/CD40160BC Decade Counter with Asynchronous Clear 5-233
CD40161BM/CD40161BC Binary Counter with Asynchronous Clear 5-233
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CD40163BM/CD40163BC Binary Counter with Synchronous Clear 5-233
CD40174BM/CD40174BC Hex D Flip-Flop 5-238
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CD4520BM/CD4520BC Dual Synchronous Up Counter 5-275
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CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector 5-298
CD4538BM/CD4538BC Dual Monostable Multivibrator 5-304
CD4541BM/CD4541BC Programmable Timer with Oscillator 5-312
CD4543BM/CD4543BC BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystal Displays 5-317
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Section 5 Contents (Continued)

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexers/Demultiplexers 5-166
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexers/Demultiplexers 5-166
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National Semiconductor

CD4000M/CD4000C Dual 3-Input NOR Gate Plus Inverter

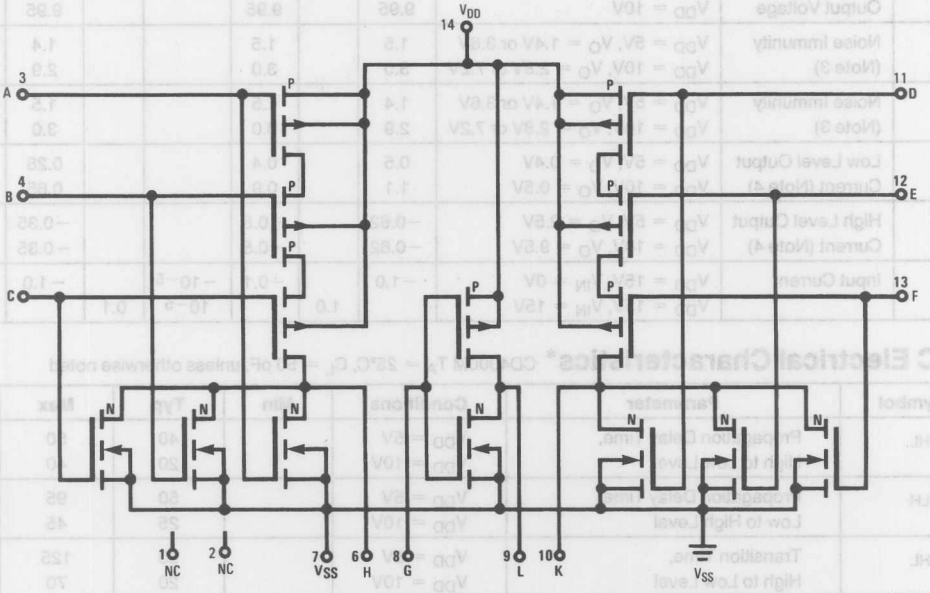
General Description

The CD4000M/CD4000C is a monolithic complementary MOS (CMOS) dual 2-input NOR gate plus an inverter. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge.

Features

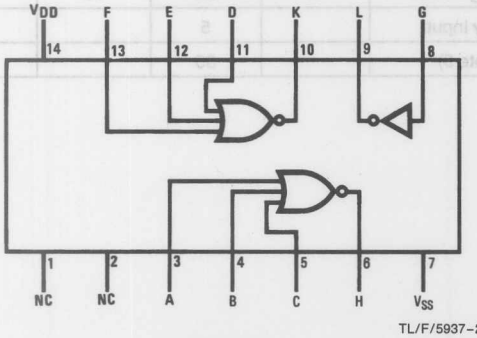
■ Wide supply voltage range	3.0V to 15V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Schematic and Connection Diagrams



TL/F/5937–1

Dual-In-Line Package



TL/F/5937–2

Top View

Order Number CD4000*

*Please look into Section 8, Appendix D for availability of various package types.

5

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$

Operating Temperature Range (T_A)
- CD4000M $-55°C$ to $+125°C$
- CD4000C $-40°C$ to $+85°C$

Storage Temperature Range (T_S) $-65°C$ to $+150°C$

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Operating V_{DD} Range $V_{SS} + 3V$ to $V_{SS} + 15V$

Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

DC Electrical Characteristics CD4000M (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.05			0.05		3	μA
		$V_{DD} = 10V$		0.1			0.1		6	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	$V_{DD} = 5V, V_O = 1.4V$ or $3.6V$	1.5		1.5			1.4		V
		$V_{DD} = 10V, V_O = 2.8V$ or $7.2V$	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	$V_{DD} = 5V, V_O = 1.4V$ or $3.6V$	1.4		1.5			1.5		V
		$V_{DD} = 10V, V_O = 2.8V$ or $7.2V$	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 0.4V$	0.5		0.4			0.28		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.1		0.9			0.65		mA
I_{DP}	High Level Output Current (Note 4)	$V_{DD} = 5V, V_O = 2.5V$	−0.62		−0.5			−0.35		mA
		$V_{DD} = 10V, V_O = 9.5V$	−0.62		−0.5			−0.35		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$	−1.0		−0.1	-10^{-5}		−1.0		μA
		$V_{DD} = 15V, V_{IN} = 15V$		1.0		10^{-5}	0.1		1.0	μA

AC Electrical Characteristics* CD4000M $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High to Low Level	$V_{DD} = 5V$		40	50	ns
		$V_{DD} = 10V$		20	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5V$		50	95	ns
		$V_{DD} = 10V$		25	45	ns
t_{THL}	Transition Time, High to Low Level	$V_{DD} = 5V$		50	125	ns
		$V_{DD} = 10V$		20	70	ns
t_{TLH}	Transition Time, Low to High Level	$V_{DD} = 5V$		70	175	ns
		$V_{DD} = 10V$		35	75	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		35		pF

*AC Parameters are guaranteed by DC correlated testing.

DC Electrical Characteristics CD4000C (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.05			0.05		15	μA
		V_{DD} = 10V		5			5		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	V_{DD} = 5V, V_O = 1.4V or 3.6V	1.5		1.5			1.4		V
		V_{DD} = 10V, V_O = 2.8V or 7.2V	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	V_{DD} = 5V, V_O = 1.4V or 3.6V	1.4		1.5			1.5		V
		V_{DD} = 10V, V_O = 2.8V or 7.2V	2.9		3.0			3.0		V
I_{DL}	Low Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.35		0.3			0.24		mA
		V_{DD} = 10V, V_O = 0.5V	0.72		0.6			0.48		mA
I_{DP}	High Level Output Current (Note 4)	V_{DD} = 5V, V_O = 2.5V	−0.35		−0.3			−0.24		mA
		V_{DD} = 10V, V_O = 9.5V	−0.3		−0.25			−0.2		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.1		1.0	μA

AC Electrical Characteristics* CD4000C T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High to Low Level	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		20	55	ns
t_{PLH}	Propagation Delay Time Low to High Level	V_{DD} = 5V		50	120	ns
		V_{DD} = 10V		25	65	ns
t_{THL}	Transition Time, High to Low Level	V_{DD} = 5V		50	200	ns
		V_{DD} = 10V		20	115	ns
t_{TLH}	Transition Time, Low to High Level	V_{DD} = 5V		70	300	ns
		V_{DD} = 10V		35	125	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		35		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: For the NOR gates V_{NH} and V_{NL} are tested at each input while all other inputs are at V_{SS}.

Note 4: I_{DN} and I_{DP} are tested one output at a time.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For explanation see 54C/74C Family Characteristics Application Note, AN-90.

CD4001M/CD4001C Quadruple 2-Input NOR Gate
CD4011M/CD4011C Quadruple 2-Input NAND Gate

General Description

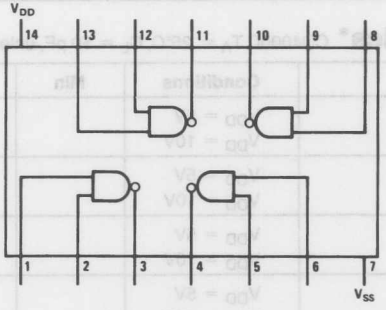
The CD4001M/CD4001C, CD4011M/CD4011C are monolithic complementary MOS (CMOS) quadruple two-input NOR and NAND gate integrated circuits. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

■ Wide supply voltage range	3.0V to 15V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Connection Diagrams

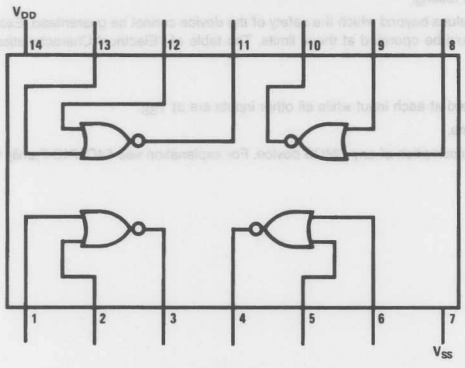
Dual-In-Line Package



TL/F/5938–1

Top View
CD4011M/CD4011C

Dual-In-Line Package



TL/F/5938–2

Top View
CD4001M/CD4001C

Order Number CD4001* or CD4011*

*Please look into Section 8, Appendix D for availability of various package types.

Distributors for availability and specifications.

Voltage on any Pin	$V_{SS}-0.3V$ to $V_{DD}+0.3V$
Operating Temperature Range	
CD4001M, CD4011M	$-55°C$ to $+125°C$
CD4001C, CD4011C	$-40°C$ to $+85°C$
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{DD} Range	$V_{SS}+3.0V$ to $V_{SS}+15V$
Lead Temp.(Soldering, 10 sec.)	260°C

DC Electrical Characteristics CD4001M, CD4011M

Symbol	Parameter	Conditions	Limits							Units
			$-55°C$		$+25°C$			$+125°C$		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD}=5.0V$		0.05		0.001	0.05		3.0	μA
		$V_{DD}=10V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD}=5.0V$		0.25		0.005	0.25		15	μW
		$V_{DD}=10V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage low Level	$V_{DD}=5.0V$, $V_I=V_{DD}$, $I_O=0A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$, $V_I=V_{DD}$, $I_O=0A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD}=5.0V$, $V_I=V_{SS}$, $I_O=0A$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10V$, $V_I=V_{SS}$, $I_O=0A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD}=5.0V$, $V_O=3.6V$, $I_O=0A$	1.5		1.5	2.25		1.4		V
		$V_{DD}=10V$, $V_O=7.2V$, $I_O=0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD}=5.0V$, $V_O=0.95V$, $I_O=0A$	1.4		1.5	2.25		1.5		V
		$V_{DD}=10V$, $V_O=2.9V$, $I_O=0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4001) (Note 2)	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4001) (Note 2)	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	-0.62		-0.5	-2.0		-0.35		mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	-0.62		-0.5	-1.0		-0.35		mA
I_DN	Output Drive Current N-Channel (4011) (Note 2)	$V_{DD}=5.0V$, $V_O=0.4V$, $V_I=V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD}=10V$, $V_O=0.5V$, $V_I=V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4011) (Note 2)	$V_{DD}=5.0V$, $V_O=2.5V$, $V_I=V_{SS}$	-0.31		-0.25	-0.5		-0.175		mA
		$V_{DD}=10V$, $V_O=9.5V$, $V_I=V_{SS}$	-0.75		-0.6	-1.2		-0.4		mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

DC Electrical Characteristics CD4001C, CD4011C

Symbol	Parameter	Conditions	Limits							Units
			−40°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	V_{DD} = 5.0V		0.5		0.005	0.5		15	μA
		V_{DD} = 10V		5.0		0.005	5.0		30	μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5.0V		2.5		0.025	2.5		75	μW
		V_{DD} = 10V		50		0.05	50		300	μW
V_{OL}	Output Voltage low Level	V_{DD} = 5.0V, V_I = V_{DD}, I_O = 0A		0.05		0	0.05		0.05	V
		V_{DD} = 10V, V_I = V_{DD}, I_O = 0A		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0V, V_I = V_{SS}, I_O = 0A	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 3.6V, I_O = 0A	1.5		1.5	2.25		1.4		V
		V_{DD} = 10V, V_O = 7.2V, I_O = 0A	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 0.95V, I_O = 0A	1.4		1.5	2.25		1.5		V
		V_{DD} = 10V, V_O = 2.9V, I_O = 0A	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4001) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}	0.35		0.3	1.0		0.24		mA
		V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.72		0.6	2.5		0.48		mA
I_DP	Output Drive Current P-Channel (4001) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}	−0.35		−0.3	−2.0		−0.24		mA
		V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.3		−0.25	−1.0		−0.2		mA
I_DN	Output Drive Current N-Channel (4011) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}	0.145		0.12	0.5		0.095		mA
		V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.3		0.25	0.6		0.2		mA
I_DP	Output Drive Current P-Channel (4011) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}	−0.145		−0.12	−0.5		−0.095		mA
		V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.35		−0.3	−1.2		−0.24		mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics*

T_A = 25°C, C_L = 15 pF, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of V_{DD} = 0.3%/°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4001M						
t_{PHL}	Propagation Delay Time High to Low Level	V_{DD} = 5.0V		35	50	ns
		V_{DD} = 10V		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	V_{DD} = 5.0V		35	65	ns
		V_{DD} = 10V		25	40	ns
t_{THL}	Transition Time High to Low Level	V_{DD} = 5.0V		65	125	ns
		V_{DD} = 10V		35	70	ns
t_{TLH}	Transition Time Low to High Level	V_{DD} = 5.0V		65	175	ns
		V_{DD} = 10V		35	75	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4001C						
t_{PHL}	Propagation Delay Time High to Low Level	V_{DD} = 5.0V		35	80	ns
		V_{DD} = 10V		25	55	ns
t_{PLH}	Propagation Delay Time Low to High Level	V_{DD} = 5.0V		35	120	ns
		V_{DD} = 10V		25	65	ns
t_{THL}	Transition Time High to Low Level	V_{DD} = 5.0V		65	200	ns
		V_{DD} = 10V		35	115	ns
t_{TLH}	Transition Time Low to High Level	V_{DD} = 5.0V		65	300	ns
		V_{DD} = 10V		35	125	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4011M						
t_{PHL}	Propagation Delay Time High to Low Level	V_{DD} = 5.0V		50	75	ns
		V_{DD} = 10V		25	40	ns
t_{PLH}	Propagation Delay Time Low to High Level	V_{DD} = 5.0V		50	75	ns
		V_{DD} = 10V		25	40	ns
t_{THL}	Transition Time High to Low Level	V_{DD} = 5.0V		75	125	ns
		V_{DD} = 10V		50	75	ns
t_{TLH}	Transition Time Low to High Level	V_{DD} = 5.0V		75	100	ns
		V_{DD} = 10V		40	60	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4011C						
t_{PHL}	Propagation Delay Time High to Low Level	V_{DD} = 5.0V		50	100	ns
		V_{DD} = 10V		25	50	ns
t_{PLH}	Propagation Delay Time Low to High Level	V_{DD} = 5.0V		50	100	ns
		V_{DD} = 10V		25	50	ns
t_{THL}	Transition Time High to Low Level	V_{DD} = 5.0V		75	150	ns
		V_{DD} = 10V		50	100	ns
t_{TLH}	Transition Time Low to High Level	V_{DD} = 5.0V		75	125	ns
		V_{DD} = 10V		40	75	ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

National Semiconductor

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

General Description

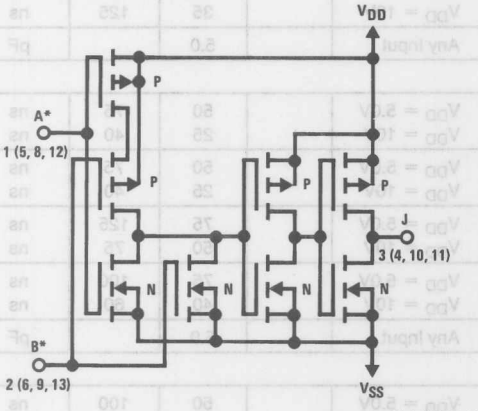
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

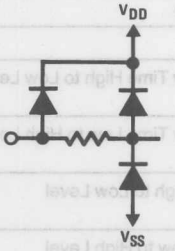
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Schematic Diagrams



TL/F/5939–1

CD4001BC/BM



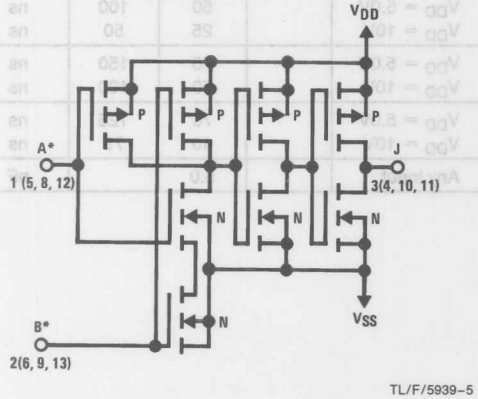
¼ of device shown

$J = \overline{A + B}$

Logical "1" = High
Logical "0" = Low

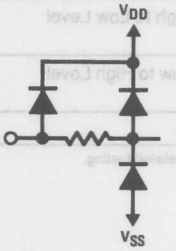
TL/F/5939–2

*All inputs protected by standard CMOS protection circuit.



TL/F/5939–5

CD4011BC/BM



¼ of device shown

$J = \overline{A \bullet B}$

Logical "1" = High
Logical "0" = Low

TL/F/5939–6

*All inputs protected by standard CMOS protection circuit.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin	$-0.5V$ to $V_{DD} + 0.5V$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

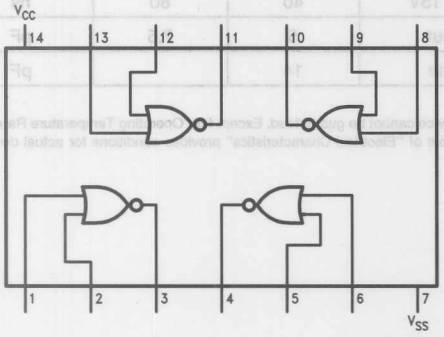
Operating Range (V_{DD})	$3\ V_{DC}$ to $15\ V_{DC}$
Operating Temperature Range	
CD4001BM, CD4011BM	$-55°C$ to $+125°C$
CD4001BC, CD4011BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4001BM, CD4011BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		0.50		0.005	0.50		15	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Connection Diagrams

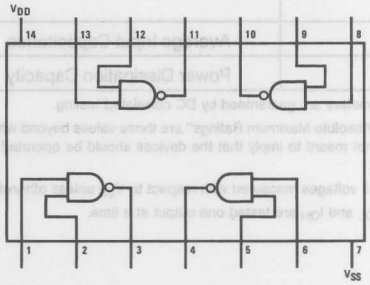
CD4001BC/CD4001BM
Dual-In-Line Package



TL/F/5939–3

Top View

CD4011BC/CD4011BM
Dual-In-Line Package



TL/F/5939–4

Top View

Order Number CD4001B* or CD4011B*

*Please look into Section 8, Appendix D for availability of various package types.

DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\|I_O\|$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\|I_O\|$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\|I_O\|$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\|I_O\|$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\|I_O\|$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\|I_O\|$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* CD4001BC, CD4001BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics* CD4011BC, CD4011BM

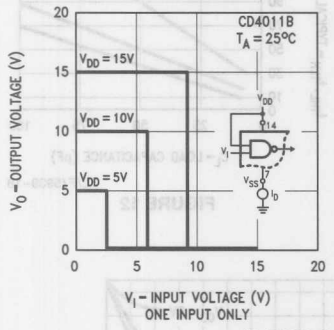
T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical Temperature Coefficient is 0.3%/°C.

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	V_{DD} = 5V	85	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

*AC Parameters are guaranteed by DC correlated testing.

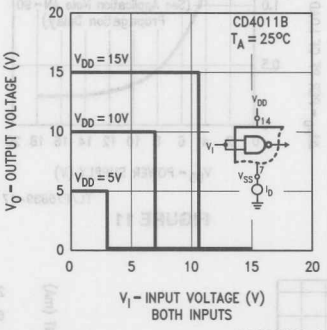
Typical Performance Characteristics

Typical Transfer Characteristics



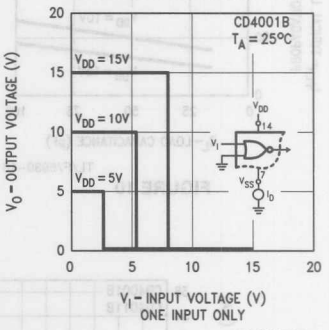
TL/F/5939–7

Typical Transfer Characteristics



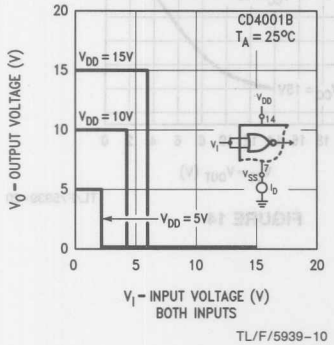
TL/F/5939–8

Typical Transfer Characteristics

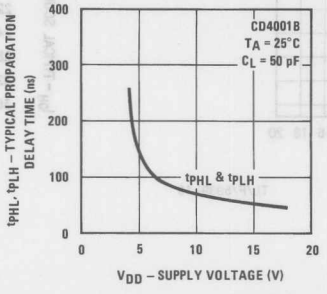


TL/F/5939–9

Typical Transfer Characteristics

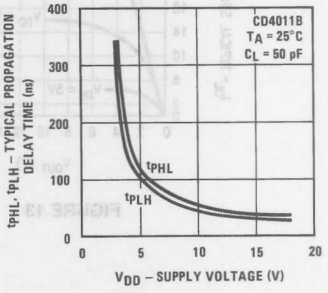


TL/F/5939–10



TL/F/5939–11

FIGURE 5



TL/F/5939–12

FIGURE 6

5

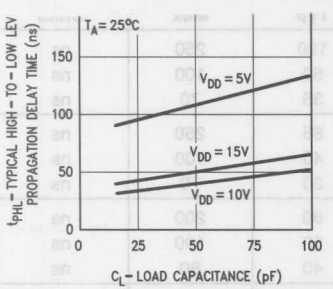


FIGURE 7

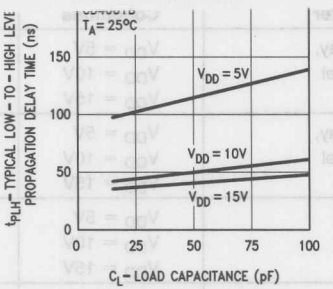


FIGURE 8

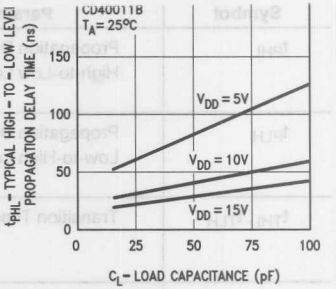


FIGURE 9

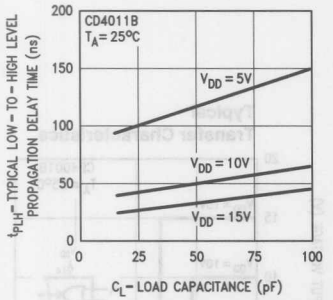


FIGURE 10

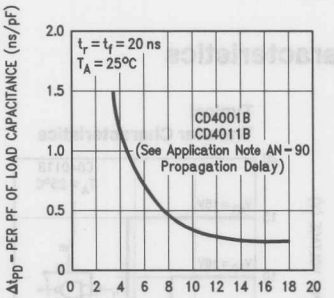


FIGURE 11

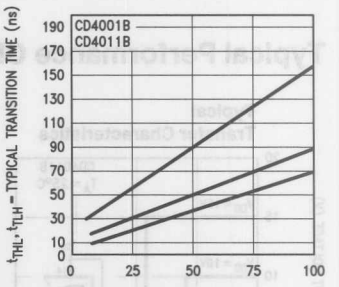


FIGURE 12

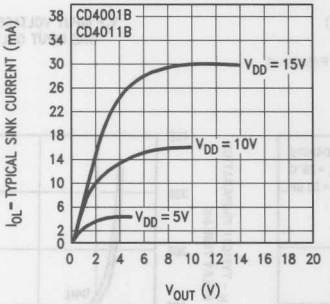


FIGURE 13

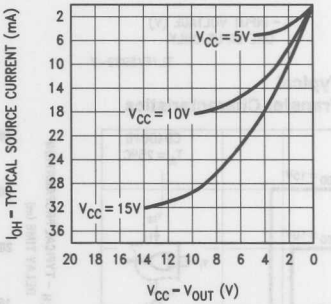


FIGURE 14

CD4002M/CD4002C Dual 4-Input NOR Gate
CD4012M/CD4012C Dual 4-Input NAND Gate

General Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

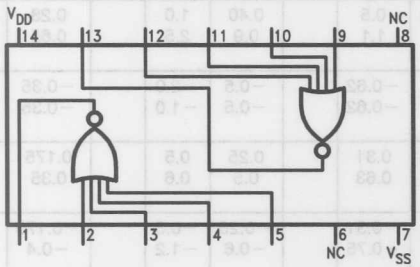
■ Wide supply voltage range	3.0V to 15V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical Electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Connection Diagrams

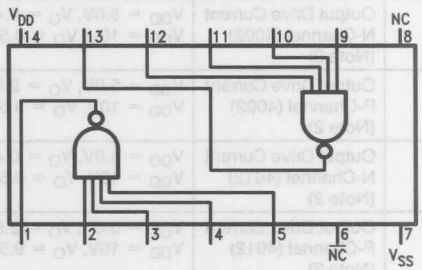
CD4002
Dual-In-Line Package



TL/F/5940–1

Top View

CD4012
Dual-In-Line Package



TL/F/5940–2

Top View

Order Number CD4002* or CD4012*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin V_{SS} −0.3V to V_{DD} +0.3V

Operating Temperature Range
- CD4002M, CD4012M −55°C to +125°C
- CD4002C, CD4012C −40°C to +85°C

Storage Temperature Range (T_S) −65°C to +150°C

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Operating Range (V_{DD}) V_{SS} +3.0V to V_{SS} +15V

Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

DC Electrical Characteristics CD4002M, CD4012M

Symbol	Parameter	Conditions	Limits							Units
			−55°C		+25°C			+125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0V		0.05		0.001	0.05		3.0	μA
		V_{DD} = 10V		0.1		0.001	0.1		6	μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5.0V		0.25		0.005	0.25		15	μW
		V_{DD} = 10V		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5.0V, V_I = V_{DD}, I_O = 0A		0.05		0	0.05		0.05	V
		V_{DD} = 10V, V_I = V_{DD}, I_O = 0A		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0V, V_I = V_{SS}, I_O = 0A	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 3.6V, I_O = 0A	1.5		1.5	2.25		1.4		V
		V_{DD} = 10V, V_O = 7.2V, I_O = 0A	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O = 0.95V, I_O = 0A	1.4		1.5	2.25		1.5		V
		V_{DD} = 10V, V_O = 2.9V, I_O = 0A	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}	0.5		0.40	1.0		0.28		mA
		V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}	−0.62		−0.5	−2.0		−0.35		mA
		V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.62		−0.5	−1.0		−0.35		mA
I_DN	Output Drive Current N-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}	0.31		0.25	0.5		0.175		mA
		V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}	−0.31		−0.25	−0.5		−0.175		mA
		V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.75		−0.6	−1.2		−0.4		mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

DC Electrical Characteristics CD4002C, CD4012C

Symbol	Parameter	Conditions	Limits							Units
			−55°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0V V_{DD} = 10V		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5.0V V_{DD} = 10V		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5.0V, V_I = V_{DD}, I_O = 0A V_{DD} = 10V, V_I = V_{DD}, I_O = 0A		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0V, V_I = V_{SS}, I_O = 0A V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O ≥ 3.6V, I_O = 0A V_{DD} = 10V, V_O ≥ 7.2V, I_O = 0A	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0V, V_O ≤ 0.95V, I_O = 0A V_{DD} = 10V, V_O ≤ 2.9V, I_O = 0A	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD} V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_DN	Output Drive Current N-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD} V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I_DP	Output Drive Current P-Channel (4002) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS} V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_DP	Output Drive Current P-Channel (4012) (Note 2)	V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS} V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4002M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4002C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
T_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4012M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4012C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
T_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

National Semiconductor

CD4002BM/CD4002BC Dual 4-Input NOR Gate
CD4012BM/CD4012BC Dual 4-Input NAND Gate

General Description

These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with doides to V_{DD} and V_{SS}.

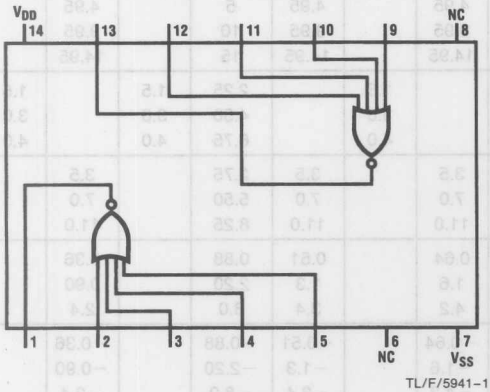
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fanout of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage: μA at 15V over full temperature range

Connection Diagrams

Dual-In-Line Packages

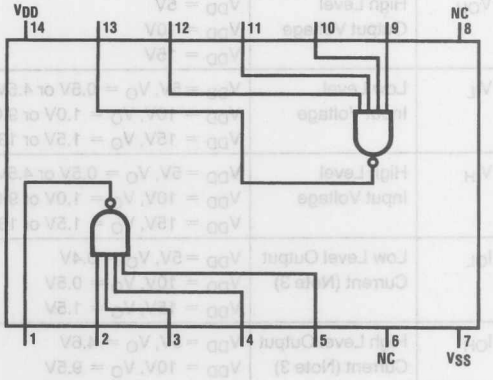
CD4002BM/CD4002BC



TL/F/5941–1

Top View

CD4012BM/CD4012BC



TL/F/5941–2

Top View

Order Number CD4002B* or CD4012B*

*Please look into Section 8, Appendix D for availability of package types.

5

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3.0V to 15V
Input Voltage (V_{IN})	0V to V_{DD} V
Operating Temperature Range (T_A)	
CD4002BM, CD4012BM	−55°C to +125°C
CD4002BC, CD4012BC	−40°C to +85°C

DC Electrical Characteristics CD4002BM, CD4012BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5		0.005	0.5		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.20		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.20		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4002BC, CD4012BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0		0.004	1.0		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0		0.005	2.0		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0		0.006	4.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay High to Low Level	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		60	100	ns
		V_{DD} = 15V		45	70	ns
t_{PLH}	Propagation Delay Low to High Level	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		60	100	ns
		V_{DD} = 15V		45	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	Any Gate		20		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics, Application Note AN-90.

5

CD4006BM/CD4006BC 18-Stage Static Shift Register

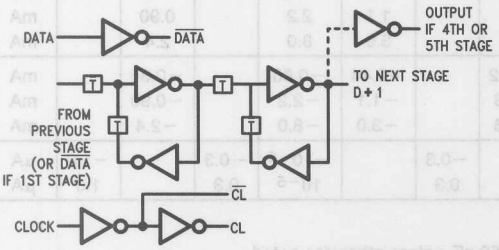
General Description

The CD4006BM/CD4006BC 18-stage static shift register is comprised of four separate shift register sections, two sections of four stages and two sections of five stages. Each section has an independent data input. Outputs are available at the fourth stage and the fifth stage of each section. A common clock signal is used for all stages. Data is shifted to the next stage on the negative-going transition of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages, or single register sections of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one package.

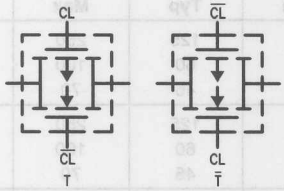
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Low clock input capacitance — 6 pF (typ.)
- Medium speed — 10 MHz (typ.) (with V_{DD} = 10V)
- Low power
- Fully static operation

Logic Diagrams



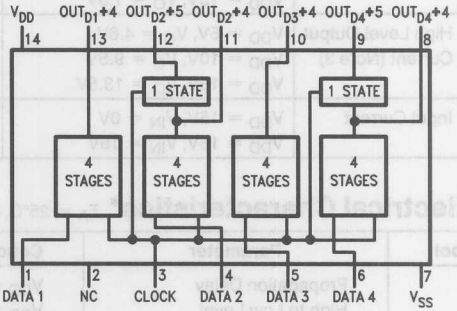
TL/F/5942–1



TL/F/5942–3

Connection Diagram

Dual-In-Line Package



TL/F/5942–2

Top View

Order Number CD4006B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

D	CL Δ	D+1
0	⎍	0
1	⎍	1
X	⎍	NC

TL/F/5942–4

X = Don't care
Δ = Level change
NC = No change

Input Voltage (V_{IN}) -0.5 to $V_{DD} + 0.5$ V_{DC}

Storage Temperature Range (T_S) $-65°C$ to $+150°C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Operating Temperature Range (T_A)

CD4006BM $-55°C$ to $+125°C$

CD4006BC $-40°C$ to $+85°C$

DC Electrical Characteristics CD4006BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5.0V$, $V_{IN} = V_{DD}$ or V_{SS}		5.0		0.005	5.0		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.010	10		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5.0V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5.0V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5.0V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5.0V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	−0.1		−0.1	-10^{-5}		−1.0		μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4006BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5.0V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.005	20		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		40		0.010	40		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5.0V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5.0V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4006BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11		11	8.25		11		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* CD4006BM/CD4006BC T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time (t_{PLH} = t_{PHL})	V_{DD} = 5.0V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	150	ns
t_{TLH}, t_{THL}	Transition Time (t_{TLH} = t_{THL})	V_{DD} = 5.0V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{DD} = 5.0V		100	200	ns
		V_{DD} = 10V		45	100	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FCL}	Clock Rise and Fall Time (t_{RCL} = t_{FCL})	V_{DD} = 5.0V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5.0V		50	100	ns
		V_{DD} = 10V		25	50	ns
		V_{DD} = 15V		20	40	ns
t_H	Minimum Hold Time	V_{DD} = 5.0V		55	110	ns
		V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		30	60	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5.0V	2.5	5.0		MHz
		V_{DD} = 10V	5.0	12		MHz
		V_{DD} = 15V	7.0	16		MHz
C_L	Input Capacitance	Data Input		5.0		pF
		CLK Input		7.5		pF

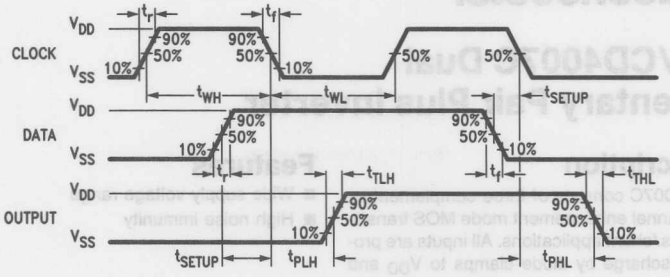
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Switching Time Waveforms



TL/F/5942–5

National Semiconductor

CD4007M/CD4007C Dual Complementary Pair Plus Inverter

General Description

The CD4007M/CD4007C consists of three complementary pairs of N- and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

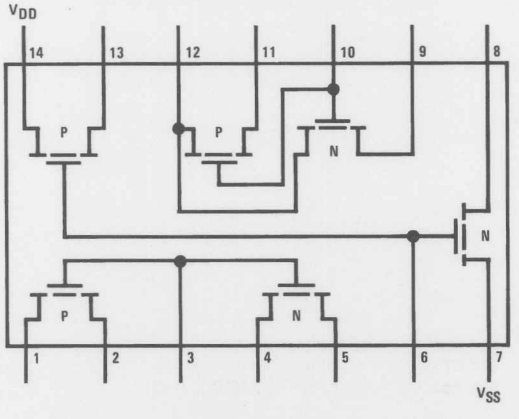
For proper operation the voltages at all pins must be constrained to be between V_{SS} − 0.3V and V_{DD} + 0.3V at all times.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} (typ.)

Connection Diagram

Dual-In-Line Package



TL/F/5943–1

Top View

Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS}.

Order Number CD4007*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$

Operating Temperature Range

CD4007M $-55°C$ to $+125°C$

CD4007C $-40°C$ to $+85°C$

Storage Temperature Range $-65°C$ to $+150°C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V_{DD} Range $V_{SS} + 3.0V$ to $V_{SS} + 15V$

Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics CD4007M

Symbol	Parameter	Conditions	Limits									Units
			$-55°C$			$+25°C$			$+125°C$			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$			0.05		0.001	0.05			3.0	μA
		$V_{DD} = 10V$			0.1		0.001	0.1			6.0	μA
P_D	Quiescent Device Dissipation Package	$V_{DD} = 5.0V$			0.25		0.005	0.25			15	μW
		$V_{DD} = 10V$			1.0		0.001	1.0			60	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$			0.05		0	0.05			0.05	V
		$V_{DD} = 10V$			0.05		0	0.05			0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$	4.95			4.95	5.0		4.95			V
		$V_{DD} = 10V$	9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V, V_O = 3.6V$			1.5		2.25	1.5			1.4	V
		$V_{DD} = 10V, V_O = 7.2V$			3.0		4.5	3.0			2.9	V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 50V, V_O = 0.95V$	3.6			3.5	2.25		3.5			V
		$V_{DD} = 10V, V_O = 2.9V$	7.1			7.0	4.5		7.0			V
I_DN	Output Drive Current N-Channel	$V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}$	0.75			0.6	1.0		0.4			mA
		$V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}$	1.6			1.3	2.5		0.95			mA
I_DP	Output Drive Current P-Channel	$V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}$	-1.75			-1.4	-4.0		-1.0			mA
		$V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}$	-1.35			-1.1	-2.5		-0.75			mA
I_I	Input Current						10					pA

DC Electrical Characteristics CD4007C

Symbol	Parameter	Conditions	Limits									Units
			$-40°C$			$+25°C$			$+85°C$			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$			0.5		0.005	0.05			15	μA
		$V_{DD} = 10V$			1.0		0.005	1.0			30	μA
P_D	Quiescent Device Dissipation Package	$V_{DD} = 5.0V$			2.5		0.025	2.5			75	μW
		$V_{DD} = 10V$			10		0.05	10			300	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$			0.05		0	0.01			0.05	V
		$V_{DD} = 10V$			0.05		0	0.01			0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$	4.95			4.95	5.0		4.95			V
		$V_{DD} = 10V$	9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All inputs)	$V_{DD} = 5.0V, V_O = 3.6V$			1.5		2.25	1.5			1.4	V
		$V_{DD} = 10V, V_O = 7.2V$			3.0		4.5	3.0			2.9	V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V, V_O = 0.95V$	3.6			3.5	2.25		3.5			V
		$V_{DD} = 10V, V_O = 2.9V$	7.1			7.0	4.5		7.0			V
I_DN	Output Drive Current N-Channel	$V_{DD} = 5.0V, V_O = 0.4V, V_I = V_{DD}$	0.35			0.3	1.0		0.24			mA
		$V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}$	1.2			1.0	2.5		0.8			mA
I_DP	Output Drive Current P-Channel	$V_{DD} = 5.0V, V_O = 2.5V, V_I = V_{SS}$	-1.3			-1.1	-4.0		-0.9			mA
		$V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}$	-0.65			-0.55	-2.5		-0.45			mA
I_I	Input Current						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

AC Electrical Characteristics* CD4007M

T_A = 25°C and C_L = 15 pF and rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	V_{DD} = 5.0V		35	60	ns
		V_{DD} = 10V		20	40	ns
$t_{TLH} = t_{THL}$	Transition Time	V_{DD} = 5.0V		50	75	ns
		V_{DD} = 10V		30	40	ns
C_I	Input Capacitance	Any Input		5.0		pF

*AC Parameters may be generated by DC correlated testing.

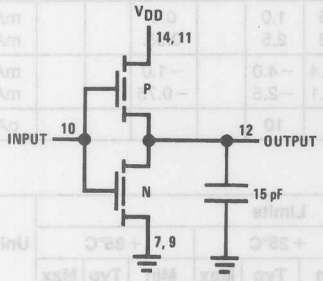
AC Electrical Characteristics* CD4007C

T_A = 25°C and C_L = 15 pF and rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C

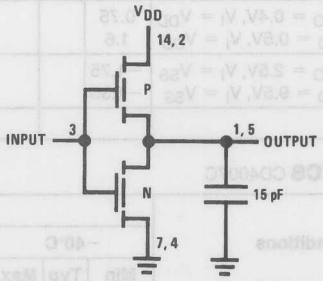
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	V_{DD} = 5.0V		35	75	ns
		V_{DD} = 10V		20	50	ns
$t_{TLH} = t_{THL}$	Transition Time	V_{DD} = 5.0V		50	100	ns
		V_{DD} = 10V		30	50	ns
C_I	Input Capacitance	Any Input		5		pF

*AC Parameters are guaranteed by DC correlated testing.

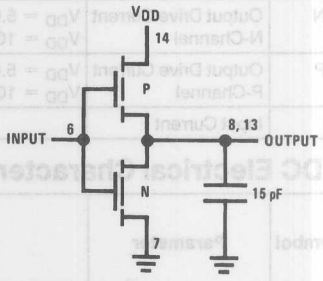
AC Test Circuits



TL/F/5943–2

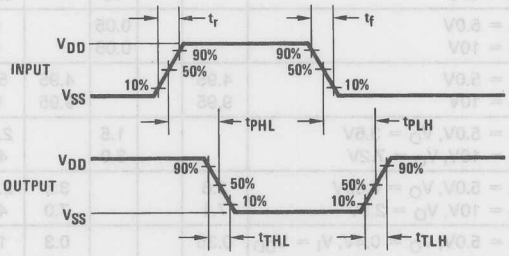


TL/F/5943–3



TL/F/5943–4

Switching Time Waveforms



TL/F/5943–5

National Semiconductor

CD4008BM/CD4008BC 4-Bit Full Adder

General Description

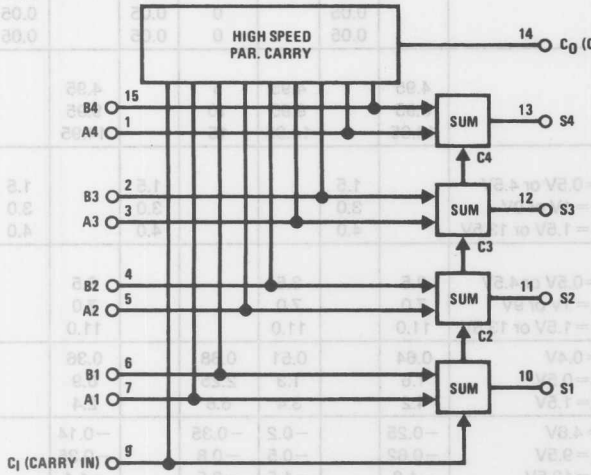
The CD4008B types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008B's. CD4008B inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the "Carry in" bit from a previous section. CD4008B outputs include the four sum bits, S1 and S4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008B section.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and GND.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 4 sum outputs plus parallel look-ahead carry-output
- Quiescent current specified to 15V
- Maximum input leakage of 1 μA at 15V (full package temperature range)

Block Diagram



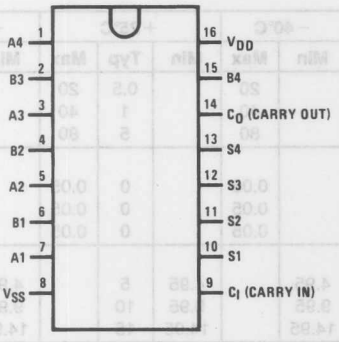
TL/F/5944–1

Truth Table

A_i	B_i	C_i	C0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Connection Diagram

Dual-In-Line Package



Top View

TL/F/5944–2

Order Number CD4008B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5V$ to $+18$ V_{DC}
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD}+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature, (T_L)	
(Soldering, 10 seconds)	260°C
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4008BM	$-55°C$ to $+125°C$
CD4008BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4008BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		5		0.3	5		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		10		0.5	10		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|<1\mu A$								
		$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|<1\mu A$								
		$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|<1\mu A$								
		$V_{DD}=5V, V_O=0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD}=10V, V_O=1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|<1\mu A$								
		$V_{DD}=5V, V_O=0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD}=10V, V_O=1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V, V_O=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V, V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V, V_O=4.6V$	−0.25		−0.2	−0.35		−0.14		mA
		$V_{DD}=10V, V_O=9.5V$	−0.62		−0.5	−0.8		−0.35		mA
		$V_{DD}=15V, V_O=13.5V$	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	$V_{DD}=15V, V_{IN}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V, V_{IN}=15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4008BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		20		0.5	20		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		40		1	40		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		80		5	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|<1\mu A$								
		$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|<1\mu A$								
		$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4008BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5			1.5		1.5	V
		$V_{DD}=10V$, $V_O=1V$ or 9V		3.0			3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or 4.5V	3.5		3.5			3.5		V
		$V_{DD}=10V$, $V_O=1V$ or 9V	7.0		7.0			7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	−0.2		−0.16	−0.35		−0.12		mA
		$V_{DD}=10V$, $V_O=9.5V$	−0.5		−0.4	−0.8		−0.3		mA
		$V_{DD}=15V$, $V_O=13.5V$	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3			−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3			0.3		1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, input t_r, $t_f = 20$ ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time Sum In to Sum Out	$V_{DD}=5V$		425	750	ns
		$V_{DD}=10V$		170	250	ns
		$V_{DD}=15V$		125	190	ns
	Carry In to Sum Out	$V_{DD}=5V$		320	650	ns
		$V_{DD}=10V$		125	225	ns
		$V_{DD}=15V$		95	175	ns
	Sum In to Carry Out	$V_{DD}=5V$		250	500	ns
		$V_{DD}=10V$		115	200	ns
		$V_{DD}=15V$		90	160	ns
	Carry In to Carry Out	$V_{DD}=5V$		130	245	ns
		$V_{DD}=10V$		60	105	ns
		$V_{DD}=15V$		45	80	ns
	Carry In to Carry Out	$C_L=15$ pF				
		$V_{DD}=5V$		100	175	ns
		$V_{DD}=10V$		45	75	ns
		$V_{DD}=15V$		35	60	ns
t_{THL}	High-to-Low Transition Time	$V_{DD}=5V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
t_{TLH}	Low-to-High Transition Time	$V_{DD}=5V$		200	400	ns
		$V_{DD}=10V$		100	200	ns
		$V_{DD}=15V$		80	160	ns
C_{IN}	Average Input Capacitance			5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

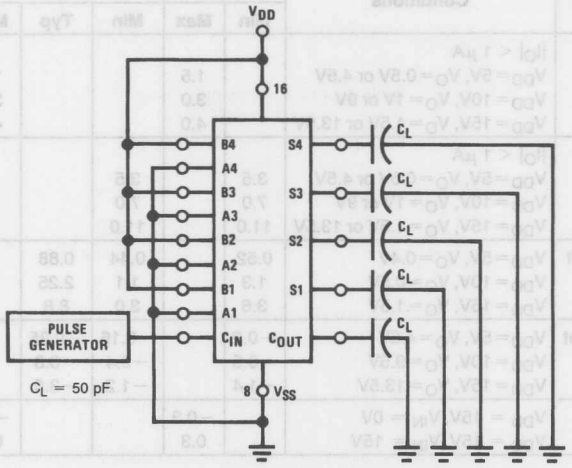
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

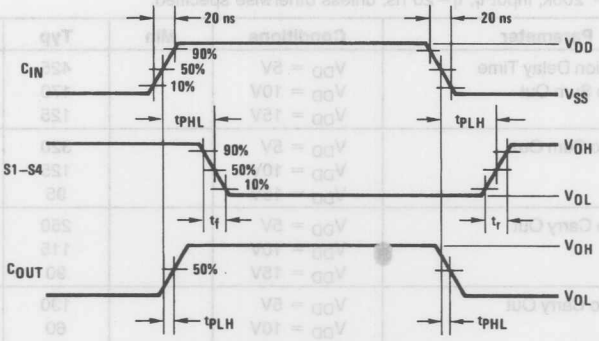
Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

AC Test Circuit and Switching Time Waveforms



TL/F/5944–3



TL/F/5944–4

National Semiconductor

CD4009M/CD4009C Hex Buffers (Inverting)
CD4010M/CD4010C Hex Buffers (Non-Inverting)

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3V to 15V providing $V_{CC} \leq V_{DD}$.

Features

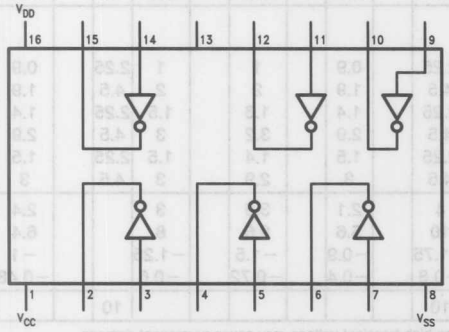
■ Wide supply voltage range	3.0V to 15V
■ Low power	100 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)
■ High current sinking capability	8 mA (min.) at V_O = 0.5V and V_{DD} = 10V

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Schematic and Connection Diagrams

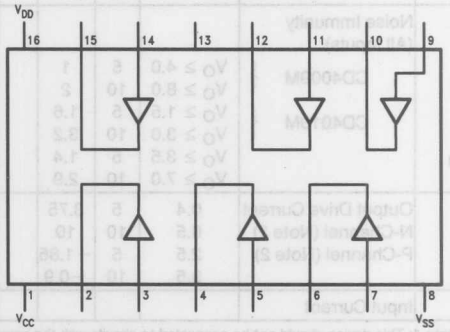
Dual-In-Line Package



TL/F/5945–2

Top View

Dual-In-Line Package



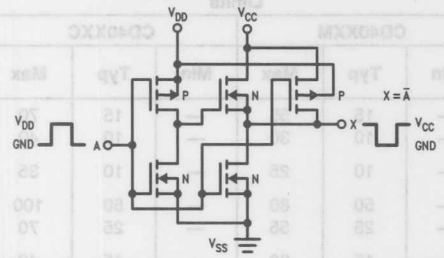
TL/F/5945–4

Top View

Order Number CD4009* or CD4010*

*Please look into Section 8, Appendix D for availability of various package types.

CD4009M/CD4009C



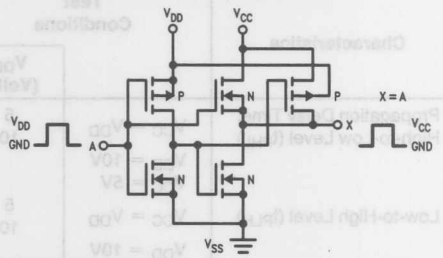
TL/F/5945–1

Hex COS/MOS to DTL or TTL converter (non-inverting).

Connect V_{CC} to DTL or TTL supply.

Connect V_{DD} to COS/MOS supply.

CD4010M/CD4010C



TL/F/5945–3

Hex COS/MOS to DTL or TTL converter (inverting).

Connect V_{CC} to DTL or TTL supply.

Connect V_{DD} to COS/MOS supply.

5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (Note 1) $V_{SS} - 0.3V$ to $V_{SS} + 15.5V$

Operating Temperature Range
- CD40XXM $-55°C$ to $+125°C$
- CD40XXC $-45°C$ to $+85°C$

Storage Temperature Range (T_S) $-65°C$ to $+150°C$

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

Operating Range (V_{DD}) $V_{SS} + 3V$ to $V_{SS} + 15V$

DC Electrical Characteristics

Symbol	Characteristics	Test Conditions (Volts)		Limits														Units
				CD40XXM							CD40XXC							
				−55°C		+25°C			+125°C		−40°C		+25°C			+85°C		
		V_O	V_{DD}	Min	Max	Min	Typ	Max	Min	Max	Min	Max	Min	Typ	Max	Min	Max	
I_{CC}	Quiescent Device		5		0.3		0.01	0.3		20		3		0.03	3		42	μA
	Current		10		0.5		0.01	0.5		30		5		0.05	5		70	μA
P_D	Quiescent Device		5		1.5		0.05	1.5		100		15		0.15	15		210	μW
	Dissipation/Package		10		5		0.1	5		300		50		0.5	50		700	μW
	Output Voltage		5		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
V_{OL}	Low Level		10		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
V_{OH}	High Level		5	4.99		4.99	5		4.95		4.99		4.99	5		4.95		V
			10	9.99		9.99	10		9.95		9.99		9.99	10		9.95		V
	Noise Immunity (All Inputs)																	
V_{NL}	CD4009M	$V_O \geq 4.0$	5	1		1	2.25		0.9		1		1	2.25		0.9		V
		$V_O \geq 8.0$	10	2		2	4.5		1.9		2		2	4.5		1.9		V
V_{NL}	CD4010M	$V_O \geq 1.5$	5	1.6		1.5	2.25		1.4		1.6		1.5	2.25		1.4		V
		$V_O \geq 3.0$	10	3.2		3	4.5		2.9		3.2		3	4.5		2.9		V
V_{NH}		$V_O \geq 3.5$	5	1.4		1.5	2.25		1.5		1.4		1.5	2.25		1.5		V
		$V_O \geq 7.0$	10	2.9		3	4.5		3		2.9		3	4.5		3		V
	Output Drive Current	0.4	5	3.75		3	4		2.1		3.6		3			2.4		mA
I_DN	N-Channel (Note 2)	0.5	10	10		8	10		5.6		9.6		8			6.4		mA
I_DP	P-Channel (Note 2)	2.5	5	−1.85		−1.25	−1.75		−0.9		−1.5		−1.25			−1		mA
		9.5	10	−0.9		−0.6	−0.8		−0.4		−0.72		−0.6			−0.48		mA
I_{IN}	Input Current						10							10				pA

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

Note 2: I_DN and I_DP are tested one output at a time.

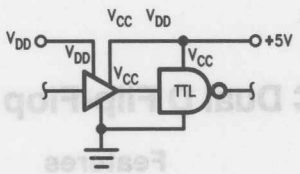
AC Electrical Characteristics*

$T_A = 25°c$, $C_L = 15$ pF, unless otherwise noted. Typical Temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Characteristics	Test Conditions		Limits						Units
			CD40XXM			CD40XXC			
		V_{DD} (Volts)	Min	Typ	Max	Min	Typ	Max	
Propagation Delay Time:									
High-to-Low Level (t_{PHL})	$V_{CC} = V_{DD}$	5	—	15	55	—	15	70	ns
		10	—	10	30	—	10	40	
	$V_{DD} = 10V$, $V_{CC} = 5V$		—	10	25	—	10	35	
Low-to-High Level (t_{PLH})	$V_{CC} = V_{DD}$	5	—	50	80	—	50	100	ns
		10	—	25	55	—	25	70	
	$V_{DD} = 10V$, $V_{CC} = 5V$		—	15	30	—	15	40	
Transition Time:									
High-to-Low Level (t_{THL})	$V_{CC} = V_{DD}$	5	—	20	45	—	20	60	ns
		10	—	16	40	—	16	50	
Low-to-High Level (t_{TLH})	$V_{CC} = V_{DD}$	5	—	80	125	—	80	160	ns
		10	—	50	100	—	50	120	
Input Capacitance (C_I)	Any Input		—	5	—	—	5	—	pF

*AC Parameters are guaranteed by DC correlated testing.

Typical Application



TL/F/5945–5

National Semiconductor

CD4013BM/CD4013BC Dual D Flip-Flop

General Description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

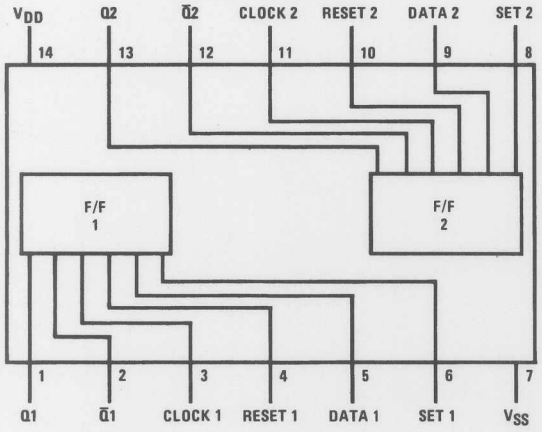
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line Package



TL/F/5946–1

Top View

Order Number CD4013B*

Please see Section 8, Appendix D for availability of various package types.

Truth Table

CL†	D	R	S	Q	$\overline{Q}$
⌐⌐	0	0	0	0	1
⌐⌐	1	0	0	1	0
⌐⌐	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
† = Level change
x = Don't care case

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temp. Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	$+3\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4013BM	$-55°C$ to $+125°C$
CD4013BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4013BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		1.0			1.0		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		2.0			2.0		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
		$V_{DD} = 15V$	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4013BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		4.0			4.0		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		8.0			8.0		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
		$V_{DD} = 15V$	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V

			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

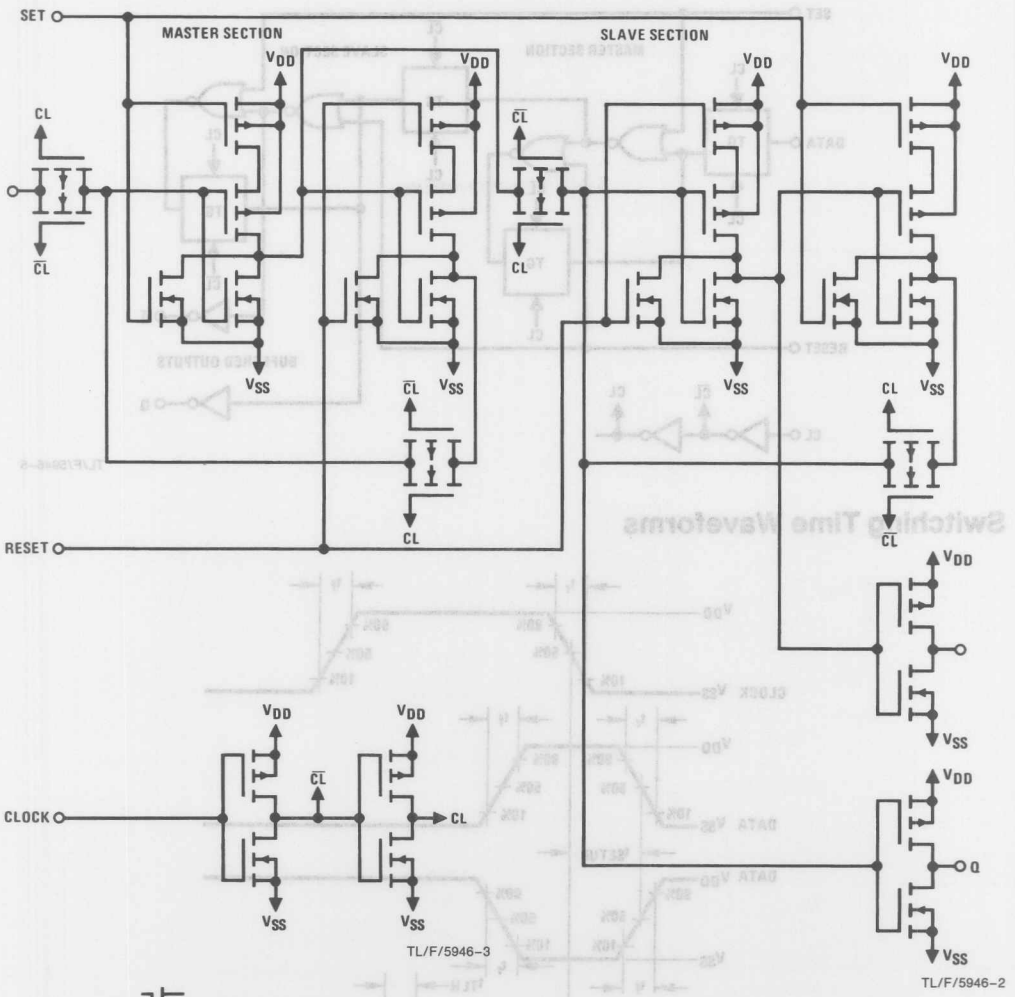
Note 3: I_{OH} and I_{OL} are measured one output at a time.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		200	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			10	μs
		$V_{DD} = 15V$			5	μs
t_{SU}	Minimum Set-Up Time	$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		15	30	ns
		$V_{DD} = 15V$		12	25	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.5	5		MHz
		$V_{DD} = 10V$	6.2	12.5		MHz
		$V_{DD} = 15V$	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Schematic Diagram



TL/F/5946-3

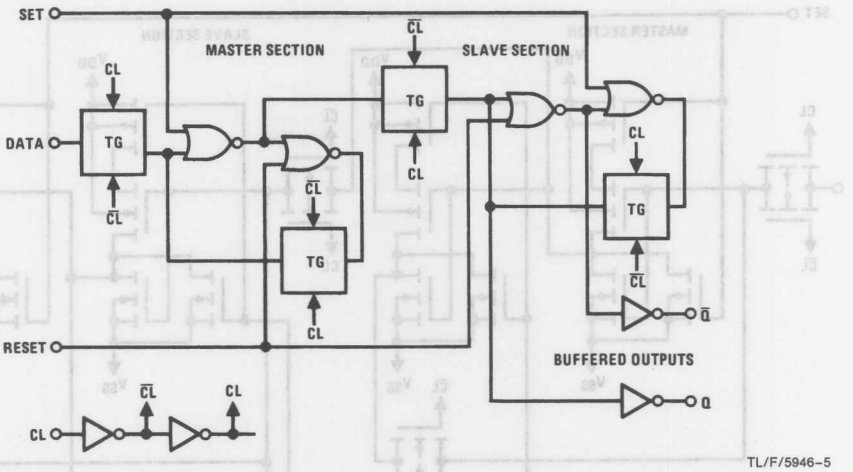
TL/F/5946-2

ALL P-SUBSTRATES ( ) CONNECTED TO V_{DD}

ALL N-SUBSTRATES ( ) CONNECTED TO V_{SS}

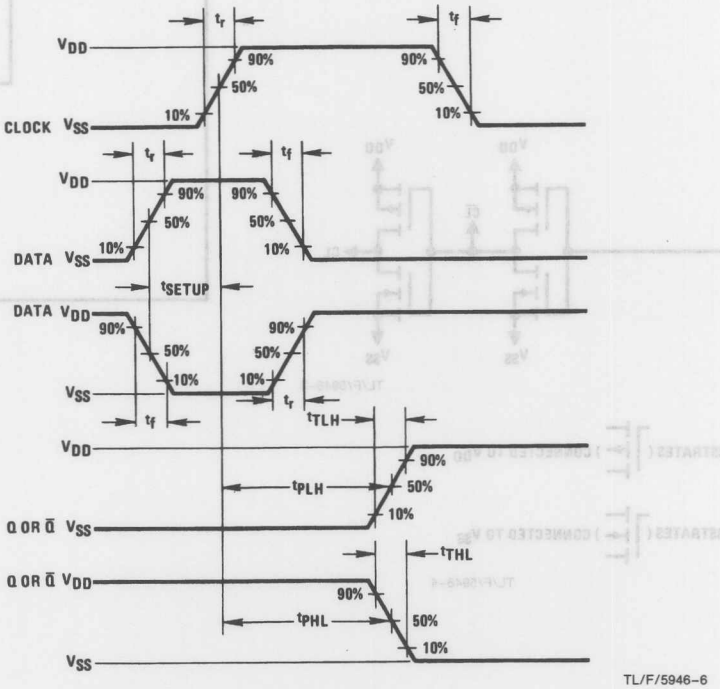
TL/F/5946-4

Logic Diagram



TL/F/5946–5

Switching Time Waveforms



TL/F/5946–6

National Semiconductor

CD4014BM/CD4014BC 8-Stage Static Shift Register

General Description

The CD4014BM/CD4014BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical "1" state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

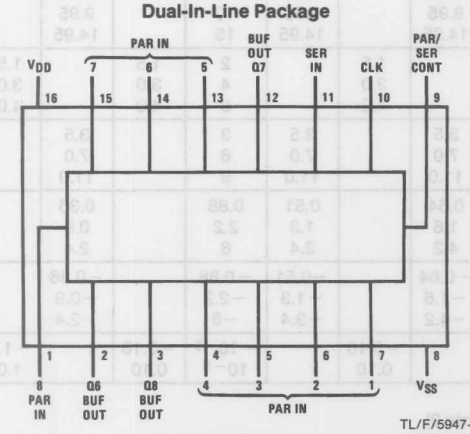
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage: 1 μA at 15V over full temperature range

Connection Diagram

Dual-In-Line Package



TL/F/5947–1

Top View

Truth Table

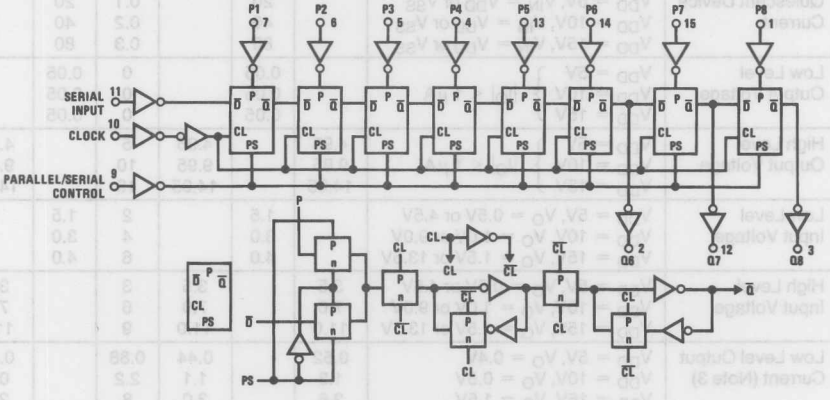
CL*	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n	
⎍	X	1	0	0	0	0	
⎍	X	1	1	0	1	0	
⎍	X	1	0	1	0	1	
⎍	X	1	1	1	1	1	
⎍	0	0	X	X	0	Q_{n-1}	
⎍	1	0	X	X	1	Q_{n-1}	
⎍	X	X	X	X	Q1	Q_n	No Change

*Level change
X = Don't care case

Order Number CD4014B*

*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



TL/F/5947–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5 to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3.0V to 15V
Input Voltage (V_{IN})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4014BM	−55°C to +125°C
CD4014BC	−40°C to +85°C

DC Electrical Characteristics CD4014BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.1	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.2	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.3	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.2		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4014BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.1	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.2	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.3	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8		2.4		mA

DC Electrical Characteristics CD4014BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		200	320	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		60	120	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5V	2.8	4		MHz
		V_{DD} = 10V	6	12		MHz
		V_{DD} = 15V	8	16		MHz
t_W	Minimum Clock Pulse Width	V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		25	50	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time (Note 4)	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_S	Minimum Set-Up Time (Note 6) Serial Input $t_H \geq$ 200 ns	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	60	ns
	Parallel Inputs $t_H \geq$ 200 ns	V_{DD} = 5V		80	160	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	60	ns
	Parallel/Serial Control $t_H \geq$ 200 ns	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_H	Minimum Hold Time Serial In, Parallel In, $t_S \geq$ 400 ns Parallel/Serial Control	V_{DD} = 5V			0	ns
		V_{DD} = 10V			10	ns
		V_{DD} = 15V			15	ns
C_I	Average Input Capacitance (Note 5)	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			110		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

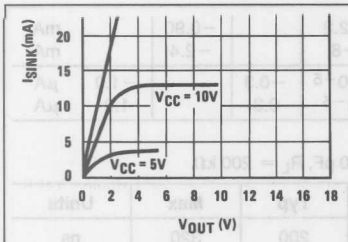
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

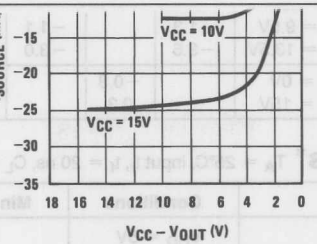
Note 4: If more than one unit is cascaded t_{rCL} should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

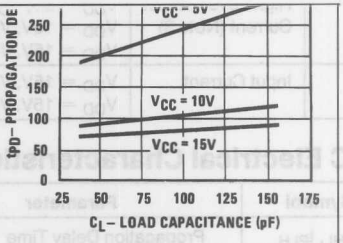
Note 6: Setup times are measured with reference to clock and a fixed hold time (t_H) as specified.



TL/F/5947–3



TL/F/5947–4



TL/F/5947–5

National Semiconductor

CD4015BM/CD4015BC Dual 4-Bit Static Shift Register

General Description

The CD4015BM/CD4015BC contains two identical, 4-stage, serial-input/parallel-output registers with independent "Data", "Clock," and "Reset" inputs. The logic level present at the input of each stage is transferred to the output of that stage at each positive-going clock transition. A logic high on the "Reset" input resets all four stages covered by that input. All inputs are protected from static discharge by a series resistor and diode clamps to V_{DD} and V_{SS}.

Features

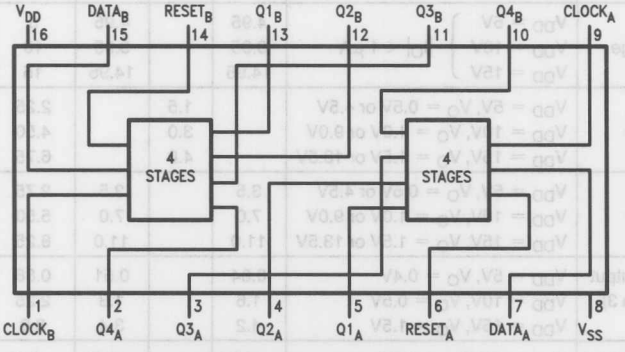
■ Wide supply voltage range	3.0V to 18V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8 MHz (typ.) clock rate @$V_{DD} - V_{SS} = 10V$
■ Fully static design	

Applications

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General purpose register

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5948–1

CL▲	D	R	Q_1	Q_n	
⌐⌐	0	0	0	Q_{n-1}	
⌐⌐	1	0	1	Q_{n-1}	
⌐⌙	X	0	Q_1	Q_n	(No change)
X	X	1	0	0	

▲ Level change

X = Don't care case

Order Number CD4015B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD}+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$+3$ to $+15$ V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4015BM	$-55°C$ to $+125°C$
CD4015BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4015BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		5		0.005	5		150	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		10		0.010	10		300	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1$ μA		0.05		0	0.05		0.05	V
		$V_{DD}=10V$ | $\|I_O\|<1$ μA		0.05		0	0.05		0.05	V
		$V_{DD}=15V$ | $\|I_O\|<1$ μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1$ μA	4.95		4.95	5		4.95		V
		$V_{DD}=10V$ | $\|I_O\|<1$ μA	9.95		9.95	10		9.95		V
		$V_{DD}=15V$ | $\|I_O\|<1$ μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		20		0.005	20		150	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		40		0.010	40		300	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

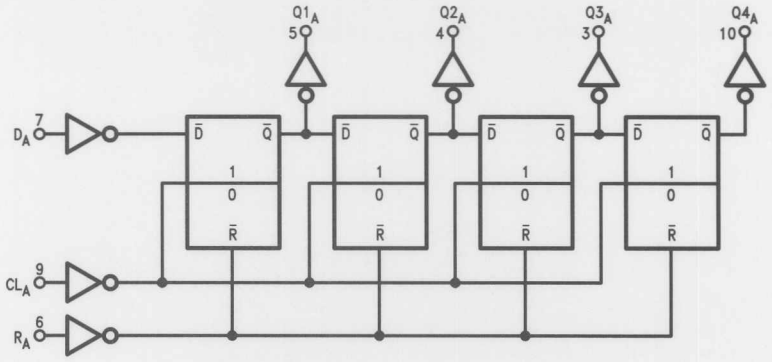
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		230	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		60	120	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WM}	Minimum Clock Pulse-Width	V_{DD} = 5V		160	250	ns
		V_{DD} = 10V		60	110	ns
		V_{DD} = 15V		50	85	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_{SU}	Minimum Data Set-Up Time	V_{DD} = 5V		50	100	μs
		V_{DD} = 10V		20	40	μs
		V_{DD} = 15V		15	30	μs
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2	3.5		MHz
		V_{DD} = 10V	4.5	8		MHz
		V_{DD} = 15V	6	11		MHz
C_{IN}	Input Capacitance	Clock Input		7.5	10	pF
		Other Inputs		5	7.5	pF
RESET OPERATION						
$t_{PHL(R)}$	Propagation Delay Time	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	V_{DD} = 5V		135	250	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	60	ns

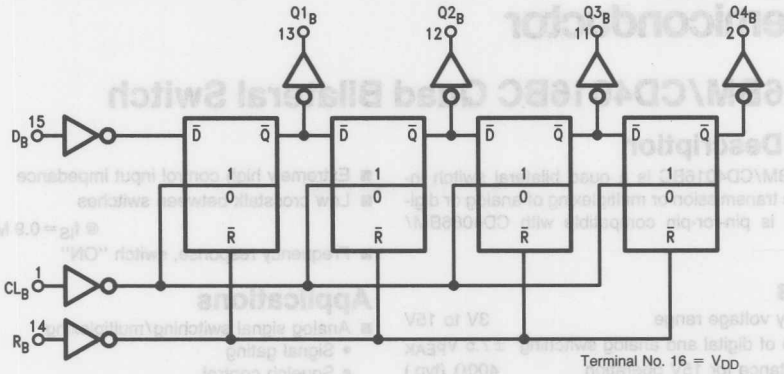
*AC Parameters are guaranteed by DC correlated testing.

Logic Diagrams



TL/F/5948–2

Logic Diagrams (Continued)



Terminal No. 16 = V_{DD}
Terminal No. 8 = GND

TL/F/5948–3

National Semiconductor

CD4016BM/CD4016BC Quad Bilateral Switch

General Description

The CD4016BM/CD4016BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4066BM/CD4066BC.

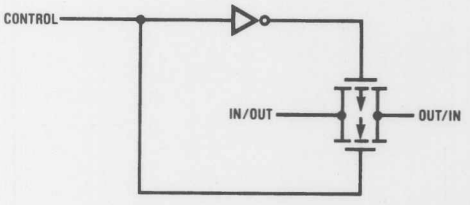
Features

- Wide supply voltage range 3V to 15V
- Wide range of digital and analog switching $\pm 7.5\ V_{PEAK}$
- "ON" resistance for 15V operation 400Ω (typ.)
- Matched "ON" resistance over 15V signal input $\Delta R_{ON} = 10\Omega$ (typ.)
- High degree of linearity 0.4% distortion (typ.) @ f_{IS} = 1 kHz, $V_{IS} = 5\ V_{p-p}$, $V_{DD} - V_{SS} = 10V$, $R_L = 10\ k\Omega$
- Extremely low "OFF" switch leakage 0.1 nA (typ.) @ $V_{DD} - V_{SS} = 10V$, $T_A = 25°C$
- Extremely high control input impedance $10^{12}\Omega$ (typ.)
- Low crosstalk between switches −50 dB (typ.) @ $f_{IS} = 0.9$ MHz, $R_L = 1\ k\Omega$
- Frequency response, switch "ON" 40 MHz (typ.)

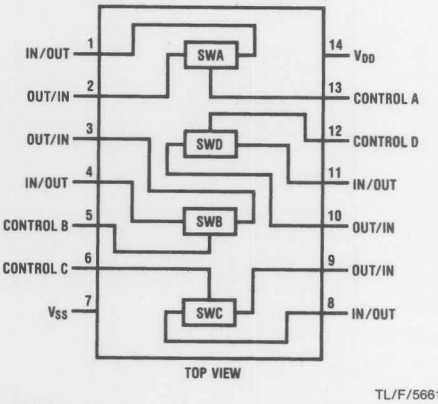
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Schematic and Connection Diagrams



Dual-In-Line Package



TL/F/5661–1

Order Number CD4016B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to + 150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4016BM	−55°C to +125°C
CD4016BC	−40°C to +85°C

DC Electrical Characteristics CD4016BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25		0.01	0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5		0.01	0.5		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
		V_C = V_{DD}, V_{IS} = V_{SS} or V_{DD}								
		V_{DD} = 10V		600		250	660		960	Ω
		V_{DD} = 15V		360		200	400		600	Ω
		R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
		V_C = V_{DD}								
		V_{DD} = 10V, V_{IS} = 4.75 to 5.25V		1870		850	2000		2600	Ω
		V_{DD} = 15V, V_{IS} = 7.25 to 7.75V		775		400	850		1230	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches (In Same Package)	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
		V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
		V_{DD} = 10V				15				Ω
		V_{DD} = 15V				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	V_C = 0, V_{DD} = 15V, V_{IS} = 15V and 0V, V_{OS} = 0V and 15V		±50		±0.1	±50		±500	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	V_{IS} = V_{SS} and V_{DD}, V_{OS} = V_{DD} and V_{SS}, I_{IS} = ±10 μA								
		V_{DD} = 5V		0.9			0.7		0.5	V
		V_{DD} = 10V		0.9			0.7		0.5	V
		V_{DD} = 15V		0.9			0.7		0.5	V
V_{IHC}	High Level Input Voltage	V_{DD} = 5V	3.5		3.5			3.5		V
		V_{DD} = 10V (see Note 6 and	7.0		7.0			7.0		V
		V_{DD} = 15V *Figure 8*)	11.0		11.0			11.0		V
I_{IN}	Input Current	V_{DD} − V_{SS} = 15V, V_{DD} ≥ V_{IS} ≥ V_{SS}, V_{DD} ≥ V_C ≥ V_{SS}		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics CD4016BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		1.0		0.01	1.0		7.5	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		2.0		0.01	2.0		15	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		4.0		0.01	4.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ or V_{DD}								
		$V_{DD}=10V$		610		275	660		840	Ω
		$V_{DD}=15V$		370		200	400		520	Ω
		$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$								
		$V_{DD}=10V$, $V_{IS}=4.75$ to $5.25V$		1900		850	2000		2380	Ω
		$V_{DD}=15V$, $V_{IS}=7.25$ to $7.75V$		790		400	850		1080	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches (In Same Package)	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				15				Ω
		$V_{DD}=15V$				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$, $V_{DD}=15V$		±50		±0.1	±50		±200	nA
		$V_{IS}=0V$ or $15V$,								
		$V_{OS}=15V$ or $0V$								
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD}								
		$V_{OS}=V_{DD}$ and V_{SS}								
		$I_{IS}=\pm 10\ \mu A$								
		$V_{DD}=5V$		0.9			0.7		0.4	V
		$V_{DD}=10V$		0.9			0.7		0.4	V
		$V_{DD}=15V$		0.9			0.7		0.4	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5			3.5		V
		$V_{DD}=10V$ (see Note 6 and	7.0		7.0			7.0		V
		$V_{DD}=15V$ *Figure 8*)	11.0		11.0			11.0		V
I_{IN}	Input Current	$V_{CC}-V_{SS}=15V$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA
		$V_{DD}\geq V_{IS}\geq V_{SS}$								
		$V_{DD}\geq V_C\geq V_{SS}$								

AC Electrical Characteristics* $T_A=25°C$, $t_r=t_f=20$ ns and $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C=V_{DD}$, $C_L=50$ pF, (*Figure 1*)				
		$R_L=200k$				
		$V_{DD}=5V$		58	100	ns
		$V_{DD}=10V$		27	50	ns
		$V_{DD}=15V$		20	40	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L=1.0\ k\Omega$, $C_L=50$ pF, (*Figures 2* and *3*)				
		$V_{DD}=5V$		20	50	ns
		$V_{DD}=10V$		18	40	ns
		$V_{DD}=15V$		17	35	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time *Control Input to Signal* Output Logical Level to High Impedance	$R_L=1.0\ k\Omega$, $C_L=50$ pF, (*Figures 2* and *3*)				
		$V_{DD}=5V$		15	40	ns
		$V_{DD}=10V$		11	25	ns
		$V_{DD}=15V$		10	22	ns
	Sine Wave Distortion	$V_C=V_{DD}=5V$, $V_{SS}=-5$		0.4		%
		$R_L=10\ k\Omega$, $V_{IS}=5\ V_{P-P}$, $f=1$ kHz, (*Figure 4*)				

AC Electrical Characteristics* (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Frequency Response — Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5\ V_{P-P}$, $20\ \text{Log}_{10}\ V_{OS}/V_{OS}$ (1 kHz) −dB, (*Figure 4*)		40		MHz
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5\ V_{P-P}$, $20\ \text{Log}_{10}\ (V_{OS}/V_{IS}) = -50$ dB, (*Figure 4*)		1.25		MHz
	Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5V$; $V_{SS} = V_{C(B)} = -5V$, $R_L = 1\ k\Omega V_{IS(A)} = 5\ V_{P-P}$, $20\ \text{Log}_{10}\ (V_{OS(B)}/V_{OS(A)}) = -50$ dB, (*Figure 5*)		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$ $R_{IN} = 1\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$ pF (*Figure 6*)		150		mV_{P-P}
	Maximum Control Input	$R_L = 1\ k\Omega$, $C_L = 50$ pF, (*Figure 7*) $V_{OS(f)} = \frac{1}{2}\ V_{OS}$(1 kHz)				
		$V_{DD} = 5V$		6.5		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		9.0		MHz
C_{IS}	Signal Input Capacitance			4		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		4		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.2		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

*AC Paramters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: If the switch input is held at V_{DD}, V_{IHC} is the control input level that will cause the switch output to meet the standard "B" series V_{OH} and I_{OH} output levels. If the analog switch input is connected to V_{SS}, V_{IHC} is the control input level — which allows the switch to *sink* standard "B" series $|I_{OH}|$, high level current, and still maintain a $V_{OL} \leq$ "B" series. These currents are shown in *Figure 8*.

AC Test Circuits and Switching Time Waveforms

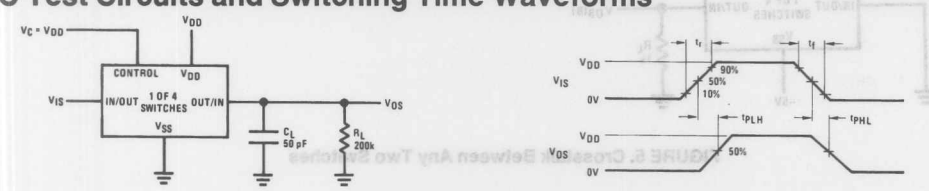
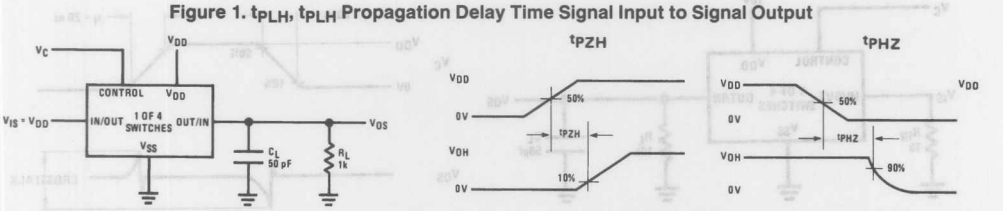


Figure 1. t_{PLH}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/F/5661–2

FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

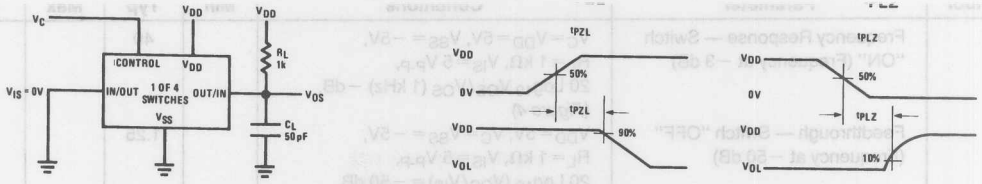
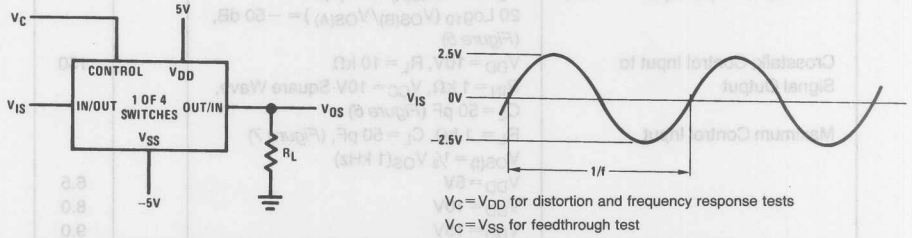


FIGURE 3. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



$V_C = V_{DD}$ for distortion and frequency response tests
$V_C = V_{SS}$ for feedthrough test

FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

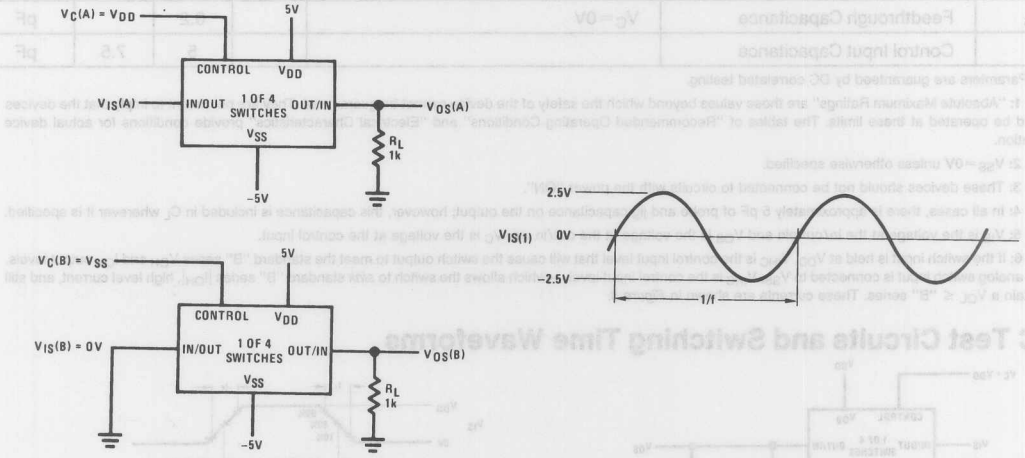
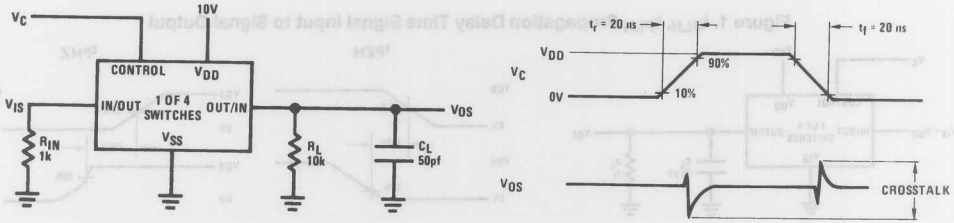


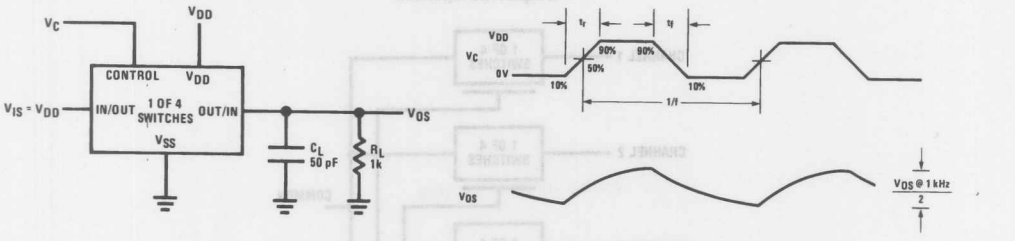
FIGURE 5. Crosstalk Between Any Two Switches



TL/F/5661–3

FIGURE 6. Crosstalk — Control to Input Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



TL/F/5661–4

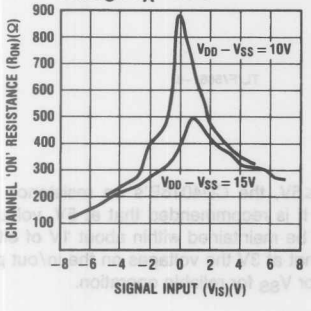
FIGURE 7. Maximum Control Input Frequency

Temperature Range	V_{DD}	V_{IS}	Switch Input I_{IS} (mA)			Switch Output $V_{OS(V)}$	
			T_{LOW}	25°C	T_{HIGH}	Min	Max
MILITARY	5	0	0.25	0.2	0.14		0.4
	5	5	−0.25	−0.2	−0.14	4.6	
	10	0	0.62	0.5	0.35		0.5
	10	10	−0.62	−0.5	−0.35	9.5	
	15	0	1.8	1.5	1.1		1.5
	15	15	−1.8	−1.5	−1.1	13.5	
COMMERCIAL	5	0	0.2	0.16	0.12		0.4
	5	5	−0.2	−0.16	−0.12	4.6	
	10	0	0.5	0.4	0.3		0.5
	10	10	−0.5	−0.4	−0.3	9.5	
	15	0	1.4	1.2	1.0		1.5
	15	15	−1.4	−1.2	−1.0	13.5	

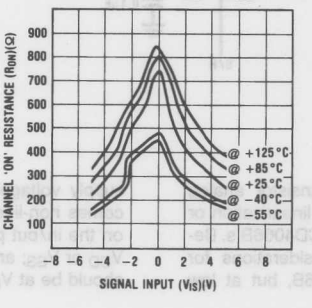
FIGURE 8. CD4016B Switch Test Conditions for V_{IHC}

Typical Performance Characteristics

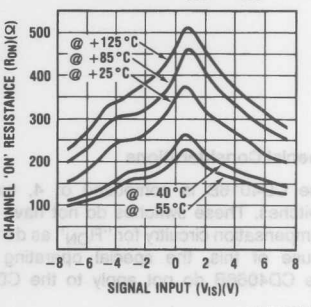
'ON' Resistance vs. Signal Voltage $T_A = 25°C$



'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 10V$



'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 15V$

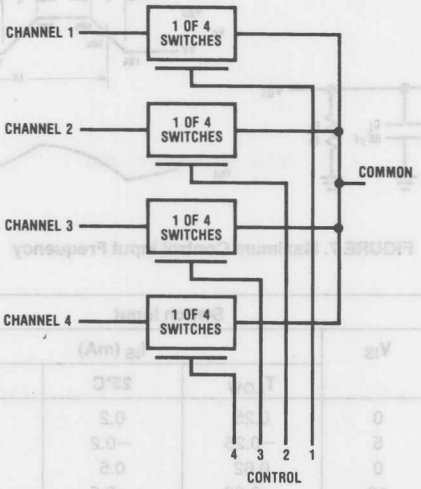


TL/F/5661–5

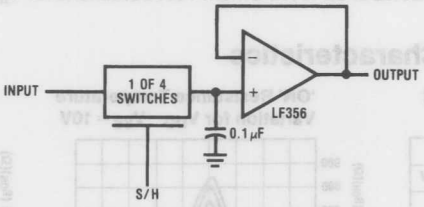
5

Typical Applications

4 Input Multiplexer



Sample/Hold Amplifier



TL/F/5661–6

Special Considerations

The CD4016B is composed of 4, two-transistor analog switches. These switches do not have any linearization or compensation circuitry for "R_{ON}" as do the CD4066B's. Because of this, the special operating considerations for the CD4066B do not apply to the CD4016B, but at low supply voltages, ≤5V, the CD4016B's on resistance becomes non-linear. It is recommended that at 5V, voltages on the in/out pins be maintained within about 1V of either V_{DD} or V_{SS}; and that at 3V the voltages on the in/out pins should be at V_{DD} or V_{SS} for reliable operation.

National Semiconductor

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

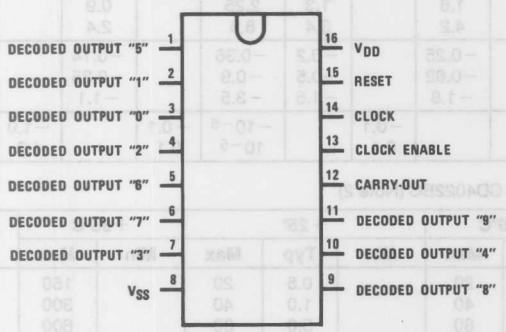
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	5.0 MHz (typ.) with 10V V_{DD}
■ Low power	10 μW (typ.)
■ Fully static operation	

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

Connection Diagrams

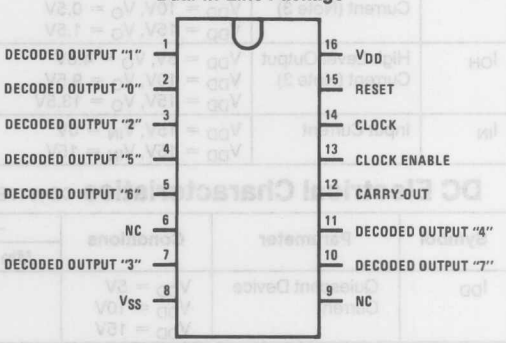
CD4017B
Dual-In-Line Package



TL/F/5950–1

Top View

CD4022B
Dual-In-Line Package



TL/F/5950–2

Top View

Order Number CD4017B* or CD4022B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4017BM, CD4022BM	$-55°C$ to $+125°C$
CD4017BC, CD4022BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4017BM, CD4022BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		5		0.3	5		150	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		10		0.5	10		300	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.25		−0.2	−0.36		−0.14		mA
		$V_{DD} = 10V, V_O = 9.5V$	−0.62		−0.5	−0.9		−0.35		mA
		$V_{DD} = 15V, V_O = 13.5V$	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4017BC, CD4022BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.5	20		150	μA
		$V_{DD} = 10V$		40		1.0	40		300	μA
		$V_{DD} = 15V$		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4017BC, CD4022BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.2		−0.16	−0.36		−0.12		mA
		$V_{DD} = 10V, V_O = 9.5V$	−0.5		−0.4	−0.9		−0.3		mA
		$V_{DD} = 15V, V_O = 13.5V$	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides condtions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwse specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_{rCL} and $t_{fCL} = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry Out Line					
		$V_{DD} = 5V$		415	800	ns
		$V_{DD} = 10V$		160	320	ns
		$V_{DD} = 15V$		130	250	ns
	Carry Out Line	$V_{DD} = 5V$ } $C_L = 15$ pF		240	480	ns
		$V_{DD} = 10V$ } $C_L = 15$ pF		85	170	ns
		$V_{DD} = 15V$ } $C_L = 15$ pF		70	140	ns
	Decode Out Lines	$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{TLH}, t_{THL}	Transition Time Carry Out and Decode Out Lines					
	t_{TLH}	$V_{DD} = 5V$		200	360	ns
		$V_{DD} = 10V$		100	180	ns
		$V_{DD} = 15V$		80	130	ns
	t_{THL}	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$ } Measured with	1.0	2		MHz
		$V_{DD} = 10V$ } Respect to Carry	2.5	5		MHz
		$V_{DD} = 15V$ } Output Line	3.0	6		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		125	250	ns
		$V_{DD} = 10V$		45	90	ns
		$V_{DD} = 15V$		35	70	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	$V_{DD} = 5V$			20	μs
		$V_{DD} = 10V$			15	μs
		$V_{DD} = 15V$			5	μs
t_{SU}	Minimum Clock Inhibit Data Setup Time	$V_{DD} = 5V$		120	240	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		32	65	ns
C_{IN}	Average Input Capacitance			5	7.5	pF

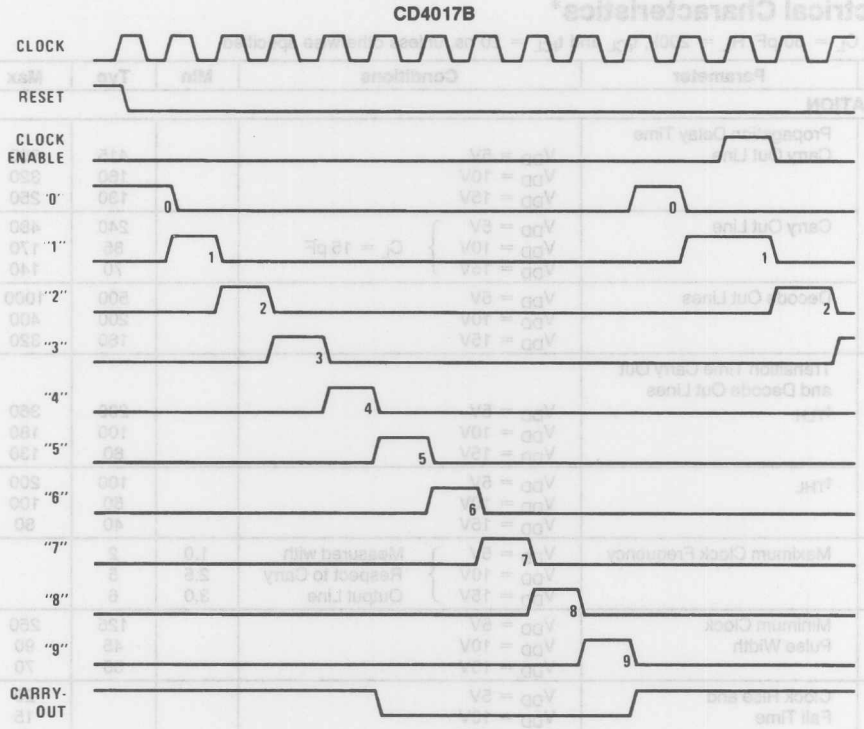
AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_{rCL} and t_{fCL} = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry Out Line	V_{DD} = 5V		415	800	ns
		V_{DD} = 10V		160	320	ns
		V_{DD} = 15V		130	250	ns
	Carry Out Line	V_{DD} = 5V, C_L = 15 pF		240	480	ns
		V_{DD} = 10V, C_L = 15 pF		85	170	ns
		V_{DD} = 15V, C_L = 15 pF		70	140	ns
	Decode Out Lines	V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_W	Minimum Reset Pulse Width	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
t_{REM}	Minimum Reset Removal Time	V_{DD} = 5V		75	150	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns

*AC Parameters are guaranteed by DC correlated testing.

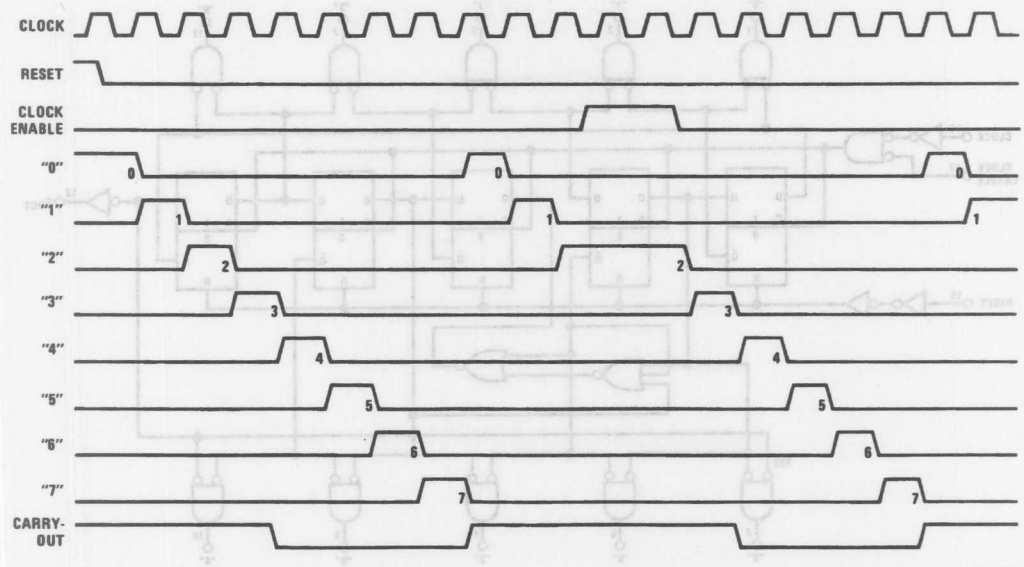
Timing Diagrams



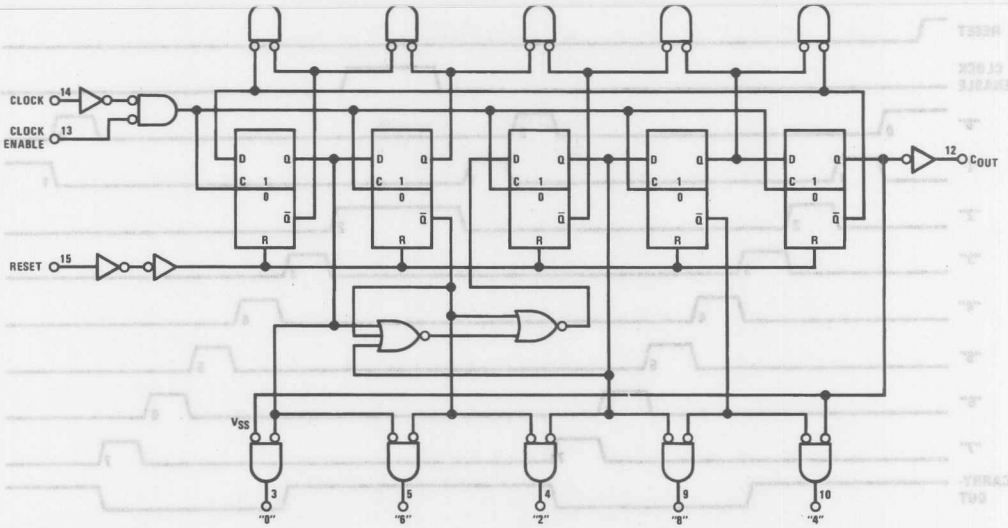
TL/F/5950–3

Timing Diagrams (Continued)

CD4022B



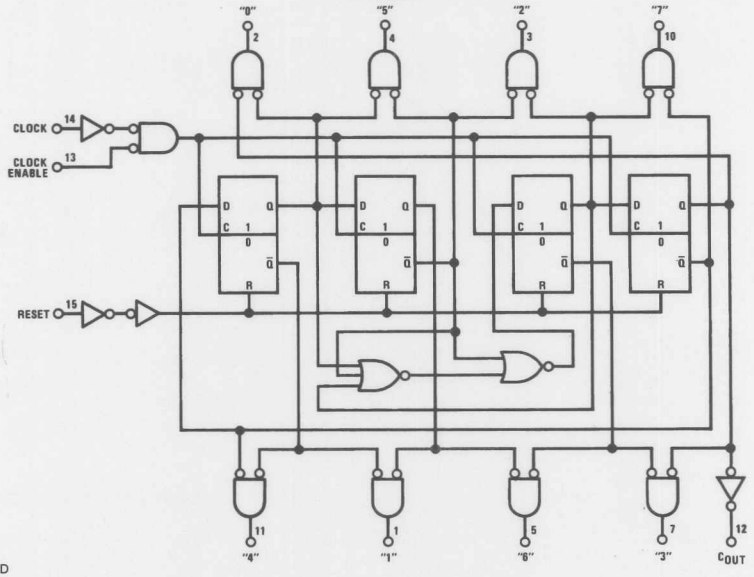
TL/F/5950–4



Terminal No. 8 = GND
Terminal No. 16 = V_{DD}

TL/F/5950–5

CD4022B



Terminal No. 16 = V_{DD}
Terminal No. 8 = GND

TL/F/5950–6

National Semiconductor

CD4018BM/CD4018BC Presettable Divide-by-N Counter

General Description

The CD4018B consists of 5 Johnson counter stages. A buffered $\overline{Q}$ output from each stage, "CLOCK", "RESET", "DATA", "PRESET ENABLE", and 5 individual "JAM" inputs are provided. The counter is advanced one count at the positive clock signal transition. A high "RESET" signal clears the counters to an "ALL ZERO" condition. A high "PRESET ENABLE" signal allows information on the "JAM" inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

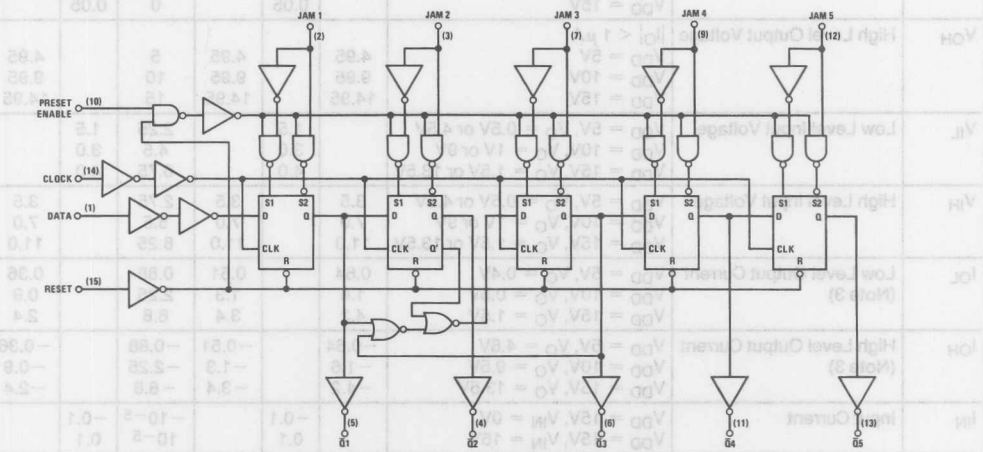
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation

Applications

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counter
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide by "N" counters/frequency synthesizers

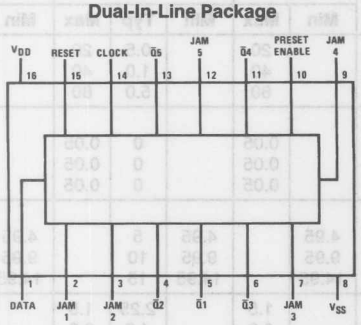
Logic Diagram



TL/F/5951–1

Connection Diagram

Dual-In-Line Package



TL/F/5951–2

Top View

Order Number CD4018B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5V$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	-0.5 to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4018BM	$-55°C$ to $+125°C$
CD4018BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4018BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5		0.3	5		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.5	10		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4018BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.5	20		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		40		1.0	40		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V

DC Electrical Characteristics CD4018BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	700	ns
		V_{DD} = 10V		95	250	ns
		V_{DD} = 15V		70	200	ns
t_{THL}, t_{TLH}	Transition Time $\overline{Q}$ Outputs	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		50	100	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	500	ns
		V_{DD} = 10V		50	200	ns
		V_{DD} = 15V		40	160	ns
t_{RCL}, t_{FCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_{SU}	Minimum Data Input Set-Up Time	V_{DD} = 5V		40	200	ns
		V_{DD} = 10V		20	100	ns
		V_{DD} = 15V		16	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	4		MHz
		V_{DD} = 10V	3	9		MHz
		V_{DD} = 15V	5	14		MHz
PRESET OR RESET OPERATION						
$t_{PLH(R)}$ $t_{PHL(PR)}$ $t_{PLH(PR)}$	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	750	ns
		V_{DD} = 10V		95	250	ns
		V_{DD} = 15V		70	200	ns
$t_{WH(R)}$ $t_{WH(PR)}$	Minimum Preset or Reset Pulse Width	V_{DD} = 5V		100	400	ns
		V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
t_{REM}	Minimum Preset or Reset Removal Time	V_{DD} = 5V		100	400	ns
		V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		63		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

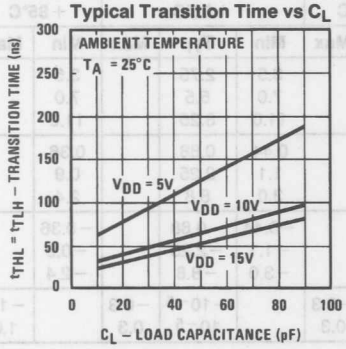
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see "54C/74C Family Characteristics", application note AN-90.

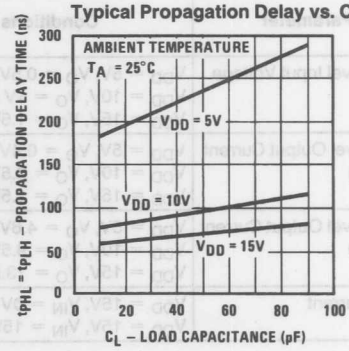
Typical Performance Characteristics

Typical Transition Time vs C_L



TL/F/5951–3

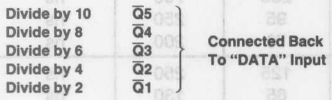
Typical Propagation Delay vs. C_L



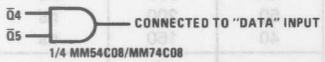
TL/F/5951–4

External Connections

External Connections for Divide by 10, 9, 8, 7, 6, 5, 4, 3, 2, Operation

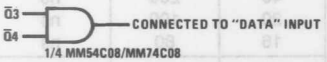


Divide by 9



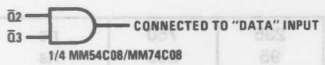
TL/F/5951–5

Divide by 7



TL/F/5951–6

Divide by 5



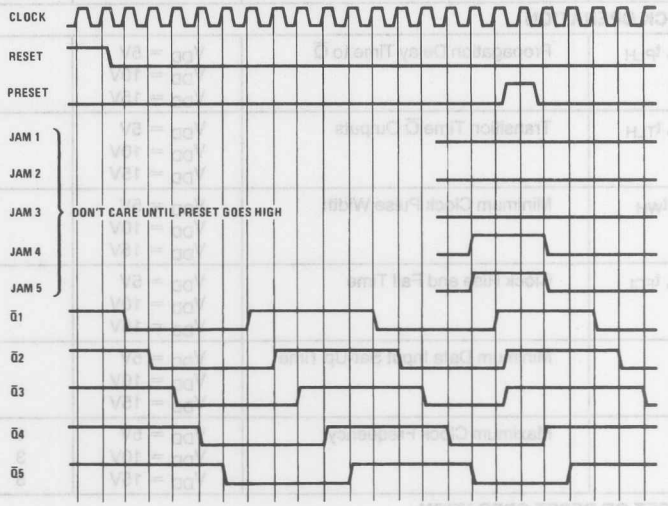
TL/F/5951–7

Divide by 3



TL/F/5951–8

Timing Diagram



TL/F/5951–9

Note: "Data" input tied to $\bar{Q}5$ for decade counter configuration

National Semiconductor

CD4019BM/CD4019BC Quad AND-OR Select Gate

General Description

The CD4019BM/CD4019BC is a complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N- and P-channel enhancement mode transistors. These complementary MOS (CMOS) transistors provide the building blocks for the 4 "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B. All inputs are protected against static discharge damage.

Features

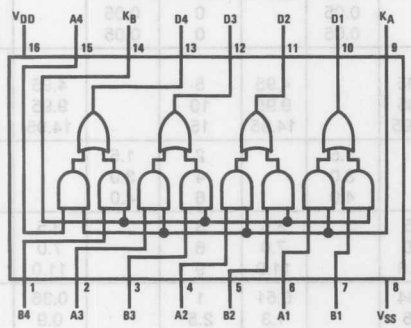
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS

Applications

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/EXCLUSIVE-OR selection

Connection and Schematic Diagrams

Dual-In-Line Package

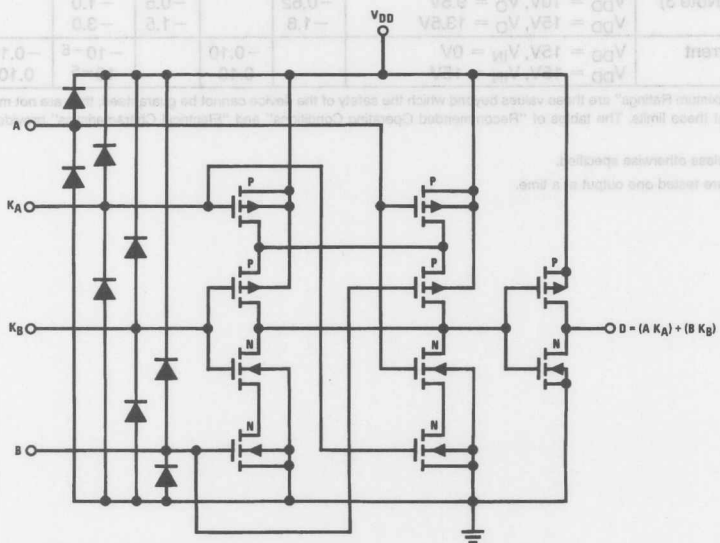


TL/F/5952–1

Top View

Order Number CD4019B*

*Please look into Section 8, Appendix D for availability of various package types.



Schematic diagram for 1 of 4 identical stages

TL/F/5952–2

5

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
Input Voltage (V_{IN})	0V to V_{DD} V
Operating Temperature Range (T_A)	
CD4019BM	−55°C to +125°C
CD4019BC	−40°C to +85°C

DC Electrical Characteristics CD4019BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.03	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.05	0.5		15	μA
		V_{DD} = 15V		1.0		0.07	1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.5		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	10		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.4		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−1.0		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.0		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4019BC (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.03	1		7.5	μA
		V_{DD} = 10V		2		0.05	2		15	μA
		V_{DD} = 15V		4		0.07	4		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	1		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.5		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	10		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.4		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−1.0		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.0		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

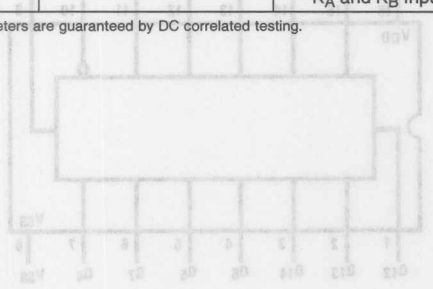
Note 2: V_{SS} = 0V unless otherwise specified.

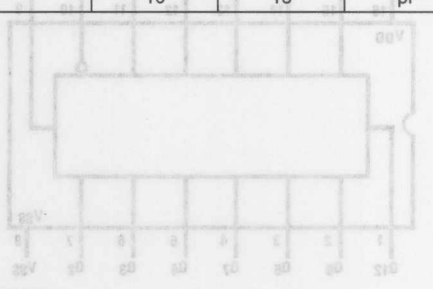
Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay, Input to Output	V_{DD} = 5V		100	300	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		45	100	ns
t_{THL}	High-to-Low Level Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{TLH}	Low-to-High Level Transition Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	All A and B Inputs		5	7.5	pF
		K_A and K_B Inputs		10	15	pF

*AC Parameters are guaranteed by DC correlated testing.





5

National Semiconductor

CD4020BM/CD4020BC
14-Stage Ripple Carry Binary Counters
CD4040BM/CD4040BC
12-Stage Ripple Carry Binary Counters
CD4060BM/CD4060BC
14-Stage Ripple Carry Binary Counters

General Description

The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

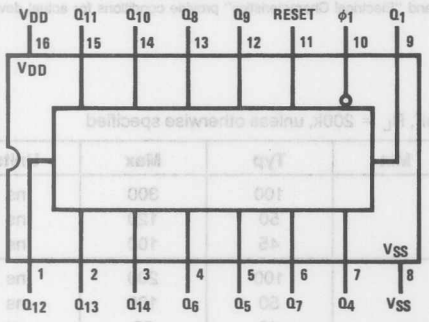
Features

■ Wide supply voltage range	1.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8 MHz typ. at V_{DD} = 10V
■ Schmitt trigger clock input	

Connection Diagrams

Dual-In-Line Package

CD4020BM/CD4020BC



TL/F/5953–1

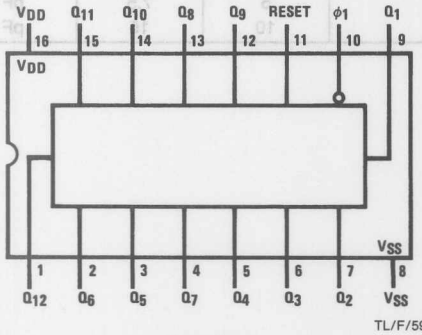
Top View

Order Number CD4020B*, CD4040B* or CD4060B*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package

CD4040BM/CD4040BC

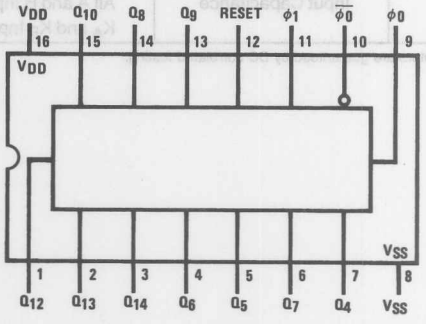


TL/F/5953–2

Top View

Dual-In-Line Package

CD4060BM/CD4060BC



TL/F/5953–3

Top View

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Package Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions

Supply Voltage (V_{DD})	+3V to +15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD40XXBM	−55°C to +125°C
CD40XXBC	−40°C to +85°C

DC Electrical Characteristics CD40XXBM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	(See Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	(See Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Data does not apply to oscillator points ϕ_0 and $\overline{\phi_0}$ of CD4060BM/CD4060BC. I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics 40XXBC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

			Min	Max	Min	Typ	Max	Min	Max	
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* CD4020BM/CD4020BC, CD4040BM/CD4040BC

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r = t_f = 20 ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	V_{DD} = 5V		250	550	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		75	150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	V_{DD} = 5V		150	330	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	335	ns
		V_{DD} = 10V		50	125	ns
		V_{DD} = 15V		40	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			No Limit	ns
		V_{DD} = 10V			No Limit	ns
		V_{DD} = 15V			No Limit	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	4		MHz
		V_{DD} = 10V	4	10		MHz
		V_{DD} = 15V	5	12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
C_{in}	Average Input Capacitance	Any Input		5	7.5	pF
C_{pd}	Power Dissipation Capacitance			50		pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4060BM/CD4060BC

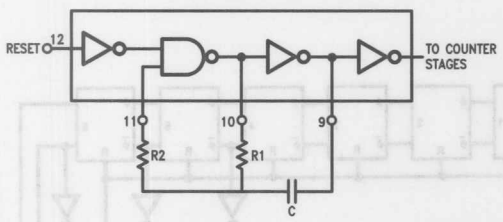
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	ns
		$V_{DD} = 15V$		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			No Limit	ns
		$V_{DD} = 10V$			No Limit	ns
		$V_{DD} = 15V$			No Limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		MHz
		$V_{DD} = 15V$	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{in}	Average Input Capacitance	Any Input		5	7.5	pF
C_{pd}	Power Dissipation Capacitance			50		pF

*AC Parameters are guaranteed by DC correlated testing.

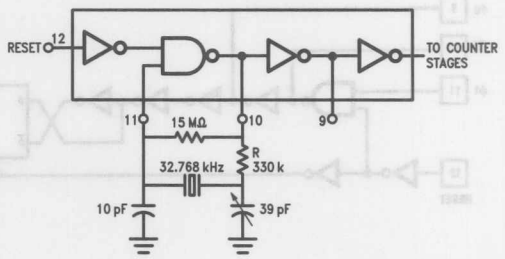
CD4060B Typical Oscillator Connections

RC Oscillator



TL/F/5953–4

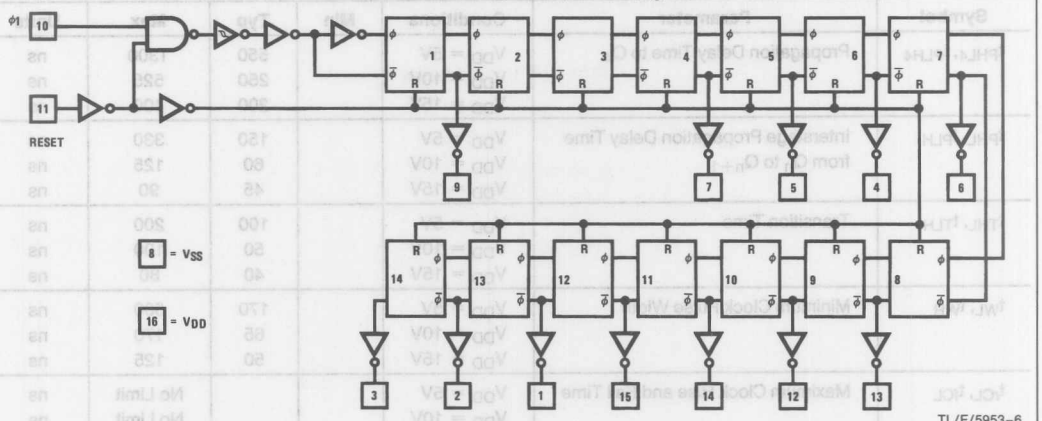
Crystal Oscillator



TL/F/5953–5

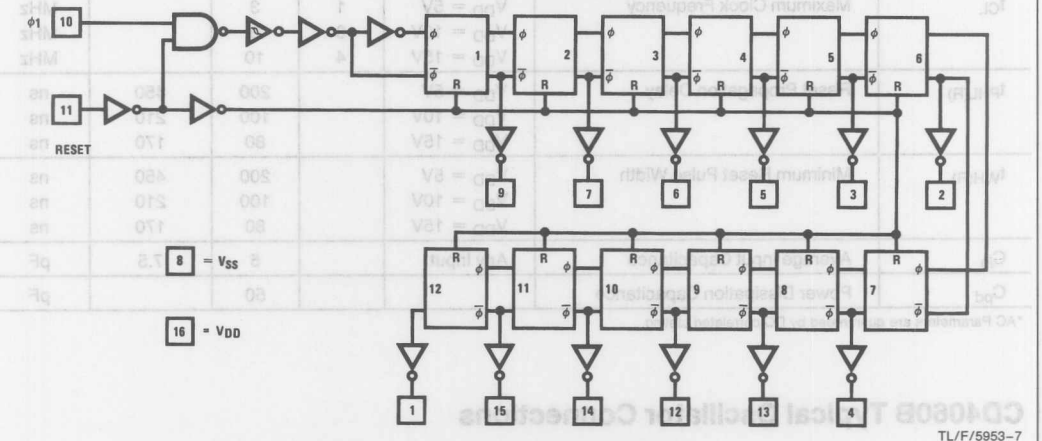
Schematic Diagrams

CD4020BM/CD4020BC Schematic Diagram



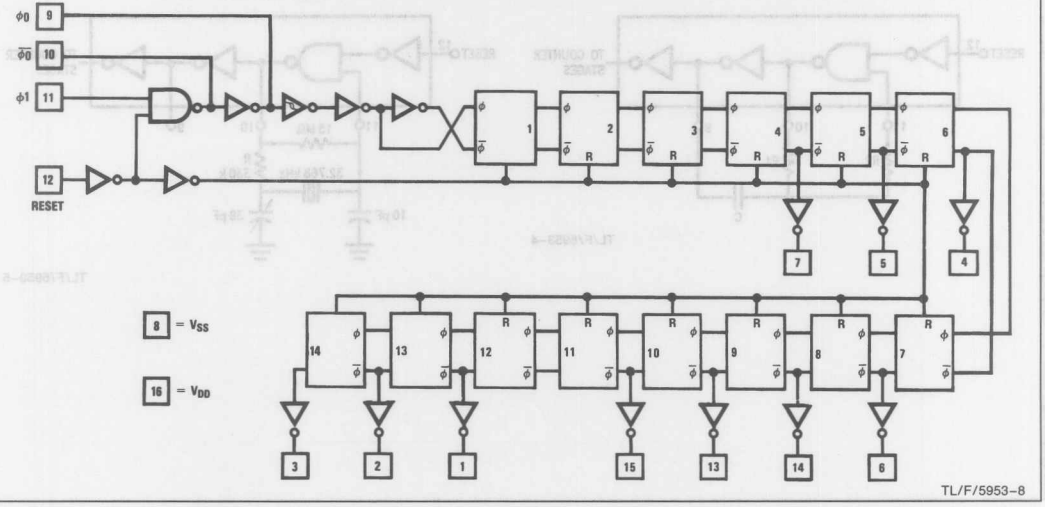
TL/F/5953–6

CD4040BM/CD4040BC Schematic Diagram



TL/F/5953–7

CD4060BM/CD4060BC Schematic Diagram



TL/F/5953–8

National Semiconductor

CD4021BM/CD4021BC 8-Stage Static Shift Register

General Description

The CD4021BM/CD4021BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh, and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is jammed into each stage of the register asynchronously with the clock.

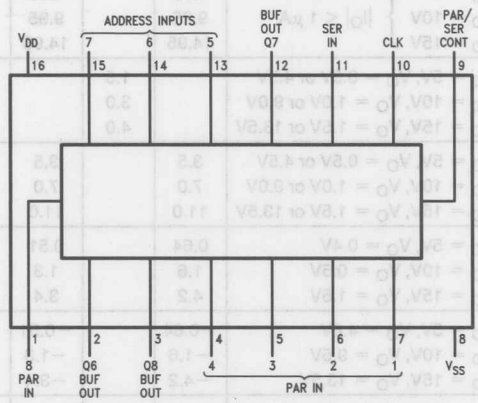
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagram

Dual-In-Line Package



TL/F/5954–1

Top View

Order Number CD4021B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

CL*	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⎍	0	0	X	X	0	Q_{n-1}	
⎍	1	0	X	X	1	Q_{n-1}	No
⎎	X	0	X	X	Q1	Q_n	Change

*Level change
X = Don't care case

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	$-0.5V$ to $+18V$
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD}+0.5V$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4021BM	$-55°C$ to $+125°C$
CD4021BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4021BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		5		0.1	5		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		10		0.2	10		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		20		0.3	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $V_{DD}=10V$ | $V_{DD}=15V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $V_{DD}=10V$ | $V_{DD}=15V$ | $\|I_O\|<1\ \mu A$	4.95		4.95	5		4.95		V
			9.95		9.95	10		9.95		V
			14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD}=10V, V_O=1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD}=10V, V_O=1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V, V_O=0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD}=15V, V_O=1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V, V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V, V_O=9.5V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD}=15V, V_O=13.5V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V, V_{IN}=0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD}=15V, V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4021BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		20		0.1	20		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		40		0.2	40		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		80		0.3	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $V_{DD}=10V$ | $V_{DD}=15V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4021BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time	V_{DD} = 5V		240	350	ns
		V_{DD} = 10V		100	175	ns
		V_{DD} = 15V		70	140	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5V	2.5	3.5		MHz
		V_{DD} = 10V	5	10		MHz
		V_{DD} = 15V	8	16		MHz
t_W	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_rCL, t_fCL	Clock Rise and Fall Time (Note 4)	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_s	Minimum Set-Up Time					
	Serial Input	V_{DD} = 5V		60	120	ns
	$t_H \geq$ 200 ns	V_{DD} = 10V		40	80	ns
	(Ref. to CL)	V_{DD} = 15V		30	60	ns
	Parallel Inputs	V_{DD} = 5V		25	50	ns
	$t_H \geq$ 200 ns	V_{DD} = 10V		15	30	ns
	(Ref. to P/S)	V_{DD} = 15V		10	20	ns

*AC Parameters are guaranteed by DC correlated testing.

	Parallel/Serial Control	V_{DD} = 15V			15	ns
t_{WH}	Minimum P/S Pulse Width	V_{DD} = 5V		150	250	ns
		V_{DD} = 10V		75	125	ns
		V_{DD} = 15V		50	100	ns
t_{REM}	Minimum P/S Removal Time (Ref. to CL)	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

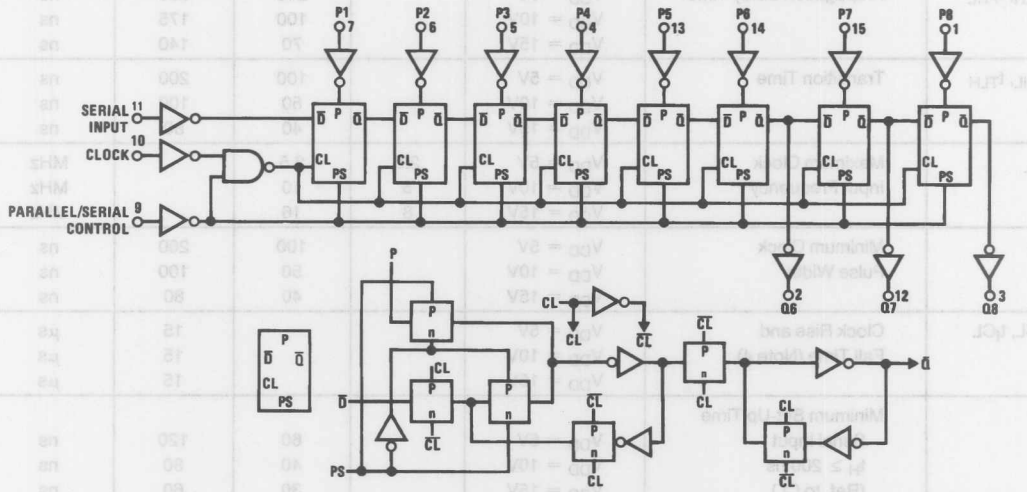
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: If more than one unit is cascaded t_rCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

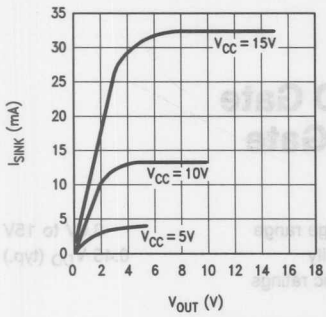
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Logic Diagram

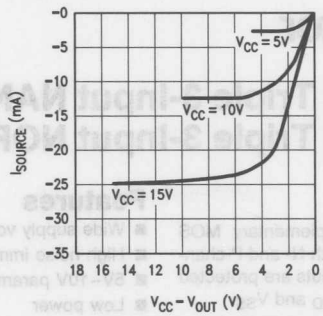


TL/F/5954–2

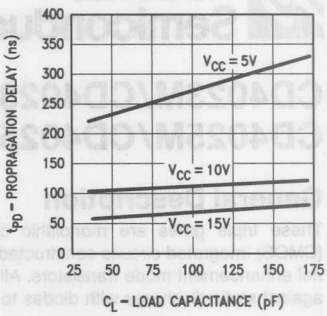
Typical Performance Characteristics



TL/F/5954–3



TL/F/5954–4



TL/F/5954–5

National Semiconductor

CD4023M/CD4023C Triple 3-Input NAND Gate
CD4025M/CD4025C Triple 3-Input NOR Gate

General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

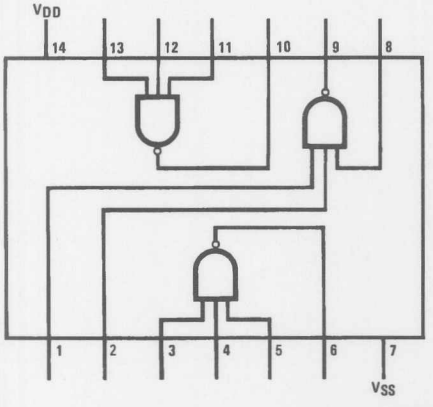
Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ 5V–10V parametric ratings	
■ Low power	

Connection Diagrams

Dual-In-Line Packages

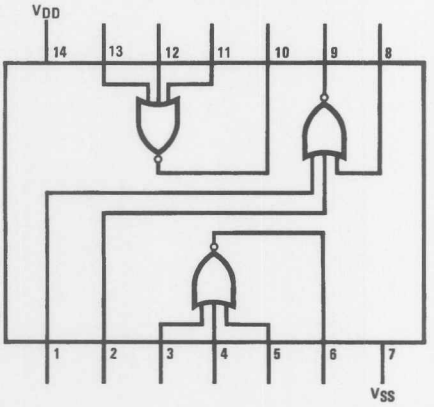
CD4023M/CD4023C



TL/F/5955–1

Top View

CD4025M/CD4025C



TL/F/5955–2

Top View

Order Number CD4023* or CD4025*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$V_{SS}-$ to $V_{DD}+0.3V$
Operating Temperature Range	
CD4023M, CD4025M	$-55°C$ to $+125°C$
CD4023C, CD4025C	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{DD} Range	$V_{SS}+3.0V$ to $V_{SS}+15V$
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics CD4023M, CD4025M

Symbol	Parameter	Conditions	Limits							Units
			$-55°C$		$+25°C$			$+125°C$		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD}=5.0V$		0.05		0.001	0.05		3.0	μA
		$V_{DD}=10V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD}=5.0V$		0.25		0.005	0.25		15	μW
		$V_{DD}=10V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD}=5.0V, V_I=V_{DD}, I_O=0A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V, V_I=V_{DD}, I_O=0A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD}=5.0V, V_I=V_{SS}, I_O=0A$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10V, V_I=V_{SS}, I_O=0A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD}=5.0V, V_O=3.6V, I_O=0A$	1.5		1.5	2.25		1.4		V
		$V_{DD}=10V, V_O=7.2V, I_O=0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD}=5.0V, V_O=0.95V, I_O=0A$	1.4		1.5	2.25		1.5		V
		$V_{DD}=10V, V_O=2.9V, I_O=0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4025) (Note 2)	$V_{DD}=5.0V, V_O=0.4V, V_I=V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD}=10V, V_O=0.5V, V_I=V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4025) (Note 2)	$V_{DD}=5.0V, V_O=2.5V, V_I=V_{SS}$	-0.62		-0.5	-2.0		-0.35		mA
		$V_{DD}=10V, V_O=9.5V, V_I=V_{SS}$	-0.62		-0.5	-1.0		-0.35		mA
I_DN	Output Drive Current N-Channel (4023) (Note 2)	$V_{DD}=5.0V, V_O=0.4V, V_I=V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD}=10V, V_O=0.5V, V_I=V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4023) (Note 2)	$V_{DD}=5.0V, V_O=2.5V, V_I=V_{SS}$	-0.31		-0.25	-0.5		-0.175		mA
		$V_{DD}=10V, V_O=9.5V, V_I=V_{SS}$	-0.75		-0.6	-1.2		-0.4		mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$		0.05		0.005	0.5		15	μA
		$V_{DD} = 10V$		5.0		0.005	5.0		30	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$		2.5		0.025	2.5		75	μW
		$V_{DD} = 10V$		50		0.05	50		300	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$		0.01		0	0.01		0.05	V
		$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.01		0	0.01		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$	4.99		4.99	5.0		4.95		V
		$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.99		9.99	10		9.95		V
I_I	Input Current					10				pA
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$	1.5		1.5	2.25		1.4		V
		$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$	1.4		1.5	2.25		1.5		V
		$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4025) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.35		0.3	1.0		0.24		mA
		$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.72		0.6	2.5		0.48		mA
I_DP	Output Drive Current P-Channel (4025) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.35		−0.3	−2.0		−0.24		mA
		$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.3		−0.25	−1.0		−0.2		mA
I_DN	Output Drive Current N-Channel (4023) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.145		0.12	0.5		0.095		mA
		$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.3		0.25	0.6		0.2		mA
I_DP	Output Drive Current P-Channel (4023) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.145		−0.12	−0.5		−0.095		mA
		$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35		−0.3	−1.2		−0.24		mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 15$ pF, and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CD4025M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	40 70	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4025C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4023M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4023C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

National Semiconductor

CD4023BM/CD4023BC Buffered Triple 3-Input NAND Gate
CD4025BM/CD4025BC Buffered Triple 3-Input NOR Gate

General Description

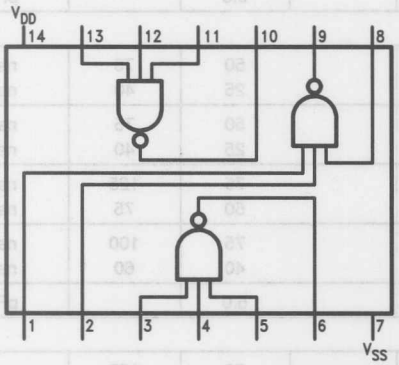
These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

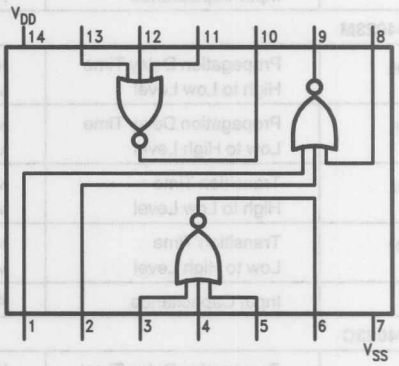
CD4023BM/CD4023BC
Dual-In-Line Package



TL/F/5956–1

Top View

CD4025BM/CD4025BC
Dual-In-Line Package



TL/F/5956–2

Top View

Order Number CD4023B* or CD4025B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD}+0.5\ V_{DC}$
Storage Temp. Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

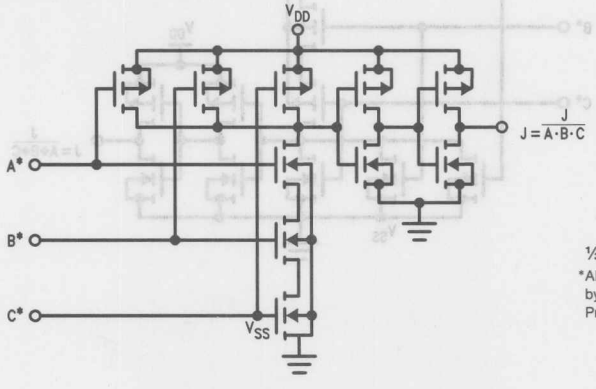
DC Supply Voltage (V_{DD})	$5\ V_{DC}$ to $15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4023BM, CD4025BM	$-55°C$ to $+125°C$
CD4023BC, CD4025BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4023BM, CD4025BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Typ	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.005	0.5		15	μA
		V_{DD} = 15V		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD}=5V, V_O=4.5V, $\lvert I_O\rvert$<1μA		1.5		2	1.5		1.5	V
		V_{DD}=10V, V_O=9.0V, $\lvert I_O\rvert$<1μA		3.0		4	3.0		3.0	V
		V_{DD}=15V, V_O=13.5V, $\lvert I_O\rvert$<1μA		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD}=5V, V_O=0.5V, $\lvert I_O\rvert$<1μA	3.5		3.5	3		3.5		V
		V_{DD}=10V, V_O=1.0V, $\lvert I_O\rvert$<1μA	7.0		7.0	6		7.0		V
		V_{DD}=15V, V_O=1.5V, $\lvert I_O\rvert$<1μA	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD}=5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.2		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Schematic Diagram

CD4023BC/CD4023BM



⅓ Device Shown

*All Inputs Protected by Standard CMOS Input Protection Circuit.

TL/F/5956–3

DC Electrical Characteristics CD4023BC, CD4025BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Typ	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.004	1.0		7.5	μA
		V_{DD} = 10V		2.0		0.005	2.0		15	μA
		V_{DD} = 15V		4.0		0.006	4.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V, $\lvert I_O \rvert$ < 1μA		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V, $\lvert I_O \rvert$ < 1μA		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V, $\lvert I_O \rvert$ < 1μA		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V, $\lvert I_O \rvert$ < 1μA	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V, $\lvert I_O \rvert$ < 1μA	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V, $\lvert I_O \rvert$ < 1μA	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

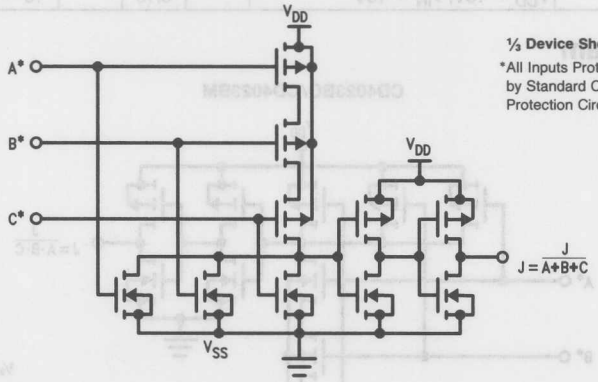
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Schematic Diagram

CD4025BM/CD4025BC



⅓ Device Shown

*All Inputs Protected by Standard CMOS Input Protection Circuit.

TL/F/5956–4

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, unless otherwise specified

Symbol	Parameter	Conditions	CD4023BC CD4023BM			CD4025BC CD4025BM			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PHL}	Propagation Delay, High-to-Low Level	$V_{DD} = 5V$		130	250		130	250	ns
		$V_{DD} = 10V$		60	100		60	100	ns
		$V_{DD} = 15V$		40	70		40	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	$V_{DD} = 5V$		110	250		120	250	ns
		$V_{DD} = 10V$		50	100		60	100	ns
		$V_{DD} = 15V$		35	70		40	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		90	200		90	200	ns
		$V_{DD} = 10V$		50	100		50	100	ns
		$V_{DD} = 15V$		40	80		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 4)	Any Gate		17			17		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note AN-90.

National Semiconductor

CD4024BM/CD4024BC
7-Stage Ripple Carry Binary Counter

General Description

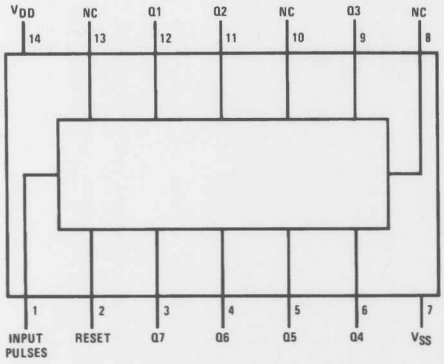
The CD4024BM/CD4024BC is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical "0" stage by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- High speed — 12 MHz (typ.) input pulse rate $V_{DD} - V_{SS} = 10V$
- Fully static operation

Connection Diagram

Dual-In-Line Package



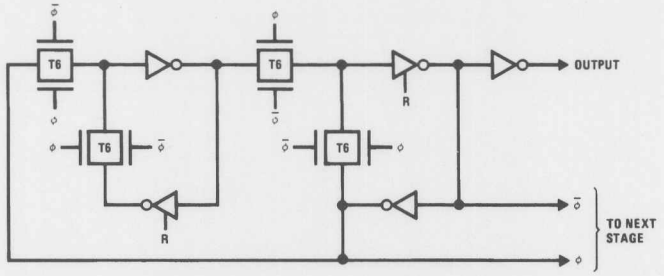
TL/F/5957–1

Top View

Order Number CD4024B*

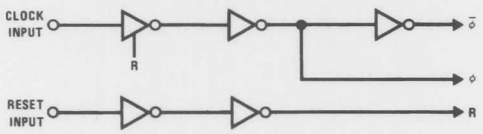
*Please look into Section 8, Appendix D for availability of various package types.

Schematic Diagrams



TL/F/5957–3

Input Logic



Flip-flop logic (1 of 7 identical stages).

TL/F/5957–4

Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (Soldering, 10 sec.) (T_L)	260°C

Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4024BM	−55°C to +125°C
CD4024BC	−40°C to +85°C

DC Electrical Characteristics CD4024BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		0.7	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ <1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ <1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ <1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ <1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4024BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.3	20		150	μA
		V_{DD} = 10V		40		0.5	40		300	μA
		V_{DD} = 15V		60		0.7	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ <1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ <1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4024BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C		+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ k, t_r and $t_f = 20$ ns unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time to Q1 Output	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width	$V_{DD} = 5V$		75	200	ns
		$V_{DD} = 10V$		40	110	ns
		$V_{DD} = 15V$		35	90	ns
t_{RCL}, t_{FCL}	Input Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			10	μs
		$V_{DD} = 15V$			8	μs
f_{CL}	Maximum Input Pulse Frequency	$V_{DD} = 5V$	1.5	5		MHz
		$V_{DD} = 10V$	4	12		MHz
		$V_{DD} = 15V$	5	15		MHz
t_{PHL}	Reset Propagation Delay Time	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
t_{WH}	Reset Minimum Pulse Width	$V_{DD} = 5V$		185	350	ns
		$V_{DD} = 10V$		85	125	ns
		$V_{DD} = 15V$		70	100	ns
C_{IN}	Input Capacitance (Note 4)	Any Input		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

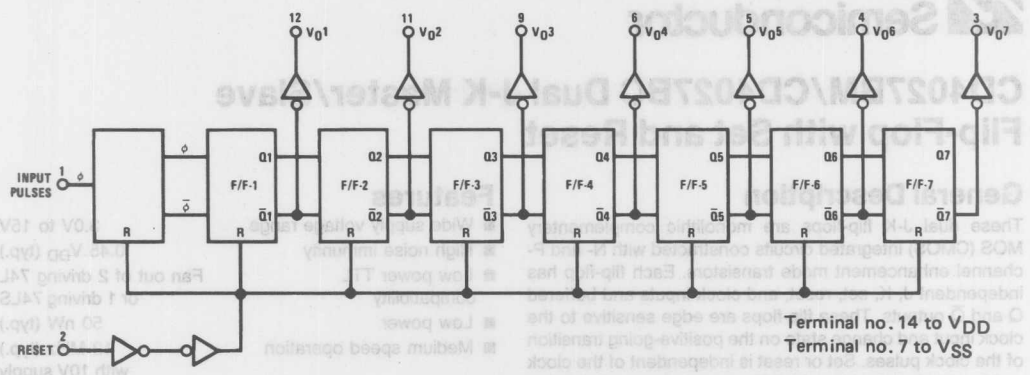
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic tesing.

Logic Diagram



Terminal no. 14 to V_{DD}
Terminal no. 7 to V_{SS}

TL/F/5957–2

National Semiconductor

CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset

General Description

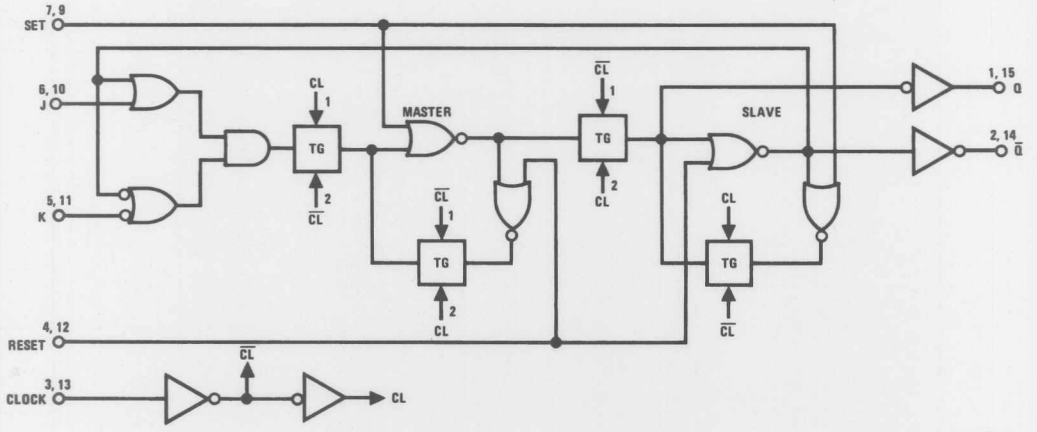
These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

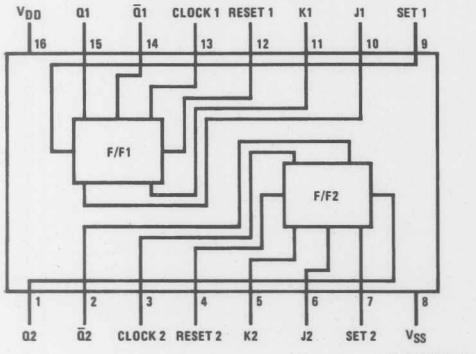
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Low power	50 nW (typ.)
■ Medium speed operation	12 MHz (typ.) with 10V supply

Schematic and Connection Diagrams



TL/F/5958–1

Dual-In-Line Package



TL/F/5958–2

Top View

Order Number CD4027B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4027BM	$-55°C$ to $+125°C$
CD4027BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4027BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		1			1		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		2			2		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		4			4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

			−55°C		+25°C			+125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		4			4		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		8			8		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

	from Clock to Q or $\overline{Q}$	V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Set to $\overline{Q}$ or Reset to Q	V_{DD} = 5V		170	340	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Set to Q or Reset to $\overline{Q}$	V_{DD} = 5V		110	220	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_S	Minimum Data Setup Time	V_{DD} = 5V		135	270	ns
		V_{DD} = 10V		55	110	ns
		V_{DD} = 15V		45	90	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency (Toggle Mode)	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_W	Minimum Clock Pulse Width ($t_{WH} = t_{WL}$)	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{WH}	Minimum Set and Reset Pulse Width	V_{DD} = 5V		80	160	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Per Flip-Flop (Note 4)		35		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

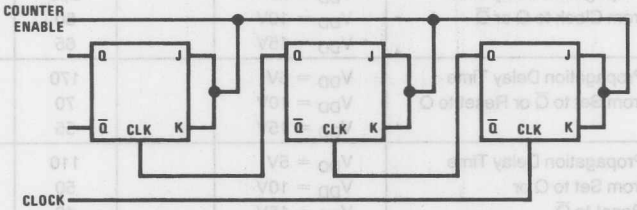
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

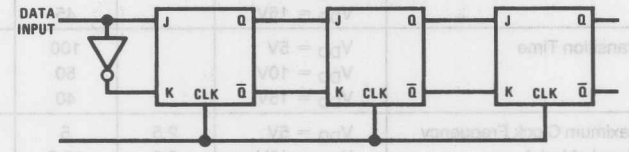
Typical Applications

Ripple Binary Counters



TL/F/5958–3

Shift Registers



TL/F/5958–4

Truth Table

	•t_{n-1} Inputs					■t_n Outputs	
CL▲	J	K	S	R	Q	Q	$\bar{Q}$
⌐⌐	I	X	O	O	O	I	O
⌐⌐	X	O	O	O	I	I	O
⌐⌐	O	X	O	O	O	O	I
⌐⌐	X	I	O	O	I	O	I
⌐⌐	X	X	O	O	X	(No Change)	
X	X	X	I	O	X	I	O
X	X	X	O	I	X	O	I
X	X	X	I	I	X	I	I

Where: I = High Level
O = Low Level
▲ = Level Change
X = Don't Care
• = t_{n-1} refers to the time interval prior to the positive clock pulse transition
■ = t_n refers to the time intervals after the positive clock pulse transition

National Semiconductor

CD4028BM/CD4028BC BCD-to-Decimal Decoder

General Description

The CD4028BM/CD4028BC is a BCD-to-decimal or binary-to-octal decoder consisting of 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the 4 inputs, A, B, C, and D, results in a high level at the selected 1-of-10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A, B, and C is decoded in octal at outputs 0–7. A high level signal at the D input inhibits octal decoding and causes outputs 0–7 to go low.

All inputs are protected against static discharge damage by diode clamps to V_{DD} and V_{SS}.

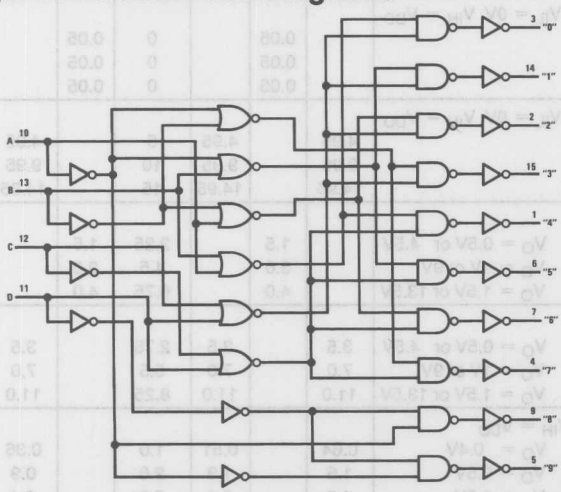
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Low power
- Glitch free outputs
- "Positive logic" on inputs and outputs

Applications

- Code conversion
- Address decoding
- Indicator-tube decoder

Logic and Connection Diagrams



TL/F/5959–1

Dual-In-Line Package



TL/F/5959–2

Top View

Order Number CD4028B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	BCD States
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	Extraordinary States
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

1 = High Level
0 = Low Level

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5 to +18V
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3 to 15V
Input Voltage (V_{IN})	0 to V_{DD}V
Operating Temperature Range (T_A)	
CD4028BM	−55°C to +125°C
CD4028BC	−40°C to +185°C

DC Electrical Characteristics CD4028BC (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.01	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.01	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1 μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1 μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1.0		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.6		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	6.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.4		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−1.0		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.0		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4028BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.01	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.01	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1 μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

DC Electrical Characteristics CD4028BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.2		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	6.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−0.2		−0.16	−0.32		−0.12		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.5		−0.4	−0.8		−0.3		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3			−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3			0.3		1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, Input $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time	$V_{CC} = 5V$		240	480	ns
		$V_{CC} = 10V$		100	200	ns
		$V_{CC} = 15V$		70	140	ns
t_{THL} or t_{TLH}	Transition Time	$V_{CC} = 5V$		175	350	ns
		$V_{CC} = 10V$		75	150	ns
		$V_{CC} = 15V$		60	110	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

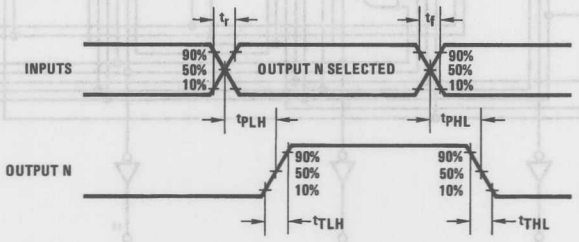
* AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Switching Time Waveforms



TL/F/5959–3

National Semiconductor

CD4029BM/CD4029BC Presettable Binary/Decade Up/Down Counter

General Description

The CD4029BM/CD4029BC is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1", the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

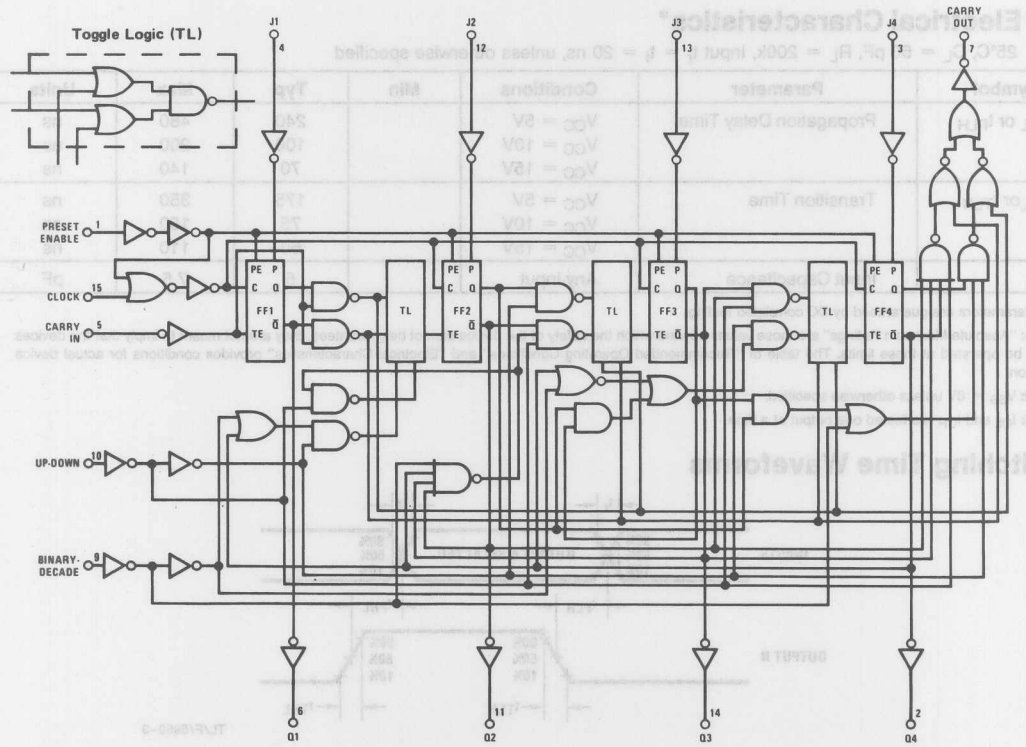
A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0". Advancement is inhibited when either or both of these two inputs is at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Parallel jam inputs
- Binary or BCD decade up/down counting

Logic Diagram



TL/F/5960–1

Absolute Maximum Ratings

(Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5V$ to $+18$ V_{DC}
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD} + 0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4029BM	$-55°C$ to $+125°C$
CD4029BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4029BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5			5	5	150	μA
		$V_{DD} = 10V$		10			10		300	μA
		$V_{DD} = 15V$		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4029BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20			20		150	μA
		$V_{DD} = 10V$		40			40		300	μA
		$V_{DD} = 15V$		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4029BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_{rCL} = t_{fCL} = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCKED OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q Outputs	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		70	140	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V		320	640	ns
		V_{DD} = 10V		135	270	ns
		V_{DD} = 15V		110	220	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	C_L = 15 pF				
		V_{DD} = 5V		285	570	ns
		V_{DD} = 10V		120	240	ns
		V_{DD} = 15V		95	190	ns
t_{THL} or t_{TLH}	Transition Time/Q or Carry Output	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH} or t_{WL}	Minimum Clock Pulse Width	V_{DD} = 5V		160	320	ns
		V_{DD} = 10V		70	135	ns
		V_{DD} = 15V		55	110	ns
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		180	360	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	3.1		MHz
		V_{DD} = 10V	3.7	7.4		MHz
		V_{DD} = 15V	4.5	9		MHz
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		65		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200 k, Input t_{rCL} = t_{fCL} = 20 ns, unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PRESET ENABLE OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q output	V_{DD} = 5V		285	570	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		95	195	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V		400	800	ns
		V_{DD} = 10V		165	330	ns
		V_{DD} = 15V		135	260	ns
t_{WH}	Minimum Preset Enable Pulse Width	V_{DD} = 5V		80	160	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{REM}	Minimum Preset Enable Removal Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		60	120	ns
		V_{DD} = 15V		50	100	ns
CARRY INPUT OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V		265	530	ns
		V_{DD} = 10V		110	220	ns
		V_{DD} = 15V		90	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time to Carry Output	C_L = 15 pF				
		V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		70	140	ns

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

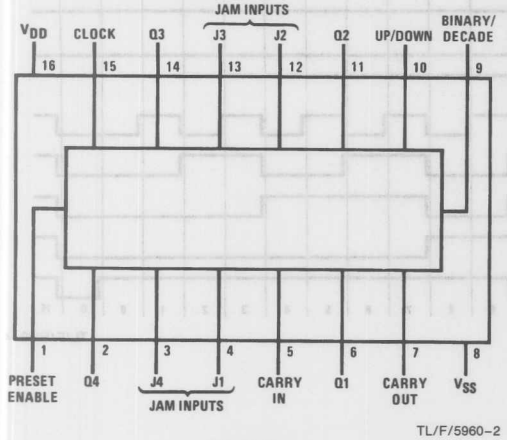
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Connection Diagram

Dual-In-Line Package



TL/F/5960–2

Top View

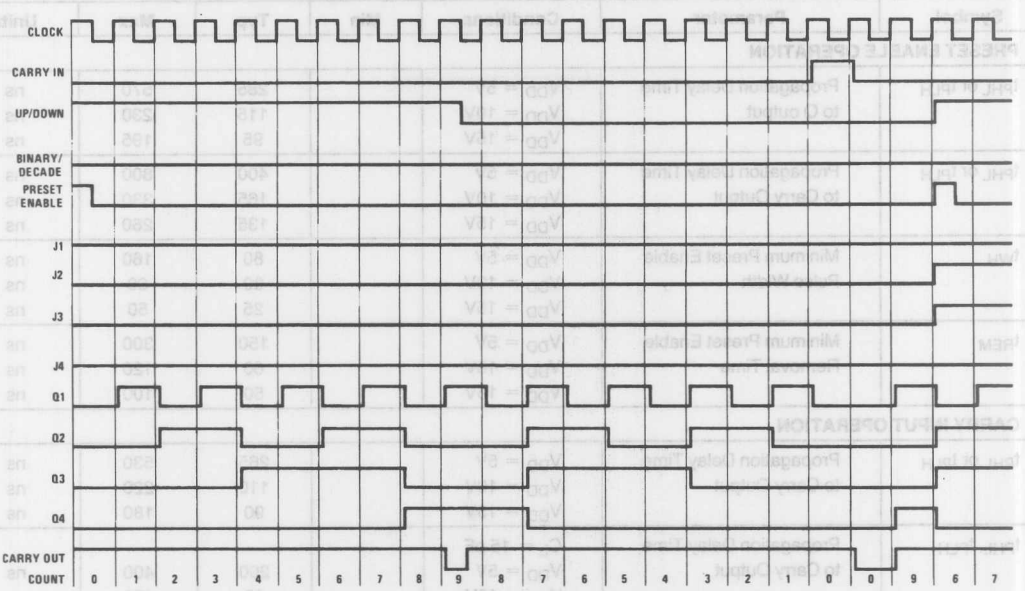
Order Number CD4029B*

*Please look into Section 8, Appendix D for availability of various package types.

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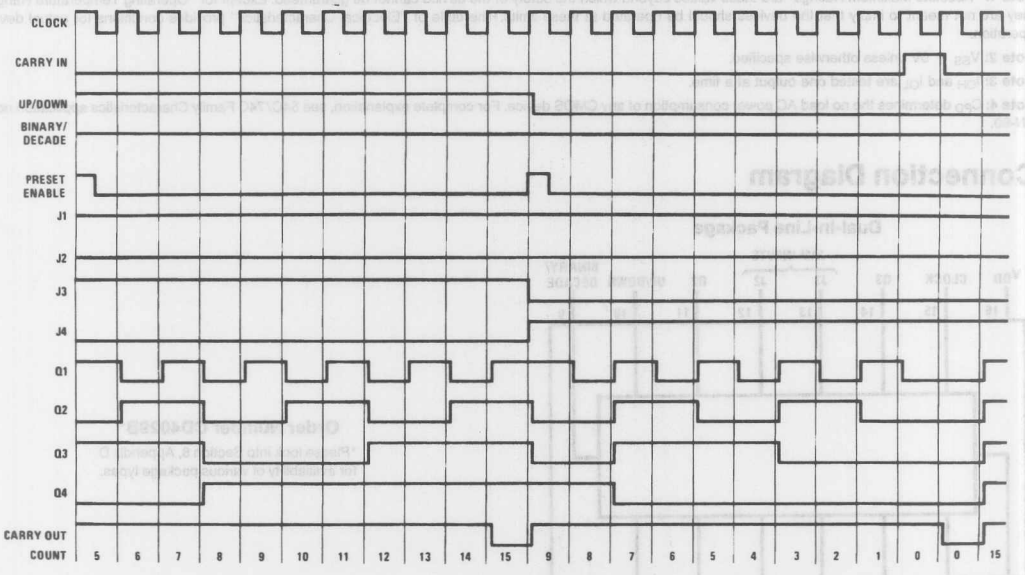
Logic Waveforms

Decade Mode



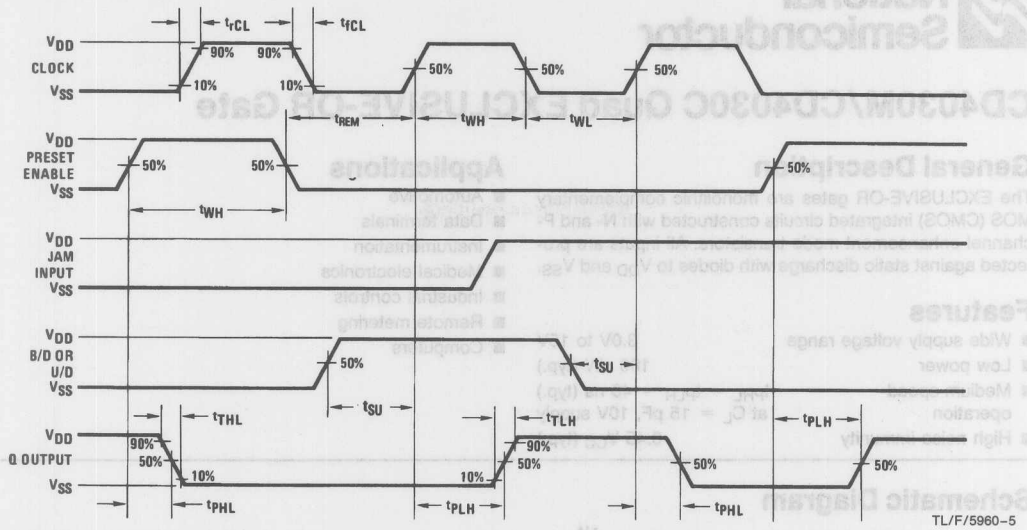
TL/F/5960–3

Binary Mode



TL/F/5960–4

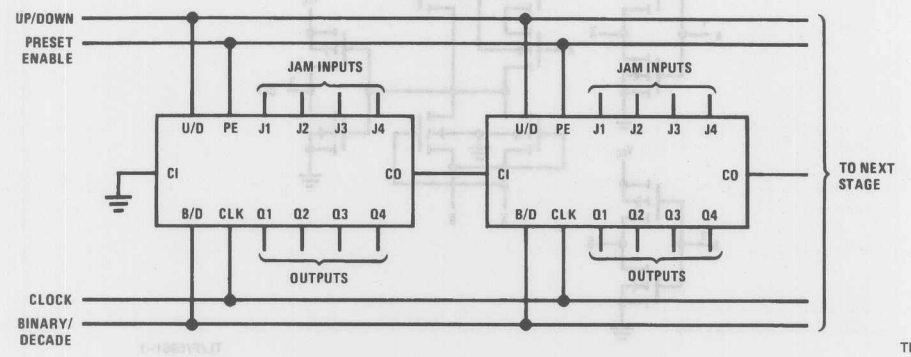
Switching Time Waveforms



TL/F/5960–5

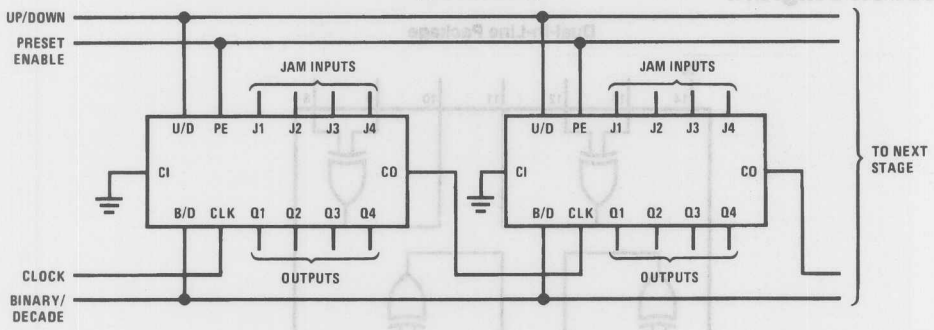
Cascading Packages

Parallel Clocking



TL/F/5960–6

Ripple Clocking



TL/F/5960–7

Carry out lines at the 2nd or later stages may have a negative-going spike due to differential internal delays. These spikes do not affect counter operation, but if the carry out is used to trigger external circuitry the carry out should be gated with the clock.

National Semiconductor

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

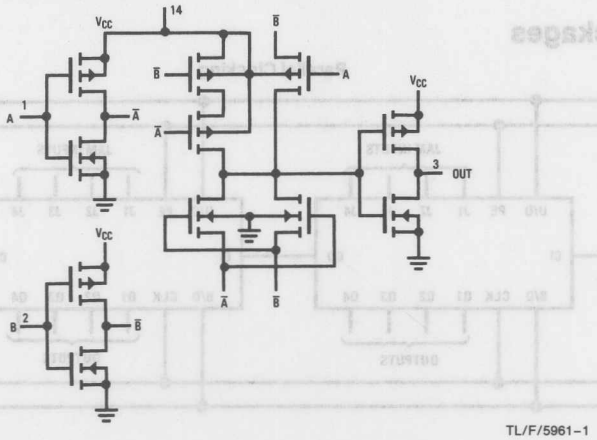
Features

■ Wide supply voltage range	3.0V to 15V
■ Low power	100 nW (typ.)
■ Medium speed operation	$t_{PHL} = t_{PLH} = 40$ ns (typ.) at $C_L = 15$ pF, 10V supply
■ High noise immunity	0.45 V_{CC} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

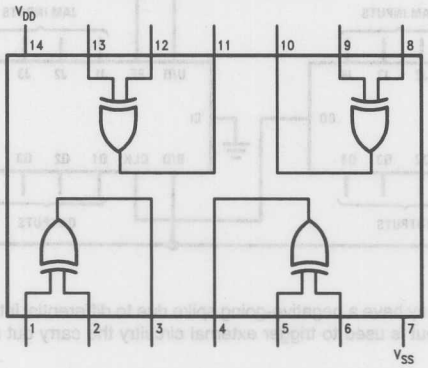
Schematic Diagram



TL/F/5961–1

Connection Diagram

Dual-In-Line Package



TL/F/5961–2

Order Number CD4030*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (Note 1) V_{SS} −0.3V to V_{SS} +15.5V

Operating Temperature Range

CD4030M −55°C to +125°C

CD4030C −40°C to +85°C

Storage Temperature Range −65°C to +150°C

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V_{DD} Range V_{SS} +3.0V to V_{SS} +15V

Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics CD4030M

Symbol	Parameter	Conditions	Limits									Units
			−55°C			+25°C			+125°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	V_{DD} = 5.0V			0.5		0.005	0.5			30	μA
		V_{DD} = 10V			1.0		0.01	1.0			60	μA
P_D	Quiescent Device Dissipation Package	V_{DD} = 5.0V			2.5		0.025	2.5			150	μW
		V_{DD} = 10V			10		0.1	10			600	μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
		V_{DD} = 10V			0.05		0	0.05			0.05	V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
		V_{DD} = 10V	9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
		V_{DD} = 10V	3.0			3.0	4.5		2.9			V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
		V_{DD} = 10V	2.9			3.0	4.5		3.0			V
I_DN	Output Drive Current N-Channel (Note 2)	V_{DD} = 5.0V	0.75			0.6	1.2		0.45			mA
		V_{DD} = 10V	1.5			1.2	2.4		0.9			mA
I_DP	Output Drive Current P-Channel (Note 2)	V_{DD} = 5.0V	−0.45			−0.3	−0.6		−0.21			mA
		V_{DD} = 10V	−0.95			−0.65	−1.3		−0.45			mA
I_I	Input Current	V_I = 0V or V_I = V_{DD}					10					pA

DC Electrical Characteristics CD4030C

Symbol	Parameter	Conditions	Limits									Units
			−40°C			+25°C			+85°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	V_{DD} = 5.0V			5.0		0.05	5.0			70	μA
		V_{DD} = 10V			10		0.1	10			140	μA
P_D	Quiescent Device Dissipation Package	V_{DD} = 5.0V			25		0.25	25			350	μW
		V_{DD} = 10V			100		1.0	100			1,400	μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5.0V			0.05		0	0.05			0.05	V
		V_{DD} = 10V			0.05		0	0.05			0.05	V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0V	4.95			4.95	5.0		4.95			V
		V_{DD} = 10V	9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
		V_{DD} = 10V	3.0			3.0	4.5		2.9			V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
		V_{DD} = 10V	2.9			3.0	4.5		3.0			V
I_DN	Output Drive Current N-Channel (Note 2)	V_{DD} = 5.0V	0.35			0.3	1.2		0.25			mA
		V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
I_DP	Output Drive Current P-Channel (Note 2)	V_{DD} = 5.0V	−0.21			−0.15	−0.6		−0.12			mA
		V_{DD} = 10 V	−0.45			−0.32	−1.3		−0.25			mA
I_I	Input Current	V_I = 0V or V_I = V_{DD}					10					pA

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AC Electrical Characteristics* CD4030M

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
t_{PHL}	Propagation Delay Time	V_{DD} = 5.0V		100	200	ns
		V_{DD} = 10V		40	100	ns
t_{PLH}	Propagation Delay Time	V_{DD} = 5.0V		100	200	ns
		V_{DD} = 10V		40	100	ns
t_{THL}	Transition Time High to Low Level	V_{DD} = 5.0V		70	150	ns
		V_{DD} = 10V		25	75	ns
t_{TLH}	Transition Time Low to High Level	V_{DD} = 5.0V		80	150	ns
		V_{DD} = 10V		30	75	ns
C_I	Input Capacitance	V_I = 0V or V_I = V_{DD}		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4030C

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
t_{PHL}	Propagation Delay Time	V_{DD} = 5.0V		100	300	ns
		V_{DD} = 10V		40	150	ns
t_{PLH}	Propagation Delay Time	V_{DD} = 5.0V		100	300	ns
		V_{DD} = 10V		40	150	ns
t_{THL}	Transition Time High to Low Level	V_{DD} = 5.0V		70	300	ns
		V_{DD} = 10V		25	150	ns
t_{TLH}	Transition Time Low to High Level	V_{DD} = 5.0V		80	300	ns
		V_{DD} = 10V		30	150	ns
C_I	Input Capacitance	V_I = 0V or V_I = V_{DD}		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

Note 2: I_DN and I_DP are tested one output at a time.

Truth Table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

National Semiconductor

CD4031BM/CD4031BC
64-Stage Static Shift Register

General Description

The CD4031BM/CD4031BC is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is low) or data at the RECIRCULATE input (when MODE CONTROL is high), which meets the setup and hold time requirements, is entered into the first stage of the register and is shifted one stage at each positive transition of the CLOCK.

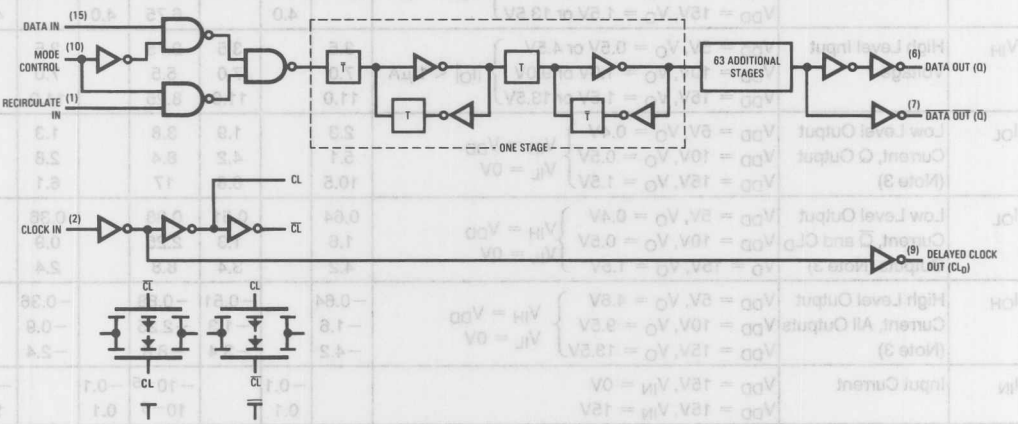
Data output is available in both true and complement forms from the 64th stage. Both the DATA OUT (Q) AND $\overline{\text{DATA OUT}}$ ($\overline{Q}$) outputs are fully buffered.

The CLOCK input of the CD4031BM/CD4031BC is fully buffered, and present only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT (CL_D) has been provided to allow reduced clock drive fan-out and transition time requirements when cascading packages.

Features

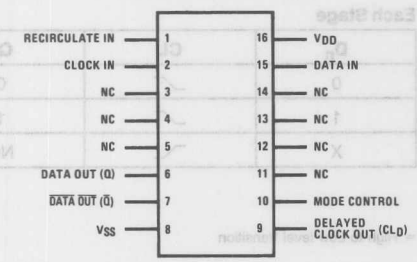
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation — DC to 8 MHz, V_{DD} = 10V (typ.)
- Fully buffered clock input — 5 pF (typ.) input capacitance
- Single phase clocking requirements
- Delayed clock output for reduced clock drive requirements
- Fully buffered outputs
- High current sinking capability — 1.6 mA
- Q output — @ V_{DD} = 5V and 25°C

Logic and Connection Diagrams



TL/F/5962–1

Dual-In-Line Package



Top View

TL/F/5962–2

Order Number CD4031B*

*Please look into Section 8, Appendix D for availability of various package types.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (T_L) (Soldering, 10 sec.)	260°C

Input Voltage (V_{IN}) 0V to V_{DD}

Operating Temperature Range (T_A)

CD4031BM	−55°C to +125°C
CD4031BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) CD4031BM

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.01	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.01	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V, V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V, V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V, $\|I_O\|$ < 1 μA		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V, $\|I_O\|$ < 1 μA	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output (Note 3)	V_{DD} = 5V, V_O = 0.4V	2.3		1.9	3.8		1.3		mA
		V_{DD} = 10V, V_O = 0.5V, V_{IH} = V_{DD}, V_{IL} = 0V	5.1		4.2	8.4		2.8		mA
		V_{DD} = 15V, V_O = 1.5V	10.5		8.8	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V, V_{IH} = V_{DD}, V_{IL} = 0V	1.6		1.3	2.25		0.9		mA
		V_D = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V, V_{IH} = V_{DD}, V_{IL} = 0V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Truth Tables

Mode Control (Data Selection)

Mode Control	Data In	Recirculate In	Data Into First Stage
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

Each Stage

D_n	CL	Q_n
0	⌐	0
1	⌐	1
X	⌙	NC

X = irrelevant NC = no change ⌐ = Low to High level transition ⌙ = High to Low level transition

DC Electrical Characteristics (Note 2) CD4031BC

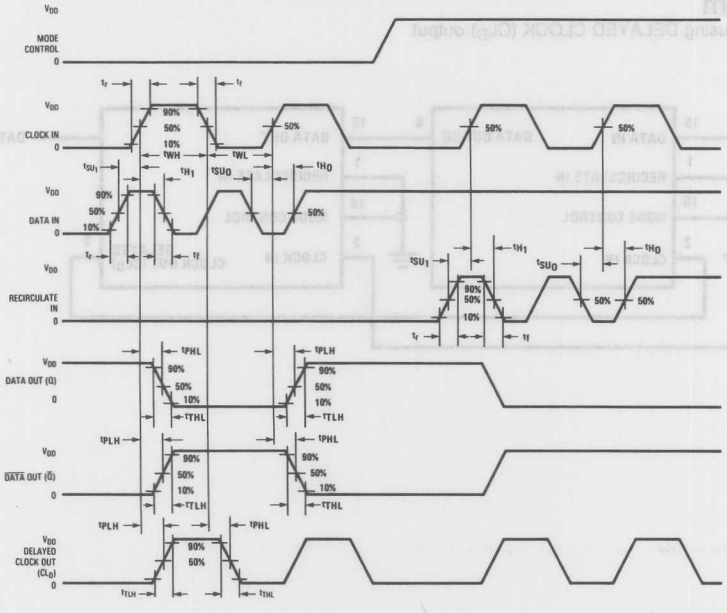
Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.01	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.01	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V, V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V, V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V, $\|I_O\|$ < 1 μA		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V, $\|I_O\|$ < 1 μA	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output (Note 3)	V_{DD} = 5V, V_O = 0.4V	1.8		1.6	3.8		1.3		mA
		V_{DD} = 10V, V_O = 0.5V, V_{IH} = V_{DD}, V_{IL} = 0V	4.0		3.5	8.4		2.8		mA
		V_{DD} = 15V, V_O = 1.5V	8.7		7.5	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V, V_{IH} = V_{DD}, V_{IL} = 0V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V, V_{IH} = V_{DD}, V_{IL} = 0V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.0		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of 'Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms



TL/F/5962–3

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input $t_r = t_f$ = 20 ns, unless otherwise specified

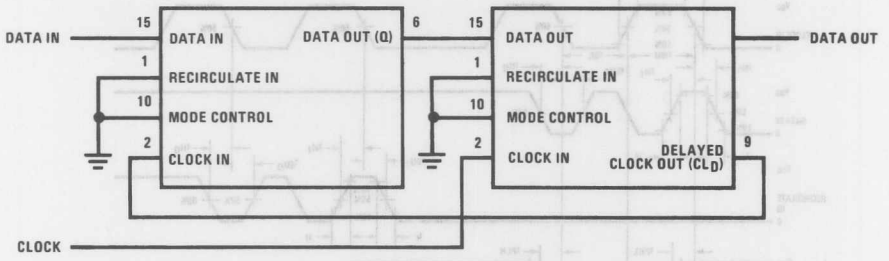
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to Q and $\overline{Q}$	V_{CC} = 5V		300	600	ns
		V_{CC} = 10V		125	250	ns
		V_{CC} = 15V		100	200	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to CL_D	V_{CC} = 5V		125	250	ns
		V_{CC} = 10V		60	125	ns
		V_{CC} = 15V		50	100	ns
t_{THL}, t_{TLH}	Output Transition Time, All Outputs	V_{CC} = 5V		100	200	ns
		V_{CC} = 10V		50	100	ns
		V_{CC} = 15V		40	80	ns
t_{SU_0}	Minimum Data Setup Time, DATA IN or	V_{CC} = 5V		100	200	ns
t_{SU_1}	RECIRCULATE IN to Clock	V_{CC} = 10V		50	100	ns
		V_{CC} = 15V		40	80	ns
t_{H_0}	Minimum Data Hold Time, Clock to DATA IN	V_{CC} = 5V		100	200	ns
t_{H_1}	or RECIRCULATE IN	V_{CC} = 10V		50	100	ns
		V_{CC} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{CC} = 5V		150	30	ns
		V_{CC} = 10V		60	125	ns
		V_{CC} = 15V		50	100	ns
f_{CL}	Maximum Clock Frequency	V_{CC} = 5V	1.6	3.2		MHz
		V_{CC} = 10V	4.0	8.0		MHz
		V_{CC} = 15V	5.0	10		MHz
t_{RCL}, t_{FCL}	Maximum Clock Input Rise and Fall Times	V_{CC} = 5V	15			μs
	(Note 4)	V_{CC} = 10V	10			μs
		V_{CC} = 15V	5			μs
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 4: When clocking cascaded packages in parallel, one should insure that: $t_{r\,CL} \leq 2\,(t_{PD} - t_H)$ where: t_{PD} = the propagation delay of the driving stage and t_H = the hold time of the driven stage.

Block Diagram

cascading packages using DELAYED CLOCK (CL_D) output



TL/F/5962–4

National Semiconductor

CD4034BM/CD4034BC 8-Stage TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

General Description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

A ENABLE (AE): "A" data port is enabled only when AE is at logical "1". This allows the use of a common bus for multiple packages.

A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B): This input controls the direction of data flow. When at logical "1", data flows from port A to B (A is input, B is output). When at logical "0", the data flow direction is reversed.

ASYNCHRONOUS/SYNCHRONOUS (A/S): When A/S is at logical "0", data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1", data transfer is independent of the CLOCK for parallel operation. In serial mode, A/S input is internally disabled such that operation is always synchronous. (Asynchronous serial operation is not possible.)

PARALLEL/SERIAL (P/S): A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0", asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

CLOCK: Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0".

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

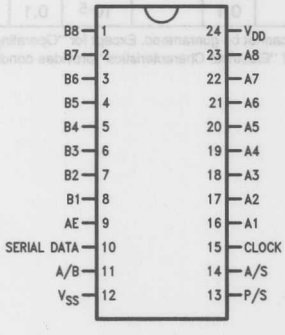
- Wide supply voltage range — 3.0V to 18V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- RCA CD4034B second source

Applications

- Parallel Input/Parallel Output
  Parallel Input/Serial Output
  Serial Input/Parallel Output
  Serial Input/Serial Output register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

Connection Diagram

Dual-In-Line Package



Top View

TL/F/5963–1

Order Number CD4034B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temp. Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	$+3\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4034BM	$-55°C$ to $+125°C$
CD4034BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4034BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		5			5		150	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		10			10		300	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95			4.95		V
		$V_{DD} = 10V$	9.95		9.95			9.95		V
		$V_{DD} = 15V$	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51			0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3			0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4			2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51			−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3			−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4			−2.4		mA
I_{IN}	Input Curent	$V_{DD} = 15V, V_{IN} = 0V$	−0.1		−0.1	-10^{-5}		−1.0		μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	TRI-STATE Leakage Current	$V_{DD} = 15V, V_O = 0V$	−0.1		−0.1	-10^{-5}		−1.0		μA
		$V_{DD} = 15V, V_O = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4034BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0			2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V, V_O = 0V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15V, V_O = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, input t_r = t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time, A (B) Synchronous Parallel Data or Serial Data Input, B (A) Parallel Data Output	V_{DD} = 5V		280	700	ns
		V_{DD} = 10V		120	270	ns
		V_{DD} = 15V		85	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, A (B) A (B) Asynchronous Parallel Data Input, B (A) Parallel Data Output	V_{DD} = 5V		280	700	ns
		V_{DD} = 10V		120	270	ns
		V_{DD} = 15V		85	190	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from A/B or AE to High Impedance State at A Outputs or from A/B to High Impedance State at B Outputs	V_{DD} = 5V, R_L = 1.0 kΩ		95	220	ns
		V_{DD} = 10V, R_L = 1.0 kΩ		60	130	ns
		V_{DD} = 15V, R_L = 1.0 kΩ		45	100	ns
t_{PZH}, t_{PZL}	Propagation Delay Time from A/B or AE to Logical "1" or Logical "0" State at A Outputs or from A/B to Logical "1" or Logical "0" State at B Outputs	V_{DD} = 5V, R_L = 1.0 kΩ		180	480	ns
		V_{DD} = 10V, R_L = 1.0 kΩ		75	190	ns
		V_{DD} = 15V, R_L = 1.0 kΩ		55	140	ns

AC Electrical Characteristics*

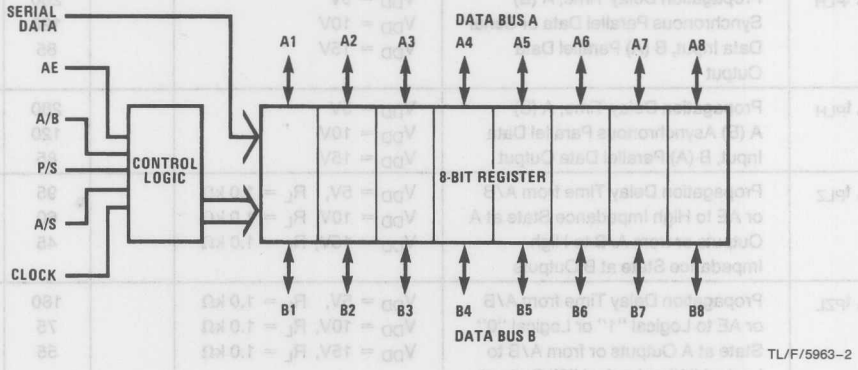
T_A = 25°C, C_L = 50 pF, R_L = 200k, input t_r = t_f = 20 ns, unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5V	2	4		MHz
		V_{DD} = 10V	5	10		MHz
		V_{DD} = 15V	7	14		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise & Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	15			μs
		V_{DD} = 15V	15			μs
t_{SU}	Parallel (A or B) and Serial Data Setup Time	V_{DD} = 5V		25	70	ns
		V_{DD} = 10V		10	30	ns
		V_{DD} = 15V		7	20	ns
t_{SU}	Control Inputs AE, A/B, P/S, A/S Setup Time	V_{DD} = 5V		110	280	ns
		V_{DD} = 10V		35	100	ns
		V_{DD} = 15V		60	60	ns
t_{WH}	Minimum High Level AE, A/B, P/S, A/S Pulse Width	V_{DD} = 5V		160	400	ns
		V_{DD} = 10V		70	160	ns
		V_{DD} = 15V		40	90	ns
C_{IN}	Average Input Capacitance	A and B Data I/O and A/B Control Input		7	15	pF
		Any Other Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		155		pF

*AC Parameters are guaranteed by DC correlated testing.

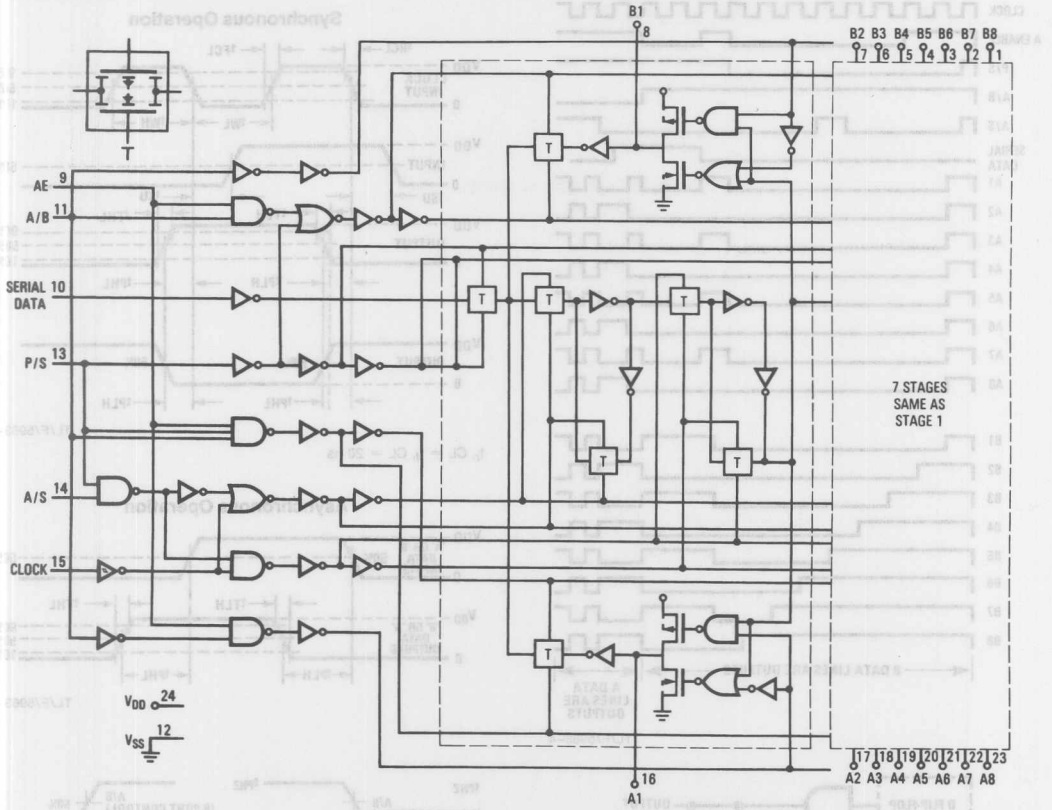
Note 4: C_{PD} determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Logic Diagram

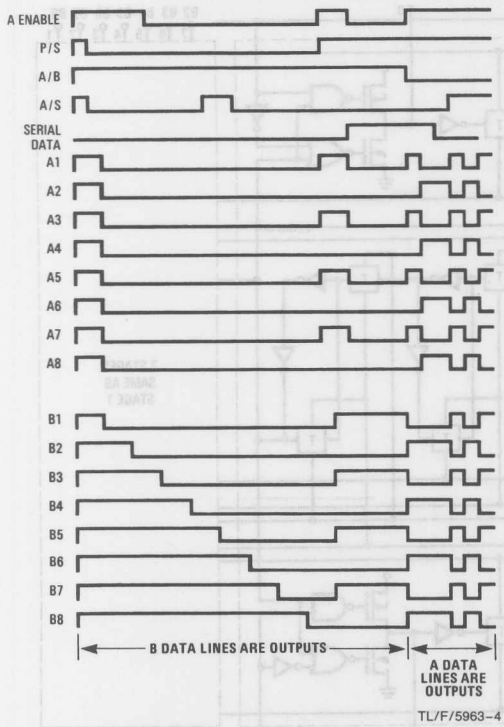


TL/F/5963–2

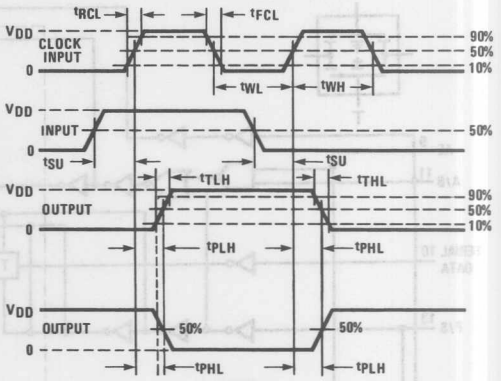
Schematic Diagram



TL/F/5963–3



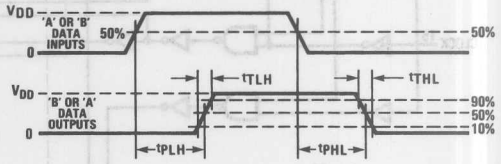
TL/F/5963–4



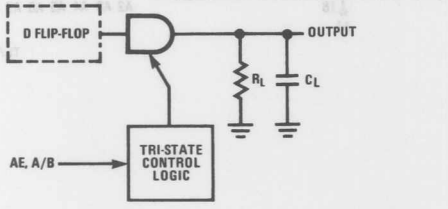
TL/F/5963–5

t_r, CL = t_f, CL = 20 ns

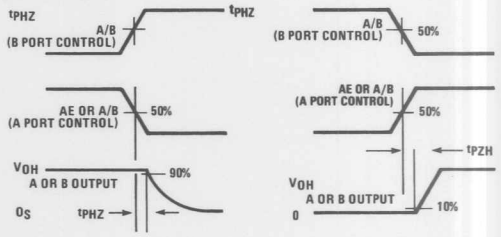
Asynchronous Operation



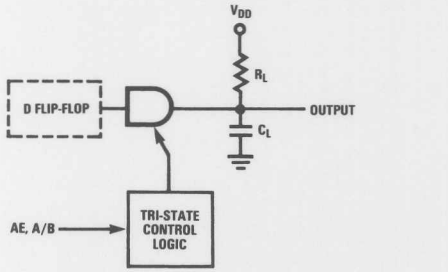
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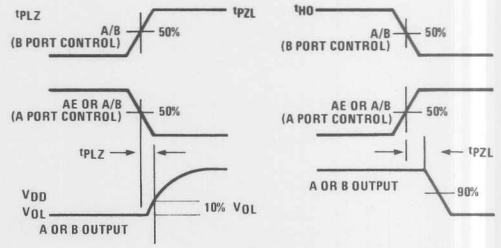
TL/F/5963–7



TL/F/5963–8

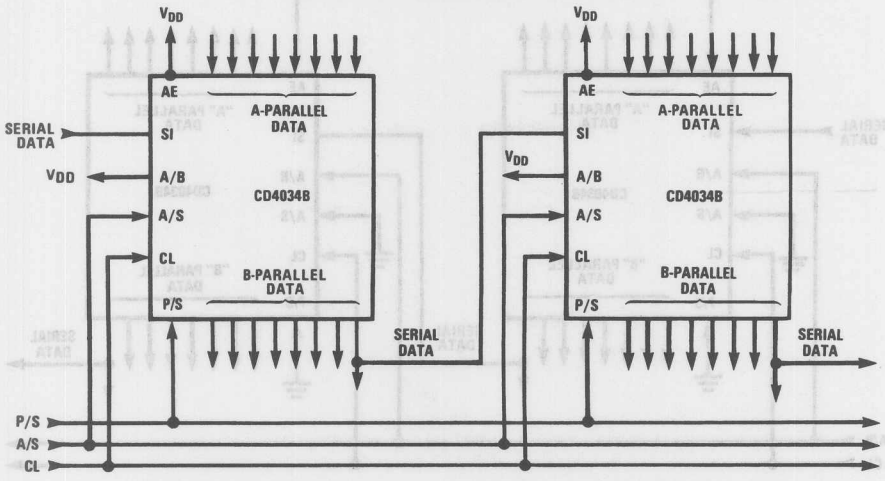


TL/F/5963–9



TL/F/5963–10

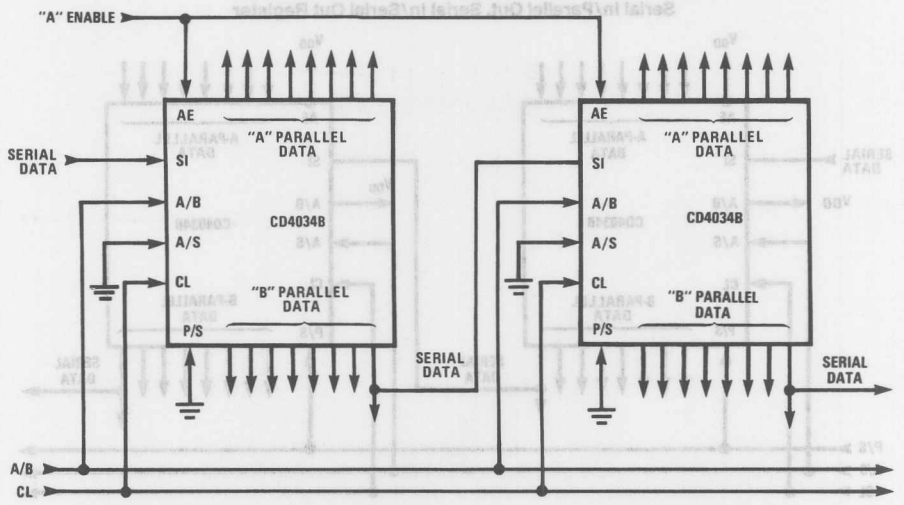
Serial In/Parallel Out, Serial In/Serial Out Register



TL/F/5963–11

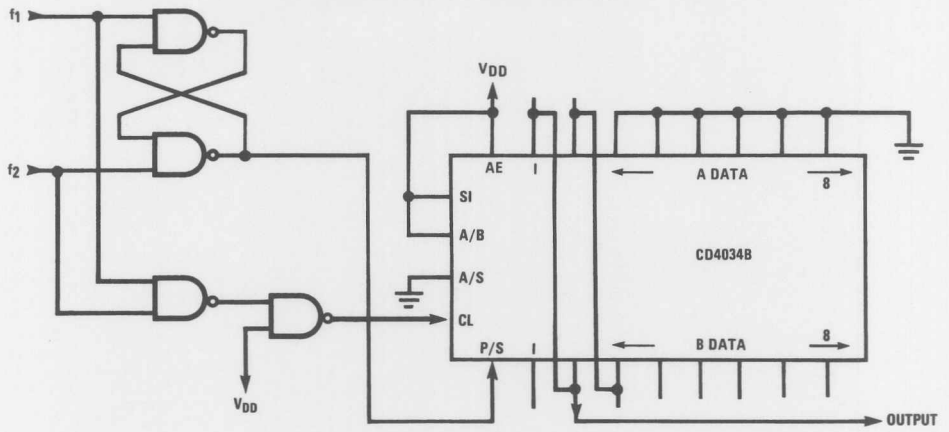
Applications (Continued)

16-Bit Serial In/Gated Parallel Out Register

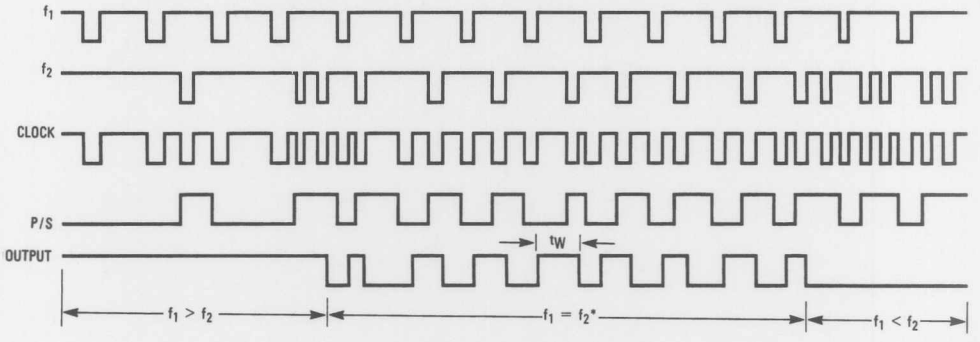


TL/F/5963–12

Frequency and Phase Comparator



TL/F/5963–13

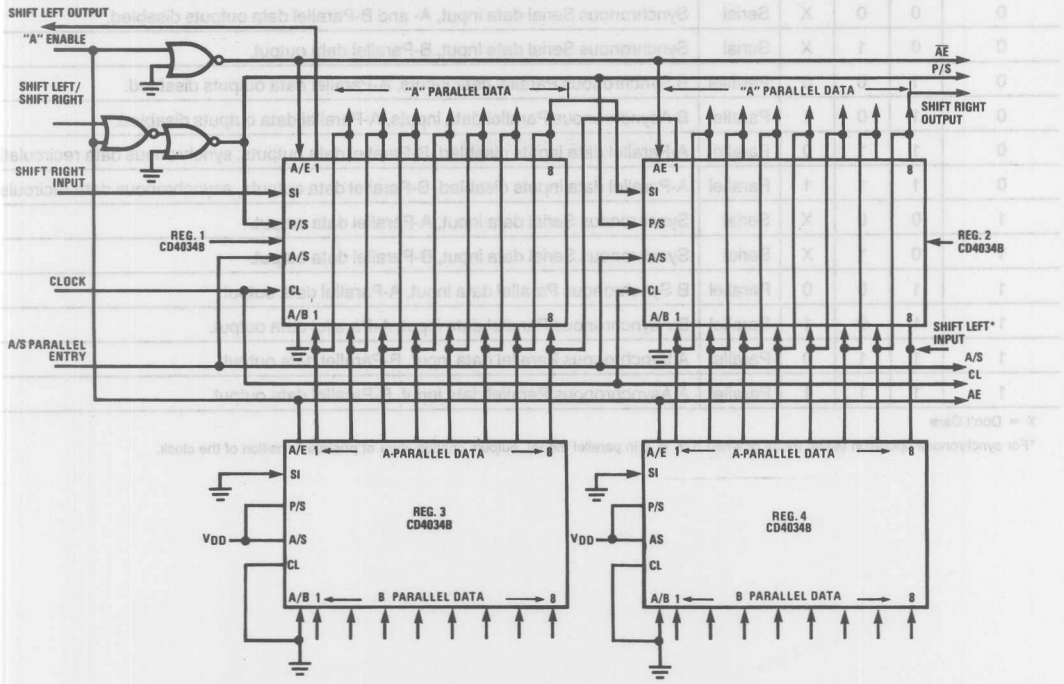


TL/F/5963–14

*When $f_1 = f_2$, t_W is proportional to the phase of f_1 with respect to f_2.

Applications (Continued)

Shift Right/Shift Left with Parallel Inputs



TL/F/5963–15

Shift left input must be disabled during parallel entry.

A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

Truth Table

"A" Enable	P/S	A/B	A/S	Mode	Operation*
0	0	0	X	Serial	Synchronous Serial data input, A- and B-Parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous Serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
1	1	0	0	Parallel	B Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.

National Semiconductor

CD4035BM/CD4035BC
4-Bit Parallel-In/Parallel-Out Shift Register

General Description

The CD4035B 4-bit parallel-in/parallel-out shift register is a monolithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. This shift register is a 4-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (parallel/serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the parallel/serial control is "high".

In the parallel or serial mode, information is transferred on positive clock transitions.

When the true/complement control is "high", the true contents of the register are available at the output terminals. When the true/complement control is "low", the outputs are the complements of the data in the register. The true/complement control functions asynchronously with respect to the clock signal.

$J\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

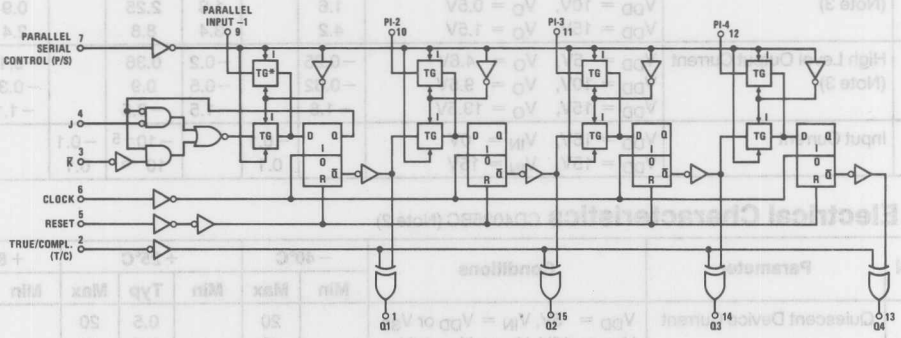
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 4-stage clocked operation
- Synchronous parallel entry on all 4 stages
- $J\overline{K}$ inputs on first stage
- Asynchronous true/complement control on all outputs
- Reset control
- Static flip-flop operation; master/slave configuration
- Buffered outputs
- Low power dissipation — 5 μW (typ.) (ceramic)
- High speed — to 5 MHz

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

Logic Diagram



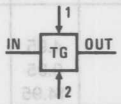
TL/F/5964–1

P/S = 0 = serial mode
T/C = 1 = true outputs
*TG = transmission gate

Input to output is:

a) A bidirectional low impedance when control input 1 is low and control input 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.



TL/F/5964–2

Input Voltage (V_{IN})	$-0.5V$ to $V_{DD}+0.5V$	DC Supply Voltage (V_{DD})	3V to 15V
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$	Input Voltage (V_{IN})	0V to V_{DD}V
Power Dissipation (P_D)		Operating Temperature Range (T_A)	
Dual-In-Line	700 mW	CD4035BM	$-55°C$ to $+125°C$
Small Outline	500 mW	CD4035BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4035BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		5		0.3	5		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		10		0.5	10		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	−0.25		−0.2	0.36		−0.14		mA
		$V_{DD}=10V$, $V_O=9.5V$	−0.62		−0.5	0.9		−0.35		mA
		$V_{DD}=15V$, $V_O=13.5V$	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4035BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		20		0.5	20		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		40		1.0	40		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4035BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		25°C		85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.2		−0.16	0.36		−0.12		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.5		−0.4	0.9		−0.3		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_r and $t_f = 20$ ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		250	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		75	150	ns
t_{THL}	Transition Time High Low to High	$V_{DD} = 5V$		90	175	ns
		$V_{DD} = 10V$		50	75	ns
		$V_{DD} = 15V$		40	60	ns
t_{TLH}	Transition Time Low to High	$V_{DD} = 5V$		135	270	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		60	120	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$	335	135		ns
		$V_{DD} = 10V$	165	50		ns
		$V_{DD} = 15V$	100	40		ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			10	μs
		$V_{DD} = 15V$			5	μs
t_S	Minimum Set-up Time J/$\overline{K}$ Lines					
		$V_{DD} = 5V$		250	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	160	ns
t_S	Parallel-In Lines	$V_{DD} = 5V$		250	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	160	ns
t_S	P/S Control	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		35	60	ns
f_{MAX}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	2.5		MHz
		$V_{DD} = 10V$	3	6		MHz
		$V_{DD} = 15V$	5	9		MHz

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns, unless otherwise specified. (Continued)

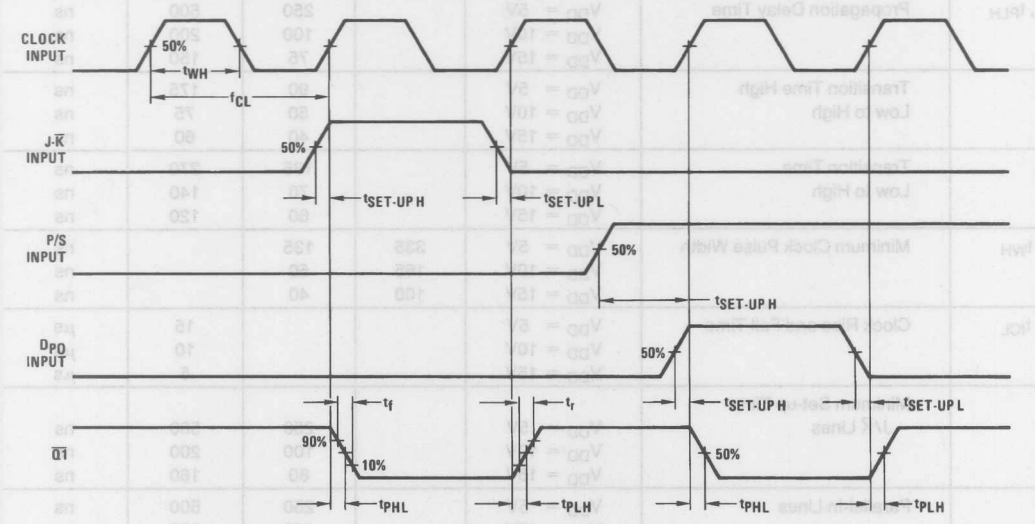
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCKED OPERATION (Continued)						
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	500	ns
		V_{DD} = 10V		150	200	ns
		V_{DD} = 15V		85	150	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		75	250	ns
		V_{DD} = 10V		30	110	ns
		V_{DD} = 15V		25	80	ns

*AC Parameters are guaranteed by DC correlated testing.

Truth Table

C_L	$t_n - 1$ (Inputs)				t_n (Outputs)
	J	$\overline{K}$	R	Q_{n-1}	Q_n
⌐‾	0	X	0	0	0
⌐‾	1	X	0	0	1
⌐‾	X	0	0	1	0
⌐‾	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⌐‾	X	1	0	1	1
‾⌙	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Switching Time Waveforms



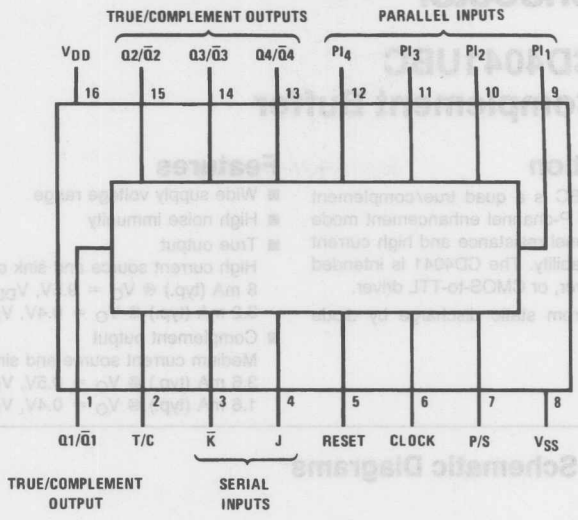
TL/F/5964–3

T/C Input Low

Reset Input Low

Connection Diagram

Dual-In-Line Package



TL/F/5964–4

Top View

Order Number CD4035B*

*Please look into Section 8, Appendix D for availability of various package types.

5

National Semiconductor

CD4041UB/CD4041UBC
Quad True/Complement Buffer

General Description

The CD4041UB/CD4041UBC is a quad true/complement buffer consisting of N- and P-channel enhancement mode transistors having low-channel resistance and high current (sourcing and sinking) capability. The CD4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver.

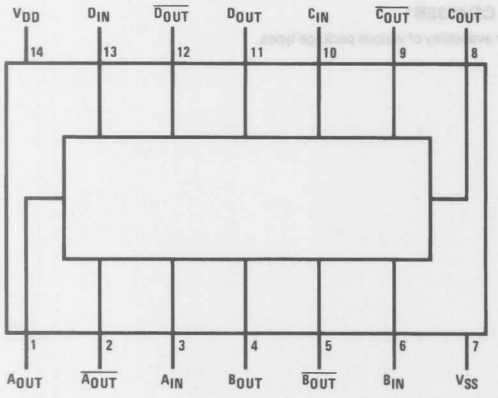
All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 40% V_{DD} (typ.)
- True output
  High current source and sink capability
  8 mA (typ.) @ V_O = 9.5V, V_{DD} = 10V
  3.2 mA (typ.) @ V_O = 0.4V, V_{DD} = 5V (two TTL loads)
- Complement output
  Medium current source and sink capability
  3.6 mA (typ.) @ V_O = 9.5V, V_{DD} = 10V
  1.6 mA (typ.) @ V_O = 0.4V, V_{DD} = 5V

Connection and Schematic Diagrams

Dual-In-Line Package



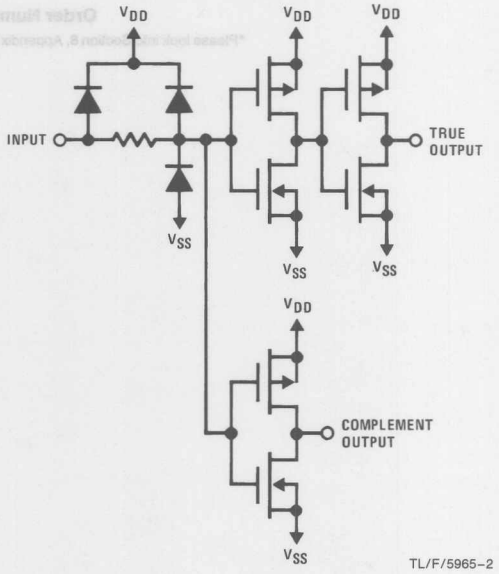
TL/F/5965–1

Top View

Order Number CD4041UB*

*Please look into Section 8, Appendix D for availability of various package types.

1 of 4 Identical Units



TL/F/5965–2

Input Voltage (V_{IN}) $-0.5V$ to $V_{DD} + 0.5V$

Storage Temperature Range (T_S) $-65°C$ to $+150°C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Lead Temp. (T_L) (Soldering, 10 sec.) 260°C

Operating Temperature Range (T_A)

CD4041UB $-55°C$ to $+125°C$

CD4041UBC $-40°C$ to $+85°C$

DC Electrical Characteristics CD4041UBM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		1		0.01	1		30	μA
		$V_{DD} = 10V$		2		0.01	2		60	μA
		$V_{DD} = 15V$		4		0.01	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.0		2	1.0		1.0	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		2.0		4	2.0		2.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		3.0		6	3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	4.0		4.0	3		4.0		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	8.0		8.0	6		8.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current	$V_{IL} = 0V$								
	True Output	$V_{DD} = 5V$, $V_O = 0.4V$	2.1		1.6	3.2		1.2		mA
	(Note 3)	$V_{DD} = 10V$, $V_O = 0.5V$	6.25		5.0	10		3.5		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	14		12	24		8		mA
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$								
	Complement Output	$V_{DD} = 5V$, $V_O = 0.4V$	1.0		0.8	1.6		0.55		mA
	(Note 3)	$V_{DD} = 10V$, $V_O = 0.5V$	2.5		2	4.0		1.4		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	5.5		4.5	9.0		3.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$								
	True Output	$V_{DD} = 5V$, $V_O = 4.6V$	−1.75		−1.4	−2.8		−1.0		mA
	(Note 3)	$V_{DD} = 10V$, $V_O = 9.5V$	−5.0		−4	−8.0		−2.8		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−11		−9	−18		−6		mA
I_{OH}	High Level Output Current	$V_{IL} = 0V$								
	Complement Output	$V_{DD} = 5V$, $V_O = 4.6V$	−0.75		−0.6	−1.2		−0.4		mA
	(Note 3)	$V_{DD} = 10V$, $V_O = 9.5V$	−2.25		−1.8	−3.6		−1.25		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.8		−4	−8		−2.7		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of 'Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4041UBC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.01	4		30	μA
		V_{DD} = 10V		8		0.01	8		60	μA
		V_{DD} = 15V		16		0.01	16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.0		2	1.0		1.0	V
		V_{DD} = 10V, V_O = 1V or 9V		2.0		4	2.0		2.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		3.0		6	3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	4.0		4.0	3		4.0		V
		V_{DD} = 10V, V_O = 1V or 9V	8.0		8.0	6		8.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V								
	True Output	V_{DD} = 5V, V_O = 0.4V	1.7		1.5	3.2		1.2		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	4.9		4.3	10		3.5		mA
		V_{DD} = 15V, V_O = 1.5V	11		10	24		8		mA
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$								
	Complement Output	V_{DD} = 5V, V_O = 0.4V	0.75		0.68	1.6		0.55		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	2.0		1.8	4.0		1.4		mA
		V_{DD} = 15V, V_O = 1.5V	4.4		3.8	9.0		3.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$								
	True Output	V_{DD} = 5V, V_O = 4.6V	−1.5		−1.3	−2.8		−1.0		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−4.0		−3.5	−8.0		−2.8		mA
		V_{DD} = 15V, V_O = 13.5V	−8.7		−7.5	−18		−6		mA
I_{OH}	High Level Output Current	V_{IL} = 0V								
	Complement Output	V_{DD} = 5V, V_O = 4.6V	−0.57		−0.50	−1.2		−0.4		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.8		−1.6	−3.6		−1.25		mA
		V_{DD} = 15V, V_O = 13.5V	−3.9		−3.4	−8.0		−2.7		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input $t_r = t_f$ = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		60	120	ns
	True Output	V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		25	50	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		75	150	ns
	Complement Output	V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	65	ns
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5V		55	110	ns
	True Output	V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns

AC Electrical Characteristics* (Continued)

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{THL}, t_{TLH}	Output Transition Time Complement Output	V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	75	ns
C_{IN}	Input Capacitance	Any Input		10	15	pF

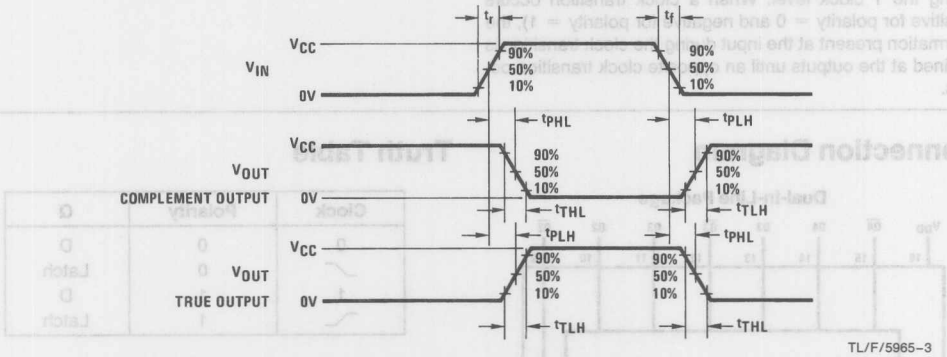
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms



TL/F/5965–3

National Semiconductor

CD4042BM/CD4042BC Quad Clocked D Latch

General Description

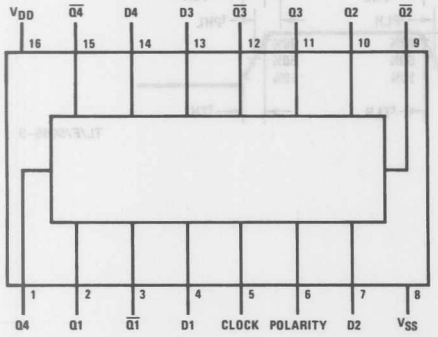
The CD4042BM/CD4042BC quad clocked "D" latch is a monolithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. The outputs Q and $\overline{Q}$ either latch or follow the data input depending on the clock level which is programmed by the polarity input. For polarity = 0; the information present at the data input is transferred to Q and $\overline{Q}$ during 0 clock level; and for polarity = 1, the transfer occurs during the 1 clock level. When a clock transition occurs (positive for polarity = 0 and negative for polarity = 1), the information present at the input during the clock transition is retained at the outputs until an opposite clock transition occurs.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Clock polarity control
- Fully buffered data inputs
- Q and $\overline{Q}$ outputs

Connection Diagram

Dual-In-Line Package



TL/F/5966–1

Top View

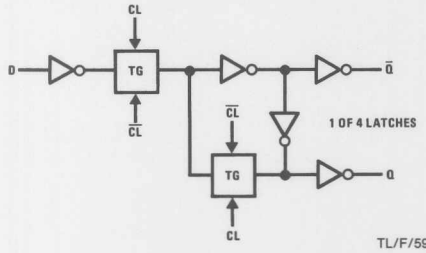
Truth Table

Clock	Polarity	Q
0	0	D
⌐	0	Latch
1	1	D
⌙	1	Latch

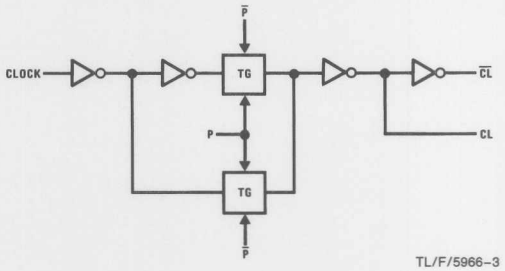
Order Number CD4042B*

*Please look into Section 8, Appendix D for availability of various package types.

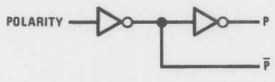
Logic Diagrams



TL/F/5966–2



TL/F/5966–3



TL/F/5966–4

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4042BM	−55°C to +125°C
CD4042BC	−40°C to +85°C

DC Electrical Characteristics CD4042BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.02	1		30	μA
		V_{DD} = 10V		2		0.02	2		60	μA
		V_{DD} = 15V		4		0.02	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Curent	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

Symbol	Parameter	Conditions	Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		4		0.02	4		30	μA
		$V_{DD} = 10V$		8		0.02	8		60	μA
		$V_{DD} = 15V$		16		0.02	16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	(Note 4)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	(Note 4)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Curent	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to Q	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		60	120	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to $\overline{Q}$	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		50	100	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to $\overline{Q}$	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		90	180	ns
t_H	Minimum Hold Time	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Setup Time	V_{DD} = 5V		0	50	ns
		V_{DD} = 10V		0	30	ns
		V_{DD} = 15V		0	25	ns
t_W	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		30	60	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

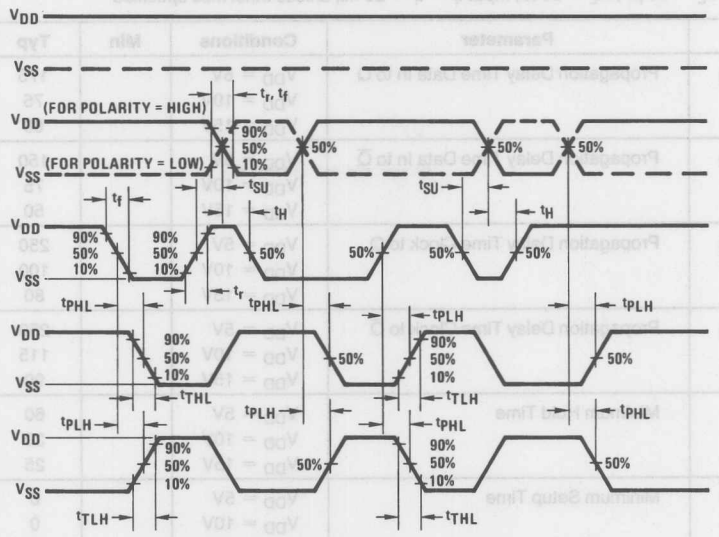
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms



TL/F/5966–5

National Semiconductor

CD4043BM/CD4043BC Quad TRI-STATE® NOR R/S Latches
CD4044BM/CD4044BC Quad TRI-STATE NAND R/S Latches

General Description

CD4043BM/CD4043BC are quad cross-couple TRI-STATE CMOS NOR latches, and CD4044BM/CD4044BC are quad cross-couple TRI-STATE CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. There is a common TRI-STATE ENABLE input for all four latches. A logic "1" on the ENABLE input connects the latch states to the Q outputs. A logic "0" on the ENABLE input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q output. The TRI-STATE feature allows common bussing of the outputs.

Features

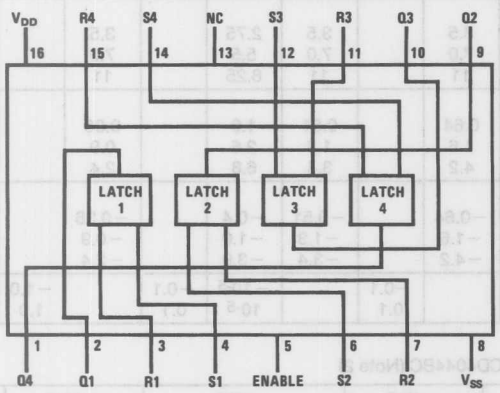
- Wide supply voltage range — 3V to 15V
- Low power — 100 nW (typ.)
- High noise immunity — 0.45 V_{DD} (typ.)
- Separate SET and RESET inputs for each latch
- NOR and NAND configuration
- TRI-STATE output with common output enable

Applications

- Multiple bus storage
- Strobed register
- Four bits of independent storage with output enable
- General digital logic

Connection Diagrams

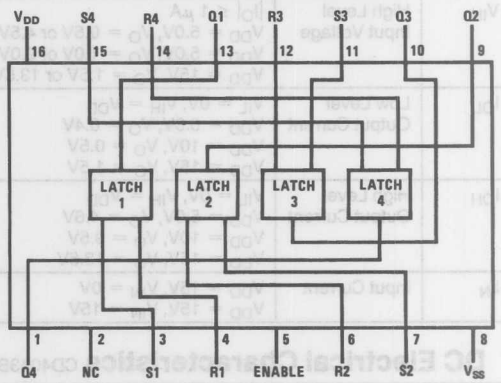
CD4043BM/CD4043BC
Dual-In-Line and Flat Packages



TL/F/5967–3

Top View

CD4044BM/CD4044BC
Dual-In-Line and Flat Packages



TL/F/5967–4

Top View

Order Number CD4043B* or CD4044B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

CD4043BM/CD4043BC

S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

CD4044BM/CD4044BC

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

OC — TRI-STATE
NC — No change
X — Don't care
Δ — Dominated by S = 1 input
ΔΔ — Dominated by R = 0 input

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Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3.0V to 15V
Input Voltage (V_{IN})	0 to V_{DD} V
Operating Temperature Range (T_A)	
CD4043BM, CD4044BM	−55°C to +125°C
CD4043BC, CD4044BC	−40°C to +85°C

DC Electrical Characteristics CD4043BM/CD4044BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5.0		0.01	5.0		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.01	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5.0V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5.0V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 5.0V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11		11	8.25		11		V
I_{OL}	Low Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V, V_O = 0.4V	0.64		0.51	1.0		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.6		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	6.8		2.4		mA
I_{OH}	High Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V, V_O = 4.6V	−0.64		−0.51	−0.4		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−1.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−3.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4043BC/CD4044BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.01	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.01	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4043BC/CD4044BC (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 5.0V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11		11			11		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5.0V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.2		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	6.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IL} = 0V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5.0V$, $V_O = 4.6V$	−0.52		−0.44	−0.32		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−0.8		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−2.4		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$	−0.3			−0.3			−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$	0.3			0.3			1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, input $t_r = t_f = 20$ ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay S or R to Q	$V_{DD} = 5.0V$		175	350	ns
		$V_{DD} = 10V$		75	175	ns
		$V_{DD} = 15V$		60	120	ns
t_{PZH}, t_{PHZ}	Propagation Delay Enable to Q (High)	$V_{DD} = 5.0V$		115	230	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		40	80	ns
t_{PZL}, t_{PLZ}	Propagation Delay Enable to Q (Low)	$V_{DD} = 5.0V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5.0V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WO}	Minimum SET or RESET Pulse Width	$V_{DD} = 5.0V$		80	160	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		20	40	ns
C_{IN}	Input Capacitance			5.0	7.5	pF

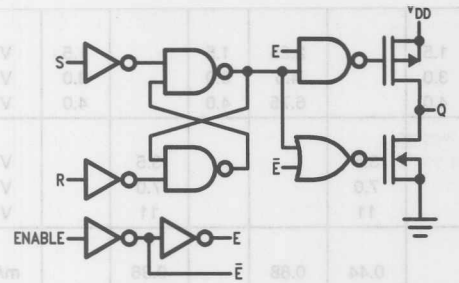
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

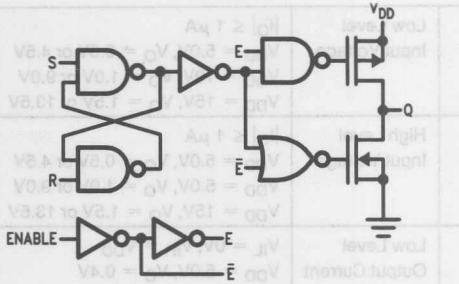
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

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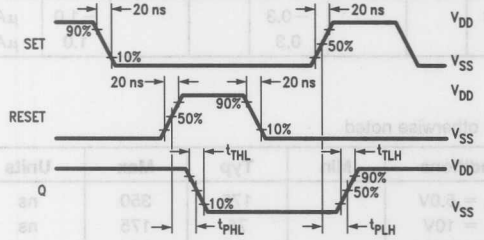
TL/F/5967–1



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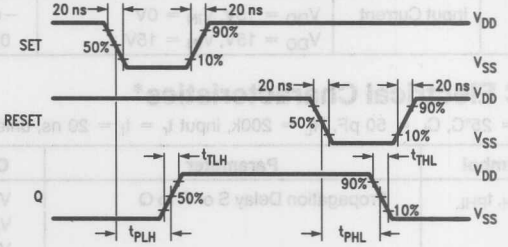
Timing Waveforms

CD4043B



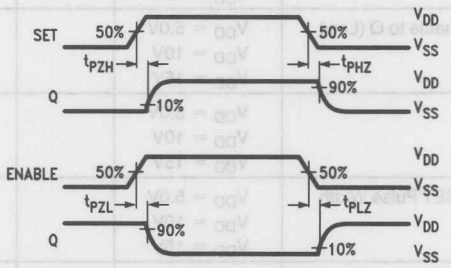
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CD4044B



TL/F/5967–6

Enable Timing



TL/F/5967–7

National Semiconductor

CD4046BM/CD4046BC Micropower Phase-Locked Loop

General Description

The CD4046B micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

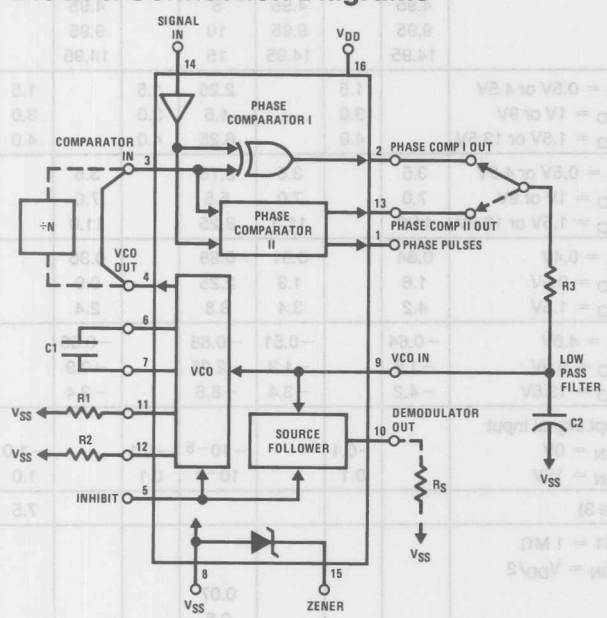
Features

■ Wide supply voltage range	3.0V to 18V
■ Low dynamic power consumption	70 μW (typ.) at f_o = 10 kHz, V_{DD} = 5V
■ VCO frequency	1.3 MHz (typ.) at V_{DD} = 10V
■ Low frequency drift with temperature	0.06%/°C at V_{DD} = 10V
■ High VCO linearity	1% (typ.)

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

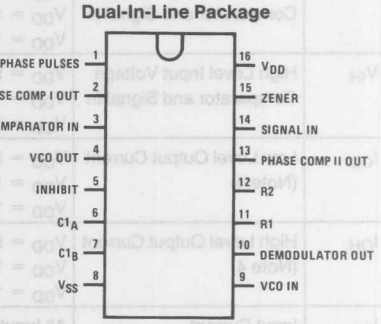
Block & Connection Diagrams



TL/F/5968–1

FIGURE 1

Dual-In-Line Package



TL/F/5968–2

Top View

Order Number CD4046B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} $+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4046BM	$-55°C$ to $+125°C$
CD4046BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4046BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	Pin 5 = V_{DD}, Pin 14 = V_{DD}, Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		5		0.005	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.015	20		600	μA
		Pin 5 = V_{DD}, Pin 14 = Open, Pin 3, 2 = V_{SS}								
		V_{DD} = 5V		45		5	35		185	μA
		V_{DD} = 10V		450		20	350		650	μA
		V_{DD} = 15V		1200		50	900		1500	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 14V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
C_{IN}	Input Capacitance	Any Input (Note 3)							7.5	pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO_{IN} = $V_{DD}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

I_{DD}	Quiescent Device Current	Pin 5 = V_{DD}, Pin 14 = V_{DD}, Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
		Pin 5 = V_{DD}, Pin 14 = Open, Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		70		5	55		205	μA
		V_{DD} = 10V		530		20	410		710	μA
		V_{DD} = 15V		1500		50	1200		1800	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
C_{IN}	Input Capacitance	Any Input (Note 3)					7.5			pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ, R2 = ∞, VCO_{IN} = $V_{DD}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

VCO SECTION

I_{DD}	Operating Current	f_o = 10 kHz, R1 = 1 MΩ, R2 = ∞, VCO_{IN} = V_{DD}/2				
		V_{DD} = 5V		20		μA
		V_{DD} = 10V		90		μA
		V_{DD} = 15V		200		μA
f_{MAX}	Maximum Operating Frequency	C1 = 50 pF, R1 = 10 kΩ, R2 = ∞, VCO_{IN} = V_{DD}				
		V_{DD} = 5V	0.4	0.8		MHz
		V_{DD} = 10V	0.6	1.2		MHz
		V_{DD} = 15V	1.0	1.6		MHz
	Linearity	VCO_{IN} = 2.5V ±0.3V, R1 ≥ 10 kΩ, V_{DD} = 5V		1		%
		VCO_{IN} = 5V ±2.5V, R1 ≥ 400 kΩ, V_{DD} = 10V		1		%
		VCO_{IN} = 7.5V ±5V, R1 ≥ 1 MΩ, V_{DD} = 15V		1		%
	Temperature-Frequency Stability No Frequency Offset, f_{MIN} = 0	%/°C ∝ 1/f. V_{DD} R2 = ∞				
		V_{DD} = 5V		0.12–0.24		%/°C
		V_{DD} = 10V		0.04–0.08		%/°C
		V_{DD} = 15V		0.015–0.03		%/°C
	Frequency Offset, $f_{MIN} \neq 0$	V_{DD} = 5V		0.06–0.12		%/°C
		V_{DD} = 10V		0.05–0.1		%/°C
		V_{DD} = 15V		0.03–0.06		%/°C
VCO_{IN}	Input Resistance	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
VCO	Output Duty Cycle	V_{DD} = 5V		50		%
		V_{DD} = 10V		50		%
		V_{DD} = 15V		50		%
t_{THL}	VCO Output Transition Time	V_{DD} = 5V		90	200	ns
t_{THL}		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		45	80	ns

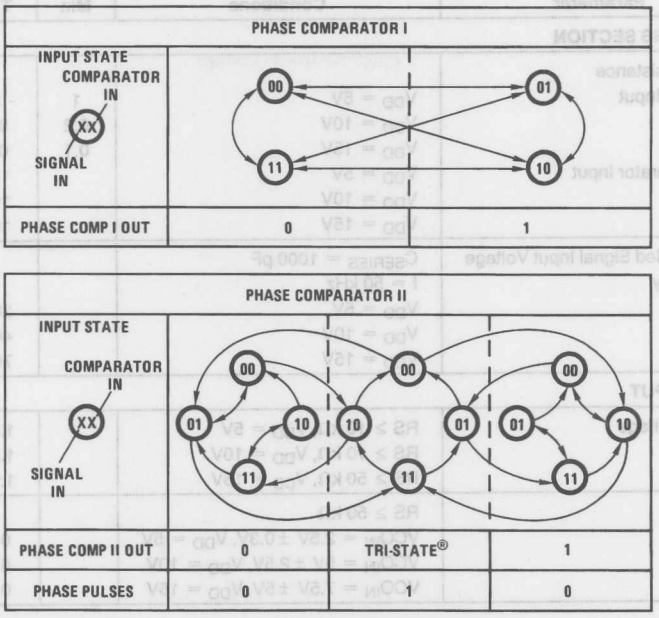
*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4046BM/CD4046BC $T_A = 25°C$, $C_L = 50$ pF (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PHASE COMPARATORS SECTION						
R_{IN}	Input Resistance					
	Signal Input	$V_{DD} = 5V$	1	3		MΩ
		$V_{DD} = 10V$	0.2	0.7		MΩ
		$V_{DD} = 15V$	0.1	0.3		MΩ
	Comparator Input	$V_{DD} = 5V$		10^6		MΩ
		$V_{DD} = 10V$		10^6		MΩ
		$V_{DD} = 15V$		10^6		MΩ
	AC-Coupled Signal Input Voltage Sensitivity	$C_{SERIES} = 1000$ pF $f = 50$ kHz				
		$V_{DD} = 5V$		200	400	mV
		$V_{DD} = 10V$		400	800	mV
		$V_{DD} = 15V$		700	1400	mV
DEMODULATOR OUTPUT						
$VCO_{IN}-V_{DEM}$	Offset Voltage	RS ≥ 10 kΩ, $V_{DD} = 5V$		1.50	2.2	V
		RS ≥ 10 kΩ, $V_{DD} = 10V$		1.50	2.2	V
		RS ≥ 50 kΩ, $V_{DD} = 15V$		1.50	2.2	V
	Linearity	RS ≥ 50 kΩ				
		$VCO_{IN} = 2.5V \pm 0.3V$, $V_{DD} = 5V$		0.1		%
		$VCO_{IN} = 5V \pm 2.5V$, $V_{DD} = 10V$		0.6		%
		$VCO_{IN} = 7.5V \pm 5V$, $V_{DD} = 15V$		0.8		%
ZENER DIODE						
V_Z	Zener Diode Voltage					
	CD4046BM	$I_Z = 50\ \mu A$	6.7	7.0	7.3	V
	CD4046BC		6.3	7.0	7.7	V
R_Z	Zener Dynamic Resistance	$I_Z = 1$ mA		100		Ω

*AC Parameters are guaranteed by DC correlated testing.

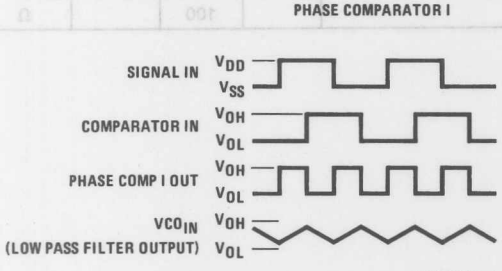
Phase Comparator State Diagrams



TL/F/5968–3

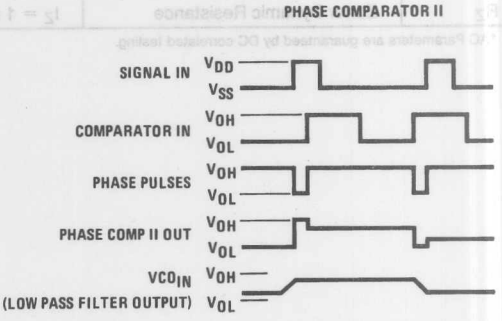
FIGURE 2

Typical Waveforms



TL/F/5968–4

FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition



TL/F/5968–5

FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

Typical Center Frequency vs C1 for R1 = 10 kΩ, 100 kΩ and 1 MΩ

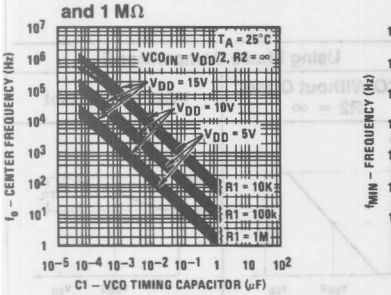


FIGURE 5a

Typical Frequency Offset vs C1 for R2 = 10 kΩ, 100 kΩ and 1 MΩ

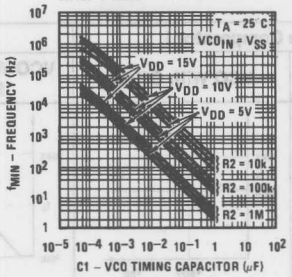


FIGURE 5b

Typical f_{MAX}/f_{MIN} vs R2/R1

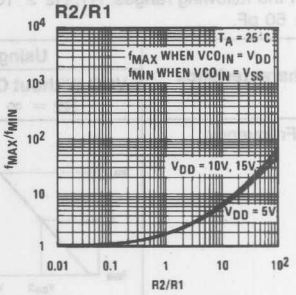


FIGURE 5c

Typical VCO Power Dissipation at Center Frequency vs R1

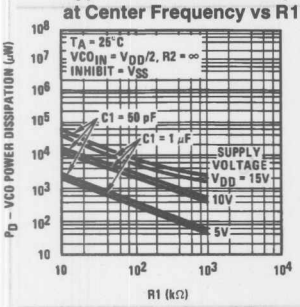


FIGURE 6a

Typical VCO Power Dissipation at f_{MIN} vs R2

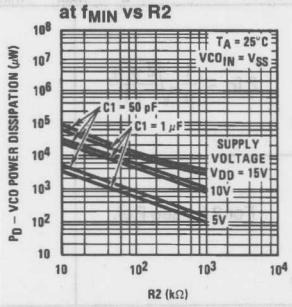


FIGURE 6b

Typical Source Follower Power Dissipation vs R_S

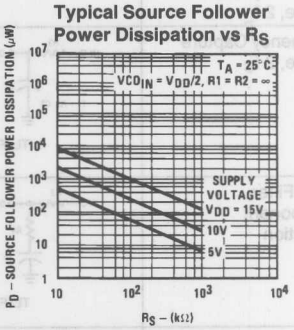


FIGURE 6c

Typical VCO Linearity vs R1 and C1

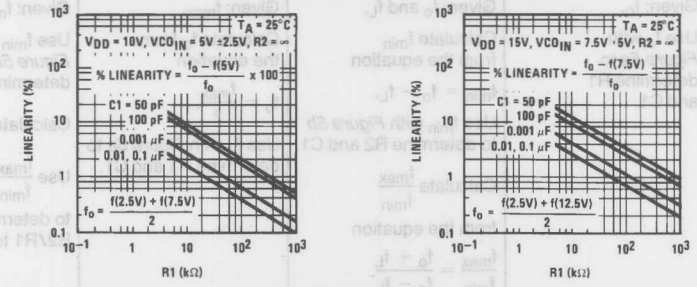


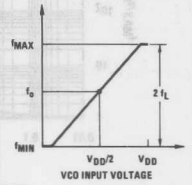
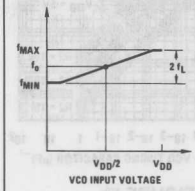
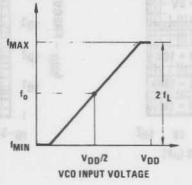
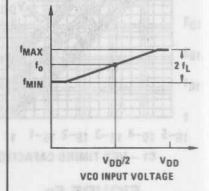
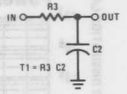
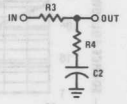
FIGURE 7

TL/F/5968–6

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

5

C1 ≥ 50 pF.

Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset R2 = ∞	VCO With Offset	VCO Without Offset R2 = ∞	VCO With Offset
VCO Frequency	 TL/F/5968–7	 TL/F/5968–8	 TL/F/5968–9	 TL/F/5968–10
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, 2 f_L	2 f_L = full VCO frequency range 2 f_L = $f_{max} - f_{min}$			
Frequency Capture Range, 2 f_C	 TL/F/5968–11 $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$		$f_C = f_L$	
Loop Filter Component Selection	 TL/F/5968–12 For 2 f_C, see Ref.			
Phase Angle Between Single and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range (2 f_L)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	Given: f_o. Use f_o with *Figure 5a* to determine R1 and C1.	Given: f_o and f_L. Calculate f_{min} from the equation $f_{min} = f_o - f_L$. Use f_{min} with *Figure 5b* to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$. Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1.	Given: f_{max}. Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$. Use f_o with *Figure 5a* to determine R1 and C1.	Given: f_{min} and f_{max}. Use f_{min} with *Figure 5b* to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$. Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1.

References

G.S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

Floyd Gardner, "Phaselock Techniques", John Wiley & Sons, 1966.

National Semiconductor

CD4047BM/CD4047BC Low Power Monostable/Astable Multivibrator

General Description

CD4047B is capable of operating in either the monostable or astable mode. It requires an external capacitor (between pins 1 and 3) and an external resistor (between pins 2 and 3) to determine the output pulse width in the monostable mode, and the output frequency in the astable mode.

Astable operation is enabled by a high level on the astable input or low level on the $\overline{\text{astable}}$ input. The output frequency (at 50% duty cycle) at Q and $\overline{Q}$ outputs is determined by the timing components. A frequency twice that of Q is available at the Oscillator Output; a 50% duty cycle is not guaranteed.

Monostable operation is obtained when the device is triggered by low-to-high transition at + trigger input or high-to-low transition at − trigger input. The device can be retriggered by applying a simultaneous low-to-high transition to both the + trigger and retrigger inputs.

A high level on Reset input resets the outputs Q to low, $\overline{Q}$ to high.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS

SPECIAL FEATURES

- Low power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

MONOSTABLE MULTIVIBRATOR FEATURES

- Positive- or negative-edge trigger
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse width expansion
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

ASTABLE MULTIVIBRATOR FEATURES

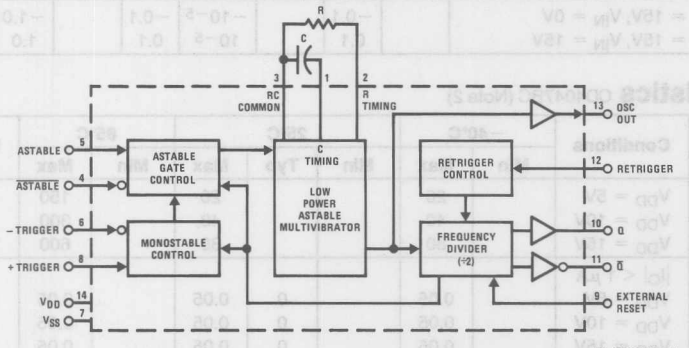
- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available
- Good astable frequency stability

  typical frequency deviation = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits trimmed to frequency V_{DD} = 10V ±10%)

Applications

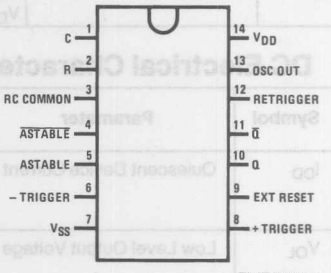
- Frequency discriminators
- Timing circuits
- Time-delay applications
- Envelope detection
- Frequency multiplication
- Frequency division

Block and Connection Diagrams



TL/F/5969–1

Dual-In-Line Package



TL/F/5969–2

Top View

Order Number CD4047B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5V$ to $+18V_{DC}$
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD}+0.5V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to $15V_{DC}$
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4047BM	$-55°C$ to $+125°C$
CD4047BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4047BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		5			5		150	μA
		$V_{DD}=10V$		10			10		300	μA
		$V_{DD}=15V$		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|<1\ \mu A$								
		$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|<1\ \mu A$								
		$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V, V_O=1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V, V_O=1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD}=15V, V_O=1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V, V_O=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V, V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V, V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V, V_O=9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD}=15V, V_O=13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V, V_{IN}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V, V_{IN}=15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4047BC (Note 2)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		20			20		150	μA
		$V_{DD}=10V$		40			40		300	μA
		$V_{DD}=15V$		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|<1\ \mu A$								
		$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|<1\ \mu A$								
		$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4047BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device oepration.

Note 2: V_{SS} = 0V unless otherwise specified.

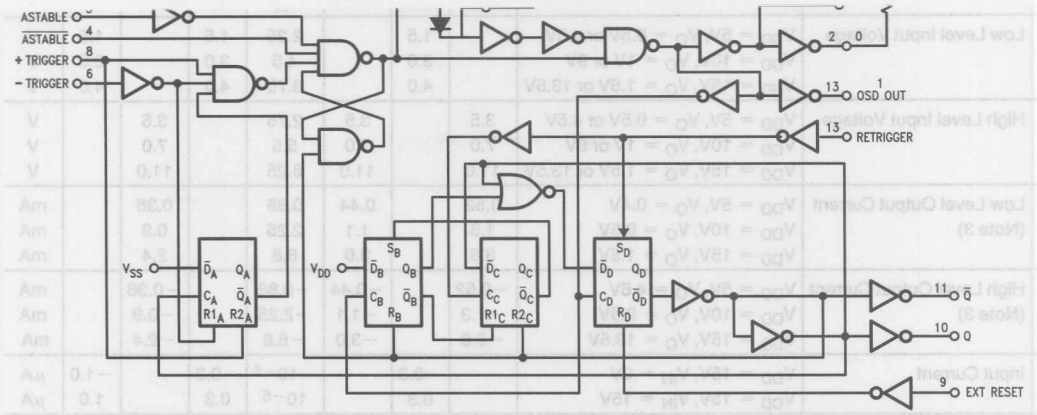
Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* CD4047B

T_A = 25°C, C_L = 50 pF, R_L = 200k, input t_r = t_f = 20 ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Astable, $\overline{\text{Astable}}$ to Osc Out	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_{PHL}, t_{PLH}	Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	V_{DD} = 5V		550	900	ns
		V_{DD} = 10V		250	500	ns
		V_{DD} = 15V		200	400	ns
t_{PHL}, t_{PLH}	+ Trigger, − Trigger to $\overline{Q}$	V_{DD} = 5V		700	1200	ns
		V_{DD} = 10V		300	600	ns
		V_{DD} = 15V		240	480	ns
t_{PHL}, t_{PLH}	+ Trigger, Retrigger to $\overline{Q}$	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		175	300	ns
		V_{DD} = 15V		150	250	ns
t_{PHL}, t_{PLH}	Reset to Q, $\overline{Q}$	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		125	250	ns
		V_{DD} = 15V		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q, $\overline{Q}$, Osc Out	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Duration	Any Input				
		V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_{RCL}, t_{FCL}	+ Trigger, Retrigger, Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			5	μs
		V_{DD} = 15V			5	μs
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.



TL/F/5969–3

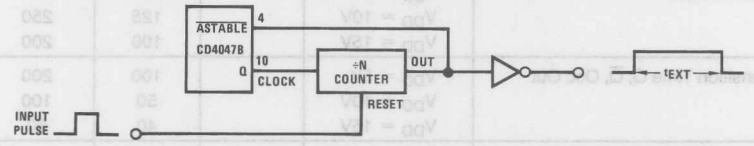
*Special input protection circuit to permit larger input-voltage swings.

Truth Table

Function	Terminal Connections			Output Pulse From	Typical Output Period or Pulse Width
	To V_{DD}	To V_{SS}	Input Pulse To		
Astable Multivibrator					
Free-Running	4, 5, 6, 14	7, 8, 9, 12		10, 11, 13	t_A (10, 11) = 4.40 RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	t_A (13) = 2.20 RC
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	t_M (10, 11) = 2.48 RC
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown*	14	5, 6, 7, 8, 9, 12	(See Figure)	(See Figure)	(See Figure)

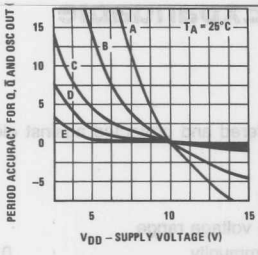
Note: External resistor between terminals 2 and 3. External capacitor between terminals 1 and 3.

***Typical Implementation of External Countdown Option**



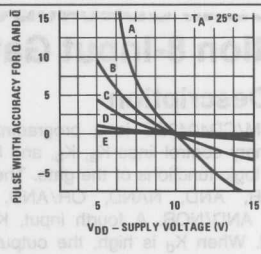
TL/F/5969–4

$$t_{EXT} = (N - 1)\, t_A + (t_M + t_A/2)$$



TL/F/5969–5

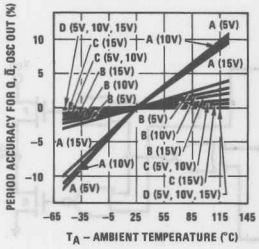
	$f_Q, \overline{Q}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF
E	100 Hz	2.2M	1000 pF



TL/F/5969–6

	t_M	R	C
A	2 μs	22k	10 pF
B	7 μs	22k	100 pF
C	60 μs	220k	100 pF
D	550 μs	220k	1000 pF
E	5.5 ms	2.2M	1000 pF

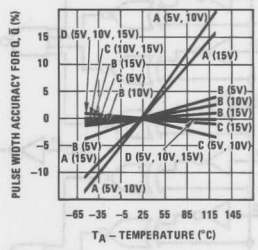
Typical Q, $\overline{Q}$ and Osc Out Period Accuracy vs Temperature Astable Mode Operation



TL/F/5969–7

	$f_Q, \overline{Q}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF

Typical Q and $\overline{Q}$ Pulse Width Accuracy vs Temperature Monostable Mode Operation

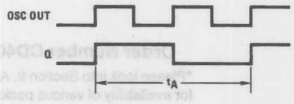


TL/F/5969–8

	t_M	R	C
A	2 μs	22k	10 pF
B	7 μs	22k	100 pF
C	60 μs	220k	100 pF
D	550 μs	220k	1000 pF

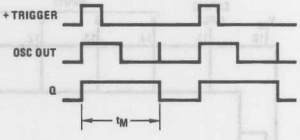
Timing Diagram

Astable Mode



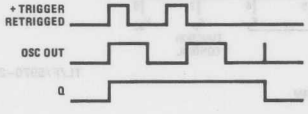
TL/F/5969–9

Monostable Mode



TL/F/5969–10

Retrigger Mode



TL/F/5969–11

National Semiconductor

CD4048BM/CD4048BC TRI-STATE® Expandable 8-Function 8-Input Gate

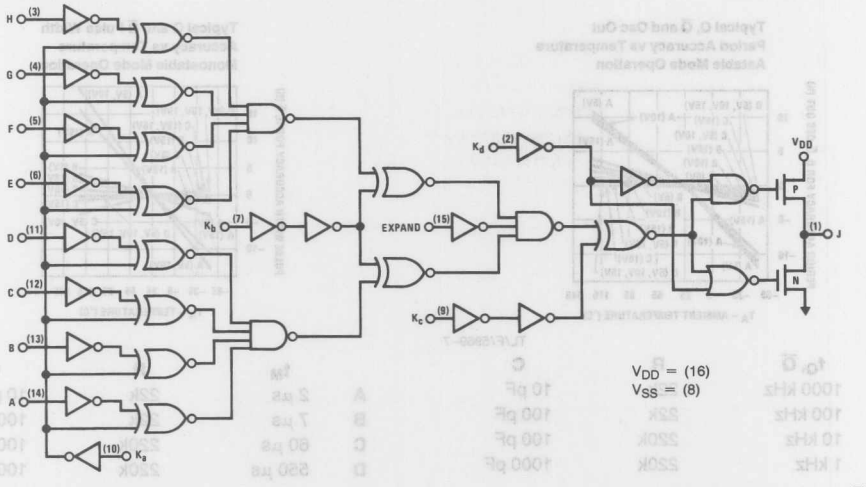
General Description

The CD4048BM/CD4048BC is a programmable 8-input gate. Three binary control lines K_a, K_b, and K_c determine the 8 different logic functions of the gate. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR. A fourth input, K_d, is a TRI-STATE control. When K_d is high, the output is enabled; when K_d is low, the output is a high impedance. This feature enables the user to connect the device to a common bus line. The Expand input permits the user to increase the number of gate inputs. For example, two 8-input CD4048's can be cascaded into a 16-input multi-function gate. When the Expand input is not used, it should be connected to V_{SS}. All inputs are buffered and protected against electrostatic effects.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- High sink and source current capability
- TTL compatibility — drives 1 standard TTL load at V_{CC} = 5V, over full temperature range
- Many logic functions in one package

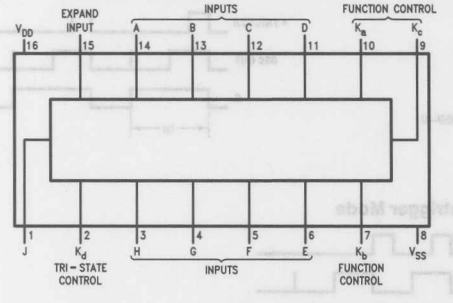
Logic Diagram



TL/F/5970–1

Connection Diagram

Dual-In-Line Package



TL/F/5970–2

Top View

Order Number CD4048B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4048BM	−55°C to +125°C
CD4048BC	−40°C to +85°C

DC Electrical Characteristics CD4048BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.01	5.0		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	2.8		2.3	4.0		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	6.4		5.2	11		3.6		mA
		V_{DD} = 15V, V_O = 1.5V	14		11.5	23		8.0		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−2.8		−2.3	−4.0		−1.6		mA
		V_{DD} = 10V, V_O = 9.5V	−6.4		−5.2	−11		−3.6		mA
		V_{DD} = 15V, V_O = 13.5V	−14		−11.5	−23		−8.0		mA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V, V_O = 0V		−0.2		−0.002	−0.2		−2	μA
		V_{DD} = 15V, V_O = 15V		0.2		0.002	0.2		2	μA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4048BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	2.3		2.0	4.0		1.6		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	5.2		4.5	11		3.6		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	11.5		9.8	23		8.0		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−2.3		−2.0	−4.0		−1.6		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−5.2		−4.5	−11		−3.6		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−11.5		−9.8	−23		−8.0		mA
I_{TL}	TRI-STATE Leakage Current	$V_{DD} = 15V$, $V_O = 0V$		−0.6		−0.005	−0.6		−2	μA
		$V_{DD} = 15V$, $V_O = 15V$		0.6		0.005	0.6		2	μA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		425	850	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time,	$R_L = 1.0$ kΩ				
	K_d to High Impedance	$V_{DD} = 5V$		175	350	ns
	(from Active Low	$V_{DD} = 10V$		125	250	ns
	or High Level)	$V_{DD} = 15V$		100	200	ns
t_{PZL}, t_{PZH}	Propagation Delay Time,	$R_L = 1.0$ kΩ				
	K_d to Active	$V_{DD} = 5V$		225	450	ns
	High or Low Level	$V_{DD} = 10V$		100	200	ns
	(from High Impedance)	$V_{DD} = 15V$		70	140	ns
t_{THL}, t_{TLH}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance				22.5	pF

*AC Parameters are guaranteed by DC correlated testing.

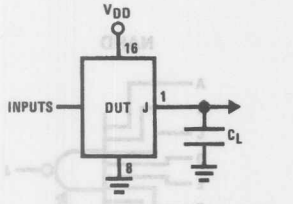
Truth Table

Output Function	Boolean Expression	Control Inputs				Unused Inputs
		K_a	K_b	K_c	K_d	
NOR	$J = \overline{A + B + C + D + E + F + G + H}$	0	0	0	1	V_{SS}
OR	$J = A + B + C + D + E + F + G + H$	0	0	1	1	V_{SS}
OR/AND	$J = (A + B + C + D) \bullet (E + F + G + H)$	0	1	0	1	V_{SS}
OR/NAND	$J = \overline{(A + B + C + D) \bullet (E + F + G + H)}$	0	1	1	1	V_{SS}
AND	$J = A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H$	1	0	0	1	V_{DD}
NAND	$J = \overline{A \bullet B \bullet C \bullet D \bullet E \bullet F \bullet G \bullet H}$	1	0	1	1	V_{DD}
AND/NOR	$J = \overline{(A \bullet B \bullet C \bullet D) + (E \bullet F \bullet G \bullet H)}$	1	1	0	1	V_{DD}
AND/OR	$J = (A \bullet B \bullet C \bullet D) + (E \bullet F \bullet G \bullet H)$	1	1	1	1	V_{DD}
Hi-Z		X	X	X	0	X

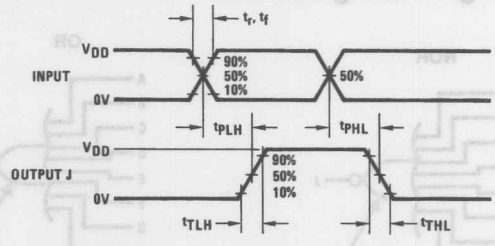
Positive logic: 0 = low level, 1 = high level, X = irrelevant, EXPAND input tied to V_{SS}.

AC Test Circuits and Switching Time Waveforms

Logic Propagation Delay Time Tests

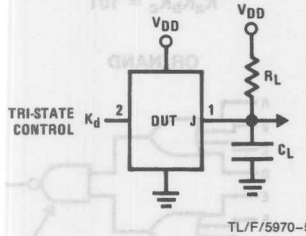


TL/F/5970–3

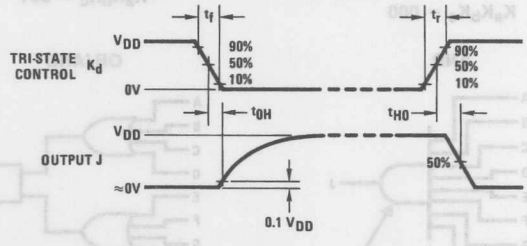


TL/F/5970–4

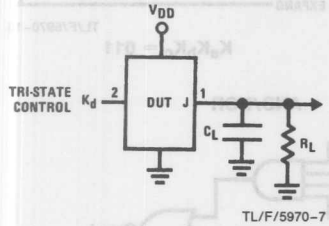
TRI-STATE Propagation Delay Time Tests



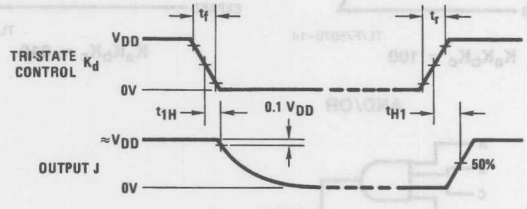
TL/F/5970–5



TL/F/5970–6

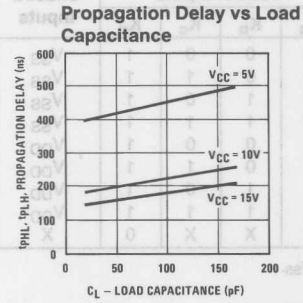


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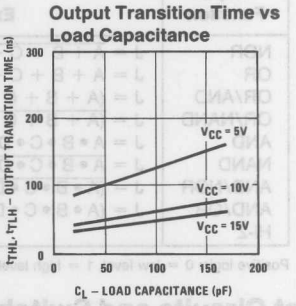


TL/F/5970–8

Typical Performance Characteristics



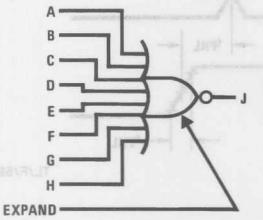
TL/F/5970–9



TL/F/5970–10

Basic Logic Configurations

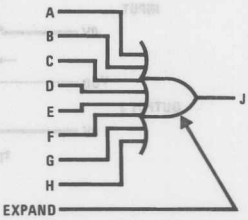
NOR



TL/F/5970–11

$K_aK_bK_c = 000$

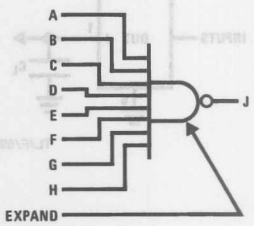
OR



TL/F/5970–12

$K_aK_bK_c = 001$

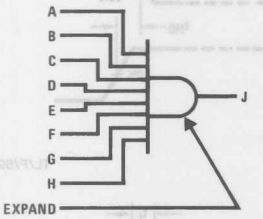
NAND



TL/F/5970–13

$K_aK_bK_c = 101$

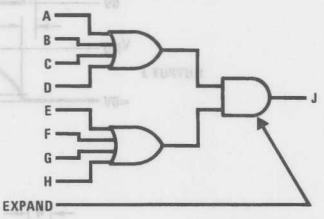
AND



TL/F/5970–14

$K_aK_bK_c = 100$

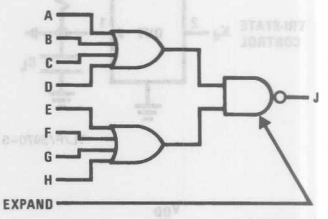
OR/AND



TL/F/5970–15

$K_aK_bK_c = 010$

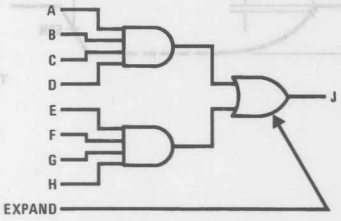
OR/NAND



TL/F/5970–16

$K_aK_bK_c = 011$

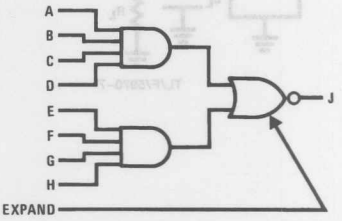
AND/OR



TL/F/5970–17

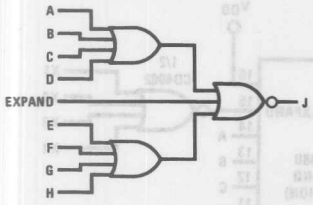
$K_aK_bK_c = 111$

AND/NOR



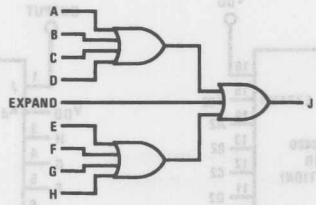
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$K_aK_bK_c = 110$



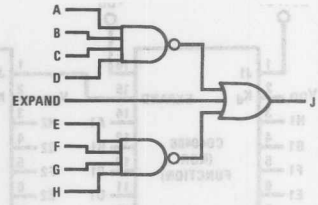
TL/F/5970–19

$K_aK_bK_c = 000$



TL/F/5970–20

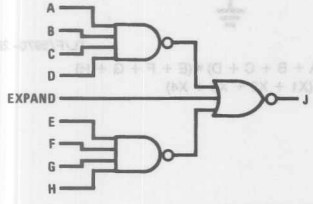
$K_aK_bK_c = 001$



TL/F/5970–21

$K_aK_bK_c = 101$

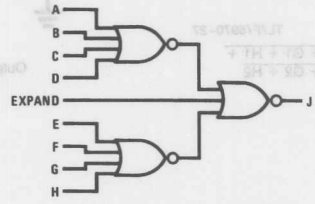
AND



TL/F/5970–22

$K_aK_bK_c = 100$

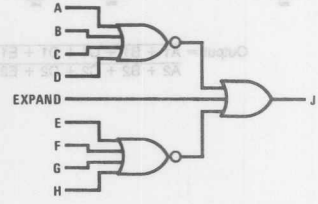
OR/AND



TL/F/5970–23

$K_aK_bK_c = 010$

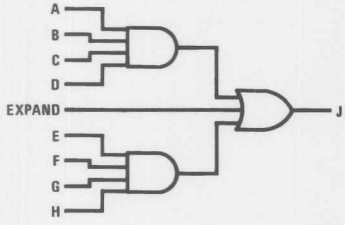
OR/NAND



TL/F/5970–24

$K_aK_bK_c = 011$

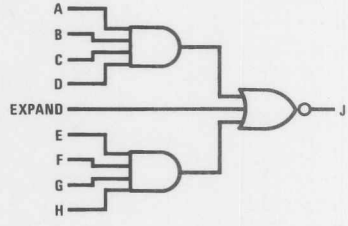
AND/OR



TL/F/5970–25

$K_aK_bK_c = 111$

AND/NOR



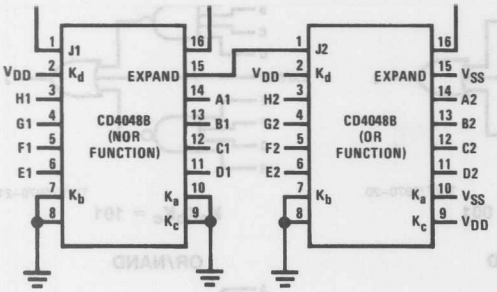
TL/F/5970–26

$K_aK_bK_c = 110$

Truth Table for EXPAND Feature

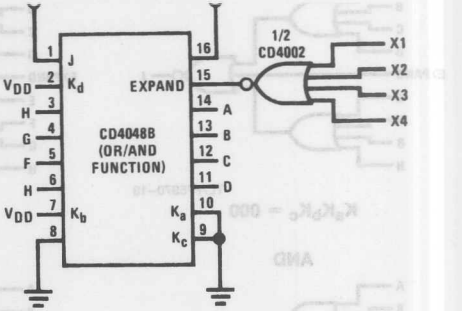
Combined Output Function	Function Needed at Expand Input	Output Boolean Expression
NOR	OR	$J = \overline{(A + B + C + D + E + F + G + H) + (EXP)}$
OR	OR	$J = (A + B + C + D + E + F + G + H) + (EXP)$
AND	NAND	$J = (ABCDEFGH) \bullet \overline{EXP}$
NAND	NAND	$J = \overline{(ABCDEFGH) \bullet \overline{EXP}}$
OR/AND	NOR	$J = (A + B + C + D) \bullet (E + F + G + H) \bullet (\overline{EXP})$
OR/NAND	NOR	$J = \overline{(A + B + C + D) \bullet (E + F + G + H) \bullet (\overline{EXP})}$
AND/NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note: Positive logic is assumed. (EXP) represents the logic level present at the EXPAND input.



TL/F/5970–27

$$\text{Output} = \overline{A1 + B1 + C1 + D1 + E1 + F1 + G1 + H1 + A2 + B2 + C2 + D2 + E2 + F2 + G2 + H2}$$



TL/F/5970–28

$$\text{Output} = (A + B + C + D) \bullet (E + F + G + H) \bullet (X1 + X2 + X3 + X4)$$

National Semiconductor

CD4049UBM/CD4049UBC Hex Inverting Buffer
CD4050BM/CD4050BC Hex Non-Inverting Buffer

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5.0V, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

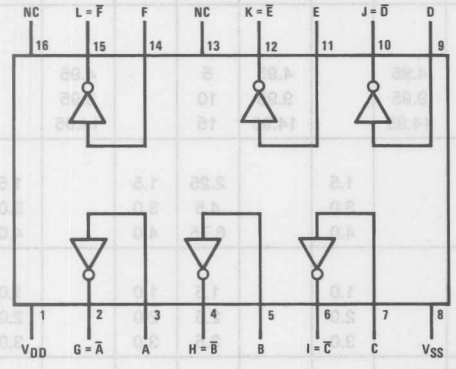
- Wide supply voltage range 3.0V to 15V
- Direct drive to 2 TTL loads at 5.0V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic level converter

Connection Diagrams

CD4049UBM/CD4049UBC
Dual-In-Line Package

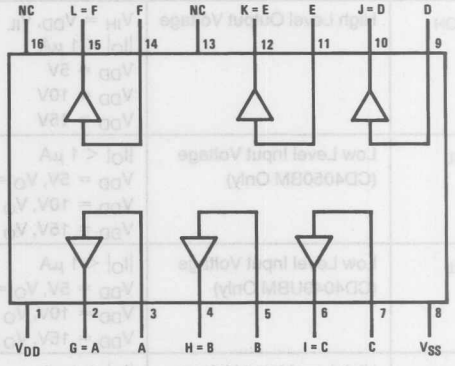


TL/F/5971–1

Top View

Order Number CD4049UB* or CD4049B*

CD4050BM/CD4050BC
Dual-In-Line Package



TL/F/5971–2

Top View

Order Number CD4050UB* or CD4050B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to +18V
Voltage at Any Output Pin (V_{OUT})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to 15V
Voltage at Any Output Pin (V_{OUT})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4049UBM, CD4050BM	−55°C to +125°C
CD4049UBC, CD4050BC	−40°C to +85°C

DC Electrical Characteristics CD4049M/CD4050BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		30	μA
		V_{DD} = 10V		2.0		0.01	2.0		60	μA
		V_{DD} = 15V		4.0		0.03	4.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049UBM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049UBM Only)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	5.6		4.6	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	12		9.8	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	35		29	40		20		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4049M/CD4050BM (Note 2) (Continued)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−1.3		−1.1	−1.6		−0.72		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−2.6		−2.2	−3.6		−1.5		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−8.0		−7.2	−12		−5.0		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4049UBC/CD4050BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		4		0.03	4.0		30	μA
		$V_{DD} = 10V$		8		0.05	8.0		60	μA
		$V_{DD} = 15V$		16		0.07	16.0		120	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0V$, $\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, $V_{IL} = 0V$, $\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BC Only)	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049UBC Only)	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 4.5V$		1.0		1.5	1.0		1.0	V
		$V_{DD} = 10V$, $V_O = 9V$		2.0		2.5	2.0		2.0	V
		$V_{DD} = 15V$, $V_O = 13.5V$		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BC Only)	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049UBC Only)	$\lvert I_O \rvert < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$	4.0		4.0	3.5		4.0		V
		$V_{DD} = 10V$, $V_O = 1V$	8.0		8.0	7.5		8.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$	12.0		12.0	11.5		12.0		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

			Min	Max	Min	Typ	Max	Min	Max	
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}, V_{IL} = 0V$								
	(Note 3)	$V_{DD} = 5V, V_O = 0.4V$	4.6		4.0	5		3.2		mA
		$V_{DD} = 10V, V_O = 0.5V$	9.8		8.5	12		6.8		mA
		$V_{DD} = 15V, V_O = 1.5V$	29		25	40		20		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}, V_{IL} = 0V$								
	(Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−1.0		−0.9	−1.6		−0.72		mA
		$V_{DD} = 10V, V_O = 9.5V$	−2.1		−1.9	−3.6		−1.5		mA
		$V_{DD} = 15V, V_O = 13.5V$	−7.1		−6.2	−12		−5		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$	−0.3		−0.3	-10^{-5}			−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$	0.3		0.3	10^{-5}			1.0	μA

AC Electrical Characteristics* CD4049UBM/CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		30	65	ns
	High-to-Low Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		45	85	ns
	Low-to-High Level	$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	ns
t_{THL}	Transition Time	$V_{DD} = 5V$		30	60	ns
	High-to-Low Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time	$V_{DD} = 5V$		60	120	ns
	Low-to-High Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

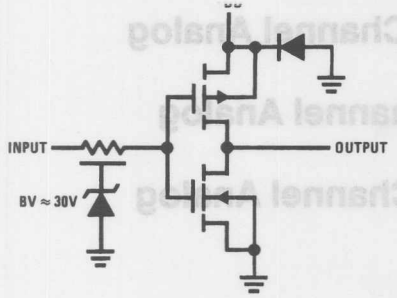
*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4050BM/CD4050BC

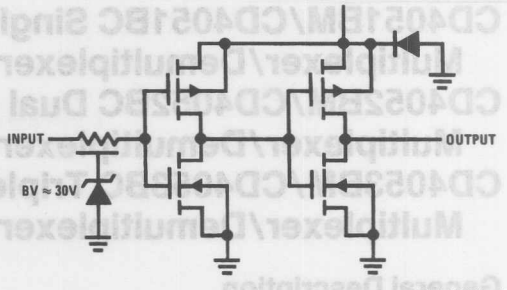
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$k, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		60	110	ns
	High-to-Low Level	$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	ns
t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		60	120	ns
	Low-to-High Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
t_{THL}	Transition Time	$V_{DD} = 5V$		30	60	ns
	High-to-Low Level	$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time	$V_{DD} = 5V$		60	120	ns
	Low-to-High Level	$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

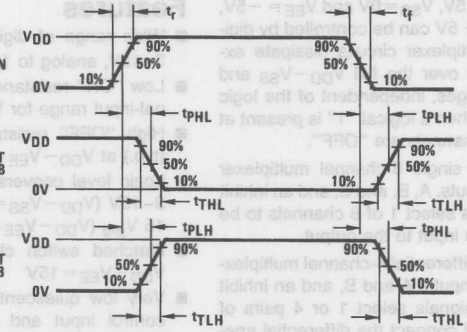


TL/F/5971–3



TL/F/5971–4

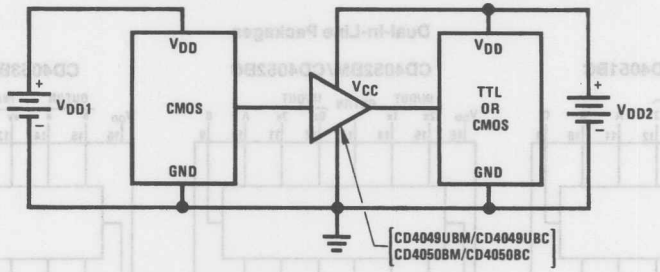
Switching Time Waveforms



TL/F/5971–5

Typical Applications

CMOS to TTL or CMOS at a Lower V_{DD}



TL/F/5971–6

Note: $V_{DD1} \geq V_{DD2}$

Note: In the case of the CD4049UBM/CD4049UBC the output drive capability increases with increasing input voltage. E.g., If V_{DD1} = 10V the CD4049UBM/CD4049UBC could drive 4 TTL loads.

National Semiconductor

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

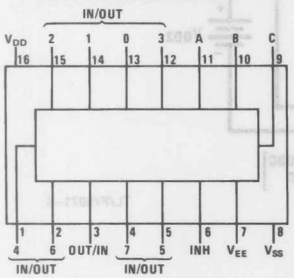
Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD}-V_{EE}=15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD}-V_{EE}=10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD}-V_{SS}=3-15V$) to switch analog signals to 15 V_{p-p} ($V_{DD}-V_{EE}=15V$)
- Matched switch characteristics: $\Delta R_{ON}=5\Omega$ (typ.) for $V_{DD}-V_{EE}=15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- Binary address decoding on chip

Connection Diagrams

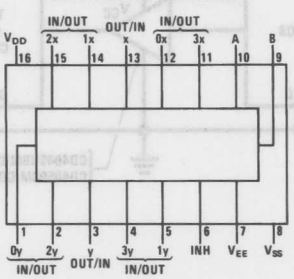
Dual-In-Line Packages

CD4051BM/CD4051BC



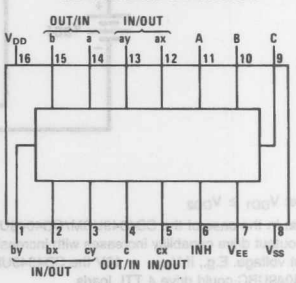
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW TL/F/5662–1

Order Number CD4051B*, CD4052B*, or CD4053B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD}+0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (T_L) (soldering, 10 sec.)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$+5\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
4051BM/4052BM/4053BM	$-55°C$ to $+125°C$
4051BC/4052BC/4053BC	$-40°C$ to $+85°C$

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		−55°C		+25°			+125°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			5			5		150	μA
		$V_{DD}=10V$			10			10		300	μA
		$V_{DD}=15V$			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE}\le V_{IS}\le V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		800		270	1050		1300	Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		310		120	400		550	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $V_{EE}=-7.5V$ $O/I=\pm7.5V$, $I/O=0V$			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V	CD4051		±200		±0.08	±200		±2000	nA
		$V_{DD}=7.5V$, $V_{EE}=-7.5V$, $O/I=0V$, $I/O=\pm7.5V$	CD4052		±200		±0.04	±200		±2000	nA
			CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF channels $V_{IS}=V_{DD}$ thru 1 kΩ									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$	$V_{EE}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$	$V_{EE}=0V$		0.1		10^{-5}	0.1		1.0	μA
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			20			20		150	μA
		$V_{DD}=10V$			40			40		300	μA
		$V_{DD}=15V$			80			80		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE}\leq V_{IS}\leq V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		850		270	1050		1200	Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		330		120	400		520	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		210		80	240		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $O/I=\pm7.5V$,	$V_{EE}=-7.5V$ $I/O=0V$		±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V, $V_{DD}=7.5V$, $V_{EE}=-7.5V$, $O/I=0V$	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
		$I/O=\pm7.5V$	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF Channels $V_{IS}=V_{DD}$ thru 1 kΩ									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$	$V_{EE}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$	$V_{EE}=0V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

AC Electrical Characteristics* $T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

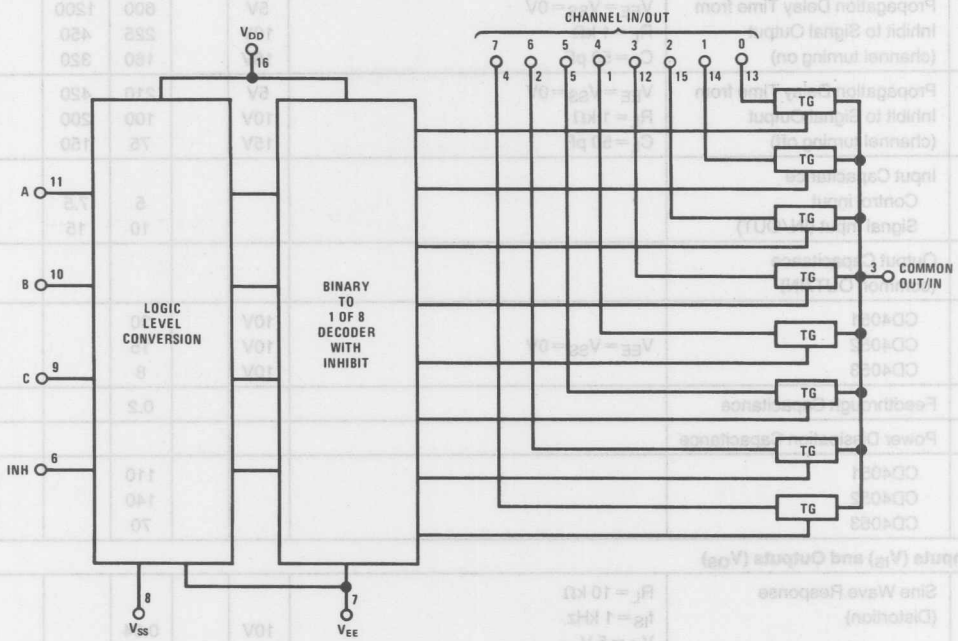
Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Units
t_{PZH}, t_{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		600 225 160	1200 450 320	ns ns ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		210 100 75	420 200 150	ns ns ns
C_{IN}	Input Capacitance Control input Signal Input (IN/OUT)				 5 10	 7.5 15	 pF pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	$V_{EE} = V_{SS} = 0V$	10V 10V 10V		30 15 8		pF pF pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10\ k\Omega$ $f_{IS} = 1$ kHz $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0V$	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1\ k\Omega$, $V_{EE} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -3$ dB	10V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -40$ dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$ $20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10V		3		MHz
t_{PHL} t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		25 15 10	55 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		500 180 120	1000 360 240	ns ns ns

*AC Parameters are guaranteed by DC correlated testing.

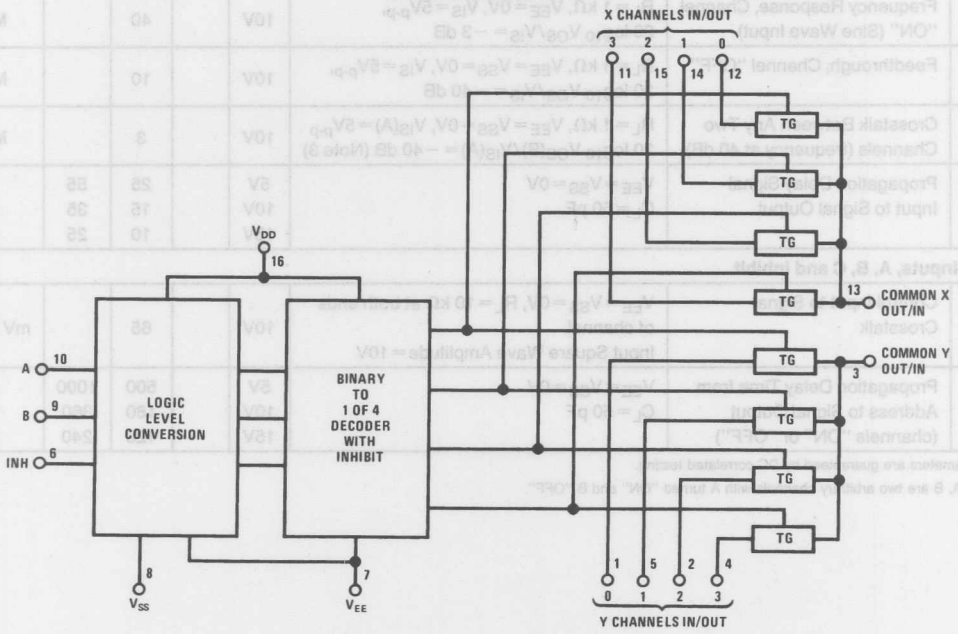
Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

Block Diagrams

CD4051BM/CD4051BC



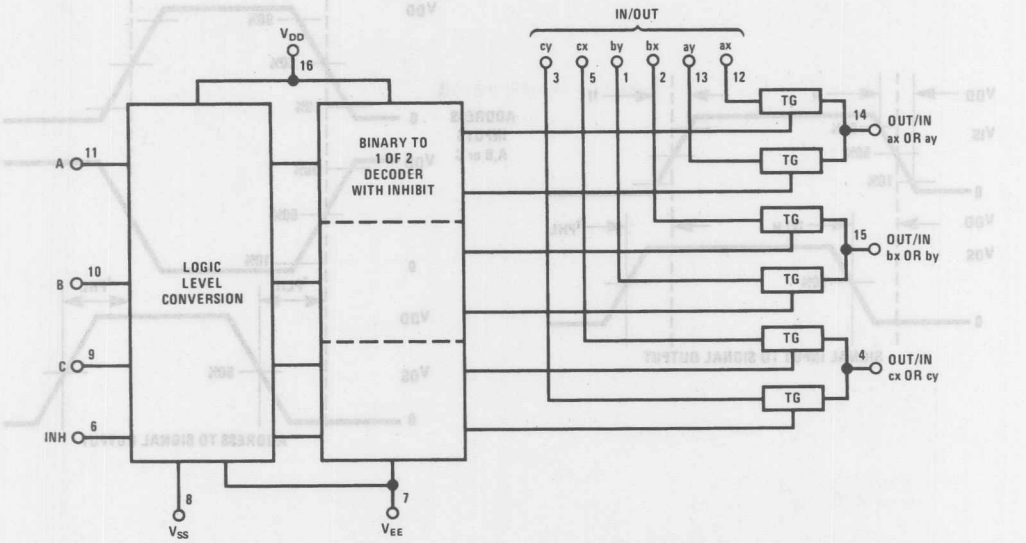
CD4052BM/CD4052BC



TL/F/5662–2

Block Diagrams (Continued)

CD4053BM/CD4053BC



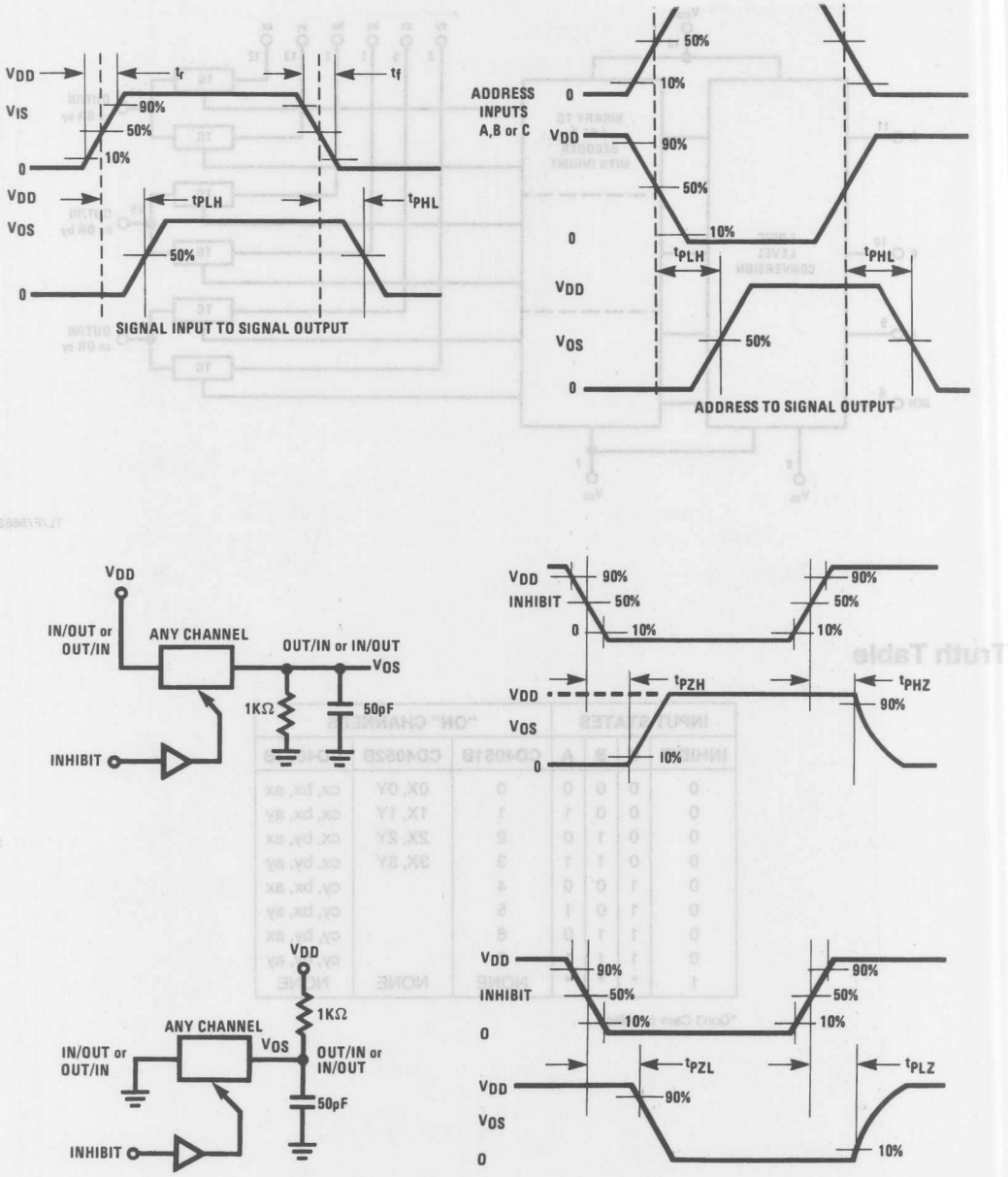
TL/F/5662–3

Truth Table

INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

*Don't Care condition.

5


VDD
VIS
0
tr
tf
90%
50%
10%
VDD
VOS
0
tPLH
tPHL
50%
SIGNAL INPUT TO SIGNAL OUTPUT
ADDRESS INPUTS A,B or C
0
VDD
50%
10%
90%
50%
10%
0
tPLH
tPHL
VDD
VOS
0
50%
ADDRESS TO SIGNAL OUTPUT
VDD
IN/OUT or OUT/IN
ANY CHANNEL
OUT/IN or IN/OUT
VOS
1KΩ
50pF
INHIBIT
VDD
INHIBIT
0
90%
50%
10%
90%
50%
10%
tPZH
tPHZ
VDD
VOS
0
10%
90%
VDD
1KΩ
ANY CHANNEL
IN/OUT or OUT/IN
VOS
OUT/IN or IN/OUT
50pF
INHIBIT
VDD
INHIBIT
0
90%
50%
10%
90%
50%
10%
tPZL
tPLZ
VDD
VOS
0
90%
10%

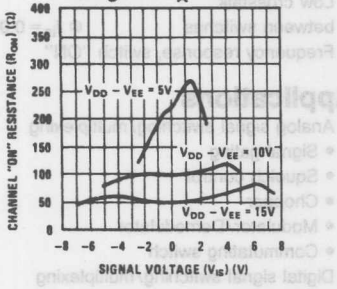
TL/F/5662–4

Special Considerations

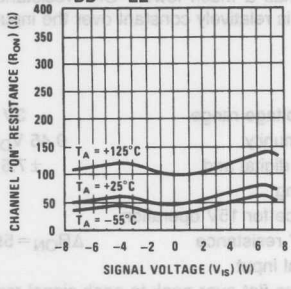
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

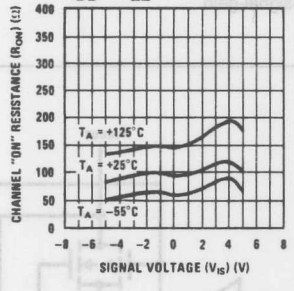
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



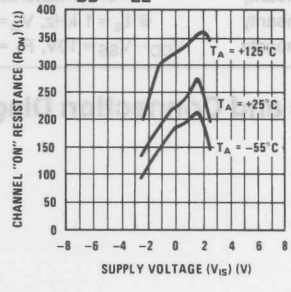
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



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5

National Semiconductor

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

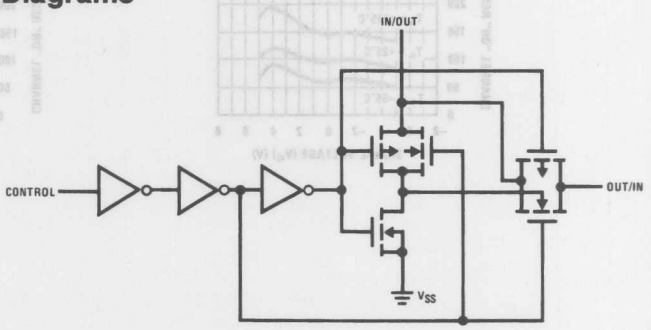
Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB (typ.) @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree linearity — 0.1% distortion (typ.) @ f_{is} = 1 kHz, V_{is} = 5V_{p-p}, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA (typ.) @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω (typ.)
- Low crosstalk between switches — −50 dB (typ.) @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz (typ.)

Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

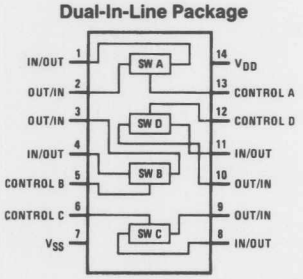
Schematic and Connection Diagrams



Order Number CD4066B*

*Please look into Section 8, Appendix D for availability of various package types.

Dual-In-Line Package



TL/F/5665–1

Top View

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		0.25		0.01	0.25		7.5	μA
		$V_{DD}=10V$		0.5		0.01	0.5		15	μA
		$V_{DD}=15V$		1.0		0.01	1.0		30	μA
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=5V$		800		270	1050		1300	Ω
		$V_{DD}=10V$		310		120	400		550	Ω
		$V_{DD}=15V$		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				10				Ω
		$V_{DD}=15V$				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$		±50		±0.1	±50		±500	nA
		$V_{IS}=15V$ and 0V,								
		$V_{OS}=0V$ and 15V								
CONTROL INPUTS										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD}								
		$V_{OS}=V_{DD}$ and V_{SS}								
		$I_{IS}=\pm 10\ \mu A$								
		$V_{DD}=5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$		3.0		4.5	3.0		3.0	V
		$V_{DD}=15V$		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$ (see note 6)	7.0		7.0	5.5		7.0		V
		$V_{DD}=15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD}-V_{SS}=15V$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA
		$V_{DD}\geq V_{IS}\geq V_{SS}$								
		$V_{DD}\geq V_C\geq V_{SS}$								

DC Electrical Characteristics CD4066BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		1.0		0.01	1.0		7.5	μA
		$V_{DD}=10V$		2.0		0.01	2.0		15	μA
		$V_{DD}=15V$		4.0		0.01	4.0		30	μA

DC Electrical Characteristics (Continued) CD4066BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
SIGNAL INPUTS AND OUTPUTS										
R_{ON}	"ON" Resistance	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C = V_{DD}$, V_{SS} to V_{DD}								
		$V_{DD} = 5V$		850		270	1050		1200	Ω
		$V_{DD} = 10V$		330		120	400		520	Ω
		$V_{DD} = 15V$		210		80	240		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		$V_{DD} = 10V$				10				Ω
		$V_{DD} = 15V$				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C = 0$		±50		±0.1	±50		±200	nA
CONTROL INPUTS										
V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD} $V_{OS} = V_{DD}$ and V_{SS} $I_{IS} = \pm 10\mu A$								
		$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$ (See note 6)	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} - V_{SS} = 15V$ $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

AC Electrical Characteristics* $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, $C_L = 50$ pF, (*Figure 1*) $R_L = 200k$				
		$V_{DD} = 5V$		25	55	ns
		$V_{DD} = 10V$		15	35	ns
		$V_{DD} = 15V$		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, (*Figures 2* and *3*)				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, (*Figures 2* and *3*)				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$ $R_L = 10\ k\Omega$, $V_{IS} = 5V_{p-p}$, $f = 1$ kHz, (*Figure 4*)		0.1		%
	Frequency Response-Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5V_{p-p}$, 20 $\text{Log}_{10}\ V_{OS}/V_{OS}$ (1 kHz) − dB, (*Figure 4*)		40		MHz

AC Electrical Characteristics* (Continued) $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5.0V$, $V_{CC} = V_{SS} = -5.0V$, $R_L = 1\ k\Omega$, $V_{IS} = 5.0V_{p-p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50$ dB, *(Figure 4)*		1.25		
	Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5.0V$; $V_{SS} = V_{C(B)} = 5.0V$, $R_L 1\ k\Omega$, $V_{IS(A)} = 5.0\ V_{p-p}$, 20 Log_{10}, $V_{OS(B)}/V_{IS(A)} = -50$ dB *(Figure 5)*		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$, $R_{IN} = 1.0\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$ pF *(Figure 6)*		150		mV_{p-p}
	Maximum Control Input	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figure 7)* $V_{OS(f)} = \frac{1}{2}\ V_{OS}$(1.0 kHz)				
		$V_{DD} = 5.0V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{IS}	Signal Input Capacitance			8.0		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		8.0		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.5		pF
C_{IN}	Control Input Capacitance			5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC}: a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0V$, I_{OL} = standard B series I_{OL}.

AC Test Circuits and Switching Time Waveforms

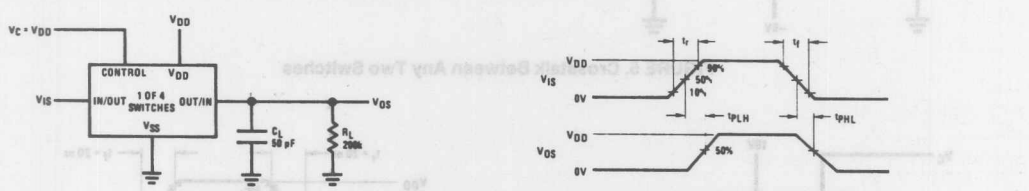


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

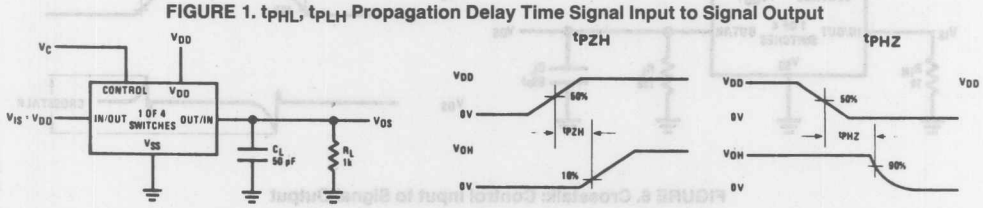


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

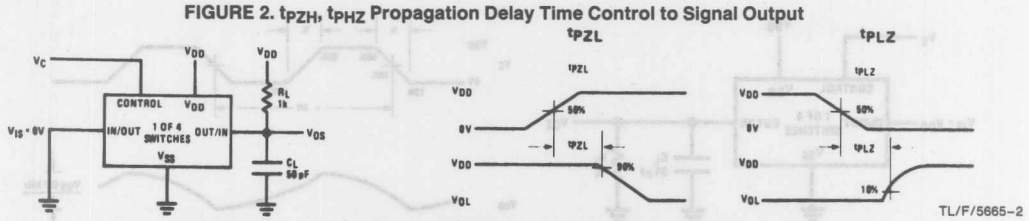


FIGURE 3. t_{PZL}, t_{PLZ} Propagtion Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

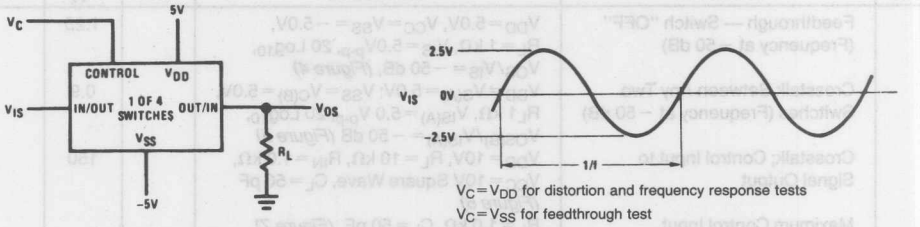


FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

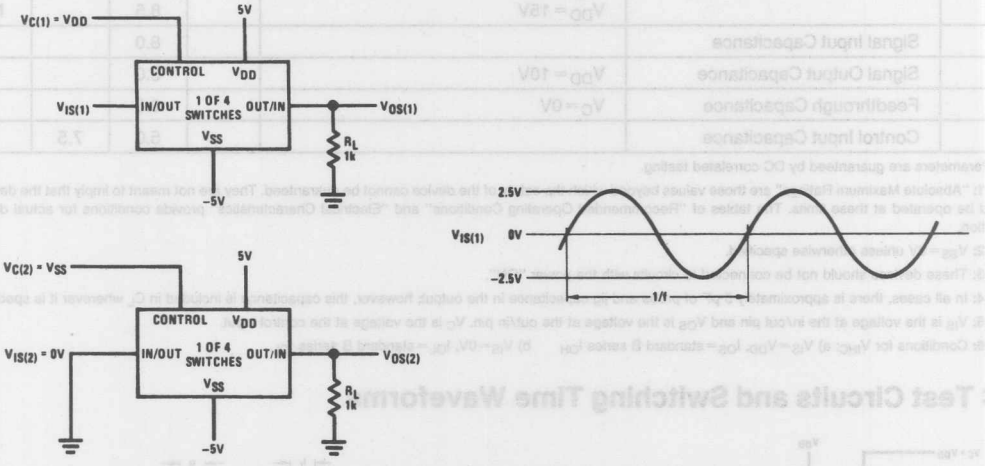


FIGURE 5. Crosstalk Between Any Two Switches

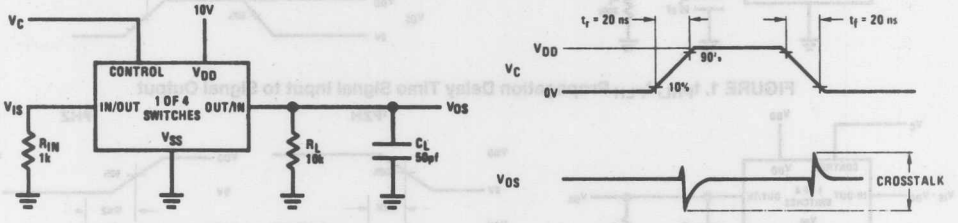
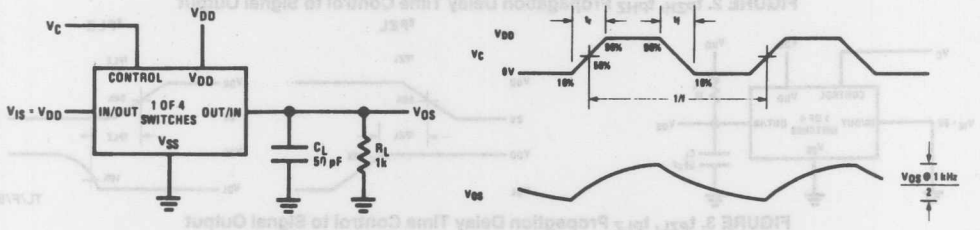


FIGURE 6. Crosstalk: Control Input to Signal Output

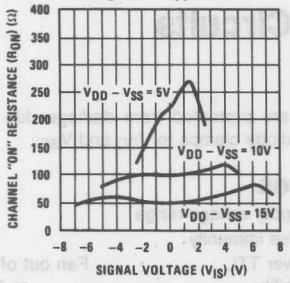


TL/F/5665–3

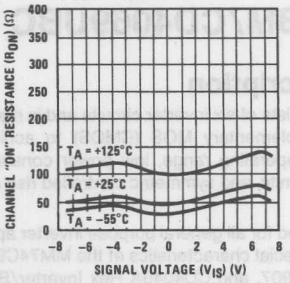
FIGURE 7. Maximum Control Input Frequency

Typical Performance Characteristics

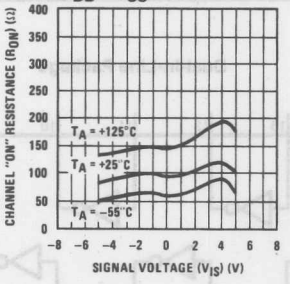
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



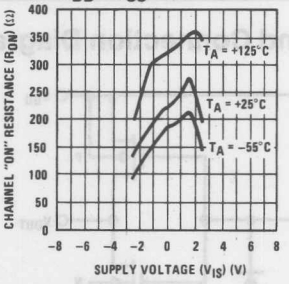
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



TL/F/5665–4

Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

5

National Semiconductor

CD4069UBM/CD4069UBC Inverter Circuits

General Description

The CD4069UB consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

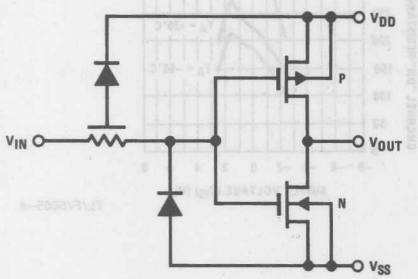
This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C903, MM74C907, and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

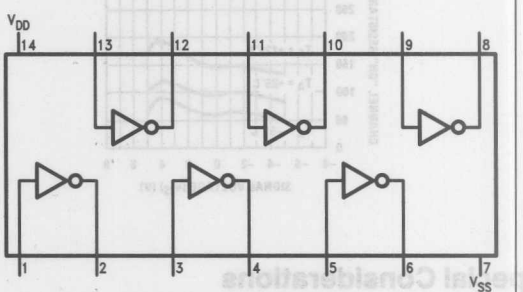
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ.
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MM54C04/MM74C04

Schematic and Connection Diagram



TL/F/5975–1

Dual-In-Line Package

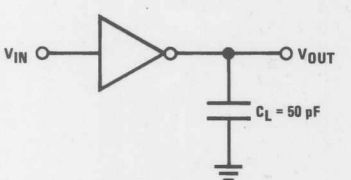


TL/F/5975–2

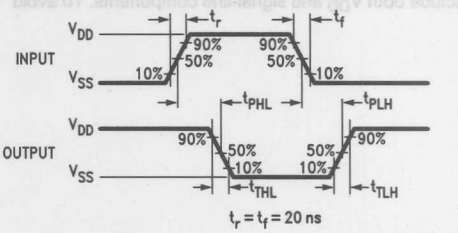
Order Number CD4069UB*

*Please look into Section 8, Appendix D for availability of various package types.

AC Test Circuits and Switching Time Waveforms



TL/F/5975–3



TL/F/5975–4

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5V$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to $15V_{DC}$
Input Voltage (V_{IN})	0V to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4069UBM	$-55°C$ to $+125°C$
CD4069UBC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4069UBM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		0.25			0.25		7.5	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		0.5			0.5		15	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		1.0			1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 4.5V$		1.0			1.0		1.0	V
		$V_{DD} = 10V$, $V_O = 9V$		2.0			2.0		2.0	V
		$V_{DD} = 15V$, $V_O = 13.5V$		3.0			3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$	4.0		4.0			4.0		V
		$V_{DD} = 10V$, $V_O = 1V$	8.0		8.0			8.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$	12.0		12.0			12.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4069UBC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V		1.0			1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0			2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0			3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0			4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0			8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0			12.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, t_r and t_f ≤ 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	V_{DD} = 5V		50	90	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		80	150	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Gate		6	15	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 4)		12		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

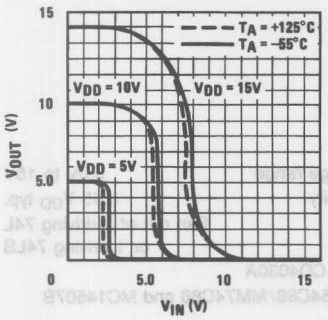
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

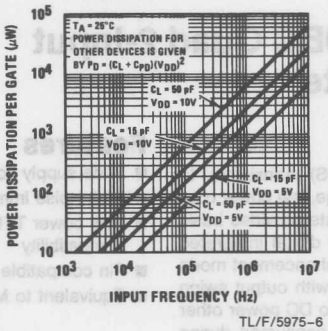
Typical Performance Characteristics

Gate Transfer Characteristics



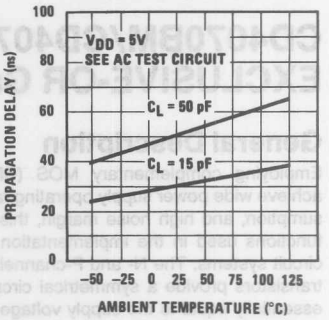
TL/F/5975–5

Power Dissipation vs Frequency



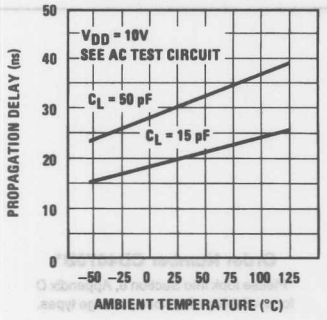
TL/F/5975–6

Propagation Delay vs Ambient Temperature



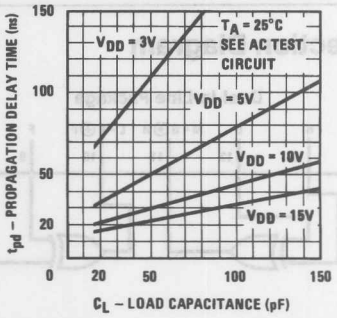
TL/F/5975–7

Propagation Delay vs Ambient Temperature



TL/F/5975–8

Propagation Delay Time vs Load Capacitance



TL/F/5975–9

National Semiconductor

CD4070BM/CD4070BC Quad 2-Input EXCLUSIVE-OR Gate

General Description

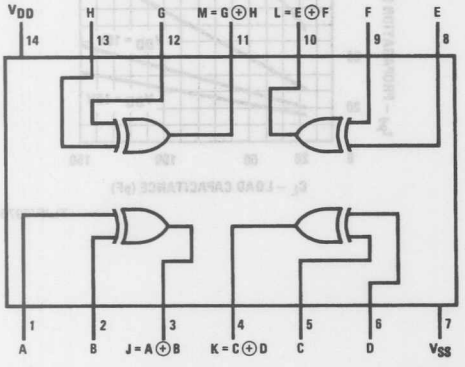
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption, and high noise margin, this gate provides basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ.
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Pin compatible to CD4030A
- Equivalent to MM54C86/MM74C86 and MC14507B

Connection Diagram

Dual-In-Line Package



TL/F/5976–1

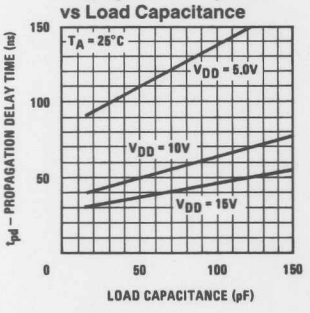
Top View

Order Number CD4070B*

*Please look into Section 8, Appendix D for availability of various package types.

Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance



TL/F/5976–2

Truth Table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD}+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4070BC	$-40°C$ to $+85°C$
CD4070BM	$-55°C$ to $+125°C$

DC Electrical Characteristics CD4070BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		0.25			0.25		7.5	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		0.5			0.5		15	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		1.0			1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|<1$ μA								
		$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|<1$ μA								
		$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|<1$ μA								
		$V_{DD}=5V$, $V_O=4.5V$		1.5			1.5		1.5	V
		$V_{DD}=10V$, $V_O=9V$		3.0			3.0		3.0	V
		$V_{DD}=15V$, $V_O=13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|<1$ μA								
		$V_{DD}=5V$, $V_O=0.5V$	3.5		3.5			3.5		V
		$V_{DD}=10V$, $V_O=1.0V$	7.0		7.0			7.0		V
		$V_{DD}=15V$, $V_O=1.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4070BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f ≤ 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	V_{DD} = 5V		110	185	ns
		V_{DD} = 10V		50	90	ns
		V_{DD} = 15V		40	75	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Input (Note 4)		20		pF

*AC Parameters are guaranteed by DC correlated testing.

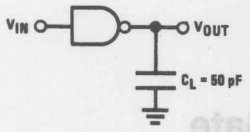
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

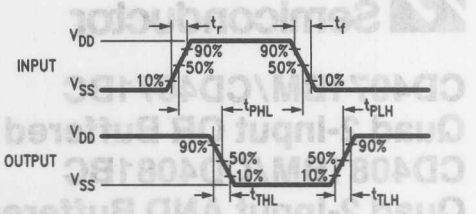
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note—AN-90.

AC Test Circuit and Switching Time Waveforms



TL/F/5976–3

Note: Delays measured with input t_r, t_f = 20 ns.



TL/F/5976–4

$t_r = t_f = 20$ ns

National Semiconductor

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

General Description

These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

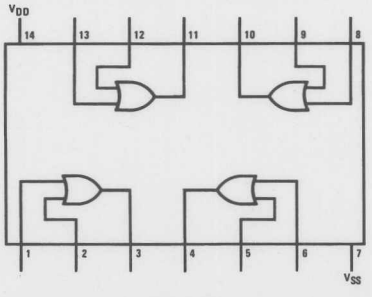
All inputs protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

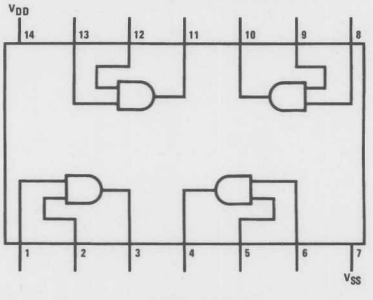
CD4071B Dual-In-Line Package



TL/F/5977–3

Top View

CD4081B Dual-In-Line Package



TL/F/5977–6

Top View

Order Number CD4071B* or CD4081B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.5V$ to $V_{DD} + 0.5V$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
V_{DD} Range	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Storage Temperature (T_S)	$-65°C$ to $+150°C$
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

Operating Range (V_{DD})	$3\ V_{DC}$ to $15\ V_{DC}$
Operating Temperature Range (T_A)	
CD4071BM, CD4081BM	$-55°C$ to $+125°C$
CD4071BC, CD4081BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4071BM/CD4081BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$		0.50		0.005	0.50		15	μA
		$V_{DD} = 15V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ | $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ | $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$ | $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.004	1		7.5	μA
		V_{DD} = 10V		2		0.005	2		15	μA
		V_{DD} = 15V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* CD4071BC/CD4071BM

T_A = 25°C, Input t_r; t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, Typical temperature coefficient is 0.3%/°C

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	90	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

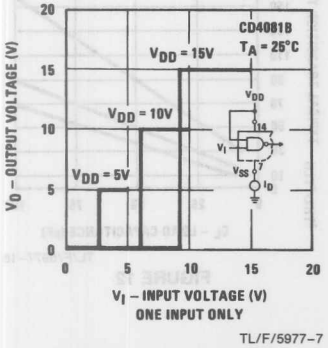
AC Electrical Characteristics* CD4081BC/CD4081BM

T_A = 25°C, Input t_r; t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ, Typical temperature coefficient is 0.3%/°C

Symbol	Parameter	Conditions	Typ	Max	Units
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

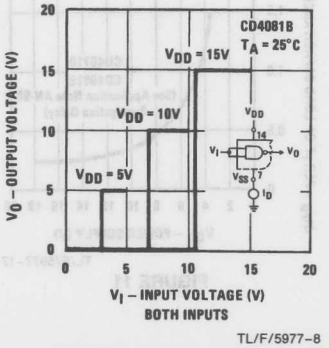
*AC Parameters are guaranteed by DC correlated testing.

Typical Performance Characteristics



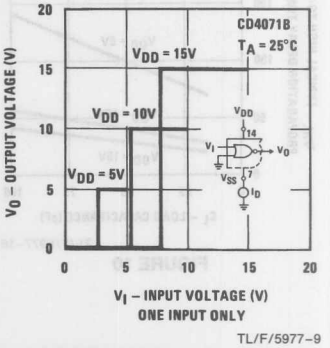
TL/F/5977–7

FIGURE 1. Typical Transfer Characteristics



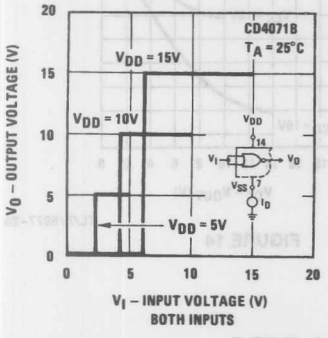
TL/F/5977–8

FIGURE 2. Typical Transfer Characteristics



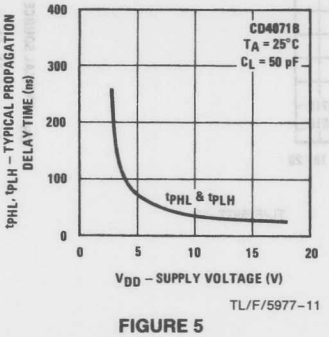
TL/F/5977–9

FIGURE 3. Typical Transfer Characteristics



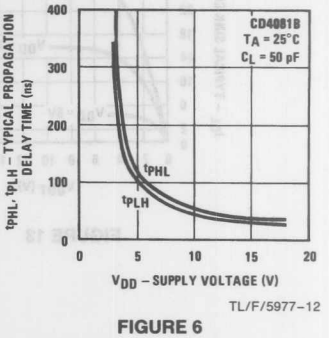
TL/F/5977–10

FIGURE 4. Typical Transfer Characteristics



TL/F/5977–11

FIGURE 5

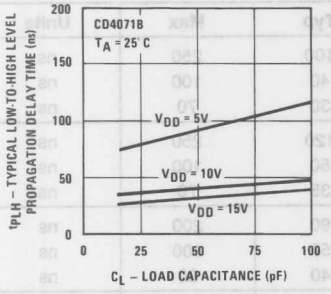


TL/F/5977–12

FIGURE 6

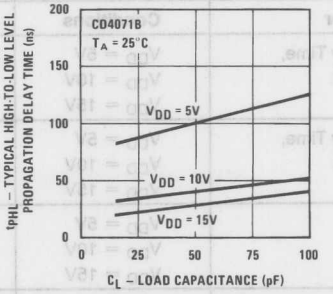
5

Typical Performance Characteristics (Continued)



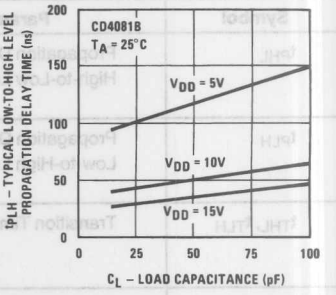
TL/F/5977–13

FIGURE 7



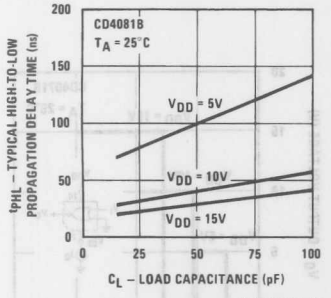
TL/F/5977–14

FIGURE 8



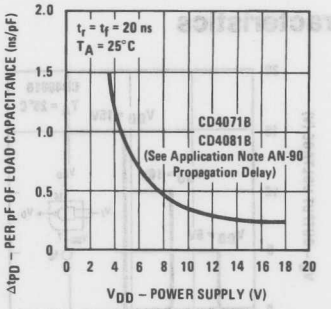
TL/F/5977–15

FIGURE 9



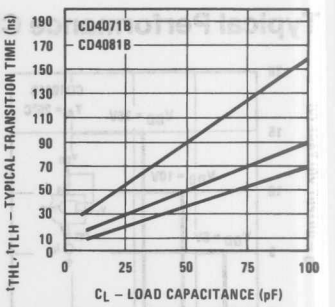
TL/F/5977–16

FIGURE 10



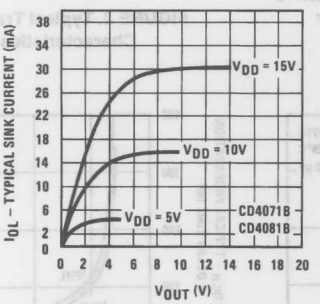
TL/F/5977–17

FIGURE 11



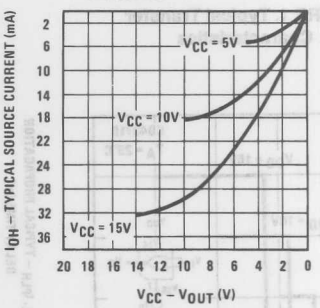
TL/F/5977–18

FIGURE 12



TL/F/5977–19

FIGURE 13

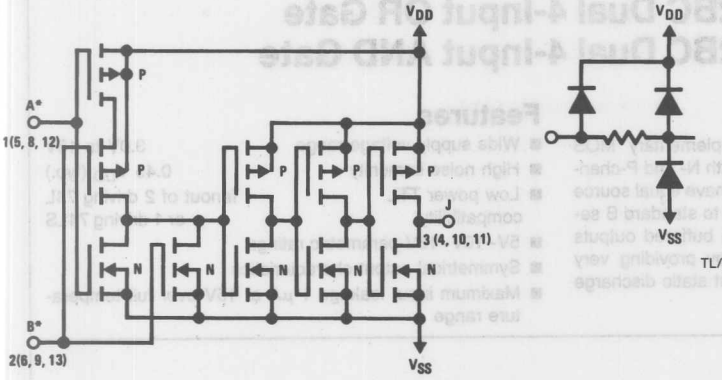


TL/F/5977–20

FIGURE 14

Schematic Diagrams

CD4071B



TL/F/5977–1

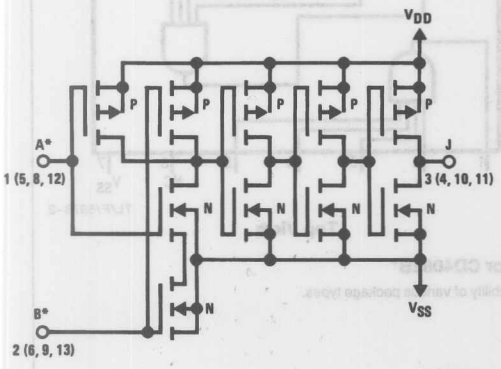
TL/F/5977–2

¼ of device shown

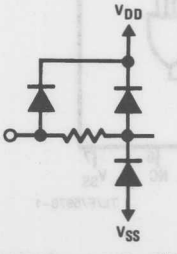
J = A + B
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4081B



TL/F/5977–4



TL/F/5977–5

¼ of device shown

J = A • B
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

National Semiconductor

CD4072BM/CD4072BC Dual 4-Input OR Gate
CD4082BM/CD4082BC Dual 4-Input AND Gate

General Description

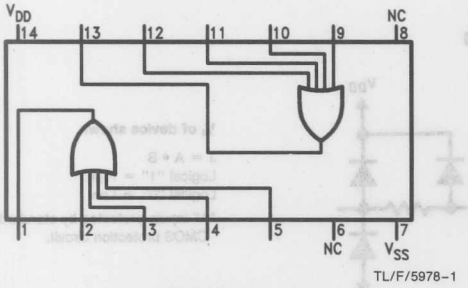
These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fanout of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

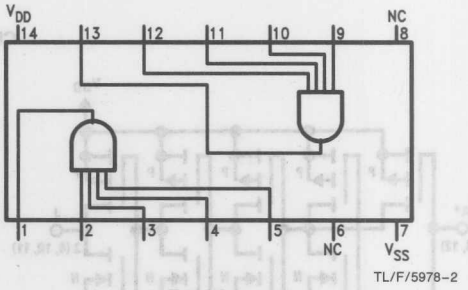
CD4072BM/CD4072BC



TL/F/5978–1

Top View

CD4082BM/CD4082BC



TL/F/5978–2

Top View

Order Number CD4072B* or CD4082B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3.0V to 15V
Input Voltage (V_{IN})	0V to V_{DD} V
Operating Temperature Range (T_A)	
CD4072BM, CD4082BM	−55°C to +125°C
CD4072BC, CD4082BC	−40°C to +85°C

DC Electrical Characteristics CD4072BM, CD4082BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0V		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.005	0.5		15	μA
		V_{DD} = 15V		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	10		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.2		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limts. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4072BC, CD4082BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0V		1.0		0.004	1.0		7.5	μA
		V_{DD} = 10V		2.0		0.005	2.0		15	μA
		V_{DD} = 15V		4.0		0.006	4.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	10		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay High to Low Level	V_{DD} = 5.0V		125	250	ns
		V_{DD} = 10V		60	100	ns
		V_{DD} = 15V		45	70	ns
t_{PLH}	Propagation Delay Low to High Level	V_{DD} = 5.0V		125	250	ns
		V_{DD} = 10V		60	100	ns
		V_{DD} = 15V		45	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5.0V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance (Note 4)	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 5)	Any Gate		20		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics, Application Note AN-90.

National Semiconductor

CD4073BM/CD4073BC
Double Buffered Triple 3-Input AND Gate
CD4075BM/CD4075BC
Double Buffered Triple 3-Input OR Gate

General Description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

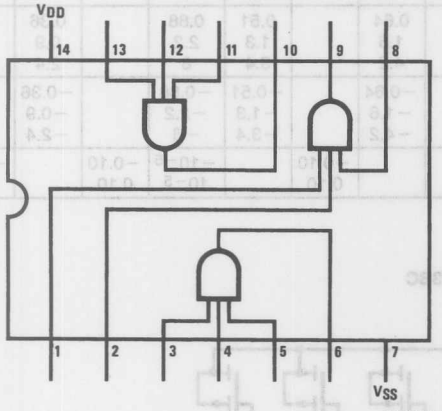
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams

Dual-In-Line Packages

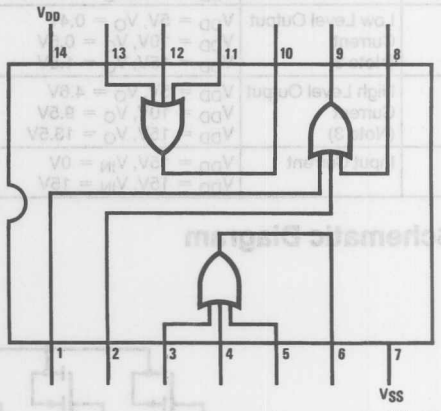
CD4073 Triple 3-Input AND Gate



TL/F/5979–1

Top View

CD4075B Triple 3-Input OR Gate



TL/F/5979–2

Top View

Order Number CD4073B* or CD4075B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Storage Temperature Range (T_S) −65°C to +150°C

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

Input Voltage (V_{IN}) 0 V_{DC} to V_{DD} V_{DC}

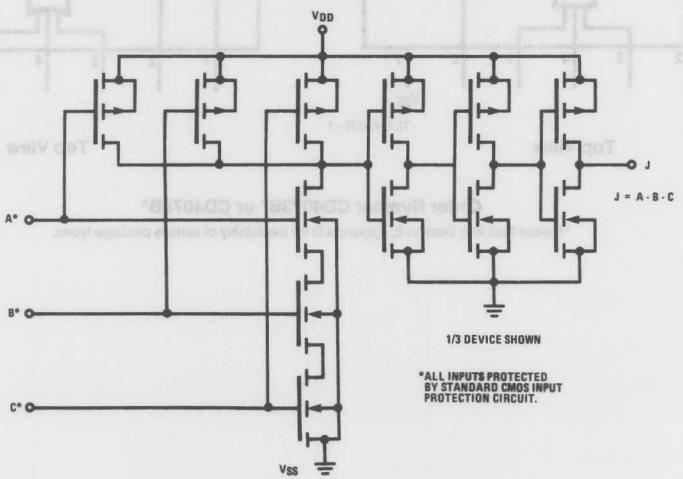
Operating Temperature Range (T_A)
- CD4073BM/CD4075BM −55°C to +125°C
- CD4073BC/CD4075BC −40°C to +85°C

DC Electrical Characteristics CD4073BM/CD4075BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5		0.005	0.5		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V, $\lvert I_O \rvert$ < 1 μA		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V, $\lvert I_O \rvert$ < 1 μA		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V, $\lvert I_O \rvert$ < 1 μA		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V, $\lvert I_O \rvert$ < 1 μA	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V, $\lvert I_O \rvert$ < 1 μA	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V, $\lvert I_O \rvert$ < 1 μA	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.2		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Schematic Diagram

CD4073BC



TL/F/5979–3

DC Electrical Characteristics CD4073BC/CD4075BC (Note 2)

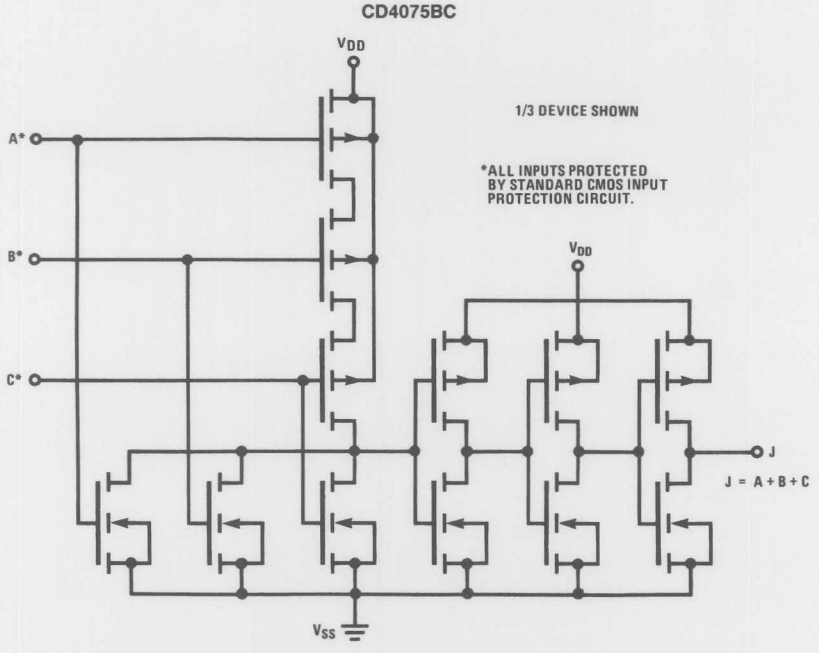
Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert$ < 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert$ < 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V, $\lvert I_O \rvert$ < 1 μA		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V, $\lvert I_O \rvert$ < 1 μA		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V, $\lvert I_O \rvert$ < 1 μA		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V, $\lvert I_O \rvert$ < 1 μA	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V, $\lvert I_O \rvert$ < 1 μA	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V, $\lvert I_O \rvert$ < 1 μA	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.2		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Schematic Diagram



TL/F/5979–4

AC Electrical Characteristics* CD4073BM/CD4073BC/CD4075BM/CD4075BC

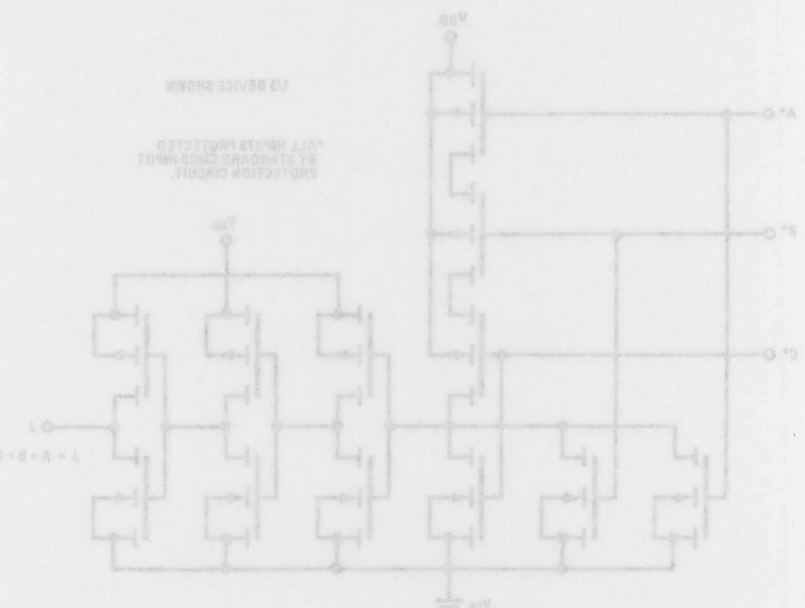
T_A = 25°C, C_L = 50 pF, R_L = 200k unless otherwise specified

Symbol	Parameter	Conditions	CD4073BC CD4073BM			CD4075BC CD4075BM			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PHL}	Propagation Delay, High to Low Level	V_{DD} = 5V		130	250		140	250	ns
		V_{DD} = 10V		60	100		70	100	ns
		V_{DD} = 15V		40	70		50	70	ns
t_{PLH}	Propagation Delay, Low to High Level	V_{DD} = 5V		140	250		130	250	ns
		V_{DD} = 10V		70	100		50	100	ns
		V_{DD} = 15V		50	70		40	70	ns
t_{THL} t_{TLH}	Transition Time	V_{DD} = 5V		90	200		90	200	ns
		V_{DD} = 10V		50	100		50	100	ns
		V_{DD} = 15V		40	80		40	80	ns
C_{IN}	Average Input Capacitance (Note 4)	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 5)	Any Gate		17			17		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.



National Semiconductor

CD4076BM/CD4076BC TRI-STATE® Quad D Flip-Flop

General Description

The CD4076BM/CD4076BC TRI-STATE quad D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. The four D type flip-flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disables allow the flip-flops to remain in their present state without disrupting the clock. If either of the two input disables is taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

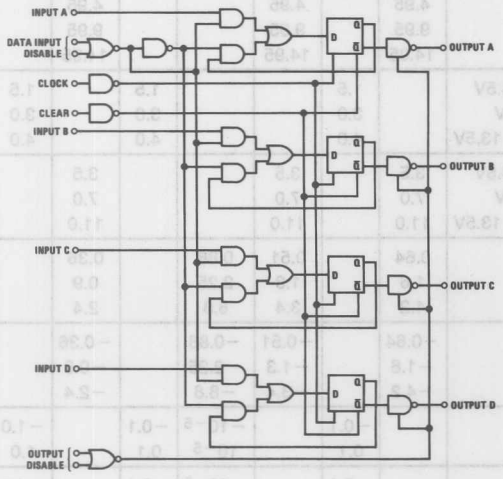
Clearing is enabled by taking the clear input to a logic "1" level. Clocking occurs on the positive-going transition.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

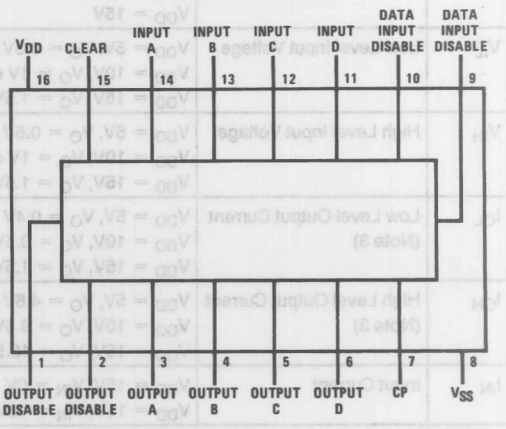
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- High impedance TRI-STATE outputs
- Inputs can be disabled without gating the clock
- Equivalent to MM54C173/MM74C173

Logic and Connection Diagrams



TL/F/5980–1

Dual-In-Line Package



TL/F/5980–2

Top View

Order Number CD4076B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

t_n		$t_n + 1$
Data Input Disable	**Data Input**	
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

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Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5V to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} + 0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	+3V to +15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4076BM	−55°C to +125°C
CD4076BC	−40°C to +85°C

DC Electrical Characteristics CD4076BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	Output Current High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4076BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	Output Current High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Clock to Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	ns
		V_{DD} = 15V		65	160	ns
t_{PHL}	Propagation Delay Time from Clear to Output	V_{DD} = 5V		240	490	ns
		V_{DD} = 10V		90	180	ns
		V_{DD} = 15V		70	145	ns
t_{SU}	Minimum Input Data Set-Up Time	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
t_H	Minimum Input Data Hold Time	V_{DD} = 5V		−40	0	ns
		V_{DD} = 10V		−12	0	ns
		V_{DD} = 15V		−10	0	ns
t_{SU}	Minimum Input Disable Set-Up Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		28	55	ns
t_H	Minimum Input Disable Hold Time	V_{DD} = 5V		−75	0	ns
		V_{DD} = 10V		−30	0	ns
		V_{DD} = 15V		−25	0	ns

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* (Continued)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, Input $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHZ}, t_{PLZ}	Propagation Delay Time from Output Disable to High Impedance State	$V_{DD} = 5V$, $R_L = 1.0k$		170	340	ns
		$V_{DD} = 10V$, $R_L = 1.0k$		70	140	ns
		$V_{DD} = 15V$, $R_L = 1.0k$		56	115	ns
	Propagation Delay from Output Disable to Logical "1" Level or Logical "0" Level (From High Impedance State)	$V_{DD} = 5V$, $R_L = 1.0k$		170	340	ns
		$V_{DD} = 10V$, $R_L = 1.0k$		70	140	ns
		$V_{DD} = 15V$, $R_L = 1.0k$		56	115	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	3.0	4.0		MHz
		$V_{DD} = 10V$	7.0	12.0		MHz
		$V_{DD} = 15V$	8.75	15.0		MHz
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5V$		150		ns
		$V_{DD} = 10V$		70		ns
		$V_{DD} = 15V$		56		ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	10			μs
		$V_{DD} = 10V$	5			μs
		$V_{DD} = 15V$	2			μs
C_{IN}	Average Input Capacitance	Data Input (A, B, C, D)		3	7.5	pF
		Other Inputs		6	15	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output			15	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

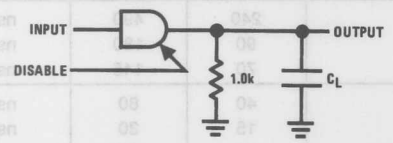
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note, AN-90.

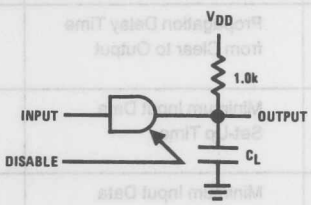
AC Test Circuits and Switching Time Waveforms

t_{PHZ} and t_{PZH}



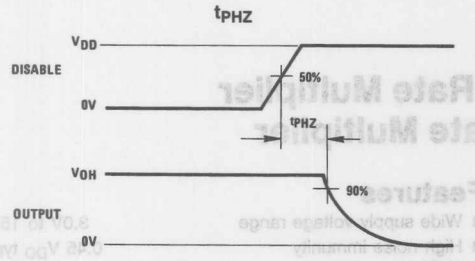
TL/F/5980–3

t_{PLZ} and t_{PZL}

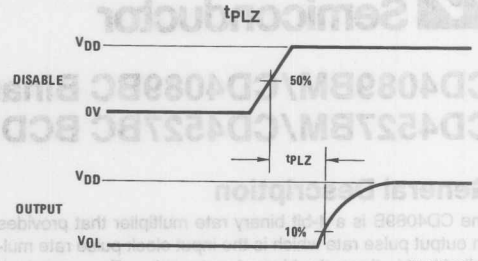


TL/F/5980–4

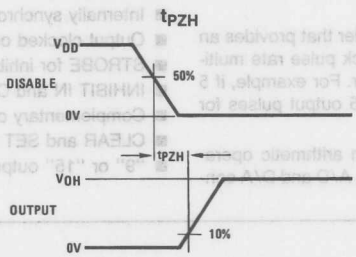
AC Test Circuits and Switching Time Waveforms (Continued)



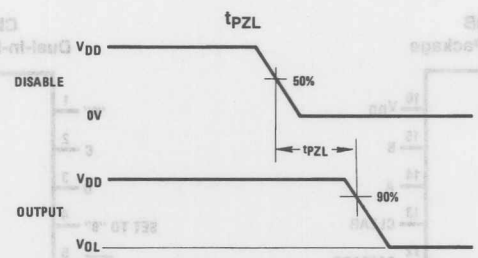
TL/F/5980–5



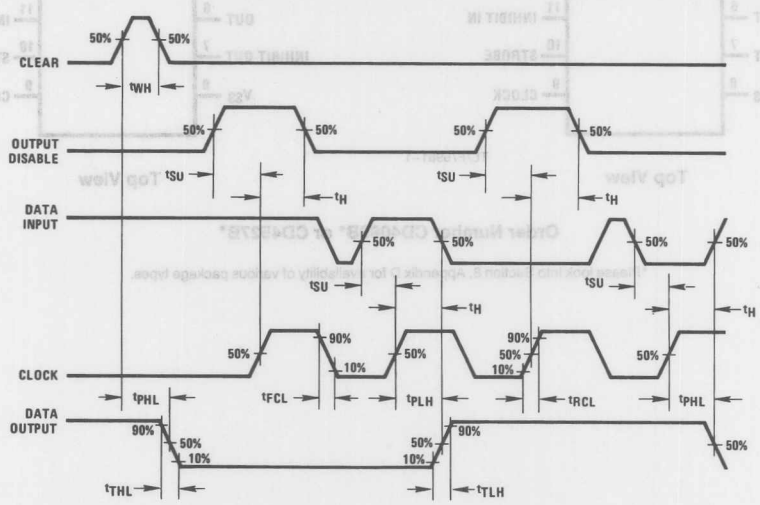
TL/F/5980–6



TL/F/5980–7



TL/F/5980–8



TL/F/5980–9

CD4089BM/CD4089BC Binary Rate Multiplier
CD4527BM/CD4527BC BCD Rate Multiplier

General Description

The CD4089B is a 4-bit binary rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $1/16$ times the binary input number. For example, if 5 is the binary input number, there will be 5 output pulses for every 16 clock pulses.

The CD4527B is a 4-bit BCD rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $1/10$ times the BCD input number. For example, if 5 is the BCD input number, there will be 5 output pulses for every 10 clock pulses.

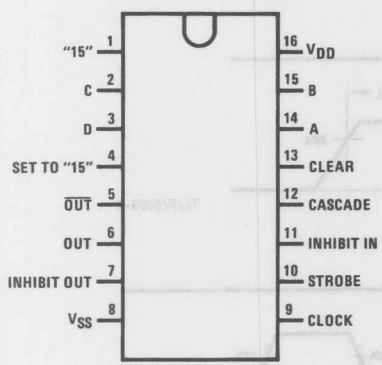
These devices may be used to perform arithmetic operations including multiplication and division, A/D and D/A conversion and frequency division.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ.
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Internally synchronous 4-bit counter
- Output clocked on the negative-going edge of clock
- STROBE for inhibiting and enabling outputs
- INHIBIT IN and CASCADE inputs for cascade operation
- Complementary output
- CLEAR and SET inputs
- "9" or "15" output and INHIBIT OUT output

Connection Diagrams

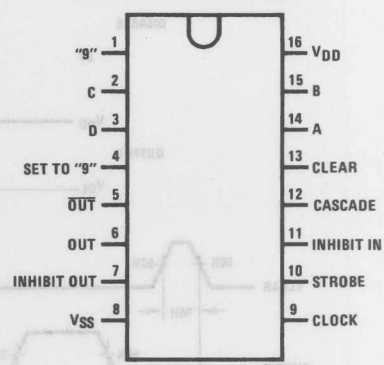
CD4089B
Dual-In-Line-Package



TL/F/5981–1

Top View

CD4527B
Dual-In-Line Package



TL/F/5981–2

Top View

Order Number CD4089B* or CD4527B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}V
Operating Temperature Range (T_A)	
CD4089BM, CD4527BM	−55°C to +125°C
CD4089BC, CD4527BC	−40°C to +85°C

DC Electrical Characteristics CD4089BM/CD4527BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 5V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 5V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4089BC/CD4527BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 5V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

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DC Electrical Characteristics CD4089BC/CD4527BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 5V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to Out or $\overline{Out}$	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		60	120	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to E_{OUT}	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		120	240	ns
		V_{DD} = 15V		75	150	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to "9" or "15"	V_{DD} = 5V		280	560	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Set or Clear to Out or $\overline{Out}$	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Cascade to Out	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Strobe to Out	V_{DD} = 5V		220	440	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		65	130	ns
t_{TLH}, t_{THL}	Transition Time, All Outputs	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
$t_{W(CL)}$	Minimum Clock Width Pulse	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	2		MHz
		V_{DD} = 10V	2.5	5		MHz
		V_{DD} = 15V	3.5	7		MHz
t_r	Maximum Clock Rise Time	V_{DD} = 5V			5	μs
		V_{DD} = 10V			1.5	μs
		V_{DD} = 15V			1.0	μs
t_f	Maximum Clock Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
$t_{W(S,R)}$	Minimum Set or Clear Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		25	55	ns

AC Electrical Characteristics* (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{REM}	Set Removal Time	V_{DD} = 5V		−45	0	ns
		V_{DD} = 10V		−20	0	ns
		V_{DD} = 15V		−10	0	ns
t_{SET-UP}	Inhibit In Set-Up Time	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		60	120	ns
		V_{DD} = 15V		45	90	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		80		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note, AN-90.

Truth Tables

CD4089B
Binary Rate Multiplier

Inputs										Number of Pulses or Output Logic Level (H or L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{Out}$	Pin 7 Inh Out	Pin 1 "15"
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
x	X	X	X	16	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

Truth Tables (Continued)

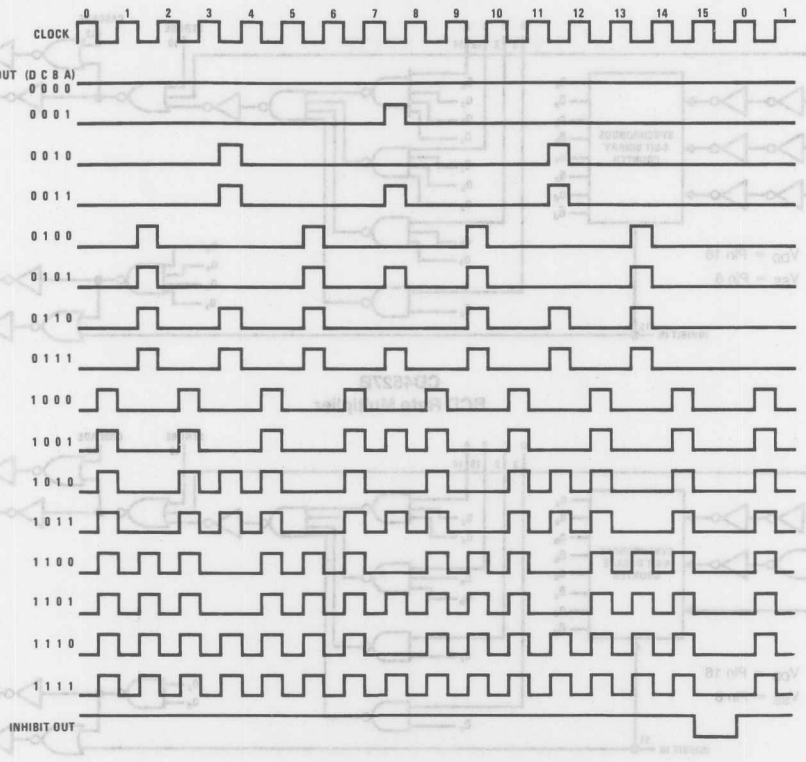
CD4527B
BCD Rate Multiplier

Inputs										Number of Pulses or Output Logic Level (H or L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{Out}$	Pin 7 Inh Out	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
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1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	1	0	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
x	X	X	X	10	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

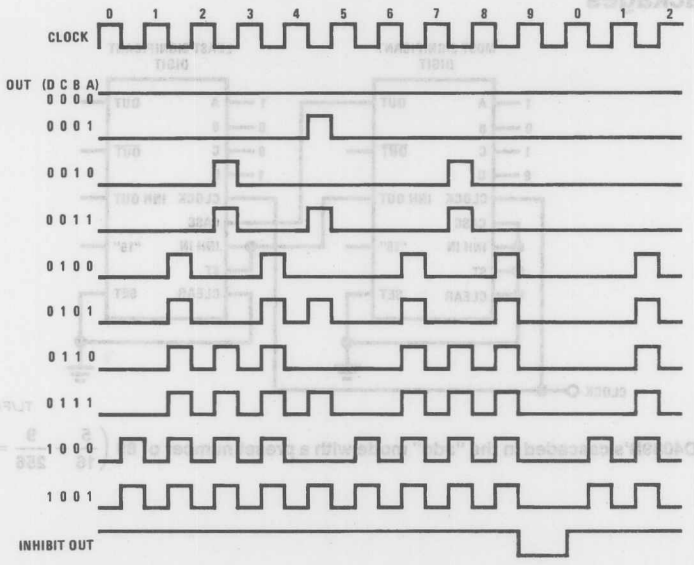
Logic Waveforms

CD4089B
Binary Rate Multiplier



TL/F/5981–3

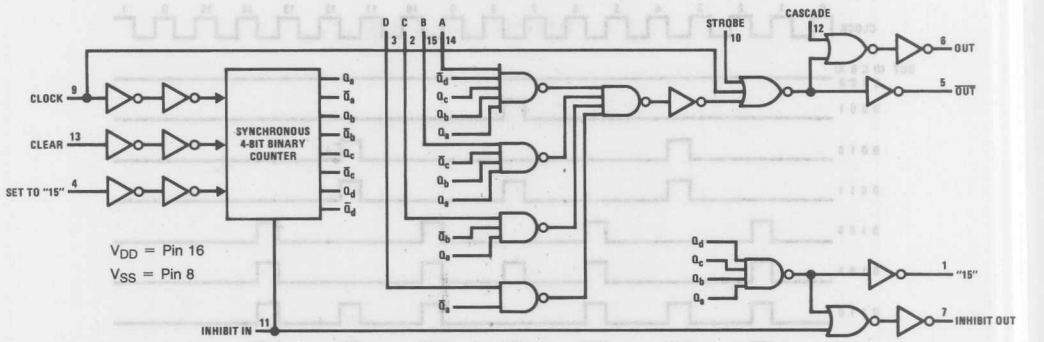
CD4527B
BCD Rate Multiplier



TL/F/5981–4

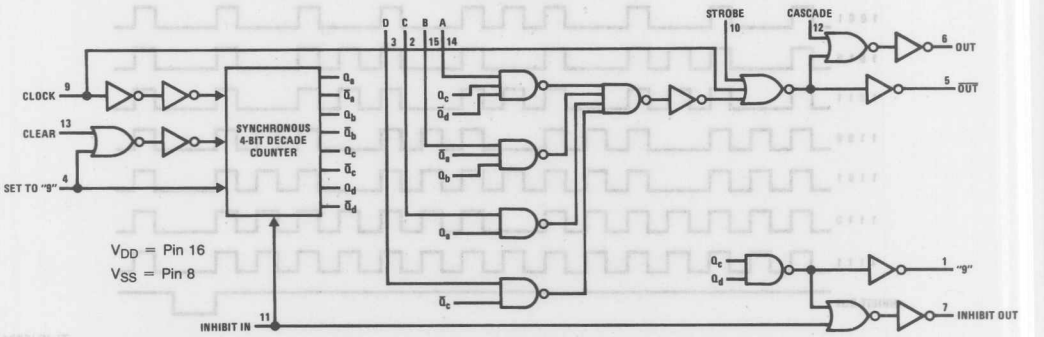
Logic Diagrams

CD4089B
Binary Rate Multiplier



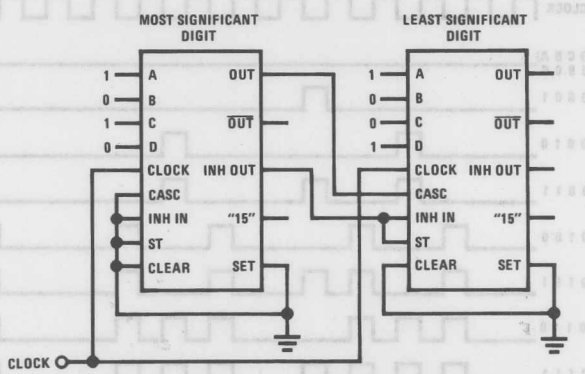
TL/F/5981–5

CD4527B
BCD Rate Multiplier



TL/F/5981–6

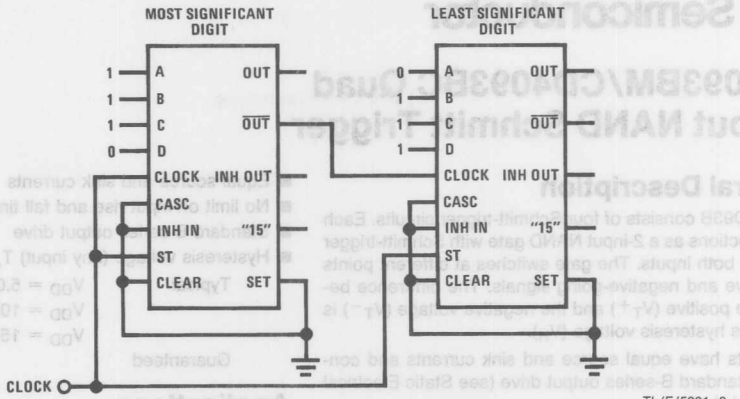
Cascading Packages



TL/F/5981–7

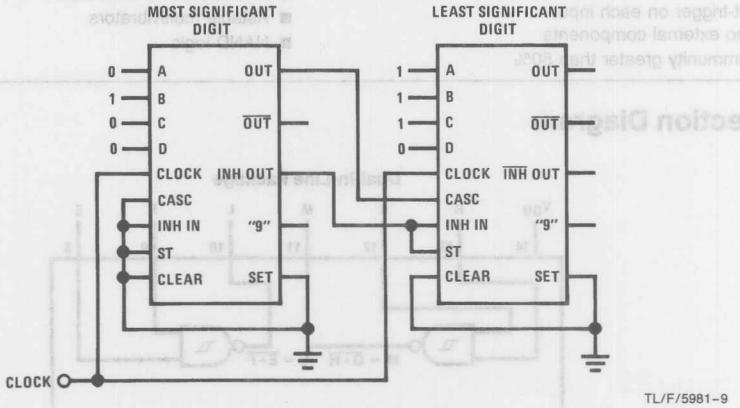
Two CD4089B's cascaded in the "add" mode with a preset number of 89 $\left(\frac{5}{16}+\frac{9}{256}=\frac{89}{256}\right)$

Cascading Packages (Continued)



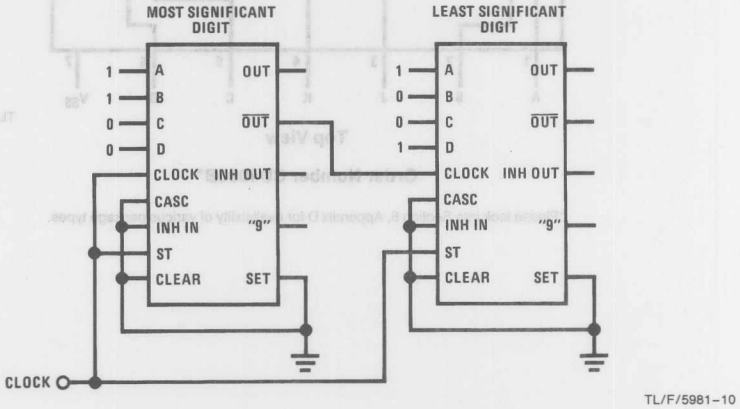
TL/F/5981–8

Two CD4089B's cascaded in the "multiply" mode with a preset number of 98 $\left(\frac{7}{16} \times \frac{14}{16} = \frac{98}{256}\right)$



TL/F/5981–9

Two CD4527B's cascaded in the "add" mode with a preset number of 27 $\left(\frac{2}{10} + \frac{7}{100} = \frac{27}{100}\right)$



TL/F/5981–10

Two CD4527B's cascaded in the "multiply" mode with a preset number of 27 $\left(\frac{3}{10} \times \frac{9}{10} = \frac{27}{100}\right)$

5

CD4093BM/CD4093BC Quad 2-Input NAND Schmitt Trigger

General Description

The CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive (V_T^+) and the negative voltage (V_T^-) is defined as hysteresis voltage (V_H).

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

Features

- Wide supply voltage range 3.0V to 15V
- Schmitt-trigger on each input with no external components
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Standard B-series output drive
- Hysteresis voltage (any input) $T_A = 25°C$

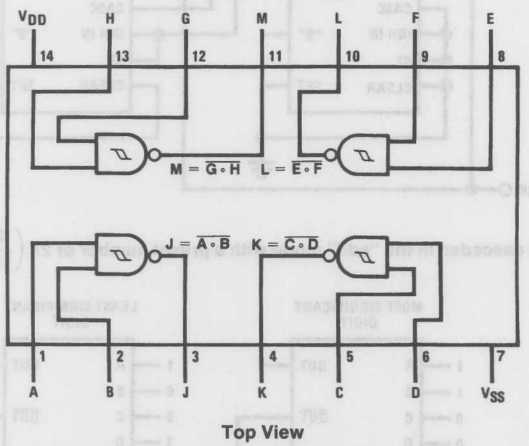
Typical	$V_{DD} = 5.0V$	$V_H = 1.5V$
	$V_{DD} = 10V$	$V_H = 2.2V$
	$V_{DD} = 15V$	$V_H = 2.7V$
Guaranteed		$V_H = 0.1\ V_{DD}$

Applications

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

Connection Diagram

Dual-In-Line Package



TL/F/5982–1

Top View

Order Number CD4093B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} $+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4093BM	$-55°C$ to $+125°C$
CD4093BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4093BM (Note 2)

Symbol	Parameter	Conditions	$-55°C$		$+25°C$			$+125°C$		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		0.25			0.25		7.5	μA
		$V_{DD} = 10V$		0.5			0.5		15.0	μA
		$V_{DD} = 15V$		1.0			1.0		30.0	μA
V_{OL}	Low Level Output Voltage	$V_{IN} = V_{DD}$, $\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IN} = V_{SS}$, $\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_T^-	Negative-Going Threshold Voltage (Any Input)	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 4.5V$	1.3	2.25	1.5	1.8	2.25	1.5	2.3	V
		$V_{DD} = 10V$, $V_O = 9V$	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		$V_{DD} = 15V$, $V_O = 13.5V$	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_T^+	Positive-Going Threshold Voltage (Any Input)	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$	2.75	3.65	2.75	3.3	3.5	2.65	3.5	V
		$V_{DD} = 10V$, $V_O = 1V$	5.5	7.15	5.5	6.2	7.0	5.35	7.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$	8.25	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_T^+ - V_T^-$) (Any Input)	$V_{DD} = 5V$	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
		$V_{DD} = 10V$	1.0	4.30	1.0	2.2	4.0	0.70	4.0	V
		$V_{DD} = 15V$	1.5	6.30	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current (Note 3)	$V_{IN} = V_{DD}$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IN} = V_{SS}$								
		$V_{DD} = 5V$, $V_O = 4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		-0.1		-10^{-5}	-0.1		-1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4093BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15.0	μA
		V_{DD} = 15V		4.0			4.0		30.0	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{SS}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_T^-	Negative-Going Threshold Voltage (Any Input)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.3	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_T^+	Positive-Going Threshold Voltage (Any Input)	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V	2.75	3.6	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	5.5	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	8.25	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_T^+ - V_T^-$) (Any Input)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
		V_{DD} = 10V	1.0	4.3	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.3	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current (Note 3)	V_{IN} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IN} = V_{SS}								
		V_{DD} = 5V, V_O = 4.6V	−0.52		0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r, t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	450	ns
		V_{DD} = 10V		120	210	ns
		V_{DD} = 15V		80	160	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		90	145	ns
		V_{DD} = 10V		50	75	ns
		V_{DD} = 15V		40	60	ns
C_{IN}	Input Capacitance	(Any Input)		5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Per Gate)		24		pF

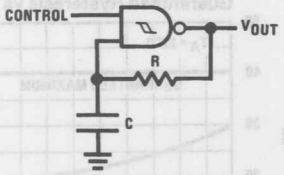
*AC Parameters are guaranteed by DC correlated testing.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Typical Applications

Gated Oscillator



TL/F/5982-2

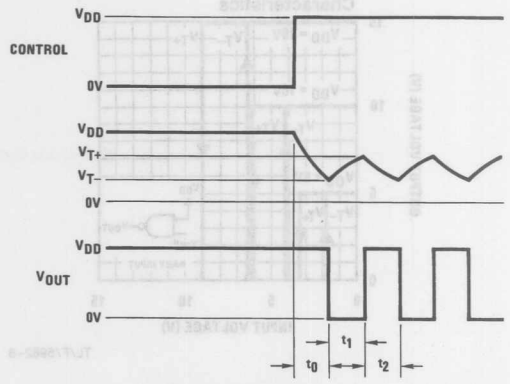
Assume $t_1 + t_2 >> t_{PHL} + t_{PLH}$ then:

$t_0 = RC\ \ell n\ [V_{DD}/V_T^-]$

$t_1 = RC\ \ell n\ [(V_{DD} - V_T^-)/(V_{DD} + V_T^+)]$

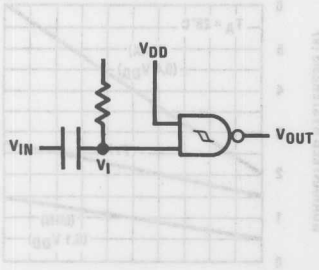
$t_2 = RC\ \ell n\ [V_T^+/V_T^-]$

$$f = \frac{1}{t_1 + t_2} = \frac{1}{RC\ \ell n \frac{(V_T^+)(V_{DD} - V_T^-)}{(V_T^-)(V_{DD} - V_T^+)}}$$

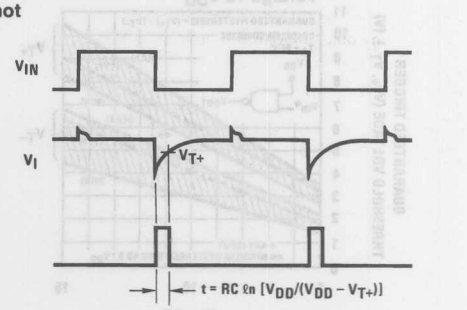


TL/F/5982-3

Gated One-Shot

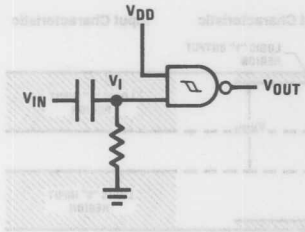


TL/F/5982-4

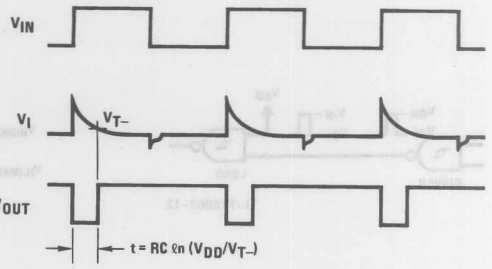


TL/F/5982-5

(a) Negative-Edge Triggered



TL/F/5982-6

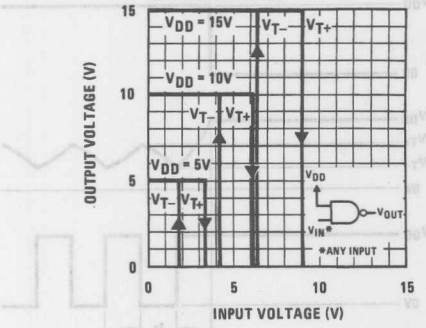


TL/F/5982-7

(b) Positive-Edge Triggered

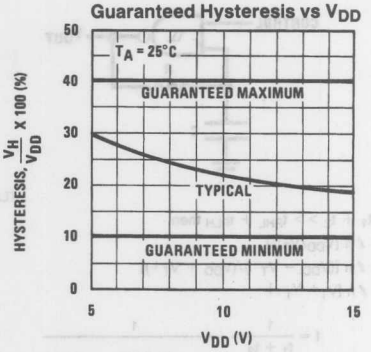
Typical Performance Characteristics

Typical Transfer Characteristics



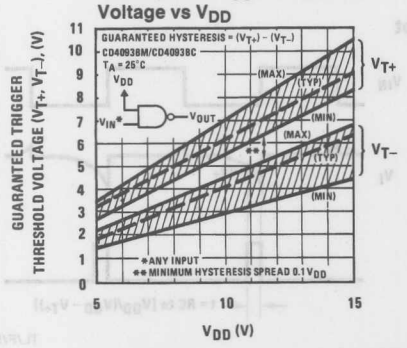
TL/F/5982-8

Guaranteed Hysteresis vs V_{DD}



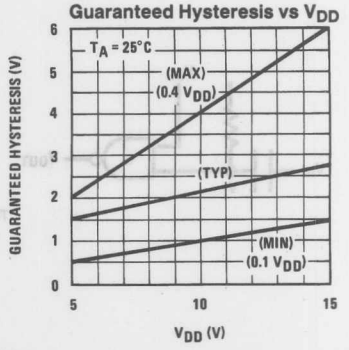
TL/F/5982-9

Guaranteed Trigger Threshold Voltage vs V_{DD}



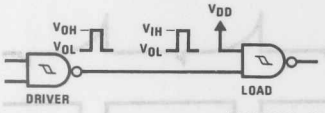
TL/F/5982-10

Guaranteed Hysteresis vs V_{DD}

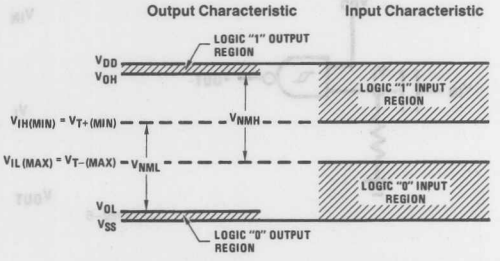


TL/F/5982-11

Input and Output Characteristics



TL/F/5982-12

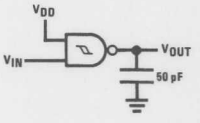


TL/F/5982-13

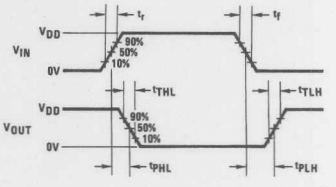
$$V_{NML} = V_{IH(MIN)} - V_{OL} \cong V_{IH(MIN)} = V_{T^+(MIN)}$$

$$V_{NMH} = V_{OH} - V_{IL(MAX)} \cong V_{DD} - V_{IL(MAX)} = V_{DD} - V_{T^-(MAX)}$$

AC Test Circuits and Switching Time Waveforms



TL/F/5982-14



TL/F/5982-15

National Semiconductor

CD4094BM/CD4094BC 8-Bit Shift Register/Latch with TRI-STATE® Outputs

General Description

The CD4094BM/CD4094BC consists of an 8-bit shift register and a TRI-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_S) can be used to cascade several devices. Data on the Q_S output is transferred to a second output, Q'_S, on the following negative clock edge.

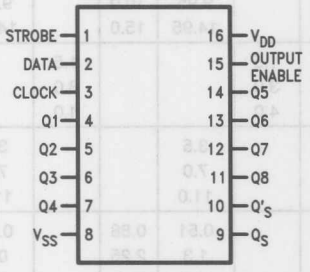
The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is high, data propagates through the latch to TRI-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken high.

Features

■ Wide supply voltage range	3.0V to 18V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ TRI-STATE outputs	

Connection Diagram

Dual-In-Line Package



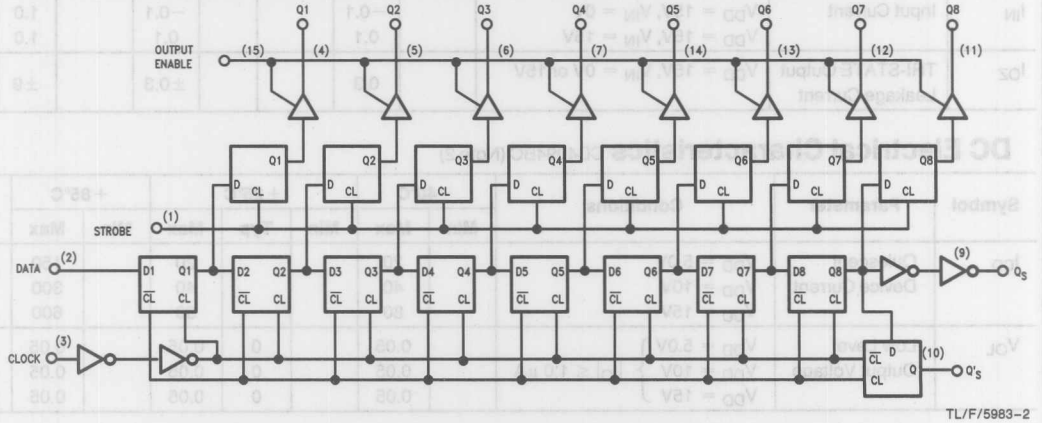
TL/F/5983–1

Top View

Order Number CD4094B*

*Please look into Section 8, Appendix D for availability of various package types.

Block or Logic Diagram



TL/F/5983–2

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} $+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	$+3.0$ to $+15$ V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4094BM	$-55°C$ to $+125°C$
CD4094BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4094BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5.0V$		5.0			5.0		150	μA
		$V_{DD} = 10V$		10			10		300	μA
		$V_{DD} = 15V$		20			20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5.0V$ | $\|I_O\| \leq 1.0$ μA		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ | $\|I_O\| \leq 1.0$ μA		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ | $\|I_O\| \leq 1.0$ μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5.0V$ | $\|I_O\| \leq 1$ μA	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$ | $\|I_O\| \leq 1$ μA	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$ | $\|I_O\| \leq 1$ μA	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5.0V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5.0V$, $V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5.0V$, $V_O = 4.6V$	−0.64		−0.51	0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.6		−1.3	2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−4.2		−3.4	8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1			−0.1		1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1			0.1		1.0	μA
I_{OZ}	TRI-STATE Output Leakage Current	$V_{DD} = 15V$, $V_{IN} = 0V$ or $15V$		0.3			±0.3		±9	μA

DC Electrical Characteristics CD4094BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5.0V$		20			20		150	μA
		$V_{DD} = 10V$		40			40		300	μA
		$V_{DD} = 15V$		80			80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5.0V$ | $\|I_O\| \leq 1.0$ μA		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ | $\|I_O\| \leq 1.0$ μA		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ | $\|I_O\| \leq 1.0$ μA		0.05		0	0.05		0.05	V

DC Electrical Characteristics CD4094BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{OH}	High Level Output Voltage	V_{DD} = 5.0V, $\lvert I_O \rvert \le 1\ \mu A$	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert \le 1\ \mu A$	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert \le 1\ \mu A$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0V, V_O = 4.6V	−0.52		−0.44	0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3			−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3			0.3		1.0	μA
I_{OZ}	TRI-STATE Output Leakage Current	V_{DD} = 15V, V_{IN} = 0V or 15V		1			1		10	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q_S	V_{DD} = 5.0V		300	600	ns
		V_{DD} = 10V		125	250	ns
		V_{DD} = 15V		95	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q'_S	V_{DD} = 5.0V		230	460	ns
		V_{DD} = 10V		110	220	ns
		V_{DD} = 15V		75	150	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Parallel Out	V_{DD} = 5.0V		420	840	ns
		V_{DD} = 10V		195	390	ns
		V_{DD} = 15V		135	270	ns
t_{PHL}, t_{PLH}	Propagation Delay Strobe to Parallel Out	V_{DD} = 5.0V		290	580	ns
		V_{DD} = 10V		145	290	ns
		V_{DD} = 15V		100	200	ns
t_{PHZ}	Propagation Delay High Level to High Impedance	V_{DD} = 5.0V		140	280	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		55	110	ns
t_{PLZ}	Propagation Delay Low Level to High Impedance	V_{DD} = 5.0V		140	280	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		55	110	ns
t_{PZH}	Propagation Delay High Impedance to High Level	V_{DD} = 5.0V		140	280	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		55	110	ns
t_{PZL}	Propagation Delay High Impedance to Low Level	V_{DD} = 5.0V		140	280	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		55	110	ns

*AC Parameters are guaranteed by DC correlated testing.

t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5.0V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{SU}	Set-Up Time Data to Clock	V_{DD} = 5.0V	80	40		ns
		V_{DD} = 10V	40	20		ns
		V_{DD} = 15V	20	10		ns
t_r, t_f	Maximum Clock Rise and Fall Time	V_{DD} = 5.0V	1			ms
		V_{DD} = 10V	1			ms
		V_{DD} = 15V	1			ms
t_{PC}	Minimum Clock Pulse Width	V_{DD} = 5.0V	200	100		ns
		V_{DD} = 10V	100	50		ns
		V_{DD} = 15V	83	40		ns
t_{PS}	Minimum Strobe Pulse Width	V_{DD} = 5.0V	200	100		ns
		V_{DD} = 10V	80	40		ns
		V_{DD} = 15V	70	35		ns
f_{MAX}	Maximum Clock Frequency	V_{DD} = 5.0V	1.5	3.0		MHz
		V_{DD} = 10V	3.0	6.0		MHz
		V_{DD} = 15V	4.0	8.0		MHz
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

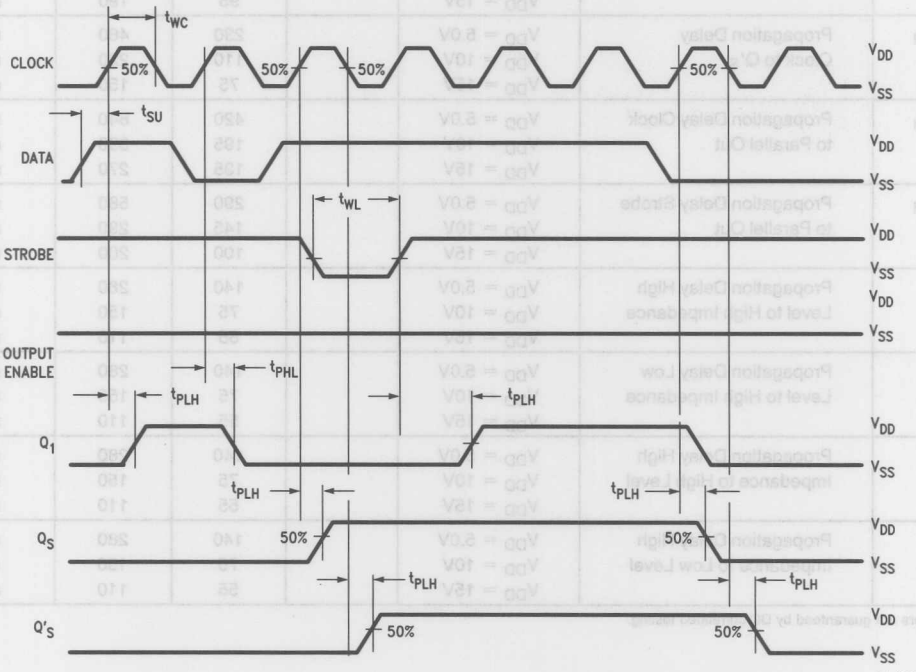
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

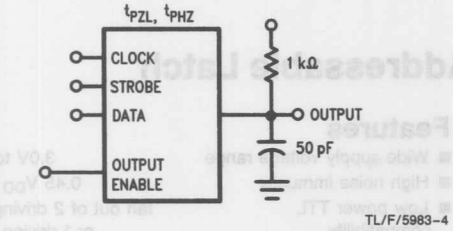
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

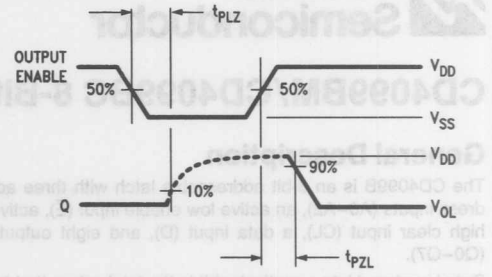
Timing Diagram



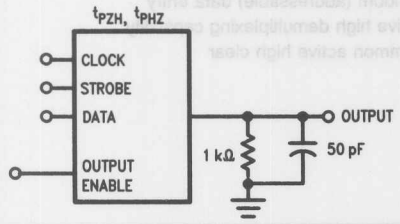
Test Circuits and Timing Diagrams for TRI-STATE



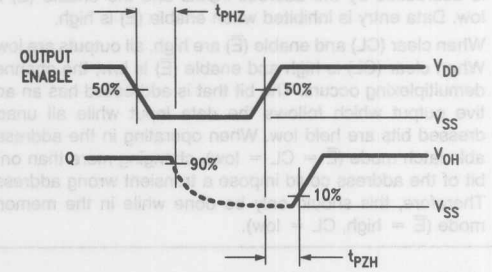
TL/F/5983–4



TL/F/5983–5



TL/F/5983–6



TL/F/5983–7

Logic Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S*	Q's
⎍	0	X	X	Hi-Z	Hi-Z	Q7	No Chg.
⎎	0	X	X	Hi-Z	Hi-Z	No Chg.	Q7
⎍	1	0	X	No Chg.	No Chg.	Q7	No Chg.
⎍	1	1	0	0	Q_N-1	Q7	No Chg.
⎍	1	1	1	1	Q_N-1	Q7	No Chg.
⎎	1	1	1	No Chg.	No Chg.	No Chg.	Q7

X = Don't Care

*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

National Semiconductor

CD4099BM/CD4099BC 8-Bit Addressable Latch

General Description

The CD4099B is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D), and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

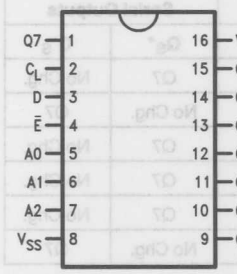
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high and enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Connection Diagram

CD4099B
Dual-In-Line Package



TL/F/5984–1

Top View

Order Number CD4099B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Mode Selection				
$\overline{E}$	CL	Addressed Latch	Unaddressed Latch	Mode
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3.0 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4099BM	−55°C to +125°C
CD4099BC	−40°C to +85°C

DC Electrical Characteristics CD4099BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5.0		0.02	5.0		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.02	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4099BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.02	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V

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	Current (Note 3)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
t_{TLH}, t_{THL}	Propagation Delay Address to Output	V_{DD} = 5V		225	450	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
T_{WH}, T_{WL}	Minimum Data Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		65	125	ns
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		75	150	ns
		V_{DD} = 10V		40	75	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Set-Up Time Data to E	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		20	40	ns
		V_{DD} = 15V		15	30	ns
t_H	Minimum Hold Time Data to E	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Set-Up Time Address to E	V_{DD} = 5V		−15	50	ns
		V_{DD} = 10V		0	30	ns
		V_{DD} = 15V		0	20	ns
t_H	Minimum Hold Time Address to E	V_{DD} = 5V		−50	15	ns
		V_{DD} = 10V		−20	10	ns
		V_{DD} = 15V		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

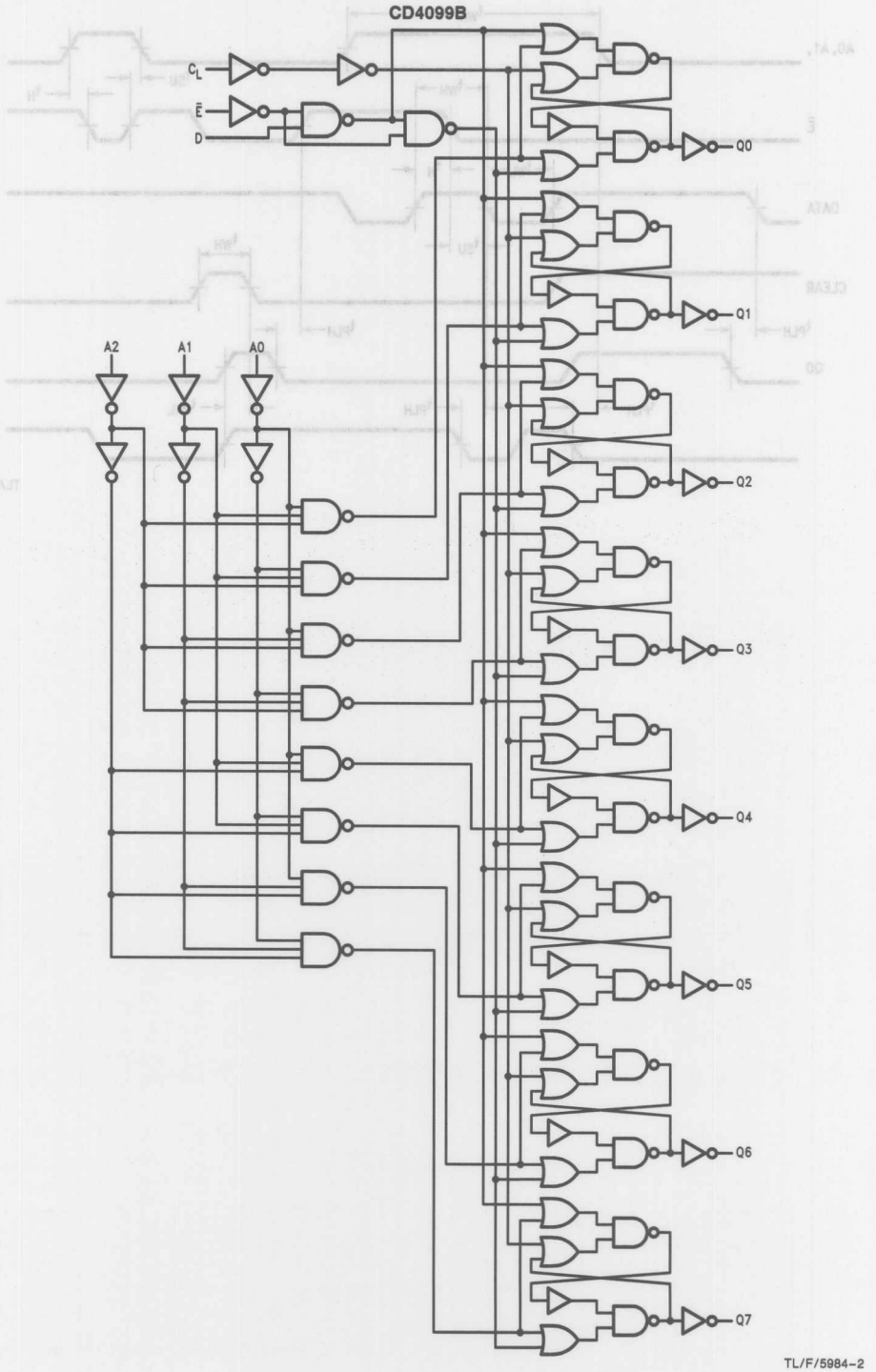
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Condtions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

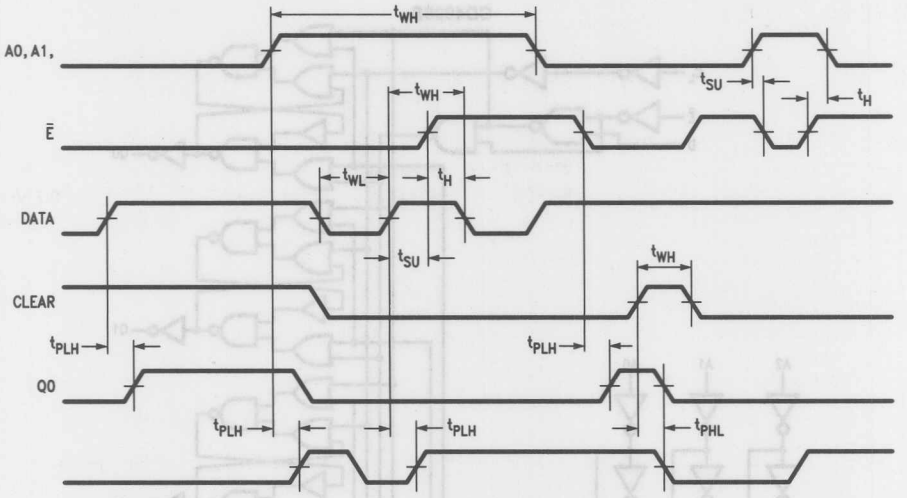
Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{CC}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

Logic Diagram



TL/F/5984–2

Switching Time Waveforms



TL/F/5984–3

National Semiconductor

CD40106BM/CD40106BC Hex Schmitt Trigger

General Description

The CD40106B Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{DD} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{DD}$ is guaranteed.

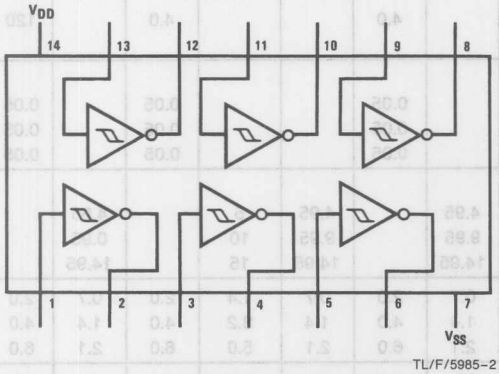
All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.7 V_{DD} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L or 1 driving 74LS
■ Hysteresis	0.4 V_{DD} (typ.) 0.2 V_{DD} guaranteed
■ Equivalent to MM54C14/MM74C14	
■ Equivalent to MC14584B	

Connection Diagram

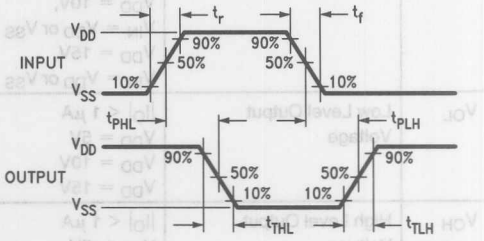
Dual-In-Line Package



TL/F/5985–2

Top View

Switching Time Waveforms



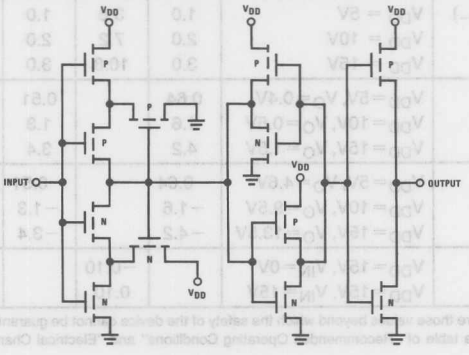
TL/F/5985–3

$t_r = t_f = 20$ ns

Order Number CD40106B*

*Please look into Section 8, Appendix D for availability of various package types.

Schematic Diagram



TL/F/5985–1

Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD}+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD40106BM	$-55°C$ to $+125°C$
CD40106BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD40106BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		0.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	V_{DD}=5V, V_O= 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		V_{DD}=10V, V_O= 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD}=15V, V_O= 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	V_{DD}=5V, V_O= 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		V_{DD}=10V, V_O= 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD}=15V, V_O= 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current (Note 3)	V_{DD}=5V, V_O=0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD}=10V, V_O=0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD}=15V, V_O=1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD}=5V, V_O=4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD}=10V, V_O=9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD}=15V, V_O=13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD}=15V, V_{IN}=0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD}=15V, V_{IN}=15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD40106BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4.0			4.0		30	μA
		V_{DD} = 10V		8.0			8.0		60	μA
		V_{DD} = 15V		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		0.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	V_{DD} = 5V, V_O = 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		V_{DD} = 10V, V_O = 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD} = 15V, V_O = 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	V_{DD} = 5V, V_O = 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		V_{DD} = 10V, V_O = 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD} = 15V, V_O = 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$) Voltage	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Input to Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	ns
		V_{DD} = 15V		70	160	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate (Note 4)		14		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

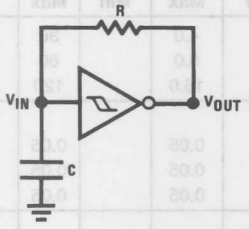
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

Typical Applications

Low Power Oscillator



$$t_1 \approx RC \ell n \frac{V_{T+}}{V_{T-}}$$

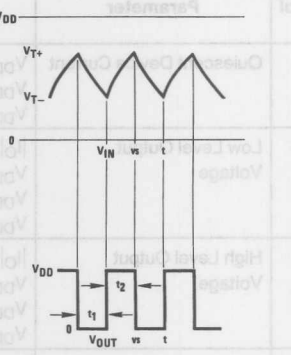
$$t_2 \approx RC \ell n \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

$$f \approx \frac{1}{RC \ell n \frac{V_{T+}(V_{DD} - V_{T-})}{V_{T-}(V_{DD} - V_{T+})}}$$

Note: The equations assume

$t_1 + t_2 >> t_{PHL} + t_{PLH}$

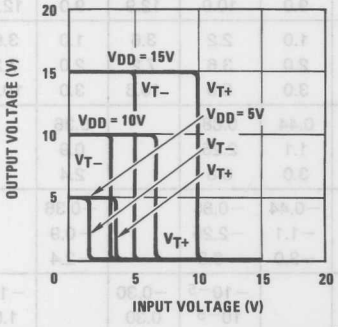
TL/F/5985–4



TL/F/5985–5

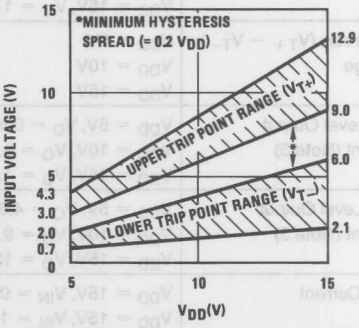
Typical Performance Characteristics

Typical Transfer Characteristics

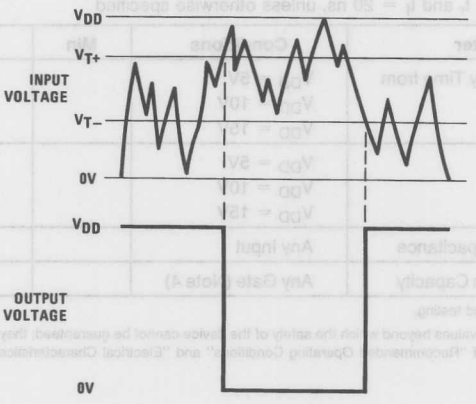


TL/F/5985–6

Guaranteed Trip Point Range



TL/F/5985–7



TL/F/5985–8

National Semiconductor

CD40160BM/CD40160BC Decade Counter with Asynchronous Clear
CD40161BM/CD40161BC Binary Counter with Asynchronous Clear
CD40162BM/CD40162BC Decade Counter with Synchronous Clear
CD40163BM/CD40163BC Binary Counter with Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the CD40162B and CD40163B is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the CD40160B and CD40161B is asynchronous and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

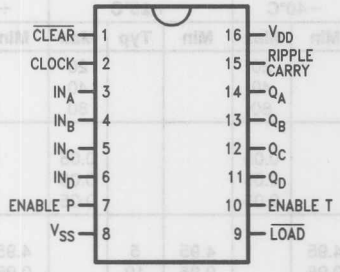
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable
- Equivalent to MC14160B, MC14161B, MC14162B, MC14163B
- Equivalent to MM74C160, MM74C161, MM74C162, MM74C163

Connection Diagram

Dual-In-Line Package



TL/F/5986–1

Top View

Order Number CD40160B*, CD40161B*, CD40162B* or CD40163B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD}+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD40XXXBM	$-55°C$ to $+125°C$
CD40XXXBC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD40160BM/CD40161BM/CD40162BM/CD40163BM (Note 2)

Symbol	Parameter	Conditions	Limits							Units
			$-55°C$		$+25°C$			$+125°C$		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5			1.5		1.5	V
		$V_{DD}=10V$, $V_O=1V$ or 9V		3.0			3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V	3.5		3.5			3.5		V
		$V_{DD}=10V$, $V_O=1V$ or 9V	7.0		7.0			7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	-0.64		-0.51	-0.88		-0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	-1.6		-1.3	-2.25		-0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	-4.2		-3.4	-8.8		-2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		-0.10		-10^{-5}	-0.10		-1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2)

Symbol	Parameter	Conditions	Limits							Units
			$-40°C$		$+25°C$			$+85°C$		
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		0.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5			1.5		1.5	V
		$V_{DD}=10V$, $V_O=1V$ or 9V		3.0			3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2) (Continued)

Symbol	Parameter	Conditions	Limits							Units
			−40°C		+25°C			+85°C		
			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Clock to Q	V_{DD} = 5V		250	400	ns
		V_{DD} = 10V		100	160	ns
		V_{DD} = 15V		80	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Clock to Carry Out	V_{DD} = 5V		290	450	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		100	160	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from T Enable to Carry Out	V_{DD} = 5V		180	290	ns
		V_{DD} = 10V		70	130	ns
		V_{DD} = 15V		60	110	ns
t_{PHL}	Propagation Time from Clear to Q (CD40160B, CD40161B Only)	V_{DD} = 5V		190	300	ns
		V_{DD} = 10V		80	150	ns
		V_{DD} = 15V		70	120	ns
t_{SU}	Minimum Time Prior to Clock that Data or Load must be Present	V_{DD} = 5V		120		ns
		V_{DD} = 10V		30		ns
		V_{DD} = 15V		25		ns
t_{SU}	Minimum Time Prior to Clock that Enable P or T must be Present	V_{DD} = 5V		170	280	ns
		V_{DD} = 10V		70	120	ns
		V_{DD} = 15V		60	100	ns
t_{SU}	Minimum Time Prior to Clock that Clear must be Present (CD40162B, CD40163B Only)	V_{DD} = 5V		120	190	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	70	ns
t_{WL} or t_{WH}	Maximum Clock Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	70	ns
t_{RCL} or t_{FCL}	Maximum Clock Rise or Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			5.0	μs
		V_{DD} = 15V			5.0	μs
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2	4		MHz
		V_{DD} = 10V	5.5	11		MHz
		V_{DD} = 15V	7	14		MHz
t_{THL} or t_{TLH}	Transition Time	All Outputs				
		V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		95		pF

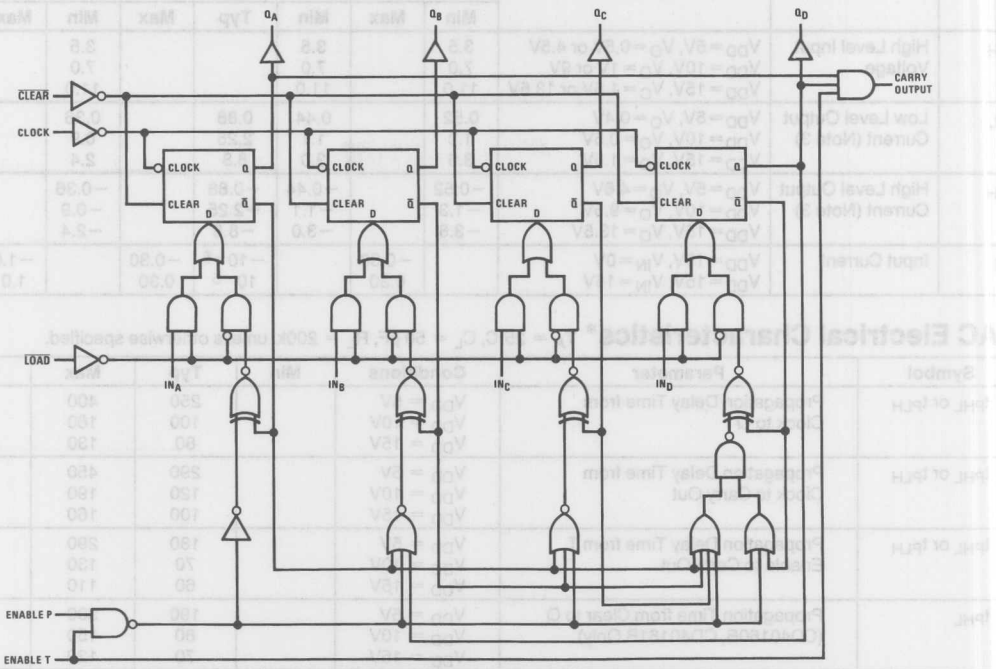
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

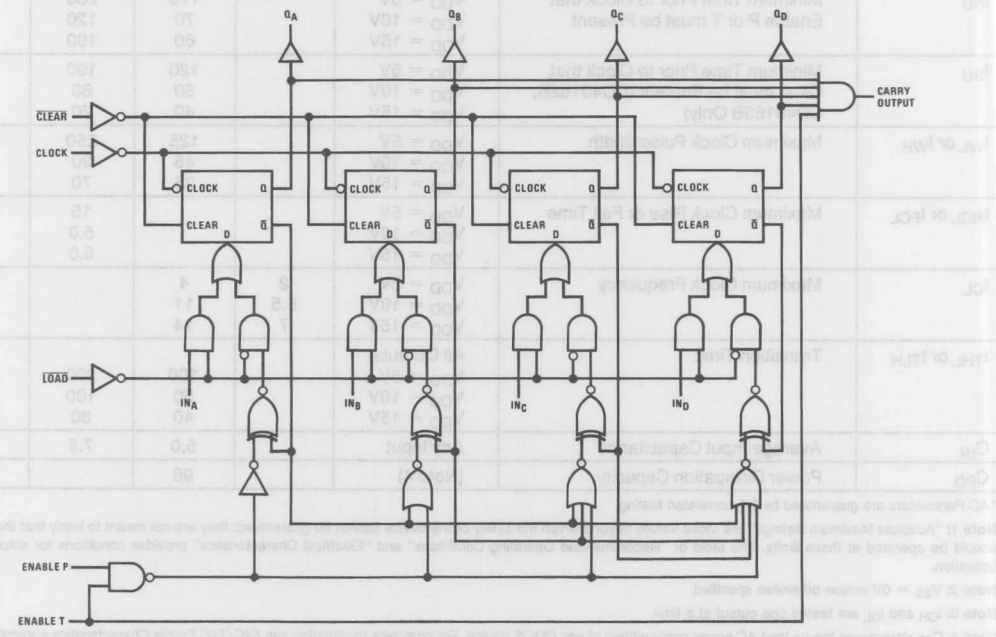
Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.



TL/F/5986–2

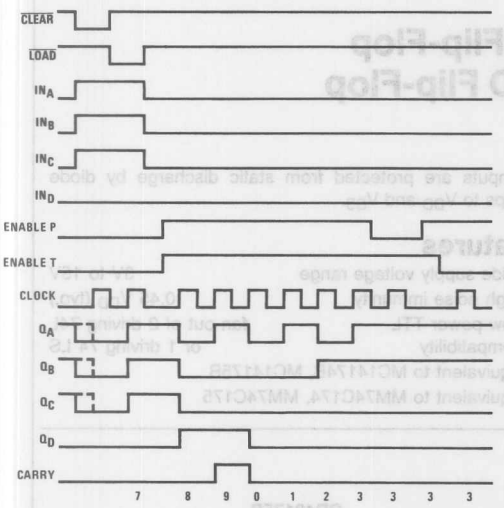
CD40161B, CD40163B Clear is Synchronous for the CD40163B



TL/F/5986–3

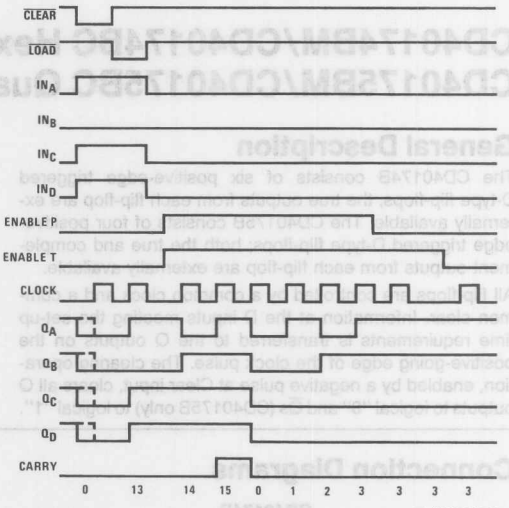
Logic Waveforms

CD40160B, . . . CD40162B Decade Counters



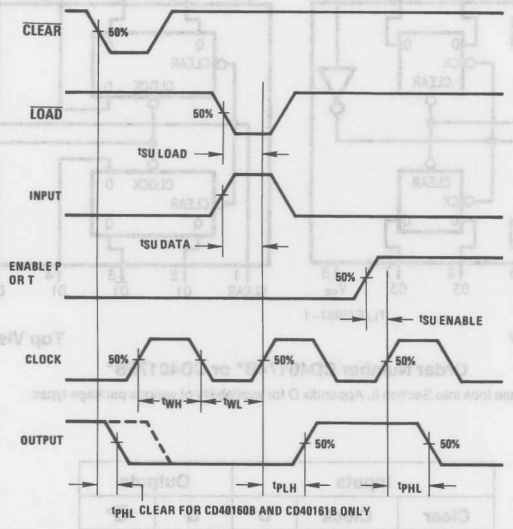
TL/F/5986–4

CD40161B, . . . CD40163B Binary Counters



TL/F/5986–5

Switching Time Waveforms

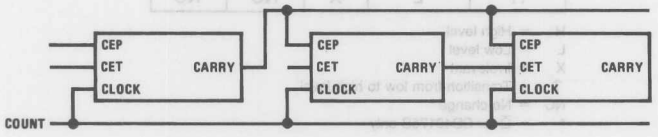


TL/F/5986–6

Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20$ ns, PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages



TL/F/5986–7

National Semiconductor

CD40174BM/CD40174BC Hex D Flip-Flop
CD40175BM/CD40175BC Quad D Flip-Flop

General Description

The CD40174B consists of six positive-edge triggered D-type flip-flops; the true outputs from each flip-flop are externally available. The CD40175B consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available.

All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0" and $\overline{Q}$s (CD40175B only) to logical "1".

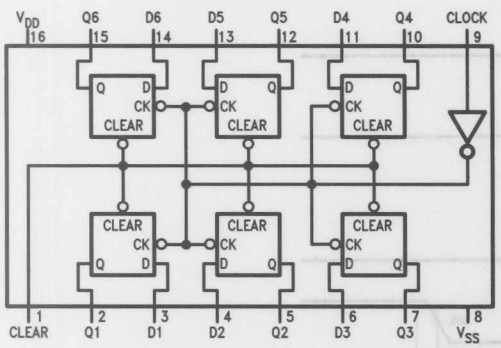
All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74 LS
- Equivalent to MC14174B, MC14175B
- Equivalent to MM74C174, MM74C175

Connection Diagrams

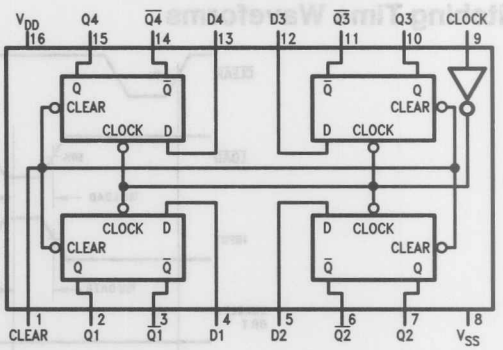
CD40174B
Dual-In-Line Package



TL/F/5987–1

Top View

CD40175B
Dual-In-Line Package



TL/F/5987–2

Top View

Order Number CD40174B* or CD40175B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change
* = $\overline{Q}$ for CD40175B only

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15 V_{DC}
Input Voltage (V_{IN})	0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD40XXXBM	−55°C to +125°C
CD40XXXBC	−40°C to +85°C

DC Electrical Characteristics CD40174BM/CD40175BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.8.8		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD40174BC/CD40175BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

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V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k and $t_r = t_f$ = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$ (CD40175 Only)	V_{DD} = 5V		190	300	ns
		V_{DD} = 10V		75	110	ns
		V_{DD} = 15V		60	90	ns
t_{PHL}	Propagation Delay Time to a Logical "0" from Clear to Q	V_{DD} = 5V		180	300	ns
		V_{DD} = 10V		70	110	ns
		V_{DD} = 15V		60	90	ns
t_{PLH}	Propagation Delay Time to a Logical "1" from Clear to $\overline{Q}$ (CD40175 Only)	V_{DD} = 5V		230	400	ns
		V_{DD} = 10V		90	150	ns
		V_{DD} = 15V		75	120	ns
t_{SU}	Time Prior to Clock Pulse that Data must be Present	V_{DD} = 5V		45	100	ns
		V_{DD} = 10V		15	40	ns
		V_{DD} = 15V		13	35	ns
t_H	Time after Clock Pulse that Data Must be Held	V_{DD} = 5V		−11	0	ns
		V_{DD} = 10V		−4	0	ns
		V_{DD} = 15V		−3	0	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH}, t_{WL}	Minimum Clock Pulse Width	V_{DD} = 5V		130	250	ns
		V_{DD} = 10V		45	100	ns
		V_{DD} = 15V		40	80	ns

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k and $t_r = t_f$ = 20 ns, unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{WL}	Minimum Clear Pulse Width	V_{DD} = 5V		120	250	ns
		V_{DD} = 10V		45	100	ns
		V_{DD} = 15V		40	80	ns
t_{RCL}	Maximum Clock Rise Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	5.0			μs
		V_{DD} = 15V	5.0			μs
t_{fCL}	Maximum Clock Fall Time	V_{DD} = 5V	15	50		μs
		V_{DD} = 10V	5.0	50		μs
		V_{DD} = 15V	5.0	50		μs
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2.0	3.5		MHz
		V_{DD} = 10V	5.0	10		MHz
		V_{DD} = 15V	6.0	12		MHz
C_{IN}	Input Capacitance	Clear Input		10	15	pF
		Other Input		5.0	7.5	pF
C_{PD}	Power Dissipation	Per Package (Note 4)		130		pF

*AC Parameters are guaranteed by DC correlated testing.

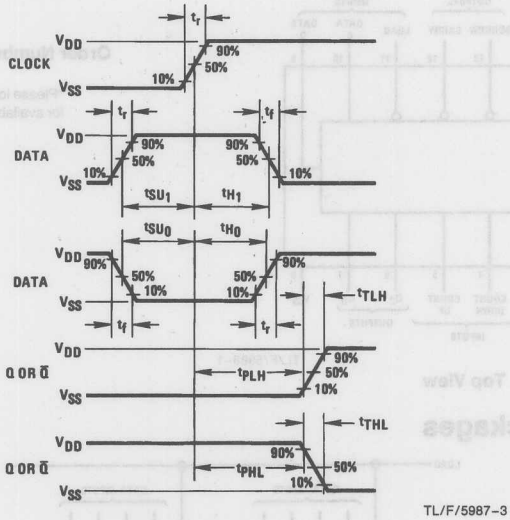
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Switching Time Waveforms



TL/F/5987–3

$t_r = t_f$ = 20 ns

National Semiconductor

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The CD40192BM and CD40192BC are BCD counters, while the CD40193BM and CD40193BC are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

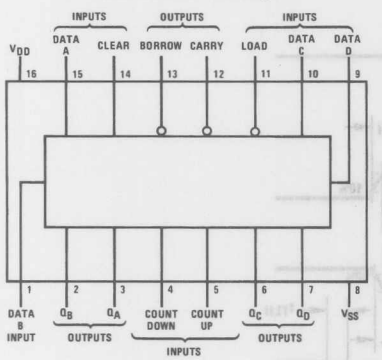
All inputs are protected against damage due to static discharge by clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Carry and borrow outputs for easy expansion to N-bit by cascading
- Asynchronous clear
- Equivalent to — MM54C192/MM74C192 and MM54C193/MM74C193

Connection Diagram

Dual-In-Line Package



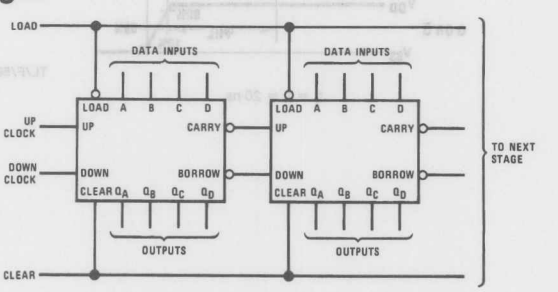
TL/F/5988–1

Top View

Order Number CD40192B* or CD40193*

*Please look into Section 8, Appendix D for availability of various package types.

Cascading Packages



TL/F/5988–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} $+0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD40192BM, CD40193BM	$-55°C$ to $+125°C$
CD40192BC, CD40193BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD40192BM/CD40193BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD40192BC/CD40193BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics CD40192BC/CD40193BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, input t_r = t_f = 20 ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} or t_{PLH}	Propagation Delay Time from Count Up or Count Down to Q	V_{DD} = 5V		250	400	ns
		V_{DD} = 10V		100	160	ns
		V_{DD} = 15V		80	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Count Up to Carry	V_{DD} = 5V		120	200	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	65	ns
t_{PHL} or t_{PLH}	Propagation Delay Time from Count Down to Borrow	V_{DD} = 5V		120	200	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	65	ns
t_{SU}	Time Prior to Load That Data Must Be Present	V_{DD} = 5V		100	160	ns
		V_{DD} = 10V		30	50	ns
		V_{DD} = 15V		25	40	ns
t_{PHL}	Propagation Delay Time from Clear to Q	V_{DD} = 5V		130	220	ns
		V_{DD} = 10V		60	100	ns
		V_{DD} = 15V		50	80	ns
t_{PLH} or t_{PHL}	Propagation Delay Time from Load to Q	V_{DD} = 5V		300	480	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		95	150	ns
t_{TLH} or t_{THL}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Count Frequency	V_{DD} = 5V	2.5	4		MHz
		V_{DD} = 10V	6	10		MHz
		V_{DD} = 15V	7.5	12.5		MHz
t_{rCL} or t_{fCL}	Maximum Count Rise or Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	5			μs
		V_{DD} = 15V	1			μs
t_{WH}, t_{WL}	Minimum Count Pulse Width	V_{DD} = 5V		120	200	ns
		V_{DD} = 10V		35	80	ns
		V_{DD} = 15V		28	65	ns
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		300	480	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		95	150	ns
t_{WL}	Minimum Load Pulse Width	V_{DD} = 5V		100	160	ns
		V_{DD} = 10V		40	65	ns
		V_{DD} = 15V		32	55	ns
C_{IN}	Average Input Capacitance	Load and Data Inputs (A,B,C,D)		5	7.5	pF
		Count Up, Count Down and Clear		10	15	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

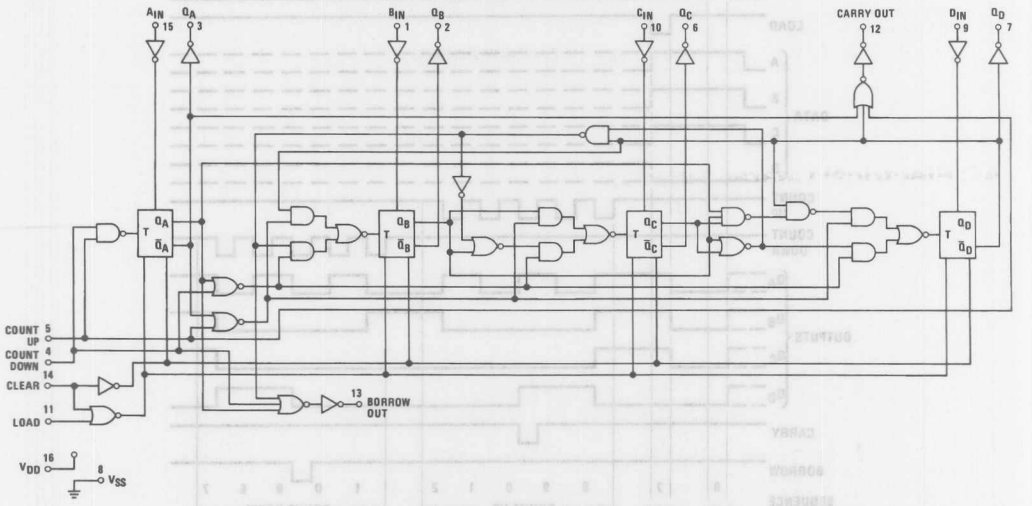
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

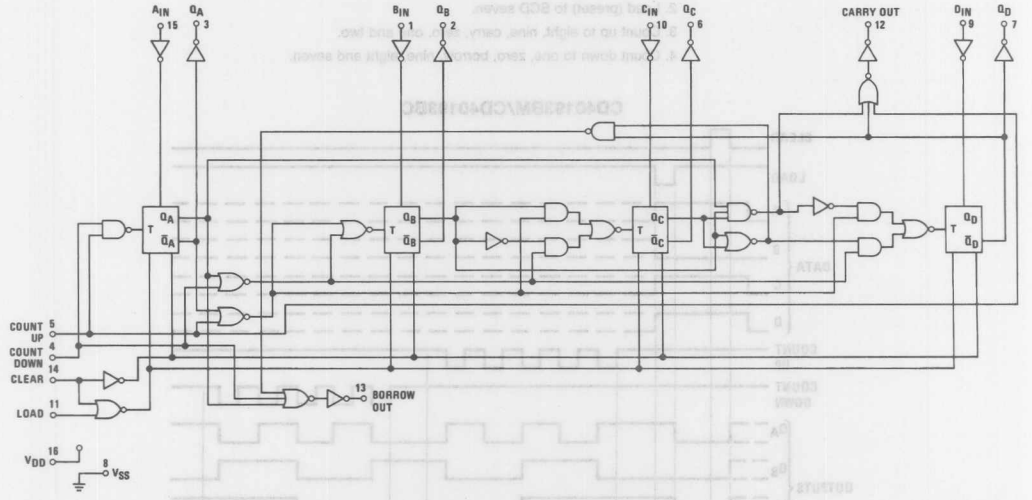
Schematic Diagrams

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter



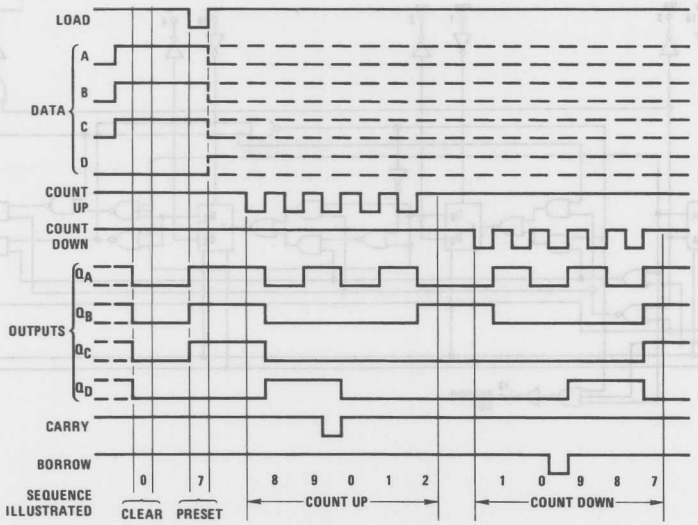
TL/F/5988–3

CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter



TL/F/5988–4

5

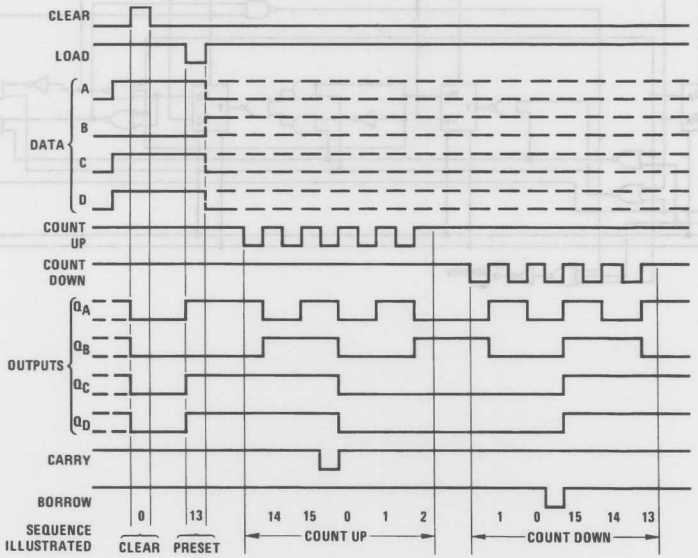


TL/F/5988–5

Sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.

CD40193BM/CD40193BC



TL/F/5988–6

Sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one and two.
4. Count down to one, zero, borrow, fifteen, fourteen and thirteen.

National Semiconductor

CD4503BM/CD4503BC Hex Non-Inverting TRI-STATE® Buffer

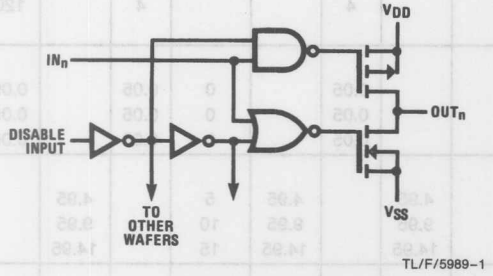
General Description

The CD4503B is a hex non-inverting TRI-STATE buffer with high output current sink and source capability. TRI-STATE outputs make it useful in bus-oriented applications. Two separate disable inputs are provided. Buffers 1 through 4 are controlled by the disable 4 input. Buffers 5 and 6 are controlled by the disable 2 input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

Features

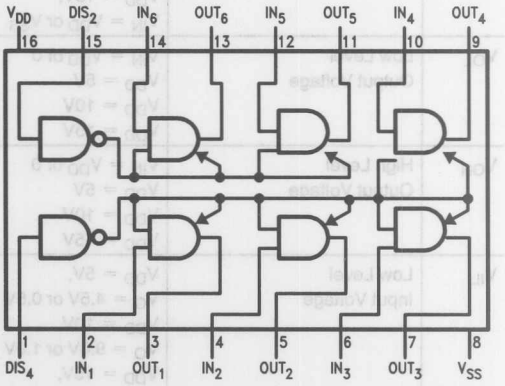
- Wide supply voltage range 3.0 V_{DC} to 18 V_{DC}
- TRI-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- Pin-for-pin replacement for MM80C97 and MC14503

Schematic and Connection Diagrams



TL/F/5989–1

Dual-In-Line Package



TL/F/5989–2

Top View

Order Number CD4503B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

In	Disable Input	Out
0	0	0
1	0	1
X	1	TRI-STATE

X = Don't Care

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	+3V to +15V
Operating Temperature Range (T_A)	
CD4503BM	−55°C to +125°C
CD4503BC	−40°C to +85°C

DC Electrical Characteristics CD4503BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1			1		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2			2		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4			4		120	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD} or 0 V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{DD} or 0 V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 4.5V, V_{OL} = 0.4V	2.80		2.30	2.55		1.60		mA
		V_{DD} = 5.0V, V_{OL} = 0.4V	3.00		2.40	2.75		1.75		mA
		V_{DD} = 10V, V_{OL} = 0.5V	7.85		6.35	7.00		4.45		mA
		V_{DD} = 15V, V_{OL} = 1.5V	19.95		16.10	25.00		11.30		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_{OH} = 4.6V	−1.28		−1.02	−1.76		−0.72		mA
		V_{DD} = 10V, V_{OH} = 9.5V	−3.20		−2.60	−4.5		−1.8		mA
		V_{DD} = 15V, V_{OH} = 13.5V	−8.20		−6.80	−17.6		−4.8		mA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V		±0.1		$±10^{-4}$	±0.1		±1.0	μA
I_{IN}	Input Current	V_{DD} = 15V		±0.1		$±10^{-4}$	±0.1		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4503BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD} or 0								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{DD} or 0								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 4.5V, V_{OL} = 0.4V	2.30		1.95	2.65		1.60		mA
		V_{DD} = 5.0V, V_{OL} = 0.4V	2.5		2.10	2.75		1.75		mA
		V_{DD} = 10V, V_{OL} = 0.5V	6.5		5.45	7.0		4.45		mA
		V_{DD} = 15V, V_{OL} = 1.5V	16.50		13.80	25.00		11.30		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_{OH} = 4.6V	−1.04		−0.88	−1.76		−0.7		mA
		V_{DD} = 10V, V_{OH} = 9.5V	−2.60		−2.2	−4.50		−1.8		mA
		V_{DD} = 15V, V_{OH} = 13.5V	−7.2		−6.0	−17.6		−4.8		mA
I_{TL}	TRI-STATE Leakage Current	V_{DD} = 15V		±0.3		$\pm 10^{-4}$	±0.3		±1.0	μA
I_{IN}	Input Current	V_{DD} = 15V		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

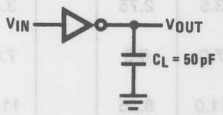
Note 2: V_{SS} = 0V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		75	100	ns
		V_{DD} = 10V		35	40	ns
		V_{DD} = 15V		25	30	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, Logical Level to High Impedance State	V_{DD} = 5V		80	125	ns
		V_{DD} = 10V		40	90	ns
		V_{DD} = 15V		35	70	ns
t_{PZL}, t_{PZH}	Propagation Delay Time, High Impedance State to Logical Level	V_{DD} = 5V		95	175	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	70	ns
t_{TLH}	Output Rise Time	V_{DD} = 5V		45	80	ns
		V_{DD} = 10V		23	40	ns
		V_{DD} = 15V		18	35	ns
t_{THL}	Output Fall Time	V_{DD} = 5V		45	80	ns
		V_{DD} = 10V		23	40	ns
		V_{DD} = 15V		18	35	ns

*AC Parameters are guaranteed by DC correlated testing.

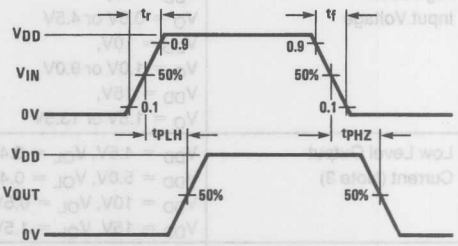
AC Test Circuits and Switching Time Waveforms

t_{PHL}, t_{PLH}



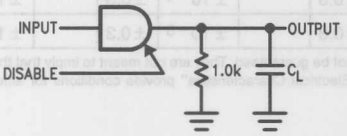
TL/F/5989–3

CMOS to CMOS



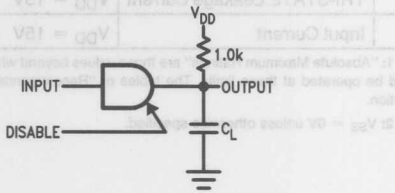
TL/F/5989–4

t_{PHZ} and t_{PZH}



TL/F/5989–5

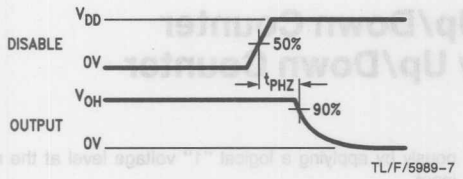
t_{PLZ} and t_{PZL}



TL/F/5989–6

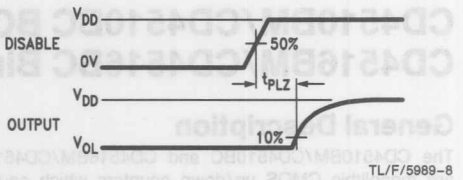
AC Test Circuits and Switching Time Waveforms (Continued)

t_{PHZ}



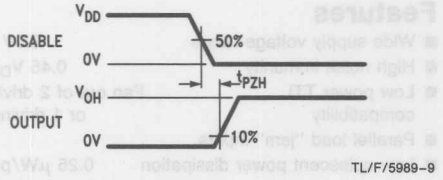
TL/F/5989–7

t_{PLZ}



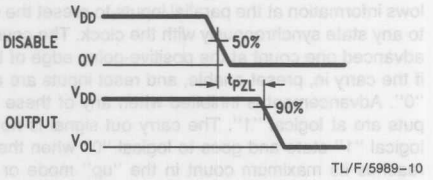
TL/F/5989–8

t_{PZH}



TL/F/5989–9

t_{PZL}



TL/F/5989–10

Note: Delays measured with input t_r, $t_f \leq 20$ ns.

5

National Semiconductor

CD4510BM/CD4510BC BCD Up/Down Counter
CD4516BM/CD4516BC Binary Up/Down Counter

General Description

The CD4510BM/CD4510BC and CD4516BM/CD4516BC are monolithic CMOS up/down counters which count in BCD and binary, respectively.

The counters count up when the up/down input is at logical "1" and vice versa. A logical "1" preset enable signal allows information at the parallel inputs to preset the counters to any state synchronously with the clock. The counters are advanced one count at the positive-going edge of the clock if the carry in, preset enable, and reset inputs are at logical "0". Advancement is inhibited when any of these three inputs are at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" when the counter reaches its maximum count in the "up" mode or its minimum count in the "down" mode, provided the carry input is at logical "0" state. The counters are cleared asynchronously by applying a logical "1" voltage level at the reset input.

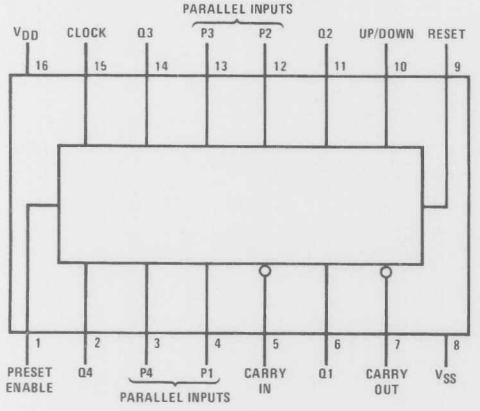
All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Parallel load "jam" inputs
- Low quiescent power dissipation — 0.25 μW/package (typ.) @ V_{CC} = 5.0V
- Motorola MC14510, MC14516 second source

Connection Diagram

Dual-In-Line Package



TL/F/5990–1

Top View

Order Number CD4510B* or CD4516B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Clock	Reset	Preset Enable	Carry In	Up/Down	Output Function
X	1	X	X	X	Reset to Zero
X	0	1	X	X	Set to P1, P2, P3, P4
↗	0	0	0	1	Count Up
↗	0	0	0	0	Count Down
↘	0	0	X	X	No Change
X	0	0	1	X	No Change

↗ = Positive Transition
↘ = Negative Transition
X = Don't Care

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (T_L) (Soldering, 10 sec.)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range	
CD4510BM, CD4516BM	−55°C to +125°C
CD4510BC, CD4516BC	−40°C to +85°C

DC Electrical Characteristics CD4510BM/CD4516BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.05	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.1	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.15	20		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.8		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.0		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.8		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−7.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4510BC/CD4516BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.05	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.1	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.15	80		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4510BC/CD4516BC (Note 2) (Continued)

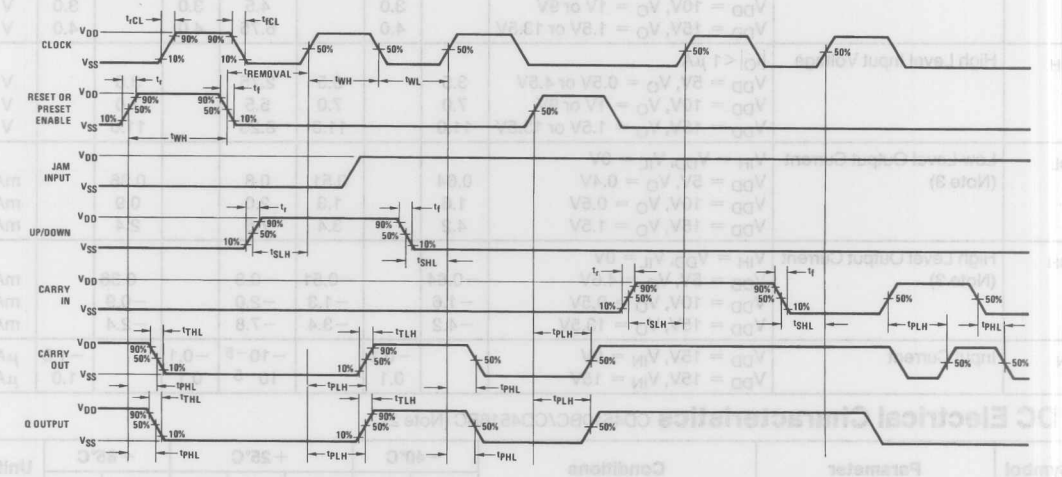
Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}, V_{IL} = 0V$								
		$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44	0.8		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1	2.0		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}, V_{IL} = 0V$								
		$V_{DD} = 5V, V_O = 4.6V$	−0.52		−0.44	−0.8		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.3		−1.1	−2.0		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−3.6		−3.0	−7.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms



TL/F/5990–2

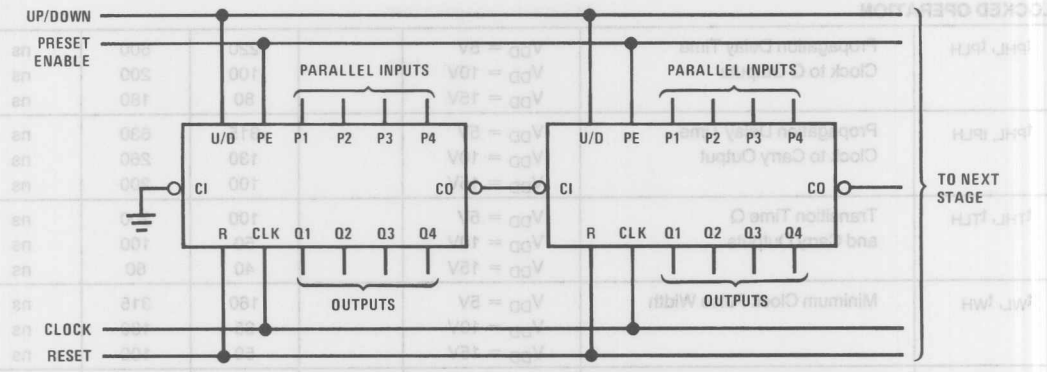
AC Electrical Characteristics* CD4510BM/CD4510BC, CD4516BM/CD4516BC

T_A = 25°C, C_L = 50 pF, R_L = 200k, $t_{rCL} = t_{fCL} = t_r = t_f$ = 20 ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q Outputs	V_{DD} = 5V		220	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Carry Output	V_{DD} = 5V		315	630	ns
		V_{DD} = 10V		130	260	ns
		V_{DD} = 15V		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q and Carry Outputs	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		160	315	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		50	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	15			μs
		V_{DD} = 15V	15			μs
t_{SU}	Minimum Carry In Setup Time	V_{DD} = 5V		100	220	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	70	ns
t_{SU}	Minimum Up/Down Setup Time	V_{DD} = 5V		200	420	ns
		V_{DD} = 10V		70	170	ns
		V_{DD} = 15V		60	150	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	3.1		MHz
		V_{DD} = 10V	3.8	7.6		MHz
		V_{DD} = 15V	5.0	10.0		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	Per Package		65		pF
RESET/PRESET ENABLE OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Q Output	V_{DD} = 5V		285	570	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		95	195	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Carry Output	V_{DD} = 5V		420	860	ns
		V_{DD} = 10V		170	350	ns
		V_{DD} = 15V		140	290	ns
t_{WH}	Minimum Reset/Preset Enable Pulse Width	V_{DD} = 5V		90	200	ns
		V_{DD} = 10V		40	100	ns
		V_{DD} = 15V		35	80	ns
t_{REM}	Minimum Reset/Preset Enable Removal Time	V_{DD} = 5V		170	330	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		60	120	ns
CARRY INPUT OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry In to Carry Output	V_{DD} = 5V		260	500	ns
		V_{DD} = 10V		110	220	ns
		V_{DD} = 15V		90	180	ns

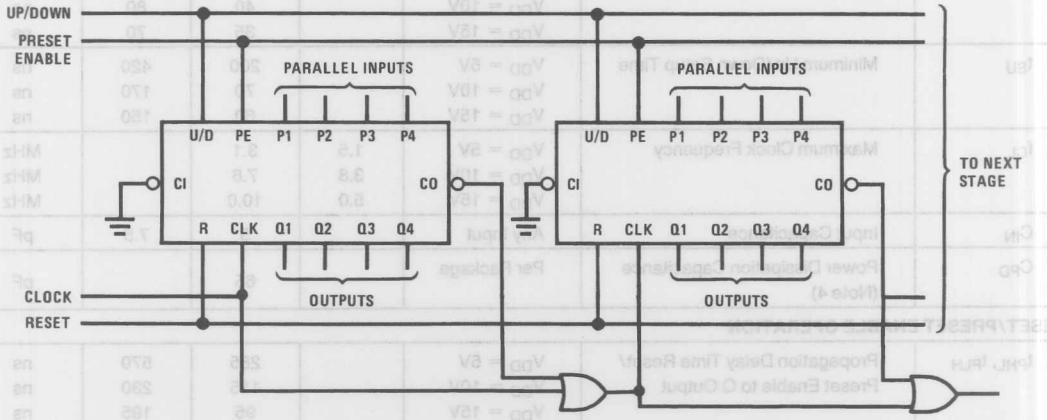
*AC Parameters are guaranteed by DC correlated testing.

Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{DD}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; P_Q = Quiescent Power Dissipation. For further details, see application note AN-90, "54C/74C Family characteristics".



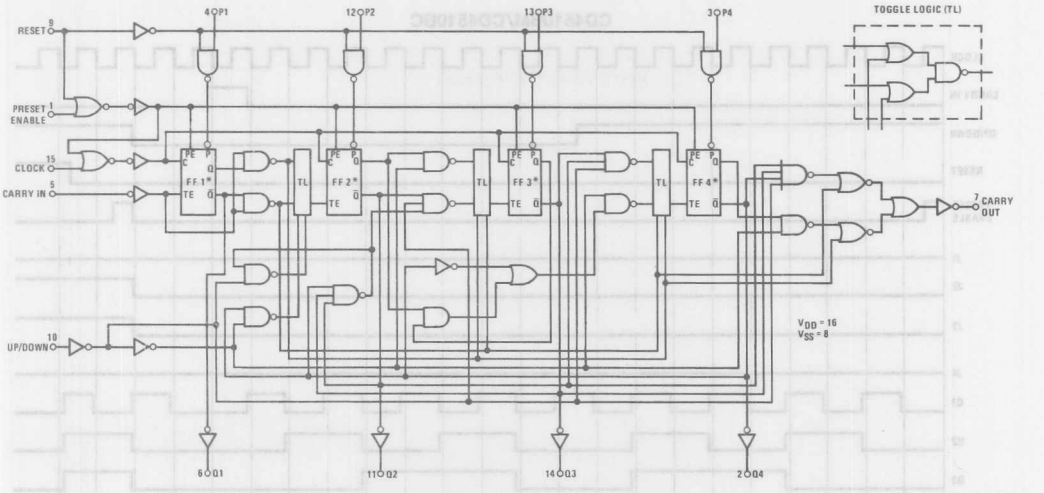
TL/F/5990–3

Ripple Clocking



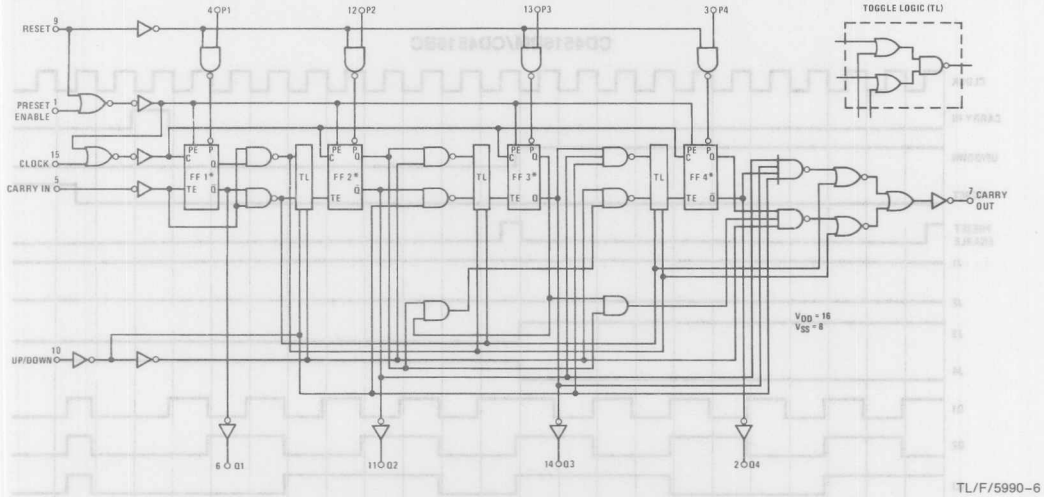
TL/F/5990–4

Schematic Diagrams



TL/F/5990–5

FIGURE 1. CD4510



TL/F/5990–6

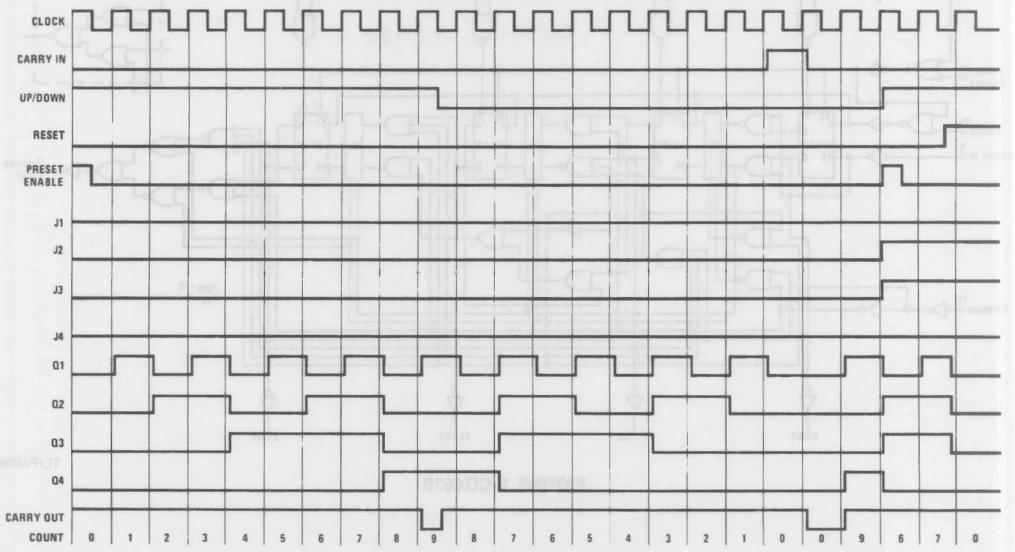
*Flip-flop toggles at the positive-going edge of clock (C) if Toggle Enable (TE) is at logical "1" and Preset Enable (PE) is at logical "0"

FIGURE 2. CD4516

5

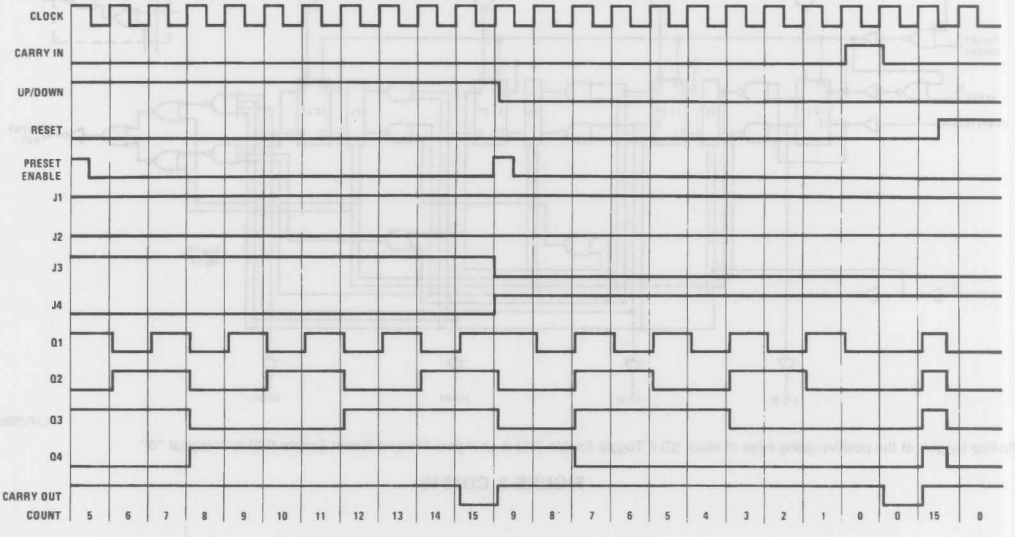
Logic Waveforms

CD4510BM/CD4510BC



TL/F/5990–7

CD4516BM/CD4516BC



TL/F/5990–8

National Semiconductor

CD4511BM/CD4511BC BCD-to-7 Segment Latch/Decoder/Driver

General Description

The CD4511BM/CD4511BC BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

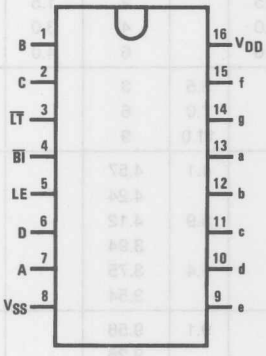
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

- Low logic circuit power dissipation
- High current sourcing outputs (up to 25 mA)
- Latch storage of code
- Blanking input
- Lamp test provision
- Readout blanking on all illegal input combinations
- Lamp intensity modulation capability
- Time share (multiplexing) facility
- Equivalent to Motorola MC14511

Connection Diagram

Dual-In-Line Package



TL/F/5991–1

Top View

Order Number CD4511B*

*Please look into Section 8, Appendix D for availability of various package types.

Segment Identification



TL/F/5991–3

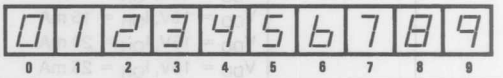
Truth Table

Inputs							Outputs							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	B
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				*

X = Don't Care

*Depends upon the BCD code applied during the 0 to 1 transition of LE.

Display



TL/F/5991–2

DC Supply Voltage (V_{DD}) −0.5V to +18V
Input Voltage (V_{IN}) −0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S) −65°C to +150°C
Power Dissipation (P_D)
Dual-In-Line 700 mW
Small Outline 500 mW
Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

Input Voltage (V_{IN}) 0V to V_{DD}
Operating Temperature Range (T_A)
CD4510BM, CD4516BM −55°C to +125°C
CD4510BC, CD4516BC −40°C to +85°C

DC Electrical Characteristics CD4511BM

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Supply Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Output Voltage Logical "0" Level	V_{DD} = 5V		0.01		0	0.01		0.05	V
		V_{DD} = 10V		0.01		0	0.01		0.05	V
		V_{DD} = 15V		0.01		0	0.01		0.05	V
V_{OH}	Output Voltage Logical "1" Level	V_{DD} = 5V	4.1		4.1	4.57		4.1		V
		V_{DD} = 10V	9.1		9.1	9.58		9.1		V
		V_{DD} = 15V	14.1		14.1	14.59		14.1		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_{OUT} = 3.8V or 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_{OUT} = 8.8V or 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_{OUT} = 13.8V or 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_{OUT} = 0.5V or 3.8V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_{OUT} = 1.0V or 8.8V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_{OUT} = 1.5V or 13.8V	11.0		11.0	9		11.0		V
V_{OH}	Output (Source) Drive Voltage	V_{DD} = 5V, I_{OH} = 0 mA	4.1		4.1	4.57		4.1		V
		V_{DD} = 5V, I_{OH} = 5 mA				4.24				V
		V_{DD} = 5V, I_{OH} = 10 mA	3.9		3.9	4.12		3.5		V
		V_{DD} = 5V, I_{OH} = 15 mA				3.94				V
		V_{DD} = 5V, I_{OH} = 20 mA	3.4		3.4	3.75		3.0		V
		V_{DD} = 5V, I_{OH} = 25 mA				3.54				V
		V_{DD} = 10V, I_{OH} = 0 mA	9.1		9.1	9.58		9.1		V
		V_{DD} = 10V, I_{OH} = 5 mA				9.26				V
		V_{DD} = 10V, I_{OH} = 10 mA	9.0		9.0	9.17		8.6		V
		V_{DD} = 10V, I_{OH} = 15 mA				9.04				V
		V_{DD} = 10V, I_{OH} = 20 mA	8.6		8.6	8.9		8.2		V
		V_{DD} = 10V, I_{OH} = 25 mA				8.75				V
		V_{DD} = 15V, I_{OH} = 0 mA	14.1		14.1	9.58		14.1		V
		V_{DD} = 15V, I_{OH} = 5 mA				14.27				V
		V_{DD} = 15V, I_{OH} = 10 mA	14.0		14.0	14.17		13.6		V
		V_{DD} = 15V, I_{OH} = 15 mA				14.07				V
		V_{DD} = 15V, I_{OH} = 20 mA	13.6		13.6	13.95		13.2		V
		V_{DD} = 15V, I_{OH} = 25 mA				13.8				V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_{OL} = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_{OL} = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_{OL} = 1.5V	4.2		3.4	8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: Devices should not be connected with power on.

DC Electrical Characteristics CD4511BC

Symbol	Parameter	Conditions	−55°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Supply Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Output Voltage Logical "0" Level	V_{DD} = 5V		0.01		0	0.01		0.05	V
		V_{DD} = 10V		0.01		0	0.01		0.05	V
		V_{DD} = 15V		0.01		0	0.01		0.05	V
V_{OH}	Output Voltage Logical "1" Level	V_{DD} = 5V	4.1		4.1	4.57		4.1		V
		V_{DD} = 10V	9.1		9.1	9.58		9.1		V
		V_{DD} = 15V	14.1		14.1	14.59		14.1		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_{OUT} = 3.8V or 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_{OUT} = 8.8V or 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_{OUT} = 13.8V or 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_{OUT} = 0.5V or 3.8V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_{OUT} = 1.0V or 8.8V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_{OUT} = 1.5V or 13.8V	11.0		11.0	9		11.0		V
V_{OH}	Output (Source) Drive Voltage	V_{DD} = 5V, I_{OH} = 0 mA	4.1		4.1	4.57		4.1		V
		V_{DD} = 5V, I_{OH} = 5 mA				4.24				V
		V_{DD} = 5V, I_{OH} = 10 mA	3.6		3.6	4.12		3.3		V
		V_{DD} = 5V, I_{OH} = 15 mA				3.94				V
		V_{DD} = 5V, I_{OH} = 20 mA	2.8		2.8	3.75		2.5		V
		V_{DD} = 5V, I_{OH} = 25 mA				3.54				V
		V_{DD} = 10V, I_{OH} = 0 mA	9.1		9.1	9.58		9.1		V
		V_{DD} = 10V, I_{OH} = 5 mA				9.26				V
		V_{DD} = 10V, I_{OH} = 10 mA	8.75		8.75	9.17		8.45		V
		V_{DD} = 10V, I_{OH} = 15 mA				9.04				V
		V_{DD} = 10V, I_{OH} = 20 mA	8.1		8.1	8.9		7.8		V
		V_{DD} = 10V, I_{OH} = 25 mA				8.75				V
		V_{DD} = 15V, I_{OH} = 0 mA	14.1		14.1	14.59		14.1		V
		V_{DD} = 15V, I_{OH} = 5 mA				14.27				V
		V_{DD} = 15V, I_{OH} = 10 mA	13.75		13.75	14.18		13.45		V
		V_{DD} = 15V, I_{OH} = 15 mA				14.07				V
		V_{DD} = 15V, I_{OH} = 20 mA	13.1		13.1	13.95		12.8		V
		V_{DD} = 15V, I_{OH} = 25 mA				13.8				V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_{OL} = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_{OL} = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_{OL} = 1.5V	3.6		3.0	8.8		2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

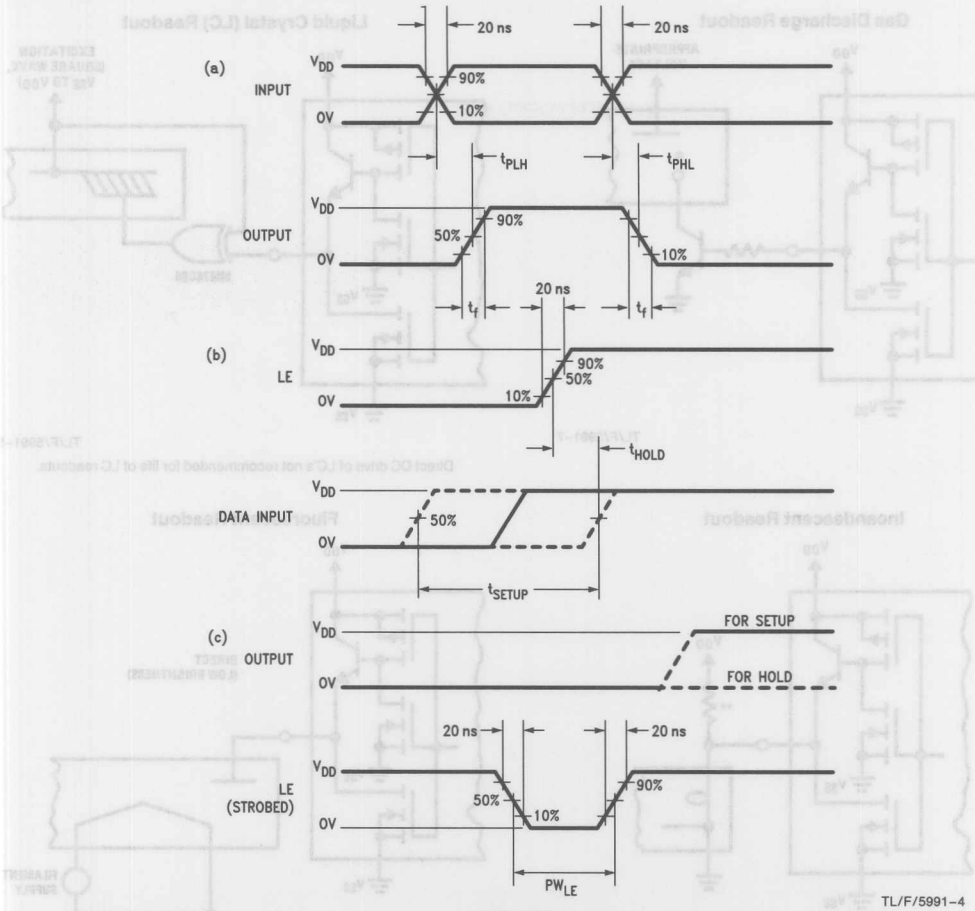
AC Electrical Characteristics*

T_A = 25°C and C_L = 50 pF, typical temperature coefficient for all values of V_{DD} = 0.3%/°C

Symbol	Parameter	Conditions	CD4511BX			Units
			Min	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0		5.0	7.5	pF
t_r	Output Rise Time	V_{DD} = 5V		40	80	ns
	(Figure 1a)	V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_f	Output Fall Time	V_{DD} = 5V		125	250	ns
	(Figure 1a)	V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		65	130	ns
t_{PLH}	Turn-Off Delay Time	V_{DD} = 5V		640	1280	ns
	(Data) *(Figure 1a)*	V_{DD} = 10V		250	500	ns
		V_{DD} = 15V		175	350	ns
t_{PHL}	Turn-On Delay Time	V_{DD} = 5V		720	1440	ns
	(Data) *(Figure 1a)*	V_{DD} = 10V		290	580	ns
		V_{DD} = 15V		195	400	ns
t_{PLH}	Turn-Off Delay Time	V_{DD} = 5V		320	640	ns
	(Blank) *(Figure 1a)*	V_{DD} = 10V		130	260	ns
		V_{DD} = 15V		100	200	ns
t_{PHL}	Turn-On Delay Time	V_{DD} = 5V		485	970	ns
	(Blank) *(Figure 1a)*	V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_{PLH}	Turn-Off Delay Time	V_{DD} = 5V		313	625	ns
	(Lamp Test) *(Figure 1a)*	V_{DD} = 10V		125	250	ns
		V_{DD} = 15V		90	180	ns
t_{PHL}	Turn-On Delay Time	V_{DD} = 5V		313	625	ns
	(Lamp Test) *(Figure 1a)*	V_{DD} = 10V		125	250	ns
		V_{DD} = 15V		90	180	ns
t_{SETUP}	Setup Time	V_{DD} = 5V	180	90		ns
	(Figure 1b)	V_{DD} = 10V	76	38		ns
		V_{DD} = 15V	40	20		ns
t_{HOLD}	Hold Time	V_{DD} = 5V	0	−90		ns
	(Figure 1b)	V_{DD} = 10V	0	−38		ns
		V_{DD} = 15V	0	−20		ns
PW_{LE}	Minimum Latch Enable	V_{DD} = 5V	520	260		ns
	Pulse Width *(Figure 1c)*	V_{DD} = 10V	220	110		ns
		V_{DD} = 15V	130	65		ns

*AC Parameters are guaranteed by DC correlated testing.

Switching Time Waveforms

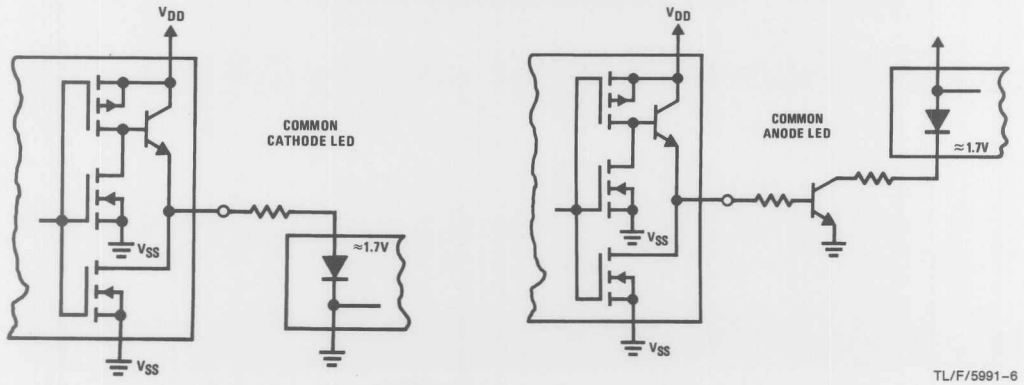


TL/F/5991–4

FIGURE 1

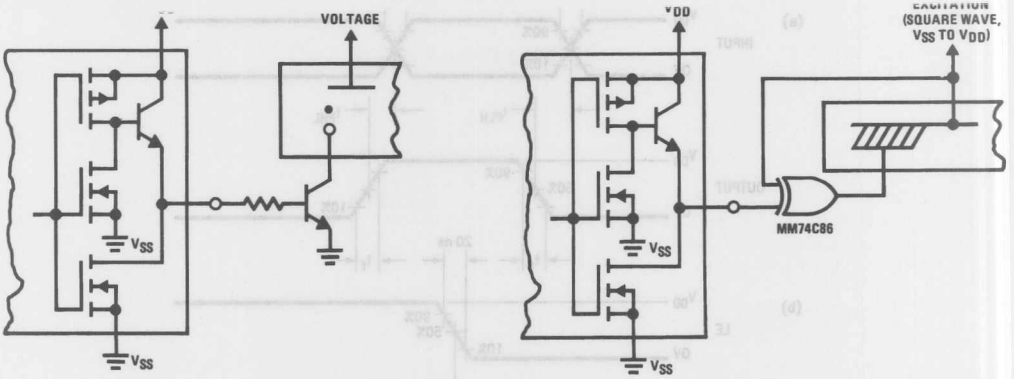
Typical Applications

Light Emitting Diode (LED) Readout



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TL/F/5991–6

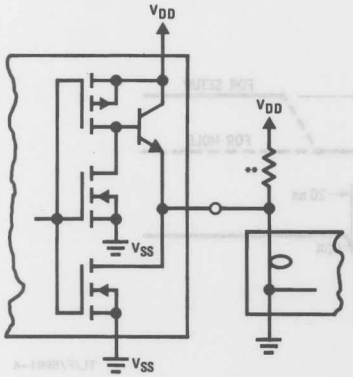


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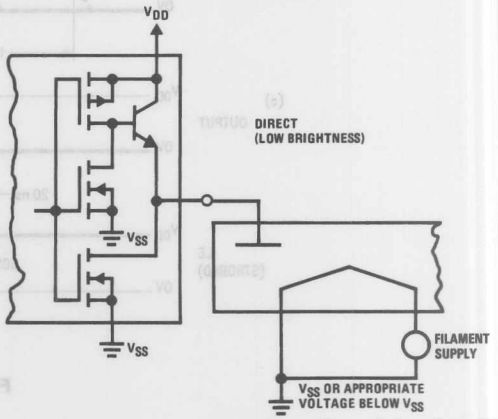
Direct DC drive of LC's not recommended for life of LC readouts.

Incandescent Readout



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Fluorescent Readout



TL/F/5991–10

**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

National Semiconductor

CD4512BM/CD4512BC 8-Channel Buffered Data Selector

General Description

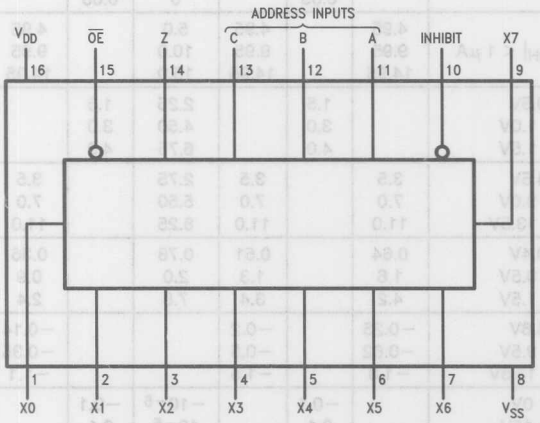
The CD4512BM/CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable ($\overline{OE}$) input forces the output into the TRI-STATE condition. Low levels at both the Inhibit and ($\overline{OE}$) inputs allow normal operation.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- TRI-STATE output
- Low quiescent power dissipation — 0.25 μW/package (typ.) @ V_{CC} = 5.0V
- Plug-in replacement for Motorola MC14512

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5993–1

Top View

Order Number CD4512B*

*Please look into Section 8, Appendix D for availability of various package types.

Address Inputs			Control Inputs		Output
C	B	A	Inhibit	$\overline{OE}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
ⓘ	ⓘ	ⓘ	1	0	0
ⓘ	ⓘ	ⓘ	ⓘ	1	Hi-Z

ⓘ = Don't care

Hi-Z = TRI-STATE condition

Xn = Data at input n

5

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	-0.5 to $V_{DD} + 0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature, (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3.0 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4512BM	$-55°C$ to $+125°C$
CD4512BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4512BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		5.0		0.005	5.0		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		10		0.010	10		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_{OL}\rvert < 1$ μA		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_{OH}\rvert < 1$ μA	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.64		0.51	0.78		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.6		1.3	2.0		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.25		−0.2			−0.14		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−0.62		−0.5			−0.35		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−1.8		−1.5			−1.1		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	TRI-STATE Output Current	$V_{DD} = 15V$, $V_O = 0V$		±0.1		-10^{-5}	±0.1		±3.0	μA
		$V_{DD} = 15V$, $V_O = 15V$								

DC Electrical Characteristics CD4512BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		20		0.005	20		150	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		40		0.010	40		300	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_{OL}\rvert < 1$ μA		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_{OH}\rvert < 1$ μA	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$		4.0		6.75	4.0		4.0	V

DC Electrical Characteristics CD4512BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.78		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.0		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16			−0.12		mA
		V_{DD} = 10V, V_O = 9.5	−0.5		−0.4			−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2			−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	TRI-STATE Output Current	V_{DD} = 15V, V_O = 0V		±1.0		$\pm 10^{-5}$	±1.0		±7.5	μA
		V_{DD} = 15V, V_O = 15V								

AC Electrical Characteristics* T_A = 25°C, t_r = t_f = 20 ns, C_L = 50 pF

Symbol	Parameter	Conditions	CD4512BM			CD4512BC			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PHL}	Propagation Delay High-to-Low Level	V_{DD} = 5V		225	500		225	750	ns
		V_{DD} = 10V		75	175		75	200	ns
		V_{DD} = 15V		57	130		57	150	ns
t_{PLH}	Propagation Delay Low-to-High Level	V_{DD} = 5V		225	500		225	750	ns
		V_{DD} = 10V		75	175		75	200	ns
		V_{DD} = 15V		57	130		57	150	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		70	200		70	200	ns
		V_{DD} = 10V		35	100		35	100	ns
		V_{DD} = 15V		25	80		25	80	ns
t_{PHZ}, t_{PLZ}	Propagation Delay into TRI-STATE from Logic Level	V_{DD} = 5V		50	125		50	125	ns
		V_{DD} = 10V		25	75		25	75	ns
		V_{DD} = 15V		19	60		19	60	ns
t_{PZH}, t_{PZL}	Propagation Delay to Logic Level from TRI-STATE	V_{DD} = 5V		50	125		50	125	ns
		V_{DD} = 10V		25	75		25	75	ns
		V_{DD} = 15V		19	60		19	60	ns
C_{IN}	Input Capacitance	(Note 4)		7.5	15		7.5	15	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		7.5	15		7.5	15	pF
C_{PD}	Power Dissipation Capacity	(Note 5)		150			150		pF

*AC Parameters are guaranteed by DC correlated testing.

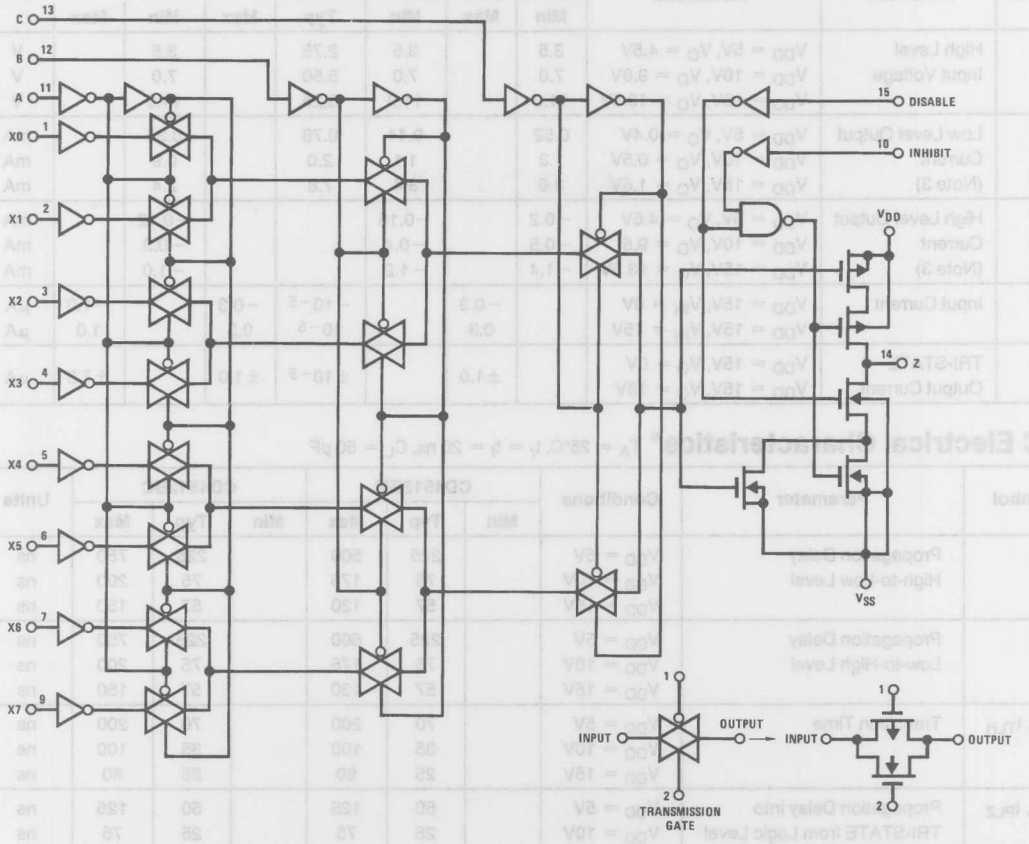
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance guaranteed by periodic testing.

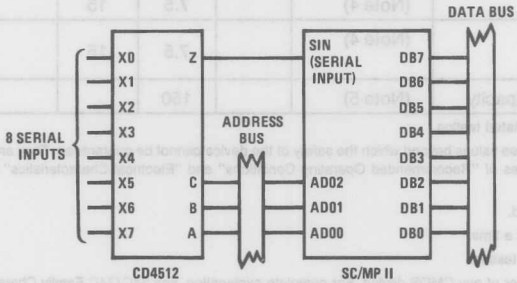
Note 5: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note, AN-90.



TL/F/5993–2

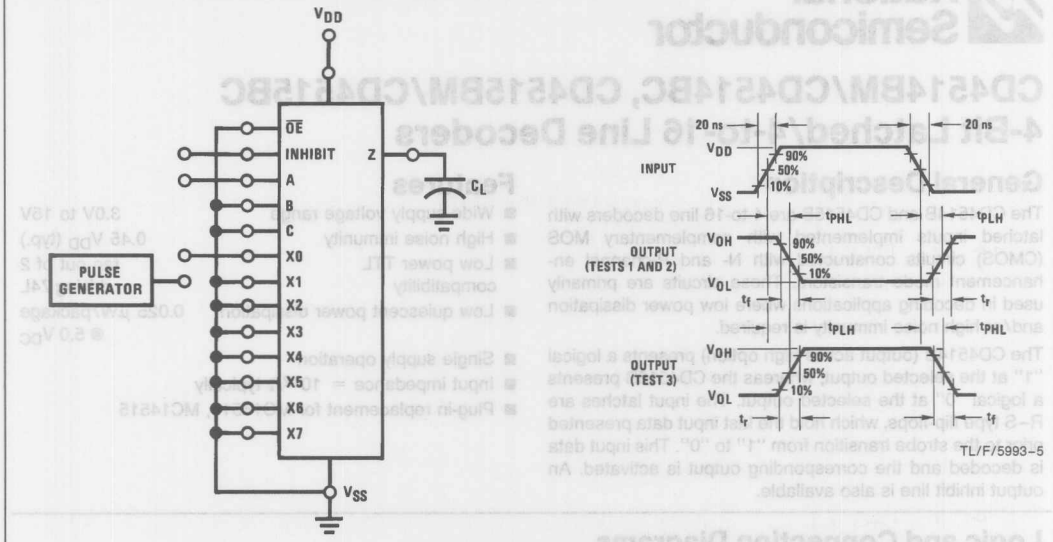
Typical Application

Serial Data Routing Interface



TL/F/5993–3

AC Test Circuit and Switching Time Waveforms



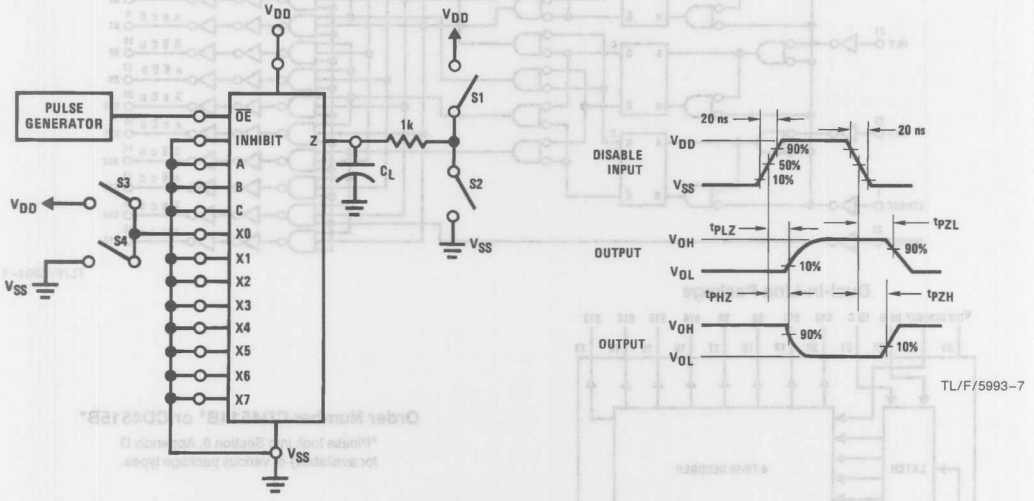
TL/F/5993–5

TL/F/5993–4

Input Connections for t_r, t_f, t_{PLH}, t_{PHL}

Test	Inhibit	A	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

TRI-STATE AC Test Circuit and Switching Time Waveforms



TL/F/5993–7

TL/F/5993–6

Switch Positions for TRI-STATE Test

Test	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

National Semiconductor

CD4514BM/CD4514BC, CD4515BM/CD4515BC 4-Bit Latched/4-to-16 Line Decoders

General Description

The CD4514B and CD4515B are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

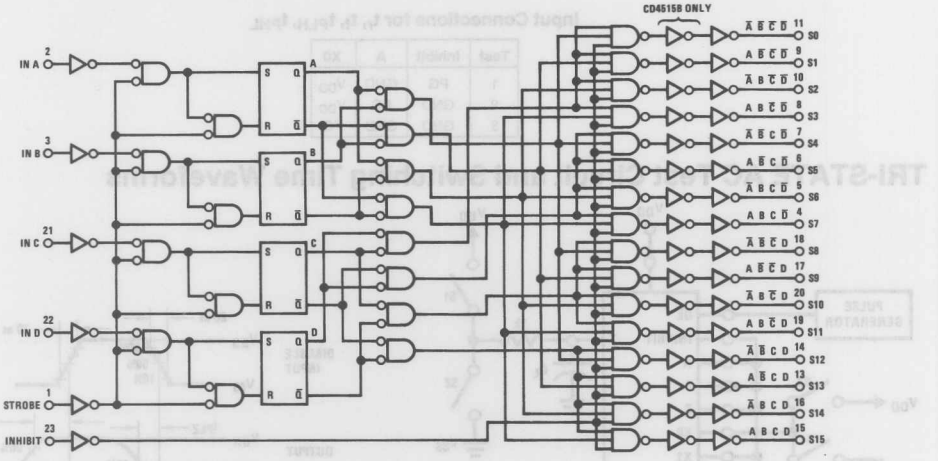
The CD4514B (output active high option) presents a logical "1" at the selected output, whereas the CD4515B presents a logical "0" at the selected output. The input latches are R–S type flip-flops, which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low quiescent power dissipation	0.025 μW/package @ 5.0 V_{DC}

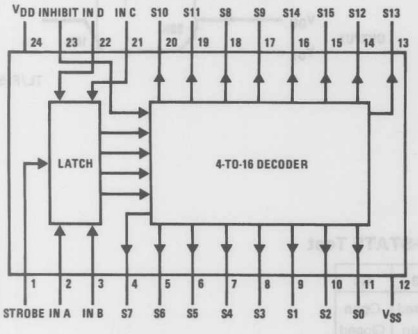
- Single supply operation
- Input impedance = $10^{12}\Omega$ typically
- Plug-in replacement for MC14514, MC14515

Logic and Connection Diagrams



TL/F/5994–1

Dual-In-Line Package



TL/F/5994–2

Top View

Order Number CD4514B* or CD4515B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4514BM, CD4515BM	−55°C to +125°C
CD4514BC, CD4515BC	−40°C to +85°C

DC Electrical Characteristics CD4514BM, CD4515BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.005	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.010	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_{IL} = 0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_{IL} = 0V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\|$ < 1 μA		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\|$ < 1 μA	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.80		2.40		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.80		−2.40		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4514BC, CD4515BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.005	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.010	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V

	Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

All types C_L = 50 pF, T_A = 25°C, t_r = t_f = 20 ns unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{THL}, t_{TLH}	Transition Times	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Times	V_{DD} = 5V		550	1100	ns
		V_{DD} = 10V		225	450	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Inhibit Propagation Delay Times	V_{DD} = 5V		400	800	ns
		V_{DD} = 10V		150	300	ns
		V_{DD} = 15V		100	200	ns
t_{SU}	Setup Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
t_{WH}	Strobe Pulse Width	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 5)		150		pF
C_{IN}	Input Capacitance	Any Input (Note 4)		5	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C and 74C Family Characteristics application note, AN-90.

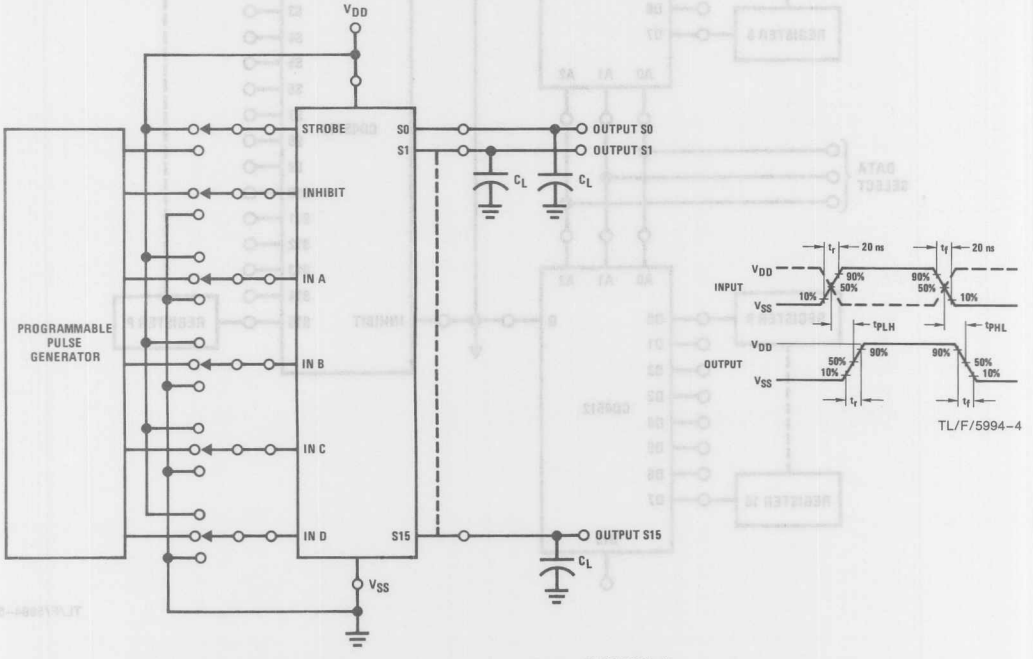
Truth Table

Decode Truth Table (Strobe = 1)

Inhibit	Data Inputs D	C	B	A	Selected Output CD4514 = Logic "1" CD4515 = Logic "0"
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514 All Outputs = 1, CD4515

X = Don't Care

AC Test Circuit and Switching Time Waveforms



TL/F/5994–3

TL/F/5994–4

FIGURE 1

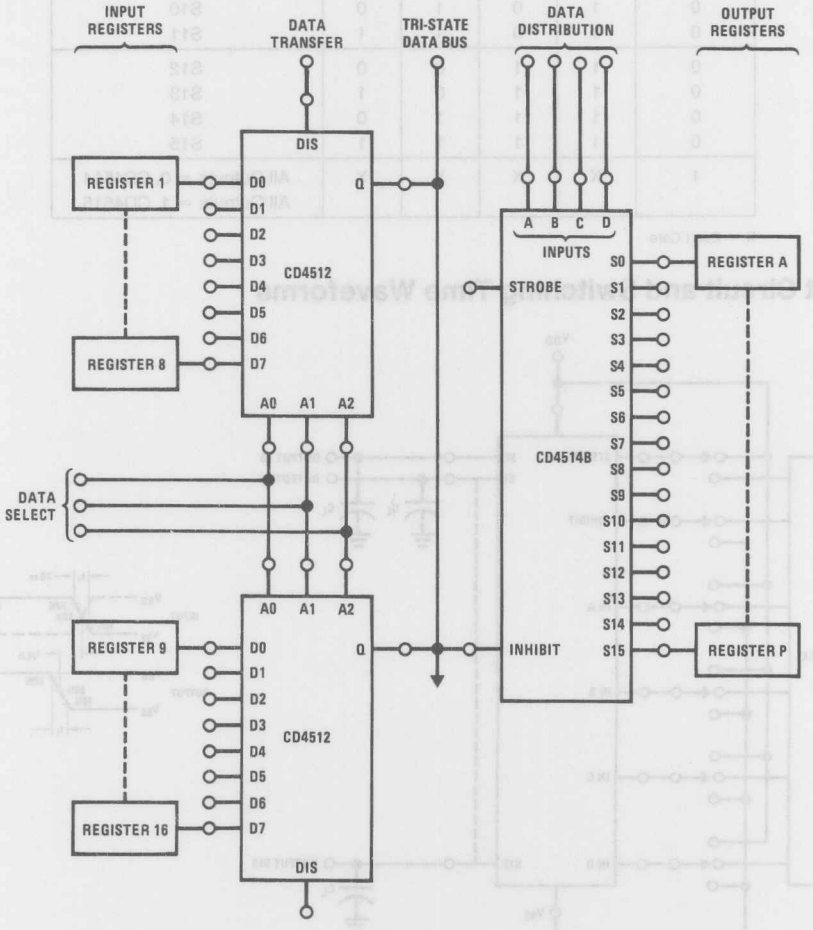
Applications

Two CD4512 8-channel data selectors are used here with the CD4514B 4-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a TRI-STATE® data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the 8 inputs on both CD4512 data selectors. One register is assigned to each input. The signals on A0, A1 and A2 choose 1-of-8 inputs for transfer out to the TRI-STATE data bus. A fourth signal, labelled Dis, disables one of the CD4512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1–16, the rate of transfer of the sequential information can also be varied. That is, if the CD4512 were addressed at a rate that is 8 times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the TRI-STATE bus is redistributed by the CD4514B 4-bit latch/decoder. Using the 4-bit address, INA–IND, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A–P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.



TL/F/5994–5

National Semiconductor

CD4518BM/CD4518BC, CD4520BM/CD4520BC Dual Synchronous Up Counters

General Description

The CD4518BM/CD4518BC dual BCD counter and the CD4520BM/CD4520BC dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors.

Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops which increment on either the positive-edge of CLOCK or negative-edge of ENABLE, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the RESET line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 6 MHz counting rate (typ.) at V_{DD} = 10V

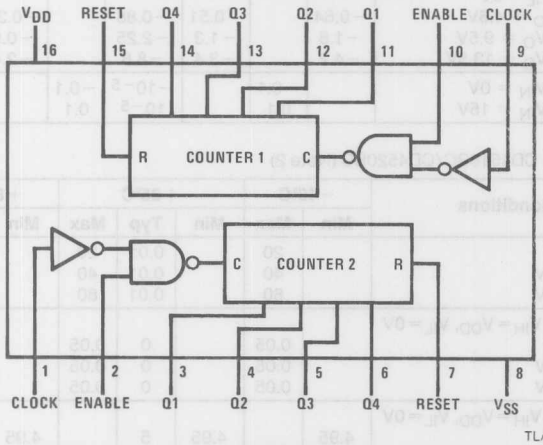
Truth Table

Clock	Enable	Reset	Action
⌐	1	0	Increment Counter
0	¬	0	Increment Counter
¬	X	0	No Change
X	⌐	0	No Change
⌐	0	0	No Change
1	¬	0	No Change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

Connection Diagram

Dual-In-Line and Flat Package



TL/F/5995–1

Top View

Order Number CD4518B* or CD4520B*

*Please look into Section 8, Appendix D for availability of various package types.

5

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} + 0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditons (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to V_{DD}
Operating Temperature Range (T_A)	
CD4518BM, CD4520BM	−55°C to +125°C
CD4518BC, CD4520BC	−40°C to +85°C

DC Electrical Characteristics CD4518BM/CD4520BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4518BC/CD4520BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4518BC/CD4520BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Clock → Q	$V_{DD} = 5V$		325	650	ns
		$V_{DD} = 10V$		110	225	ns
		$V_{DD} = 15V$		85	170	ns
t_{PHL}	Propagation Delay Time Reset → Q	$V_{DD} = 5V$		220	560	ns
		$V_{DD} = 10V$		90	230	ns
		$V_{DD} = 15V$		65	160	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	1.5	3		MHz
		$V_{DD} = 10V$	3.0	6		MHz
		$V_{DD} = 15V$	4.0	8		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		10	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		35	70	ns
t_{RCL}, t_{FC}	Maximum Clock or Enable Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	10			μs
		$V_{DD} = 15V$	5			μs
t_{WH}, t_{WL}	Minimum Enable Pulse Width	$V_{DD} = 5V$		125	250	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}	Minimum Reset Pulse Width	$V_{DD} = 5V$		180	375	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	130	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Either Counter (Note 4)		50		pF

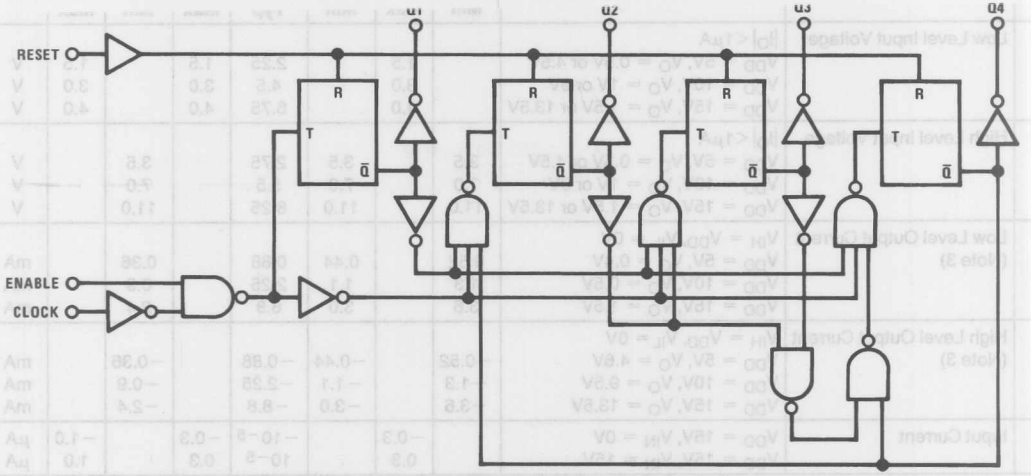
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

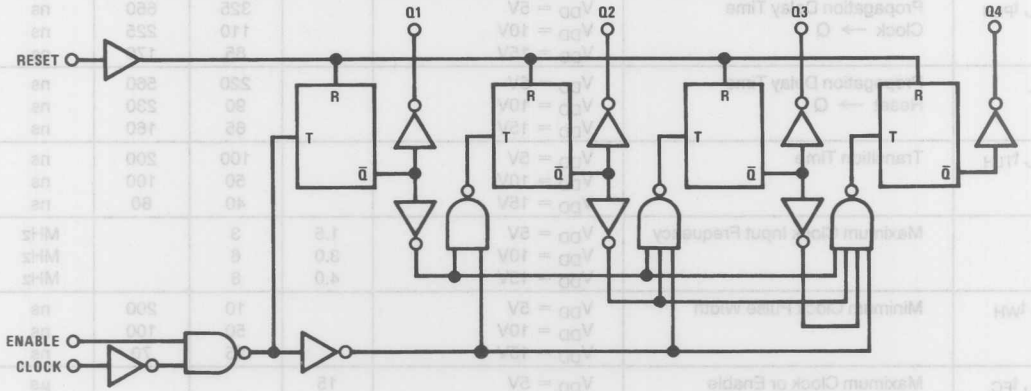
Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of a CMOS device. For a complete explanation, see "54C/74C Family Characteristics", application note AN-90.



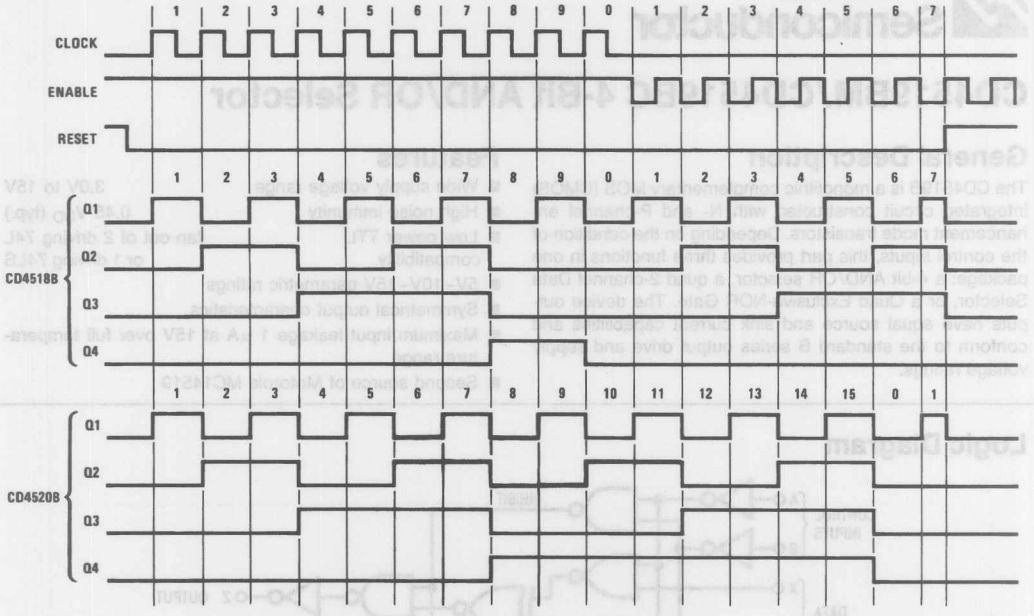
TL/F/5995–2

Binary Counter (CD4520B) ½ Device Shown



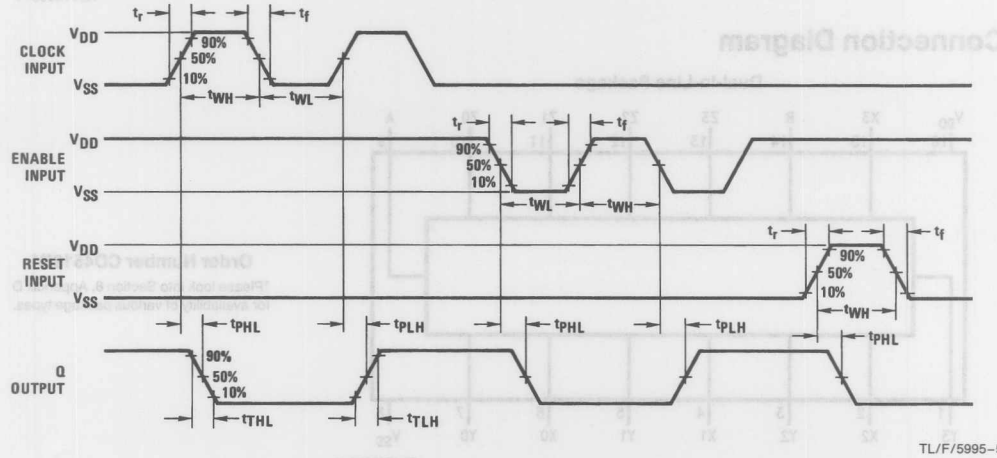
TL/F/5995–3

Timing Diagrams



TL/F/5995–4

Switching Time Waveforms



TL/F/5995–5

5

National Semiconductor

CD4519BM/CD4519BC 4-Bit AND/OR Selector

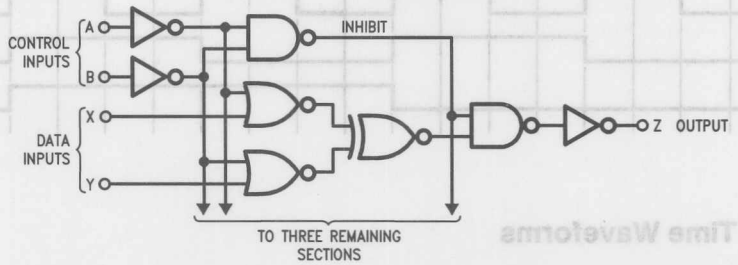
General Description

The CD4519B is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Depending on the condition of the control inputs, this part provides three functions in one package: a 4-bit AND/OR selector, a quad 2-channel Data Selector, or a Quad Exclusive-NOR Gate. The device outputs have equal source and sink current capabilities and conform to the standard B series output drive and supply voltage ratings.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range
- Second source of Motorola MC14519

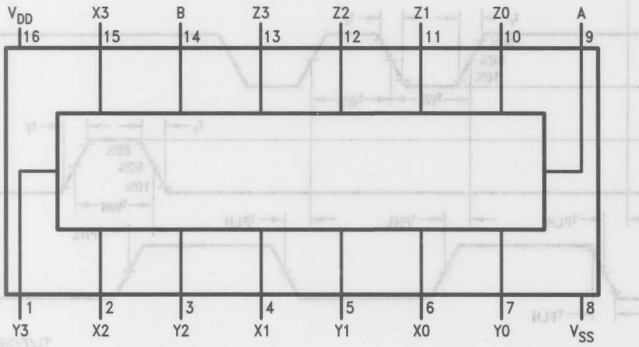
Logic Diagram



TL/F/5996–1

Connection Diagram

Dual-In-Line Package



TL/F/5996–2

Top View

Order Number CD4519B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Control Inputs		Output
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \bullet Y_n$

Note: $X_n \bullet Y_n = \overline{\overline{X_n} + \overline{Y_n}} = X_nY_n + \overline{X}_n\overline{Y}_n$

Absolute Maximum Ratings

(Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 sec.)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	$+3\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4519BM	$-55°C$ to $+125°C$
CD4519BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4519BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		1		0.005	1		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		2		0.006	2		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		4		0.007	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4519BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		4			4		30	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		8			8		60	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4519BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200$ kΩ, $t_r = t_f = 20$ ns, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay High-to-Low Level or Low-to-High Level	*(Figure 1)*				
		$V_{DD} = 5V$		180	360	ns
		$V_{DD} = 10V$		75	150	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	*(Figure 1)*				
		$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{pd}	Power Dissipation Capacity	Any Gate (Note 5)		25		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Condtions" and Electrical Characteristics" provides conditions for actual device operation.

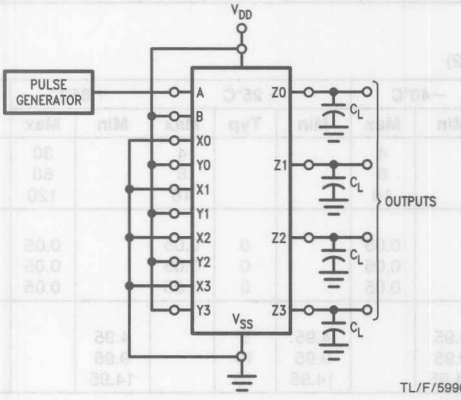
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

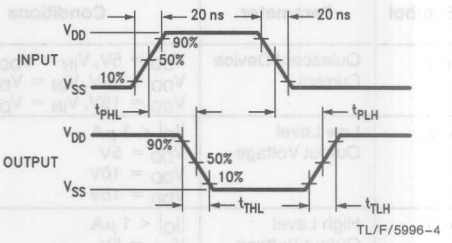
Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family characteristics application note AN-90.

AC Test Circuit and Switching Time Waveforms



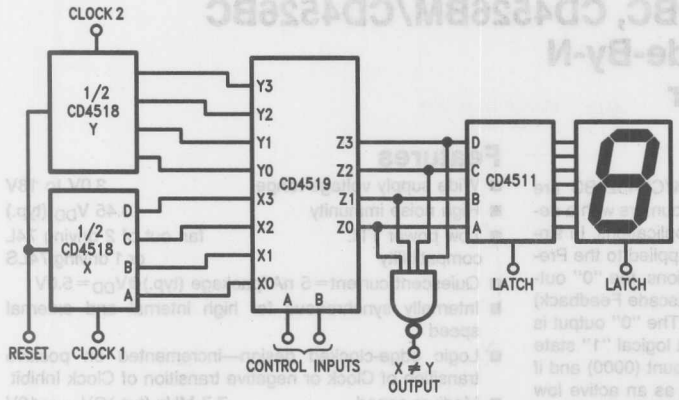
TL/F/5996–3



TL/F/5996–4

FIGURE 1

A	B	
0	0	Display Zero
0	1	Display Counter Y
1	0	Display Counter X
1	1	Compare Counters



TL/F/5996–5

CD4522BM/CD4522BC, CD4526BM/CD4526BC Programmable Divide-By-N 4-Bit Binary Counter

General Description

The CD4522BM/CD4522BC, CD4526BM/CD4526BC are CMOS programmable cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications, the "0" output is applied to the Preset Enable input. For multi-stage applications, the "0" output is used in conjunction with the CF (Cascade Feedback) input to perform the divide-by-N function. The "0" output is normally at logical "0" level; it will go to a logical "1" state only when the counter is at its terminal count (0000) and if CF is at logical "1" level. Thus, CF acts as an active low inhibit for the "0" output. This feature allows cascade divide-by-N operations with no additional gate required (see Applications section). The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

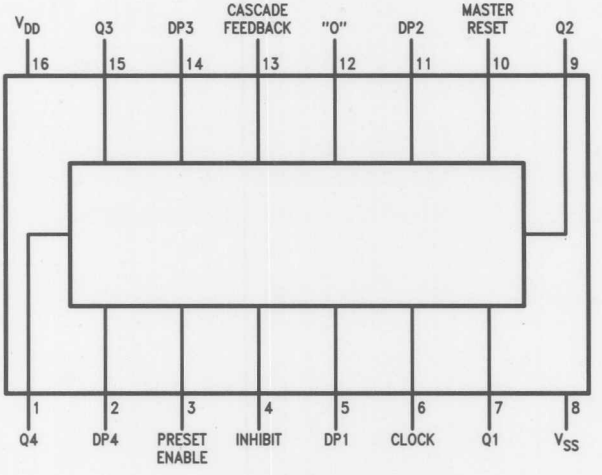
- Wide supply voltage range 3.0V to 18V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- Quiescent current = 5 nA/package (typ.)@V_{DD} = 5.0V
- Internally synchronous for high internal and external speed
- Logic edge-clocked design—incremented on positive transition of Clock or negative transition of Clock Inhibit
- Medium speed 7.7 MHz (typ.)@V_{DD} = 10V
- Asynchronous Preset Enable

Applications

- Programmable down counter
- Programmable frequency divider
- Frequency synthesizers
- Phase-locked loops

Connection Diagram

Dual-In-Line Package



TL/F/5997–1

Top View

Order Number CD4522B* or CD4526B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$3\ V_{DC}$ to $15\ V_{DC}$
Input Voltage (V_{IN})	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4522BM, CD4526BM	$-55°C$ to $+125°C$
CD4522BC, CD4526BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4522BM, CD4526BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5		0.005	5		150	μA
		$V_{DD} = 10V$		10		0.010	10		300	μA
		$V_{DD} = 15V$		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		20		0.005	20		150	μA
		$V_{DD} = 10V$		40		0.010	40		300	μA
		$V_{DD} = 15V$		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PHL}, t_{PLH}	Propagation Delay Time from Clock to Q Outputs	V_{DD} = 5V		350	825	ns
		V_{DD} = 10V		130	345	ns
		V_{DD} = 15V		90	240	ns
t_{PHL}, t_{PLH}	Propagation Delay Time from Clock to "0" Output	V_{DD} = 5V		200	500	ns
		V_{DD} = 10V		80	250	ns
		V_{DD} = 15V		60	190	ns
PW_C	Minimum Clock Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
f_{CL}	Maximum Clock Pulse Frequency	V_{DD} = 5V	1.5	2.9		MHz
		V_{DD} = 10V	3.0	7.7		MHz
		V_{DD} = 15V	4.0	11		MHz
T_{rCL}, T_{fCL}	Maximum Clock or Inhibit Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	15			μs
		V_{DD} = 15V	15			μs
t_{HOLD}	Hold Time	V_{DD} = 5V		40	125	ns
		V_{DD} = 10V		25	50	ns
		V_{DD} = 15V		20	40	ns
PW_{PE}	Minimum Preset Enable Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
PW_{MR}	Minimum Master Reset Pulse Width	V_{DD} = 5V		160	350	ns
		V_{DD} = 10V		75	180	ns
		V_{DD} = 15V		50	120	ns
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 5)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

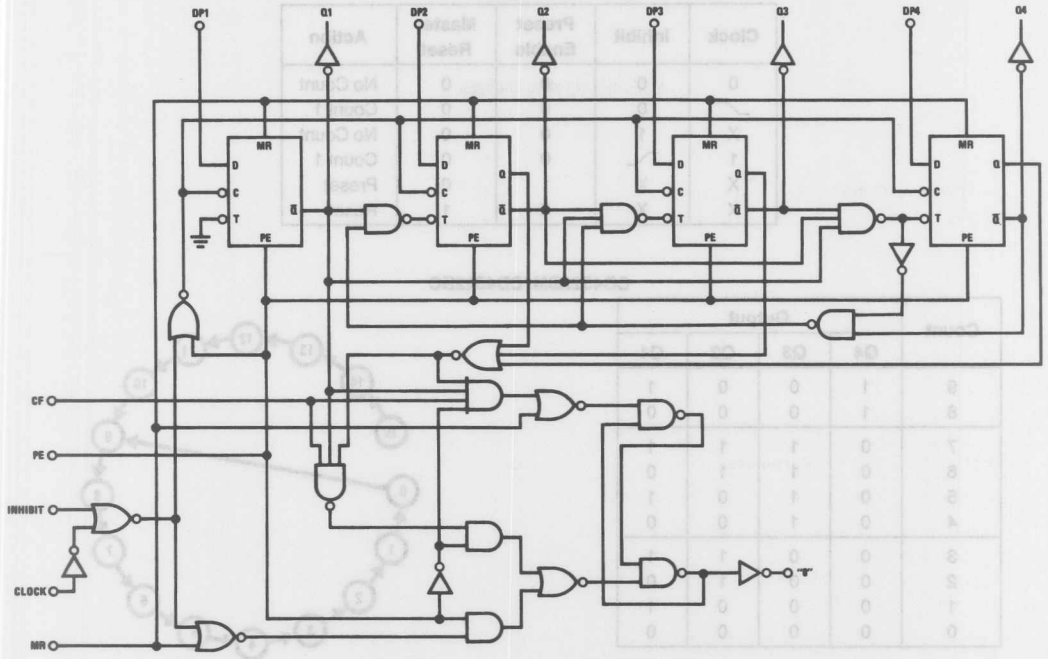
Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

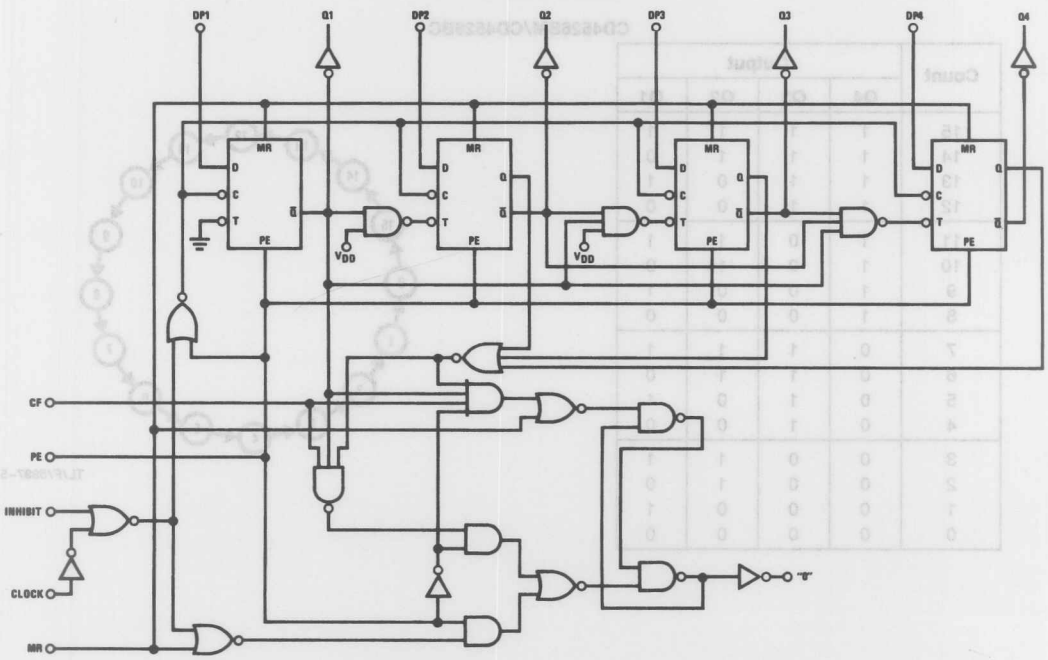
Logic Diagrams

CD4522BM/CD4522BC



TL/F/5997–2

CD4526BM/CD4526BC



TL/F/5997–3

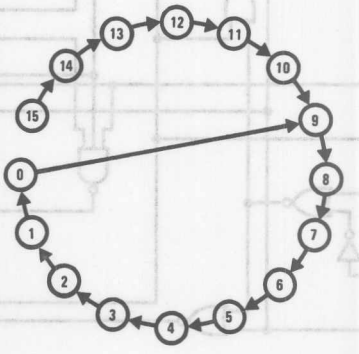
Truth Tables and Count Sequences

Both Types

Clock	Inhibit	Preset Enable	Master Reset	Action
0	0	0	0	No Count
⌐	0	0	0	Count 1
X	1	0	0	No Count
1	⌐	0	0	Count 1
X	X	1	0	Preset
X	X	X	1	Reset

CD4522BM/CD4522BC

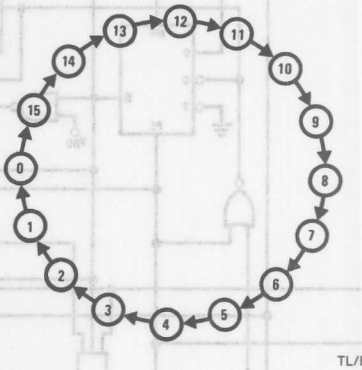
Count	Output			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



TL/F/5997–4

CD4526BM/CD4526BC

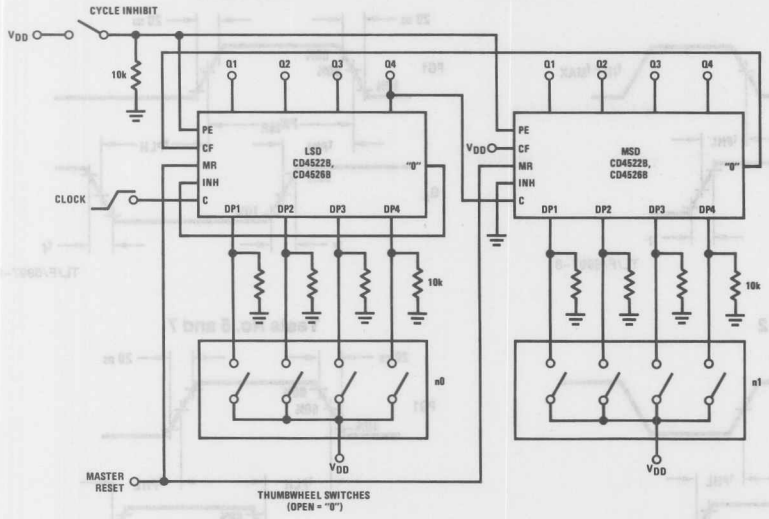
Count	Output			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



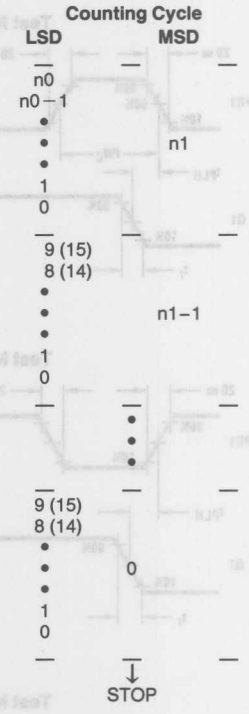
TL/F/5997–5

Typical Applications

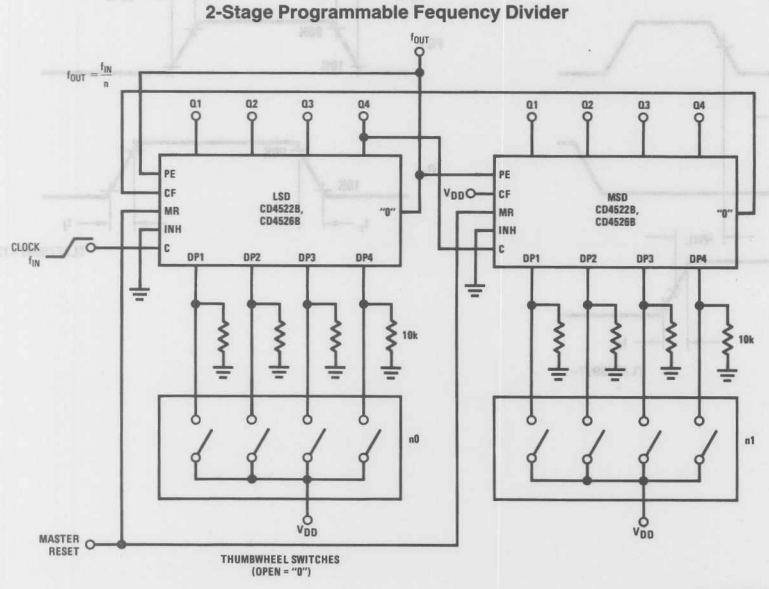
2-Stage Programmable Down Counter



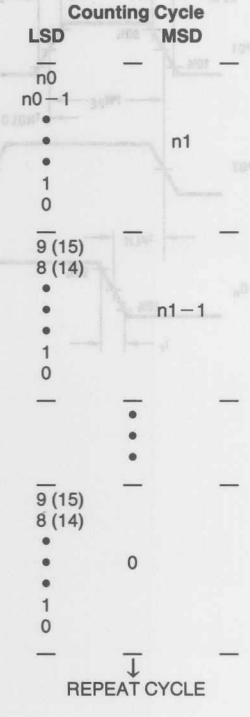
TL/F/5997–6



2-Stage Programmable Fequency Divider



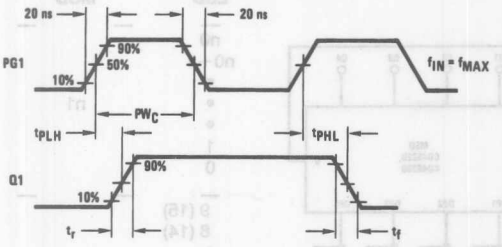
TL/F/5997–7



Note: When cascading more than 2 packages, tie "0" output of the nth package to CF input of the (n – 1)th package for all n = 2, 3.

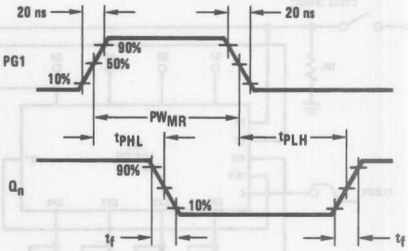
Switching Time Waveforms

Test No. 1



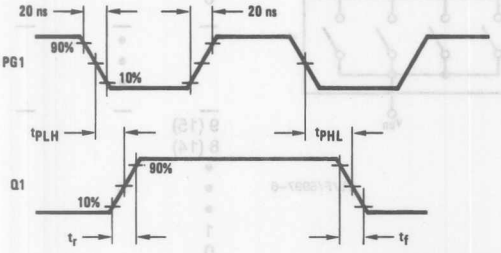
TL/F/5997–8

Test No. 4



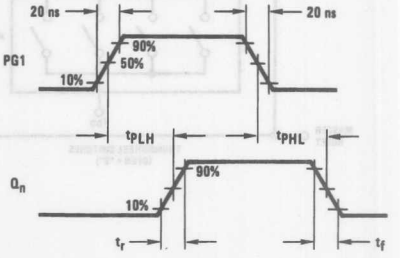
TL/F/5997–9

Test No. 2



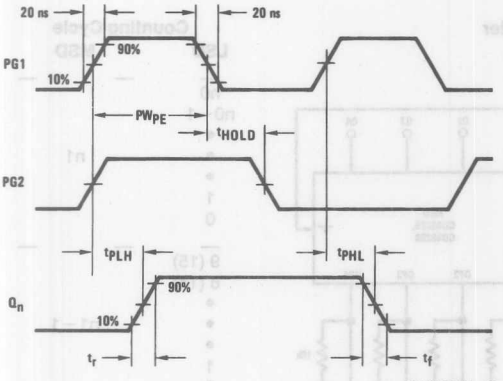
TL/F/5997–10

Tests No. 5 and 7



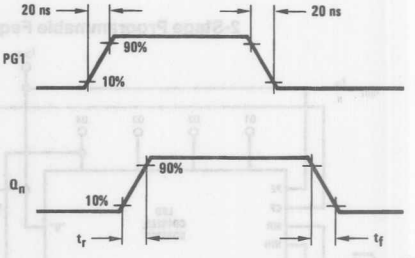
TL/F/5997–11

Test No. 3



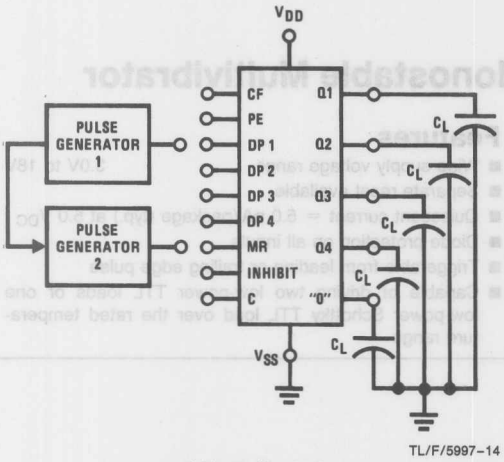
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Test No. 6

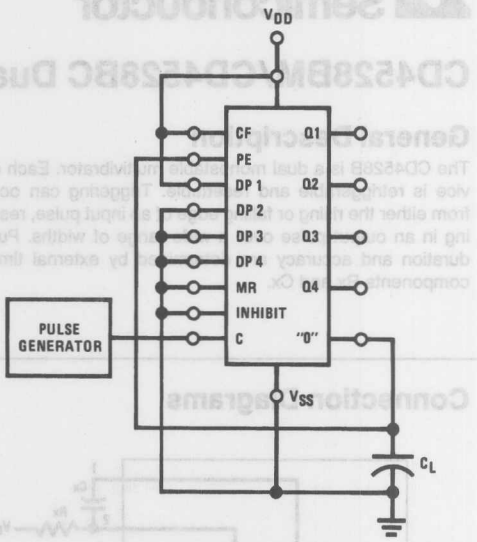


TL/F/5997–13

AC Test Circuits



a) Tests No. 1–6



b) Test No. 7

FIGURE 1. Test Circuits

Test Conditions

TABLE I

Characteristic	Test No.	Clock	Inhibit	PE	MR	DP_n	CF	Output
t_r, t_f, t_{PLH}, t_{PHL}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{MAX}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{HOLD}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	*Fig. 1b*	V_{SS}	*Fig. 1b*	V_{DD}	"0"

5

National Semiconductor

CD4528BM/CD4528BC Dual Monostable Multivibrator

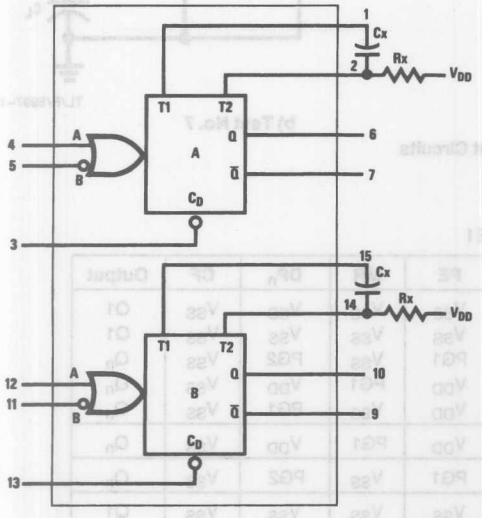
General Description

The CD4528B is a dual monostable multivibrator. Each device is retriggerable and resettable. Triggering can occur from either the rising or falling edge of an input pulse, resulting in an output pulse over a wide range of widths. Pulse duration and accuracy are determined by external timing components Rx and Cx.

Features

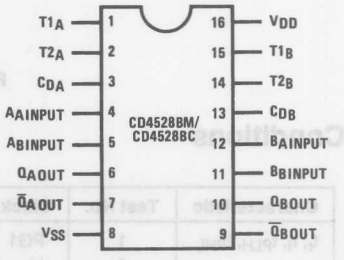
- Wide supply voltage range 3.0V to 18V
- Separate reset available
- Quiescent current = 5.0 nA/package (typ.) at 5.0 V_{DC}
- Diode protection on all inputs
- Triggerable from leading or trailing edge pulse
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range

Connection Diagrams



TL/F/5998–1

Dual-In-Line Package



TL/F/5998–2

Top View

Order Number CD4528B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage, All Inputs (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0V to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
CD4528BM	$-55°C$ to $+125°C$
CD4528BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4528BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5	0.005		5		150	μA
		$V_{DD} = 10V$		10	0.010		10		300	μA
		$V_{DD} = 15V$		20	0.015		20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$		0.05			0.05		0.05	V
		$V_{DD} = 10V$		0.05			0.05		0.05	V
		$V_{DD} = 15V$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10.0		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.25		−0.2	−0.36		−0.14		mA
		$V_{DD} = 10V, V_O = 9.5V$	−0.62		−0.5	−0.9		−0.35		mA
		$V_{DD} = 15V, V_O = 13.5V$	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

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DC Electrical Characteristics CD4528BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* CD4528BM

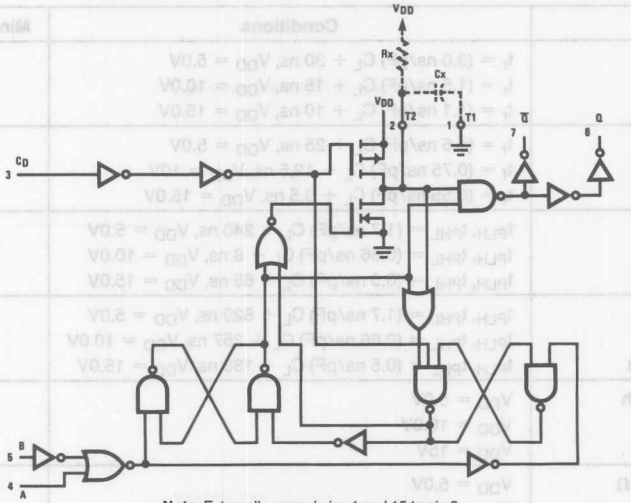
T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, Input t_r = t_f = 20 ns, unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Output Rise Time	t_r = (3.0 ns/pF) C_L + 30 ns, V_{DD} = 5.0V		180	400	ns
	t_r = (1.5 ns/pF) C_L + 15 ns, V_{DD} = 10.0V		90	200	ns
	t_r = (1.1 ns/pF) C_L + 10 ns, V_{DD} = 15.0V		65	160	ns
Output Fall Time	t_f = (1.5 ns/pF) C_L + 25 ns, V_{DD} = 5.0V		100	200	ns
	t_f = (0.75 ns/pF) C_L + 12.5 ns, V_{DD} = 10V		50	100	ns
	t_f = (0.55 ns/pF) C_L + 9.5 ns, V_{DD} = 15.0V		35	80	ns
Turn-Off, Turn-On Delay	t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns, V_{DD} = 5.0V		230	500	ns
A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 8 ns, V_{DD} = 10.0V		100	250	ns
Cx = 15 pF, Rx = 5.0 kΩ	t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns, V_{DD} = 15.0V		65	150	ns
Turn-Off, Turn-On Delay	t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns, V_{DD} = 5.0V		230	500	ns
A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns, V_{DD} = 10.0V		100	250	ns
Cx = 100 pF, Rx = 10 kΩ	t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns, V_{DD} = 15.0V		65	150	ns
Minimum Input Pulse Width	V_{DD} = 5.0V		60	150	ns
A or B	V_{DD} = 10.0V		20	50	ns
Cx = 15 pF, Rx = 5.0 kΩ	V_{DD} = 15V		20	50	ns
Cx = 1000 pF, Rx = 10 kΩ	V_{DD} = 5.0V		60	150	ns
	V_{DD} = 10.0V		20	50	ns
	V_{DD} = 15.0V		20	50	ns
Output Pulse Width Q or $\overline{Q}$	V_{DD} = 5.0V		550		ns
For Cx < 0.01 μF (See Graph for Appropriate V_{DD} Level)	V_{DD} = 10.0V		350		ns
Cx = 15 pF, Rx = 5.0 kΩ	V_{DD} = 15.0V		300		ns
For Cx > 0.01 μF Use	V_{DD} = 5.0V	15	29	45	μs
PW_{out} = 0.2 Rx Cx In [V_{DD} − V_{SS}]	V_{DD} = 10.0V	10	37	90	μs
Cx = 10,000 pF, Rx = 10 kΩ	V_{DD} = 15.0V	15	42	95	μs
Pulse Width Match between Circuits	V_{DD} = 5.0V		6	25	%
in the Same Package	V_{DD} = 10.0V		8	35	%
Cx = 10,000 pF, Rx = 10 kΩ	V_{DD} = 15.0V		8	35	%
Reset Propagation Delay,	V_{DD} = 5.0V		325	600	ns
t_{PLH}, t_{PHL}	V_{DD} = 10.0V		90	225	ns
Cx = 15 pF, Rx = 5.0 kΩ	V_{DD} = 15.0V		60	170	ns
Cx = 1000 pF, Rx = 10 kΩ	V_{DD} = 5.0V		7.0		μs
	V_{DD} = 10.0V		6.7		μs
	V_{DD} = 15.0V		6.7		μs
Minimum Retrigger Time	V_{DD} = 5.0V		0		ns
Cx = 15 pF, Rx = 5.0 kΩ	V_{DD} = 10.0V		0		ns
	V_{DD} = 15.0V		0		ns
Cx = 1000 pF, Rx = 10 kΩ	V_{DD} = 5.0V		0		ns
	V_{DD} = 10.0V		0		ns
	V_{DD} = 15.0V		0		ns

*AC parameters are guaranteed by DC correlated testing.

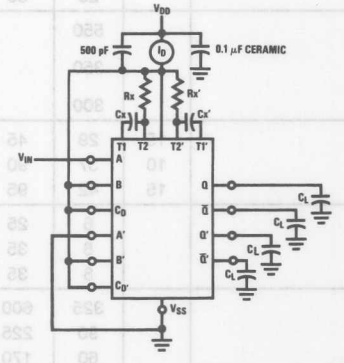
5

Logic Diagrams (½ of Device Shown)

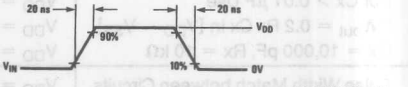


Note: Externally ground pins 1 and 15 to pin 8.

TL/F/5998–3



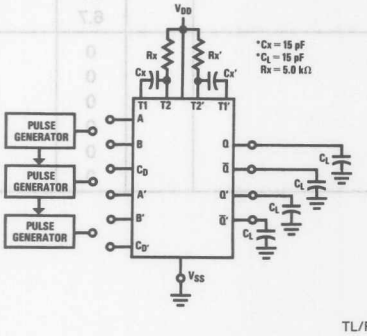
TL/F/5998–4



TL/F/5998–10

Duty Cycle = 50%

FIGURE 1. Power Dissipation Test Circuit and Waveforms



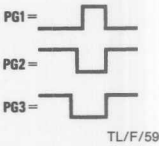
TL/F/5998–5

Input Connections

Characteristics	C_D	A	B
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, PW_{in}	PG3	PG1	PG2

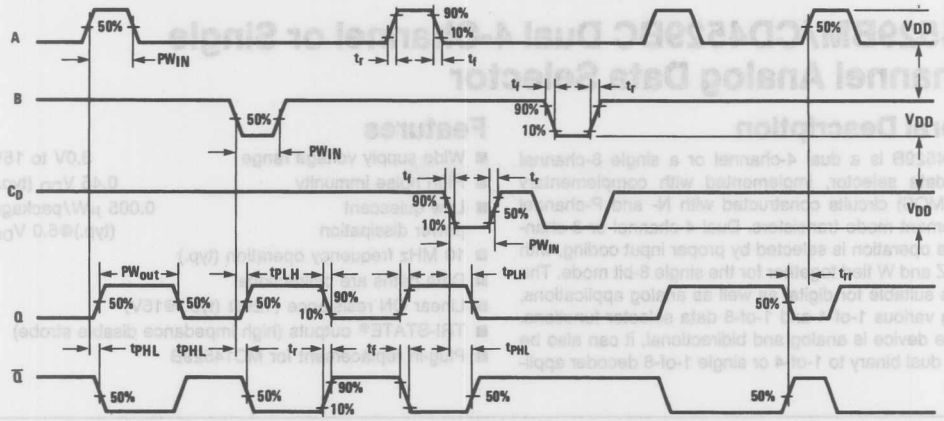
*Includes capacitance of probes, wiring, and fixture parasitic.

Note: AC test waveforms for PG1, PG2, and PG3 on next page.



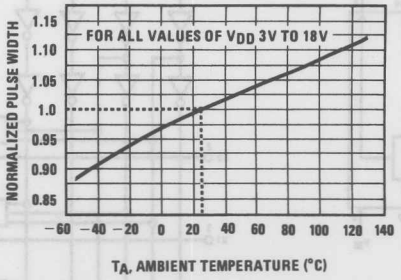
TL/F/5998–6

FIGURE 2. AC Test Circuit



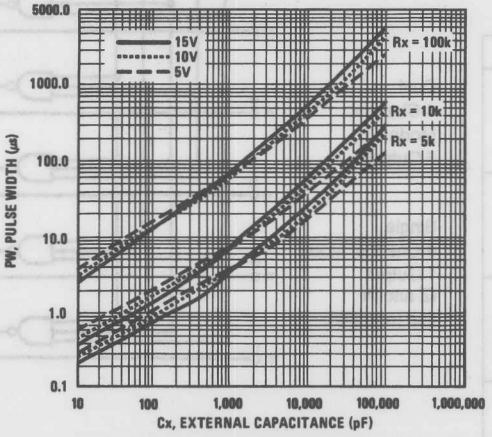
TL/F/5998–7

FIGURE 3. AC Test Waveforms



TL/F/5998–8

FIGURE 4. Normalized Pulse Width vs Temperature



TL/F/5998–9

FIGURE 5. Pulse Width vs Cx

5

National Semiconductor

CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector

General Description

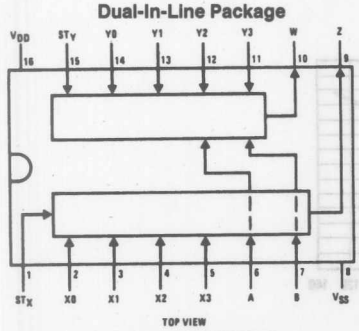
The CD4529B is a dual 4-channel or a single 8-channel analog data selector, implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. Dual 4-channel or 8-channel mode operation is selected by proper input coding, with outputs Z and W tied together for the single 8-bit mode. The device is suitable for digital as well as analog applications, including various 1-of-4 and 1-of-8 data selector functions. Since the device is analog and bidirectional, it can also be used for dual binary to 1-of-4 or single 1-of-8 decoder applications.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low quiescent power dissipation — 0.005 μW/package (typ.)@5.0 V_{DC}
- 10 MHz frequency operation (typ.)
- Data paths are bidirectional
- Linear ON resistance [120Ω (typ.)@15V]
- TRI-STATE® outputs (high impedance disable strobe)
- Plug-in replacement for MC14529B

Connection Diagram

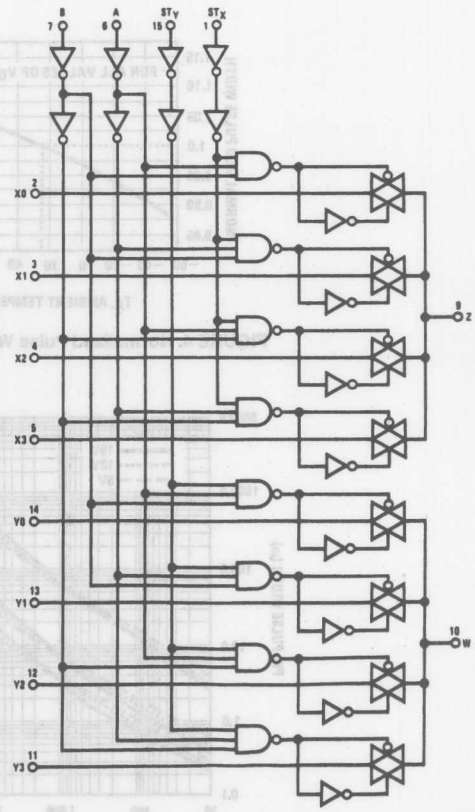
Dual-In-Line Package



Order Number CD4529B*

*Please look into Section 8, Appendix D for availability of various package types.

Logic Diagram



TL/F/5999–1

Truth Table

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance (TRI-STATE)		

X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0 to V_{DD}
Operating Temperature Range (T_A)	
CD4529BM	−55°C to +125°C
CD4529BC	−40°C to +85°C

DC Electrical Characteristics CD4529BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.001	1.0		60	μA
		V_{DD} = 10V		1.0		0.002	1.0		60	μA
		V_{DD} = 15V		2.0		0.003	2.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		400		165	480		640	Ω
		V_{IN} = −5V		400		100	480		640	Ω
		V_{IN} = ±0.25V		400		155	480		640	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		240		135	270		400	Ω
		V_{IN} = −7.5V		240		75	270		400	Ω
		V_{IN} = ±0.25V		240		100	270		400	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		400		165	480		640	Ω
		V_{IN} = 0.25V		400		100	480		640	Ω
		V_{IN} = 5.6V		400		160	480		640	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		400	Ω
		V_{IN} = 0.25V		250		75	270		400	Ω
		V_{IN} = 9.3V		250		110	270		400	Ω
I_{OFF}	Input to Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V, V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −5V, V_{DD} = 5V, V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±2500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±2500	nA

DC Electrical Characteristics CD4529BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.001	5.0		70	μA
		V_{DD} = 10V		5.0		0.002	5.0		70	μA
		V_{DD} = 15V		10.0		0.003	10.0		140	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5.00		4.95		V
		V_{DD} = 10V	9.95		9.95	10.00		9.95		V
		V_{DD} = 15V	14.95		14.95	15.00		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V, V_{OUT} = 4.5 or 0.5 V_{DC}		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_{OUT} = 9.0 or 1.0 V_{DC}		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_{OUT} = 13.5 or 1.5 V_{DC}		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V, V_{OUT} = 0.5 or 4.5 V_{DC}	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_{OUT} = 1.0 or 9.0 V_{DC}	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_{OUT} = 1.5 or 13.5 V_{DC}	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		410		165	480		560	Ω
		V_{IN} = −5V		410		100	480		560	Ω
		V_{IN} = ±0.25V		410		155	480		560	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		250		135	270		350	Ω
		V_{IN} = −7.5V		250		75	270		350	Ω
		V_{IN} = ±0.25V		250		100	270		350	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		410		165	480		560	Ω
		V_{IN} = 0.25V		410		100	480		560	Ω
		V_{IN} = 5.6V		410		160	480		560	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		350	Ω
		V_{IN} = 0.25V		250		75	270		350	Ω
		V_{IN} = 9.3V		250		110	270		350	Ω
I_{OFF}	Input-Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V								
		V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±500	nA
		V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V								
		V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±1000	nA
		V_{IN} = −7.5V, V_{OUT}=7.5V		±250		±0.0015	±250		±1000	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

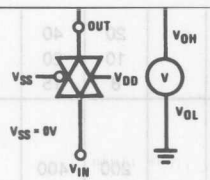
Note 3: Switch OFF is defined as $|I_O| \leq 10$ μA, switch ON as defined by R_{ON} specification.

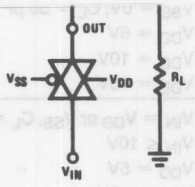
AC Characteristics* CD4529BM/CD4539BC

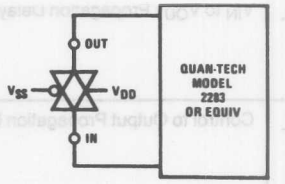
$T_A = 25°C$, $R_L = 1\ k\Omega$, $t_r = t_f = 20$ ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	V_{IN} to V_{OUT} Propagation Delay	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		10	20	ns
		$V_{DD} = 15V$		8	15	ns
t_{PLH}, t_{PHL}	Control to Output Propagation Delay	$V_{IN} = V_{DD}$ or V_{SS}, $C_L = 50$ pF				
		$V_{IN} \leq 10V$				
		$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		50	120	ns
f_{MAX}	Maximum Control Input Pulse Frequency	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		5		MHz
		$V_{DD} = 10V$		10		MHz
		$V_{DD} = 15V$		12		MHz
	Crosstalk, Control to Output	$R_{OUT} = 10\ k\Omega$, $C_L = 50$ pF, $V_{SS} = 0$				
		$V_{DD} = 5V$		5.0		mV
		$V_{DD} = 10V$		5.0		mV
		$V_{DD} = 15V$		5.0		mV
	Noise Voltage	$f = 100$ Hz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		24		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		25		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		30		$nV/\sqrt{cycle}$
		$f = 100$ kHz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		15		$nV/\sqrt{cycle}$
	Sine Wave (Distortion)	$V_{IN} = 1.77$Vrms Centered at 0V, $R_L = 10\ k\Omega$, $f = 1$ kHz, $V_{SS} = -5V$, $V_{DD} = 5V$		0.36		%
I_{LOSS}	Insertion Loss, $I_{LOSS} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$	$V_{IN} = 177$Vrms Centered at 0V, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$		2.0		dB
		$R_L = 10\ k\Omega$		0.8		dB
		$R_L = 100\ k\Omega$		0.25		dB
		$R_L = 1\ M\Omega$		0.01		dB
BW	Bandwidth, -3dB	$V_{IN} = 177$Vrms Centered at 0 Vdc, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	35			MHz
		$R_L = 10\ k\Omega$	28			MHz
		$R_L = 100\ k\Omega$	27			MHz
		$R_L = 1\ M\Omega$	26			MHz
	Feedthrough and Crosstalk, $20 \log_{10} \frac{V_{OUT}}{V_{IN}} = -50$ db	$V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	850			kHz
		$R_L = 10\ k\Omega$	100			kHz
		$R_L = 100\ k\Omega$	12			kHz
		$R_L = 1\ M\Omega$	1.5			Khz

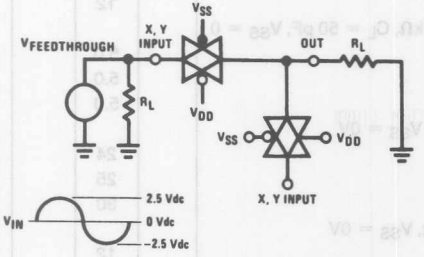
*AC Parameters are guaranteed by DC correlated testing.



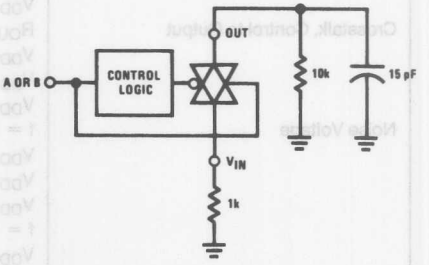




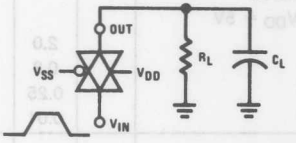
Frequency Response

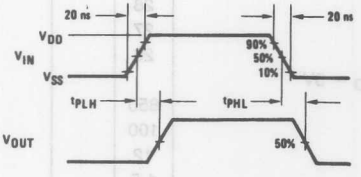


Crosstalk

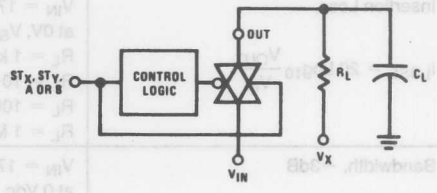


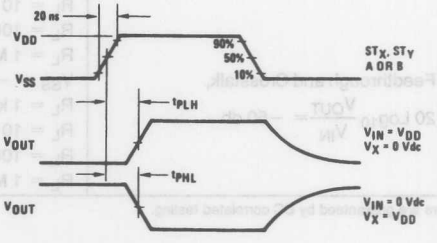
Propagation Delay



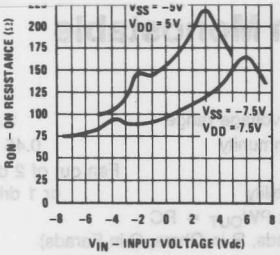


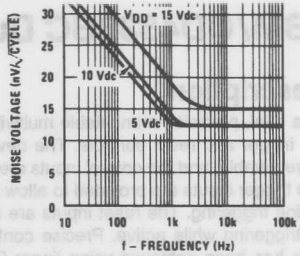
Turn-ON Delay Time



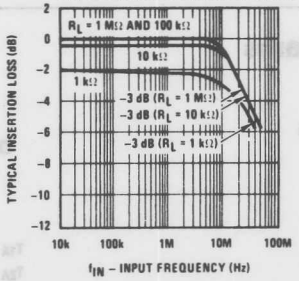


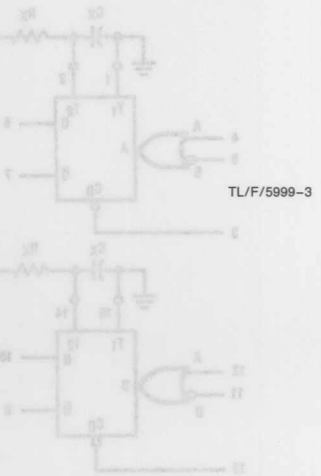
TL/F/5999–2





Typical Insertion Loss/ Bandwidth Characteristics





TL/F/5999–3

5

National Semiconductor

CD4538BM/CD4538BC Dual Precision Monostable

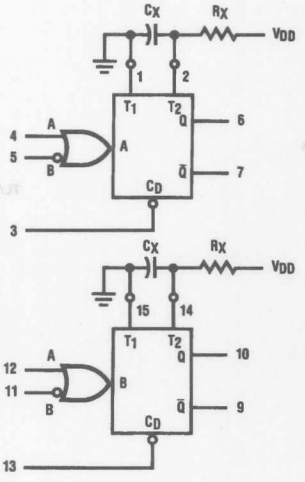
General Description

The CD4538B is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active low and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- New formula: $PW_{OUT} = RC$ (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range — 1 μs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current — 5 nA (typ.) @ 5 V_{DC}
- Pin compatible to CD4528B

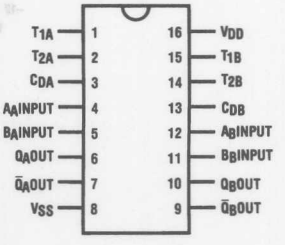
Block and Connection Diagrams



TL/F/6000–1

R_X and C_X are External Components
V_{DD} = Pin 16
V_{SS} = Pin 8

Dual-In-Line Package
CD4538BM
CD4538BC



TL/F/6000–2

Top View

Order Number CD4538B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	-0.5 to $+18$ V_{DC}
Input Voltage (V_{IN})	$-0.5V$ to $V_{DD} + 0.5$ V_{DC}
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4538BM	$-55°C$ to $+125°C$
CD4538BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4538BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{DD} = 10V$, $V_{DD} = 15V$; $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, All Outputs Open		5		0.005	5		150	μA
				10		0.010	10		300	μA
				20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$, $V_{DD} = 10V$, $V_{DD} = 15V$; $\|I_O\| < 1$ μA, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
				0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$, $V_{DD} = 10V$, $V_{DD} = 15V$; $\|I_O\| < 1$ μA, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	4.95		4.95	5		4.95		V
			9.95		9.95	10		9.95		V
			14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1$ μA								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$; $V_{DD} = 10V$, $V_O = 0.5V$; $V_D = 15V$, $V_O = 1.5V$; $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	0.64		0.51	0.88		0.36		mA
			1.6		1.3	2.25		0.9		mA
			4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$; $V_{DD} = 10V$, $V_O = 9.5V$; $V_D = 15V$, $V_O = 13.5V$; $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	−0.64		−0.51	−0.88		−0.36		mA
			−1.6		−1.3	−2.25		−0.9		mA
			−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current, Pin 2 or 14	$V_{DD} = 15V$, $V_{IN} = 0V$ or $15V$		±0.02		$±10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current Other Inputs	$V_{DD} = 15V$, $V_{IN} = 0V$ or $15V$		±0.1		$±10^{-5}$	±0.1		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for acutal device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4538BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{DD} = 10V, V_{DD} = 15V; $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, All Outputs Open		20		0.005	20		150	μA
				40		0.010	40		300	μA
				80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V; $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V; $\lvert I_O \rvert < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O \rvert < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_D = 15V, V_O = 1.5V; $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_D = 15V, V_O = 13.5V; $V_{IL} = V_{SS}$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current, Pin 2 or 14	V_{DD} = 15V, V_{IN} = 0V or 15V		±0.02		$\pm 10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current Other Inputs	V_{DD} = 15V, V_{IN} = 0V or 15V		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for acutal device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

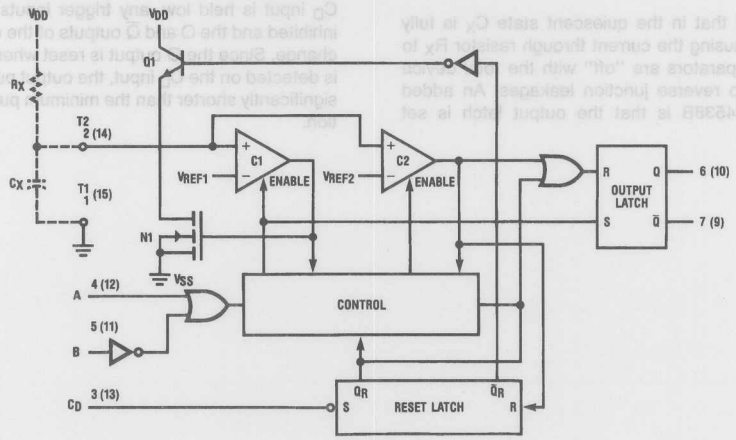
AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, and $t_r = t_f = 20$ ns unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{TLH}, t_{THL}	Output Transition Time	$V_{DD} = 5V$			100	200	ns
		$V_{DD} = 10V$			50	100	ns
		$V_{DD} = 15V$			40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Trigger Operation— A or B to Q or $\overline{Q}$					
		$V_{DD} = 5V$			300	600	ns
		$V_{DD} = 10V$			150	300	ns
		$V_{DD} = 15V$			100	220	ns
		Reset Operation— C_D to Q or $\overline{Q}$					
		$V_{DD} = 5V$			250	500	ns
		$V_{DD} = 10V$			125	250	ns
		$V_{DD} = 15V$			95	190	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width A, B, or C_D	$V_{DD} = 5V$			35	70	ns
		$V_{DD} = 10V$			30	60	ns
		$V_{DD} = 15V$			25	50	ns
t_{RR}	Minimum Retrigger Time	$V_{DD} = 5V$				0	ns
		$V_{DD} = 10V$			0	0	ns
		$V_{DD} = 15V$				0	ns
C_{IN}	Input Capacitance	Pin 2 or 14			10		pF
		Other Inputs			5	7.5	pF
PW_{OUT}	Output Pulse Width (Q or $\overline{Q}$) (**Note:** For Typical Distribution, see *Figure 9*)	$R_X = 100$ kΩ, $C_X = 0.002$ μF	$V_{DD} = 5V$	208	226	244	μs
			$V_{DD} = 10V$	211	230	248	μs
			$V_{DD} = 15V$	216	235	254	μs
		$R_X = 100$ kΩ, $C_X = 0.1$ μF	$V_{DD} = 5V$	8.83	9.60	10.37	ms
			$V_{DD} = 10V$	9.02	9.80	10.59	ms
			$V_{DD} = 15V$	9.20	10.00	10.80	ms
		$R_X = 100$ kΩ, $C_X = 10.0$ μF	$V_{DD} = 5V$	0.87	0.95	1.03	s
			$V_{DD} = 10V$	0.89	0.97	1.05	s
			$V_{DD} = 15V$	0.91	0.99	1.07	s
Pulse Width Match between Circuits in the Same Package $C_X = 0.1$ μF, $R_X = 100$ kΩ		$R_X = 100$ kΩ, $C_X = 0.1$ μF	$V_{DD} = 5V$		±1		%
			$V_{DD} = 10V$		±1		%
			$V_{DD} = 15V$		±1		%
Operating Conditions							
R_X	External Timing Resistance			5.0		**	kΩ
C_X	External Timing Capacitance			0		No Limit	pF

*AC parameters are guaranteed by DC correlated testing.

**The maximum usable resistance R_X is a function of the leakage of the Capacitor C_X, leakage of the CD4538B, and leakage due to board layout, surface resistance, etc.

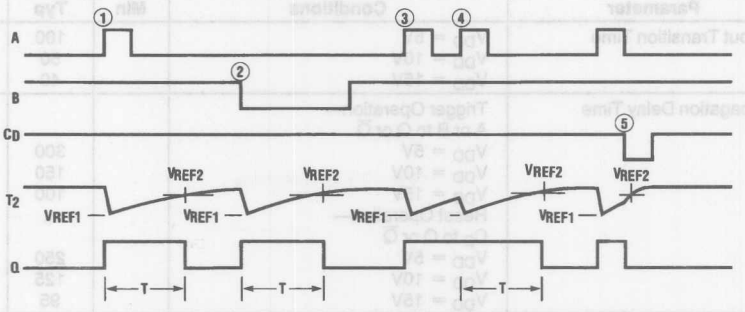
Logic Diagram



TL/F/6000–3

FIGURE 1

Theory of Operation



TL/F/6000–4

FIGURE 2

Trigger Operation

The block diagram of the CD4538B is shown in *Figure 1*, with circuit operation following.

As shown in *Figures 1* and *2*, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})②.

It should be noted that in the quiescent state C_X is fully charged to V_{DD}, causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

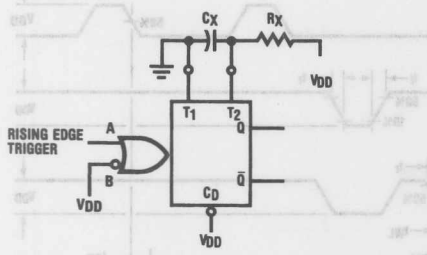
Retrigger Operation

The CD4538B is retriggered if a valid trigger occurs③ followed by another valid trigger④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated④, the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

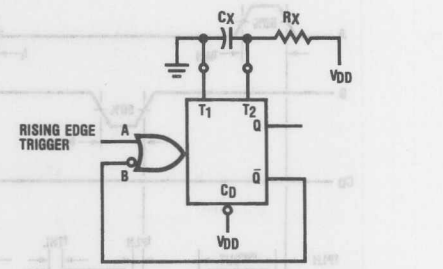
Reset Operation

The CD4538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

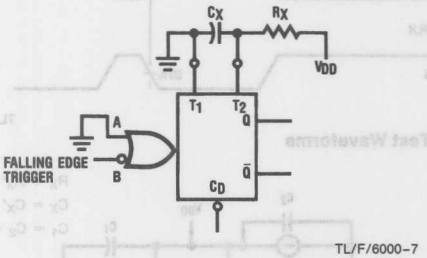
Typical Applications



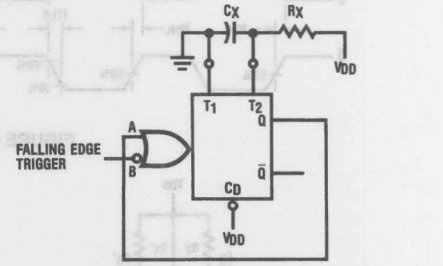
TL/F/6000–5



TL/F/6000–6



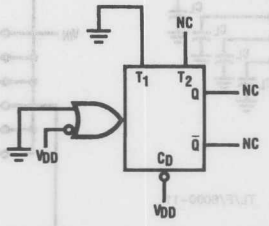
TL/F/6000–7



TL/F/6000–8

FIGURE 3. Retriggerable Monostables Circuitry

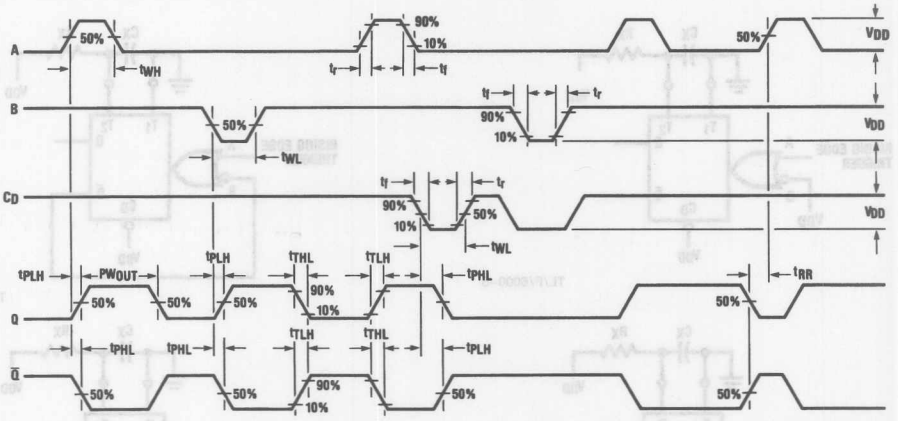
FIGURE 4. Non-Retriggerable Monostables Circuitry



TL/F/6000–9

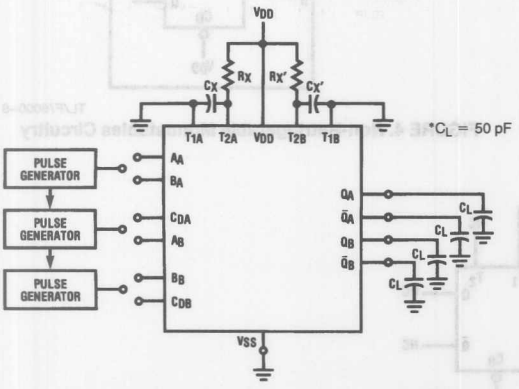
FIGURE 5. Connection of Unused Sections

Typical Applications (Continued)

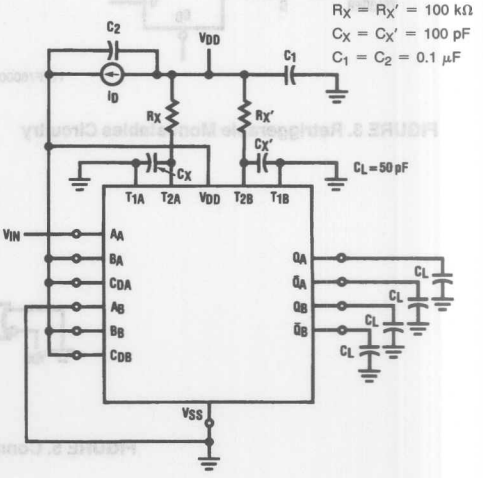


TL/F/6000–10

FIGURE 6. Switching Test Waveforms



TL/F/6000–11



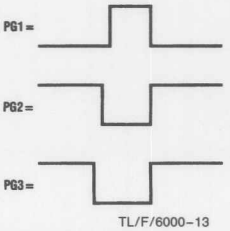
TL/F/6000–12

Input Connections

Characteristics	CD	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL} PW_{OUT}, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

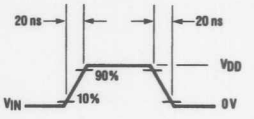
*Includes capacitance of probes, wiring, and fixture parasitic

Note: Switching test waveforms for PG1, PG2, PG3 are shown in *Figure 6.*



TL/F/6000–13

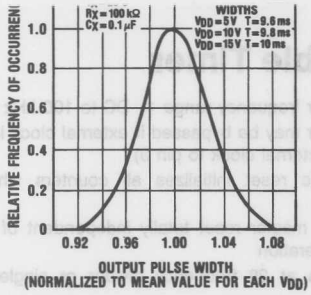
FIGURE 7. Switching Test Circuit



TL/F/6000–14

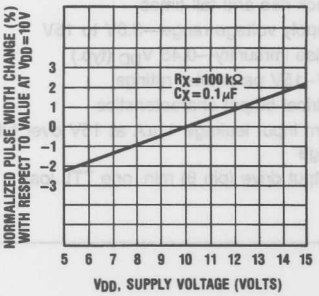
Duty Cycle = 50%

FIGURE 8. Power Dissipation Test Circuit and Waveforms



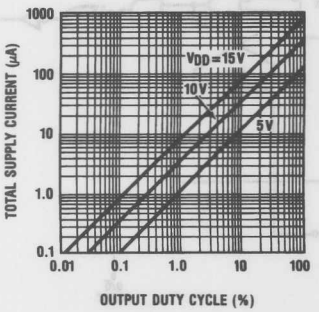
TL/F/6000–15

FIGURE 9. Typical Normalized Distribution of Units for Output Pulse Width



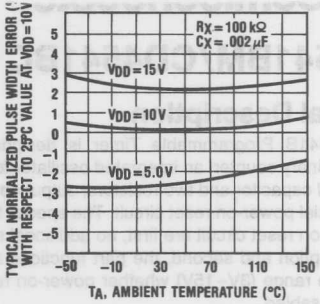
TL/F/6000–17

FIGURE 10. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}



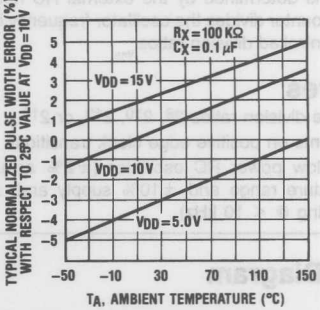
TL/F/6000–19

FIGURE 11. Typical Total Supply Current Versus Output Duty Cycle, R_X = 100 kΩ, C_L = 50 pF, C_X = 100 pF, One Monostable Switching Only



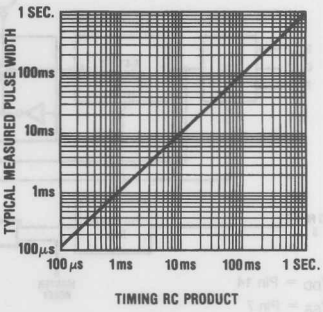
TL/F/6000–16

FIGURE 12. Typical Pulse Width Error Versus Temperature



TL/F/6000–18

FIGURE 13. Typical Pulse Width Error Versus Temperature



TL/F/6000–20

FIGURE 14. Typical Pulse Width Versus Timing RC Product

5

National Semiconductor

CD4541BM/CD4541BC Programmable Timer

General Description

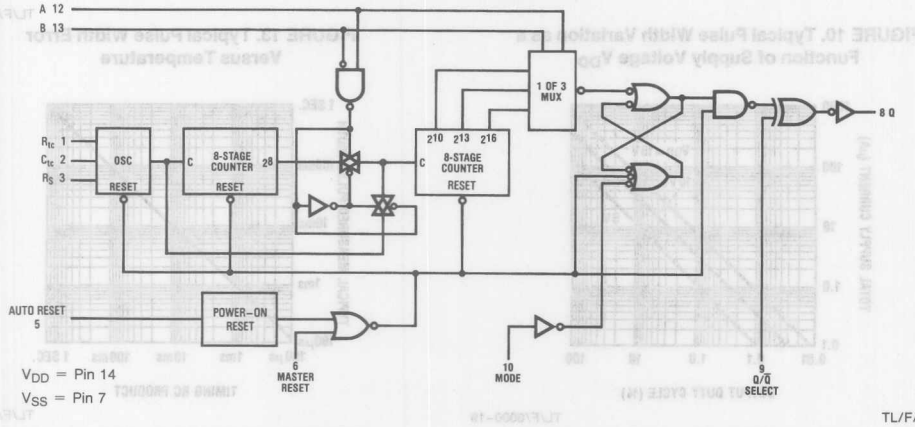
The CD4541B Programmable Timer is designed with a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The special features of the power-on reset circuit are first, no additional static power consumption and second, the part functions across the full voltage range (3V–15V) whether power-on reset is enabled or disabled.

Timing and the counter are initialized by turning on power, if the power-on reset is enabled. When the power is already on, an external reset pulse will also initialize the timing and counter. After either reset is accomplished, the oscillator frequency is determined by the external RC network. The 16-stage counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

Features

- Available division ratios 2^8, 2^{10}, 2^{13}, or 2^{16}
- Increments on positive edge clock transitions
- Built-in low power RC oscillator (±2% accuracy over temperature range and ±10% supply and ±3% over processing @ < 10 kHz)
- Oscillator frequency range ≈ DC to 100 kHz
- Oscillator may be bypassed if external clock is available (apply external clock to pin 3)
- Automatic reset initializes all counters when power turns on
- External master reset totally independent of automatic reset operation
- Operates at 2^n frequency divider or single transition timer
- Q/$\overline{Q}$ select provides output logic level flexibility
- Reset (auto or master) disables oscillator during resetting to provide no active power dissipation
- Clock conditioning circuit permits operation with very slow clock rise and fall times
- Wide supply voltage range—3.0V to 15V
- High noise immunity—0.45 V_{DD} (typ.)
- 5V–10V–15V parameter ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range
- High output drive (pin 8) min. one TTL load

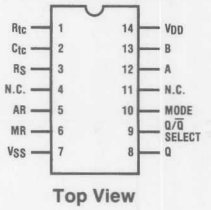
Logic Diagram



TL/F/6001–1

Connection Diagram

Dual-In-Line Package



N.C.—Not connected

Top View

TL/F/6001–2

Order Number CD4541B*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD})	−0.5V to +18V
Input Voltage (V_{IN})	−0.5V to V_{DD} +0.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (soldering, 10 sec.)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage (V_{DD})	3V to 15V
Input Voltage (V_{IN})	0 to V_{DD}
Operating Temperature Range	
CD4541BM	−55°C to +125°C
CD4541BC	−40°C to +85°C

DC Electrical Characteristics (Note 2)—CD4541BM

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.005	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.010	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	2.85		2.27	3.6		1.6		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	4.96		4.0	9.0		2.8		mA
		V_{DD} = 15V, V_O = 1.5V	19.3		15.6	34.0		10.9		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 2.5V	7.96		6.42	13.0		4.49		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	4.19		3.38	8.0		2.37		mA
		V_{DD} = 15V, V_O = 3.5V	16.3		13.2	30.0		9.24		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2)—CD4541BC

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.005	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.010	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V $\lvert I_O \rvert$ < 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V

5

DC Electrical Characteristics (Note 2)—CD4541BC (Continued)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	2.32		1.96	3.6		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	3.18		2.66	9.0		2.18		mA
		V_{DD} = 15V, V_O = 1.5V	12.4		10.4	34.0		8.50		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 2.5V	5.1		4.27	130		3.5		mA
		V_{DD} = 10V, V_O = 9.5V	2.69		2.25	8.0		1.85		mA
		V_{DD} = 15V, V_O = 13.5V	10.5		8.8	30.0		7.22		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF (refer to test circuits)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Output Rise Time	V_{DD} = 5V		50	200	ns
		V_{DD} = 10V		30	100	ns
		V_{DD} = 15V		25	80	ns
t_{THL}	Output Fall Time	V_{DD} = 5V		50	200	ns
		V_{DD} = 10V		30	100	ns
		V_{DD} = 15V		25	80	ns
t_{PLH}, t_{PHL}	Turn-Off, Turn-On Propagation Delay, Clock to Q (2^8 Output)	V_{DD} = 5V		1.8	4.0	μs
		V_{DD} = 10V		0.6	1.5	μs
		V_{DD} = 15V		0.4	1.0	μs
t_{PHL}, t_{PLH}	Turn-On, Turn-Off Propagation Delay, Clock to Q (2^{16} Output)	V_{DD} = 5V		3.2	8.0	μs
		V_{DD} = 10V		1.5	3.0	μs
		V_{DD} = 15V		1.0	2.0	μs
$t_{WH(CL)}$	Clock Pulse Width	V_{DD} = 5V	400	200		ns
		V_{DD} = 10V	200	100		ns
		V_{DD} = 15V	150	70		ns
f_{CL}	Clock Pulse Frequency	V_{DD} = 5V		2.5	1.0	MHz
		V_{DD} = 10V		6.0	3.0	MHz
		V_{DD} = 15V		8.5	4.0	MHz
$t_{WH(R)}$	MR Pulse Width	V_{DD} = 5V	400	170		ns
		V_{DD} = 10V	200	75		ns
		V_{DD} = 15V	150	50		ns
C_I	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)			100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Truth Table

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

Division Ratio Table

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

Operating Characteristics

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f = \frac{1}{2.3\, R_{tc} C_{tc}} \text{ if } (1\text{ kHz} \leq f \leq 100\text{ kHz})$$

and $R_S \approx 2\, R_{tc}$ where $R_S \geq 10\text{ k}\Omega$

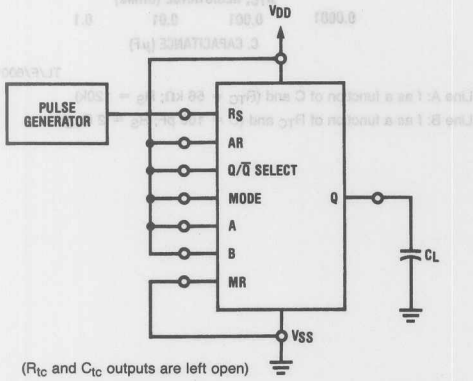
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13}, and 2^{16}). The 2^n counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is "1", 2^{16} is selected for both states of B.

However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0". Correspondingly, when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

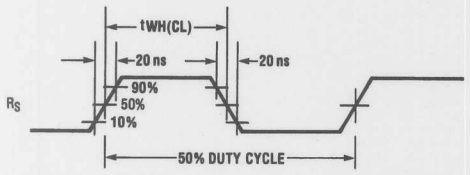
When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

Power Dissipation Test Circuit and Waveforms



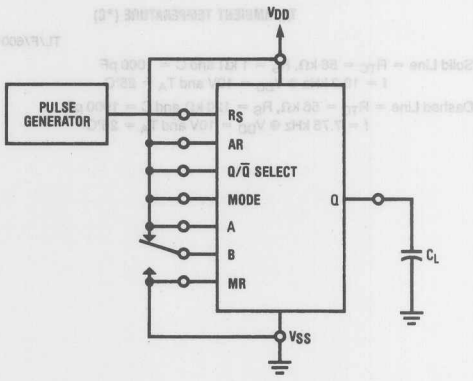
(R_{tc} and C_{tc} outputs are left open)

TL/F/6001–3

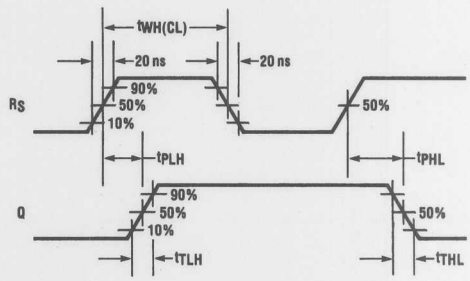


TL/F/6001–5

Switching Time Test Circuit and Waveforms



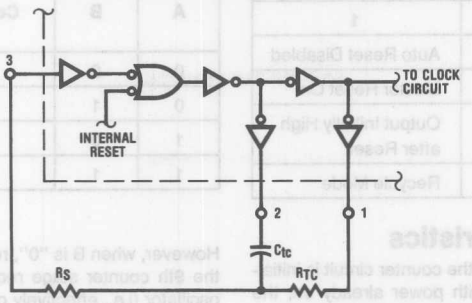
TL/F/6001–4



TL/F/6001–6

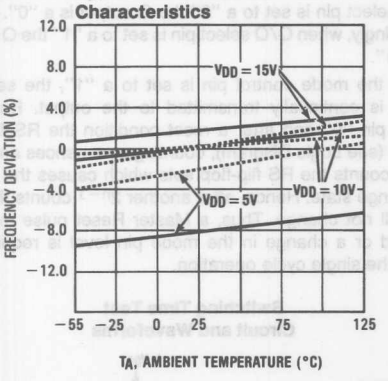
Operating Characteristics (Continued)

Oscillator Circuit Using RC Configuration



TL/F/6001–7

Typical RC Oscillator Characteristics

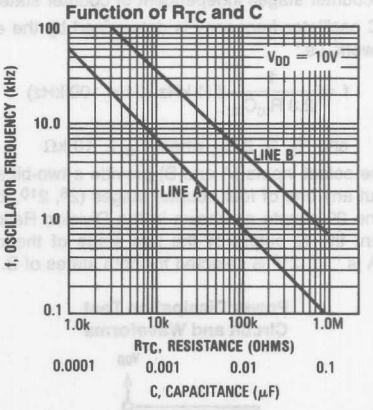


TL/F/6001–8

Solid Line = R_{TC} = 56 kΩ, R_S = 1 kΩ and C = 1000 pF
f = 10.2 kHz @ V_{DD} = 10V and T_A = 25°C

Dashed Line = R_{TC} = 56 kΩ, R_S = 120 kΩ and C = 1000 pF
f = 7.75 kHz @ V_{DD} = 10V and T_A = 25°C

RC Oscillator Frequency as a Function of R_{TC} and C



TL/F/6001–9

Line A: f as a function of C and (R_{TC} = 56 kΩ; R_S = 120k)

Line B: f as a function of R_{TC} and (C = 100 pF; R_S = 2 R_{TC})

National Semiconductor

CD4543BM/CD4543BC BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals

General Description

The CD4543BM/CD4543BC is a monolithic CMOS BCD-to-7-segment latch/decoder/driver for use with liquid crystal and other types of displays. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-7-segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI) and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display, and the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features
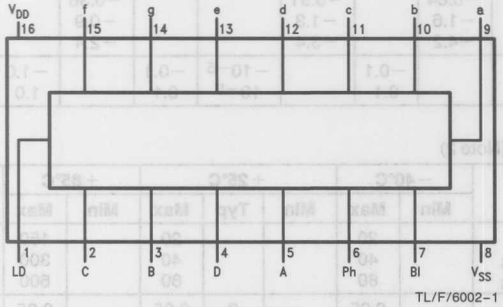
- Wide supply voltage range — 3.0V to 18V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L or 1 driving 74LS
- Low power dissipation — 50 nA/package (typ.) at $V_{DD} = 5.0V$
- Latch storage
- Blanking input
- Blank for all illegal inputs
- Direct-drive LCD, LED and VF displays
- Pin-for-pin replacement for CD4056B (with pin 7 tied to V_{SS})
- Pin-for-pin replacement for Motorola MC14543B

Applications

- Instrument (e.g., counter, DVM, etc.) display driver
- Computer/calculator display driver
- Cockpit display driver
- Various clock, watch, and timer users

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/6002–1

Top View

Order Number CD4543B*

*Please look into Section 8, Appendix D for availability of various package types.

Inputs							Outputs							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as Above

X = Don't care

† = Above combinations

* = For liquid crystal readouts, apply a square wave to Ph. For common cathode LED readouts, select Ph = 0. For common anode LED readouts, select Ph = 1.

** = Depends upon the BCD code previously applied when LD = 1.

Display Format



TL/F/6002–2

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD}) $-0.5\ V_{DC}$ to $+18\ V_{DC}$

Input Voltage (V_{IN}) $-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$

Storage Temp. Range (T_S) $-65°C$ to $+150°C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD}) $3\ V_{DC}$ to $15\ V_{DC}$

Input Voltage (V_{IN}) $0\ V_{DC}$ to $V_{DD}\ V_{DC}$

Operating Temperature Range (T_A)

CD4543BM $-55°C$ to $+125°C$

CD4543BC $-40°C$ to $+85°C$

DC Electrical Characteristics CD4543BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		5			5		150	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		10			10		300	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51			0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3			0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4			2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51			−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3			−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4			−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4543BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS}		20			20		150	μA
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS}		40			40		300	μA
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5V$ } $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$ } $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$ } $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5			1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0			3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5			3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0			7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.52		0.44			0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.3		1.1			0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	3.6		3.0			2.4		mA

DC Electrical Characteristics CD4543BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		+25°			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF, V_{SS} = 0, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_r	Output Rise Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_f	Output Fall Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}	Turn-ON Propagation Delay Time	V_{DD} = 5V		450	1100	ns
		V_{DD} = 10V		170	440	ns
		V_{DD} = 15V		110	330	ns
t_{PHL}	Turn-OFF Propagation Delay Time	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		180	440	ns
		V_{DD} = 15V		120	330	ns
t_{SET-UP}	Set-Up Time	V_{DD} = 5V		−5	80	ns
		V_{DD} = 10V		−2	30	ns
		V_{DD} = 15V		0	20	ns
t_{HOLD}	Hold Time	V_{DD} = 5V		30	120	ns
		V_{DD} = 10V		20	45	ns
		V_{DD} = 15V		15	30	ns
PW_{LD}	Latch Disable Pulse Width	V_{DD} = 5V		50	250	ns
		V_{DD} = 10V		30	100	ns
		V_{DD} = 15V		20	80	ns
C_{IN}	Input Capacitance	Per Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	See C_{PD} Measurement Waveforms (Note 4)		300		pF

*AC Parameters are guaranteed by DC correlated testing.

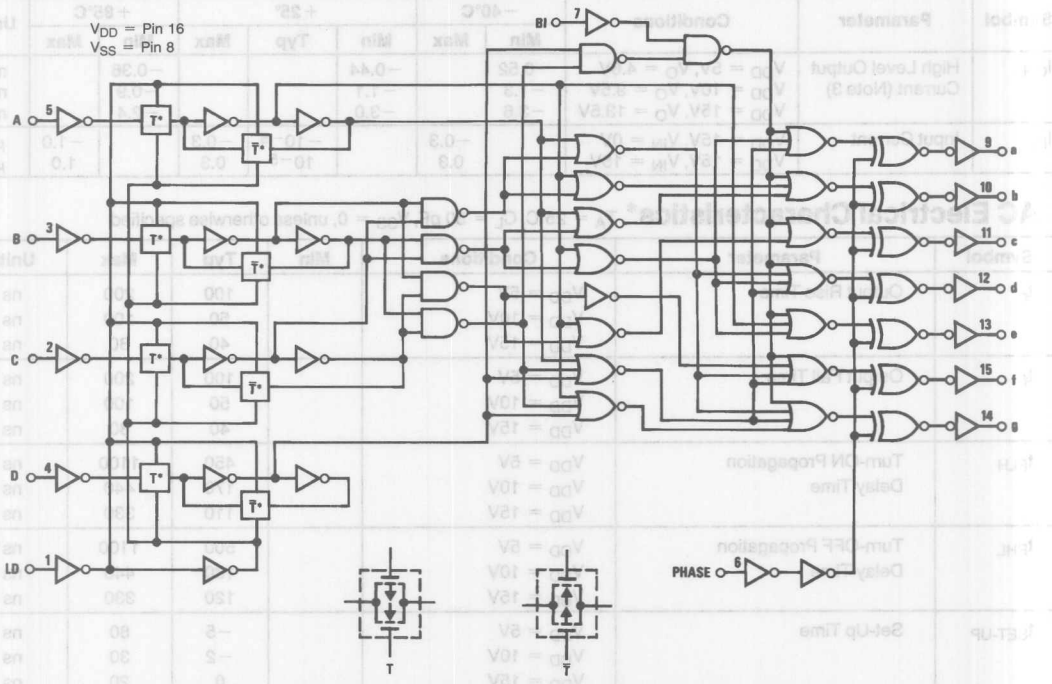
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of a CMOS device. For a complete explanation, see "MM54C/74C Family Characteristics" Application Note AN-90.

Logic Diagram

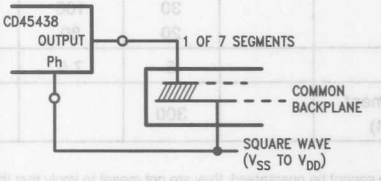


*Transmission gates

TL/F/6002–3

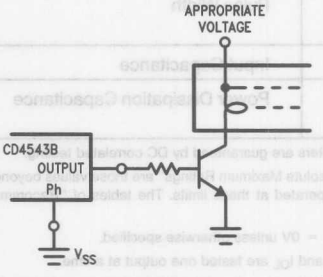
Typical Applications

Liquid Crystal (LC) Readout



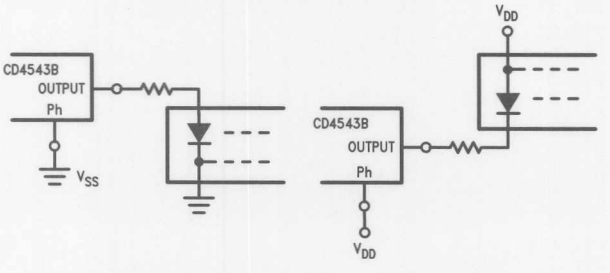
TL/F/6002–4

Incandescent Readout



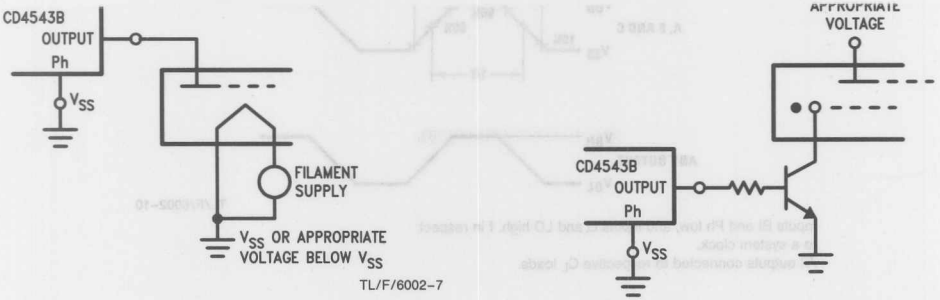
TL/F/6002–5

Light Emitting Diode (LED) Readout



TL/F/6002–6

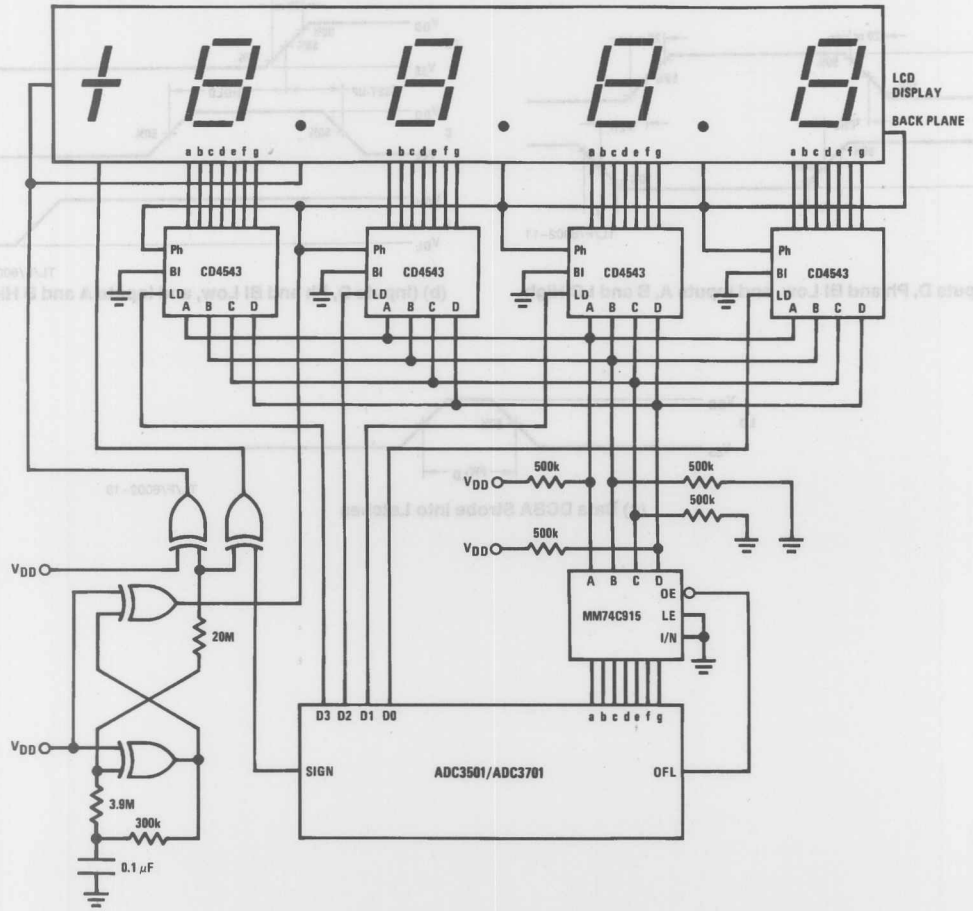
Note: Bipolar transitors may be added for gain (for $V_{DD} \leq 10V$ or $I_{OUT} \geq 10$ mA)



TL/F/6002–7

TL/F/6002–8

3½-Digit DVM with LCD Display

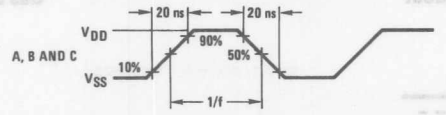


TL/F/6002–9

Display 9.999 when overflowed. All digits can also be blanked at overflow by typing OFL to BI on the CD4543's.

Switching Time Waveforms

C_{PD} Measurement Waveforms

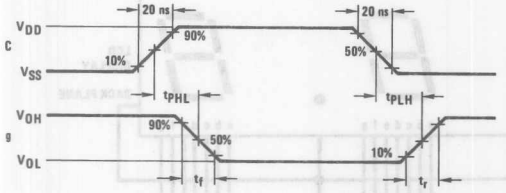




TL/F/6002–10

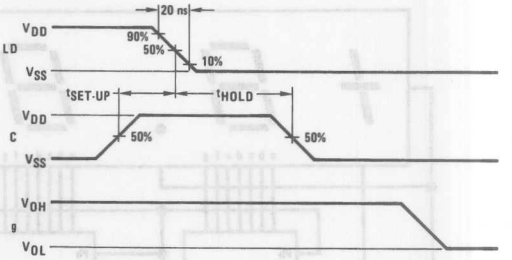
Inputs BI and Ph low, and inputs D and LD high. f in respect to a system clock.
All outputs connected to respective C_L loads.

Dynamic Signal Waveforms



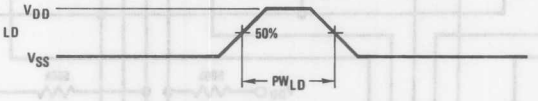
TL/F/6002–11

(a) Inputs D, Ph and BI Low, and Inputs A, B and LD High



TL/F/6002–12

(b) (Inputs D, Ph and BI Low, and Inputs A and B High



TL/F/6002–13

(c) Data DCBA Strobe into Latches

National Semiconductor

CD4723BM/CD4723BC Dual 4-Bit Addressable Latch
CD4724BM/CD4724BC 8-Bit Addressable Latch

General Description

The CD4723B is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0, A1), an active low enable input ($\overline{E}$), and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0–Q3). The CD4724B is an 8-bit addressable latch with three address inputs (A0–A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D) and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

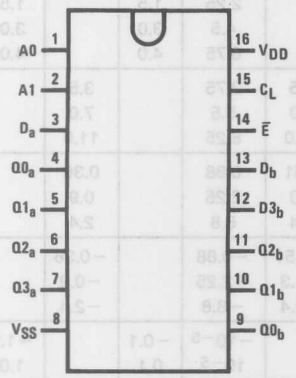
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high and enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Connection Diagrams

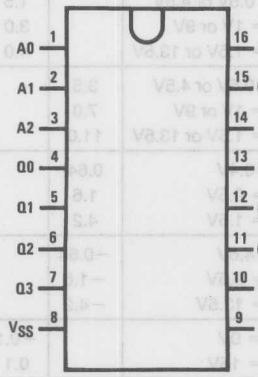
CD4723B
Dual-In-Line Package



TL/F/6003–1

Top View

CD4724B
Dual-In-Line Package



TL/F/6003–2

Top View

Order Number CD4723B* or CD4724B*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Mode Selection				
$\overline{E}$	CL	Addressed Latch	Unaddressed Latch	Mode
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Hold Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to '0"	Reset to "0"	Clear

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

DC Supply Voltage (V_{DD}) $-0.5V$ to $+18\ V_{DC}$
Input Voltage (V_{IN}) $-0.5V$ to $V_{DD} + 0.5\ V_{DC}$
Storage Temperature (T_S) $-65°C$ to $+150°C$
Power Dissipation (P_D)
Dual-In-Line 700 mW
Small Outline 500 mW
Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD}) 3.0V to 15 V_{DC}
Input Voltage (V_{IN}) 0V to V_{DD} V_{DC}
Operating Temperature Range (T_A)
CD4723BM/CD4724BM $-55°C$ to $+125°C$
CD4723BC/CD4724BC $-40°C$ to $+85°C$

DC Electrical Characteristics CD4723BM/CD4724BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$		5.0		0.02	5.0		150	μA
		$V_{DD} = 10V$		10		0.02	10		300	μA
		$V_{DD} = 15V$		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V, V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10V, V_O = 0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD} = 15V, V_O = 1.5V$	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10V, V_O = 9.5V$	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD} = 15V, V_O = 13.5V$	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4723BC/CD4724BC (Note 2)

Symbol	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.02	20		150	μA
		V_{DD} = 10V		40		0.02	40		300	μA
		V_{DD} = 15V		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1$ μA								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics*

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Data to Output	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	V_{DD} = 5V		225	450	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
T_{WH}, T_{WL}	Minimum Data Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		65	125	ns
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		75	150	ns
		V_{DD} = 10V		40	75	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Setup Time Data to E	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		20	40	ns
		V_{DD} = 15V		15	30	ns
t_H	Minimum Hold Time Data to E	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Setup Time Address to E	V_{DD} = 5V		−15	50	ns
		V_{DD} = 10V		0	30	ns
		V_{DD} = 15V		0	20	ns
t_H	Minimum Hold Time Address to E	V_{DD} = 5V		−50	15	ns
		V_{DD} = 10V		−20	10	ns
		V_{DD} = 15V		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and Electrical Characteristics" provide conditions for actual device operation.

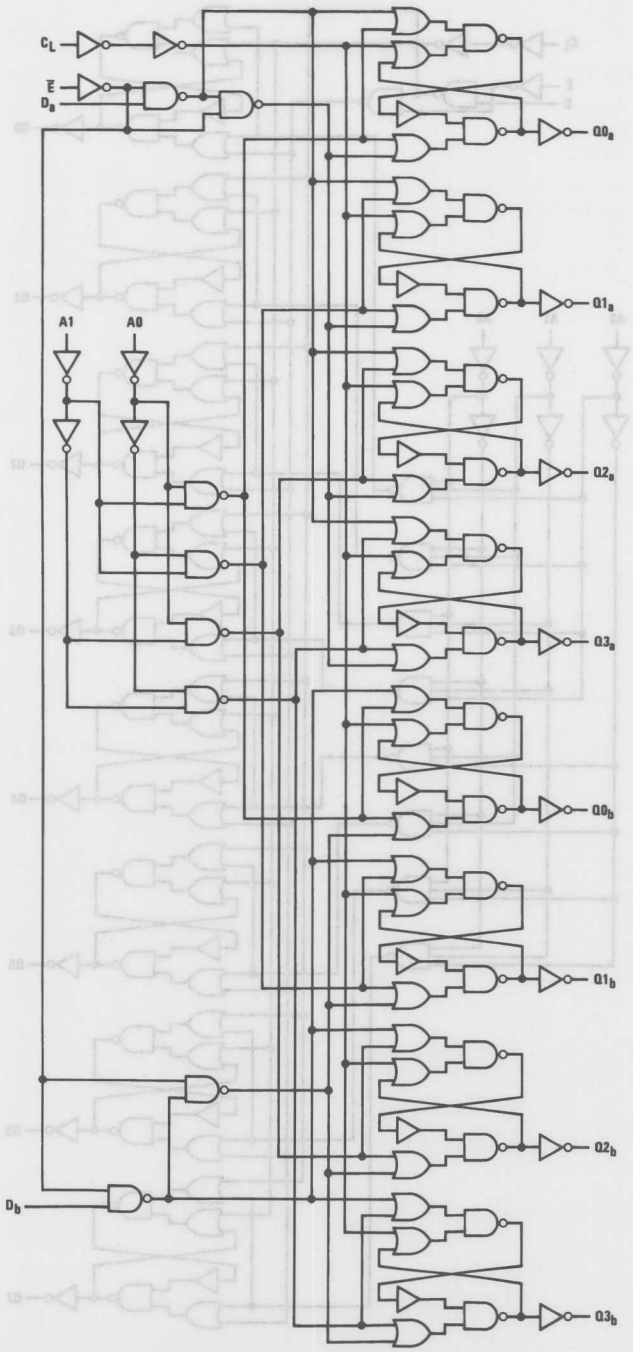
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{CC}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see Application Note AN-90, "54C/74C Family Characteristics".

Logic Diagrams

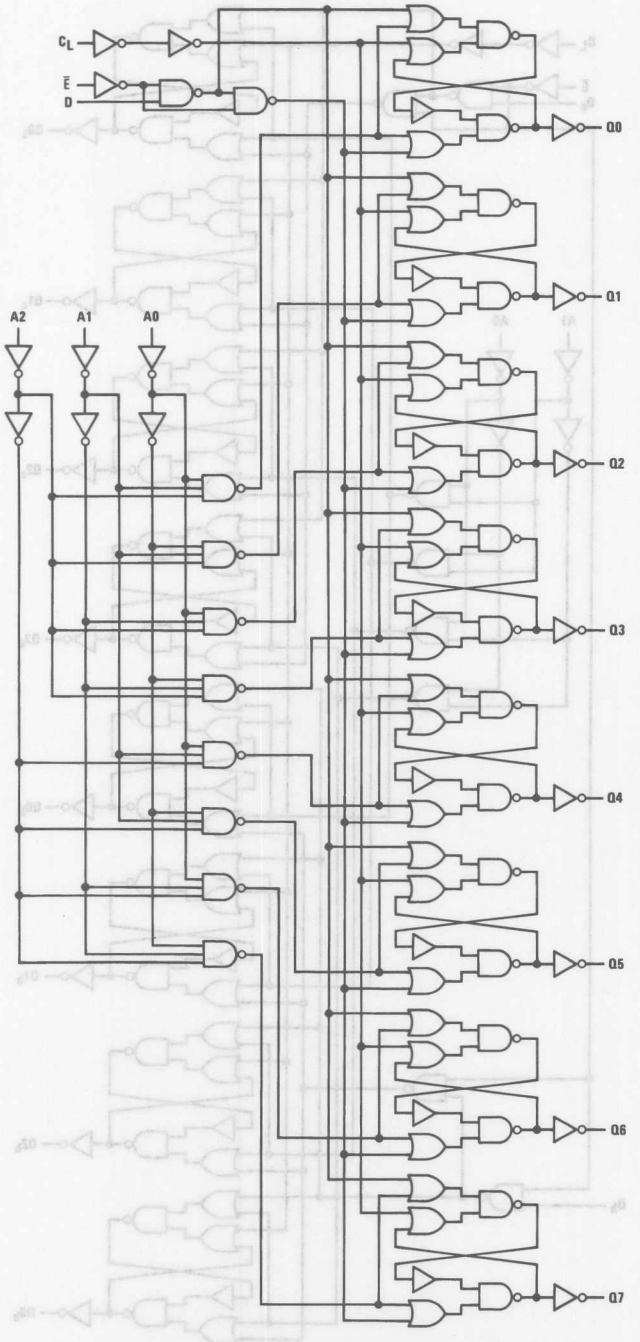
CD4723B



TL/F/6003–3

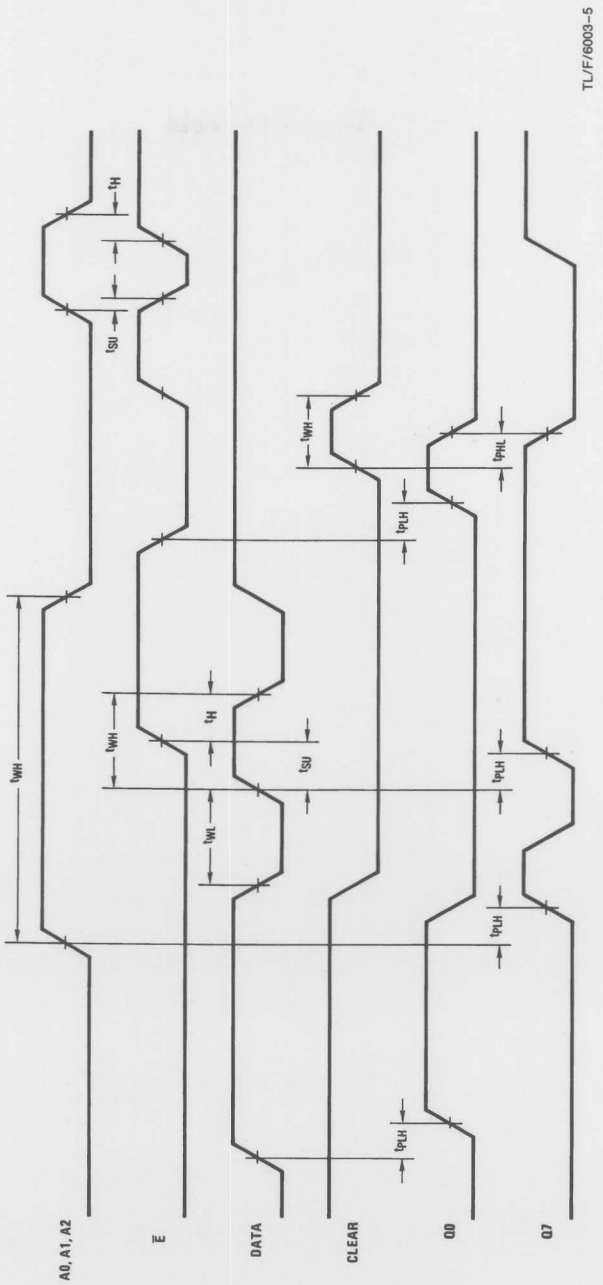
Logic Diagrams (Continued)

CD4724B



TL/F/6003–4

Switching Time Waveforms



Switching Time Waveforms

Section 6
MM54CXXX/MM74CXXX

Section 6 Contents

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National Semiconductor

ADC0808, ADC0809 8-Bit μP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

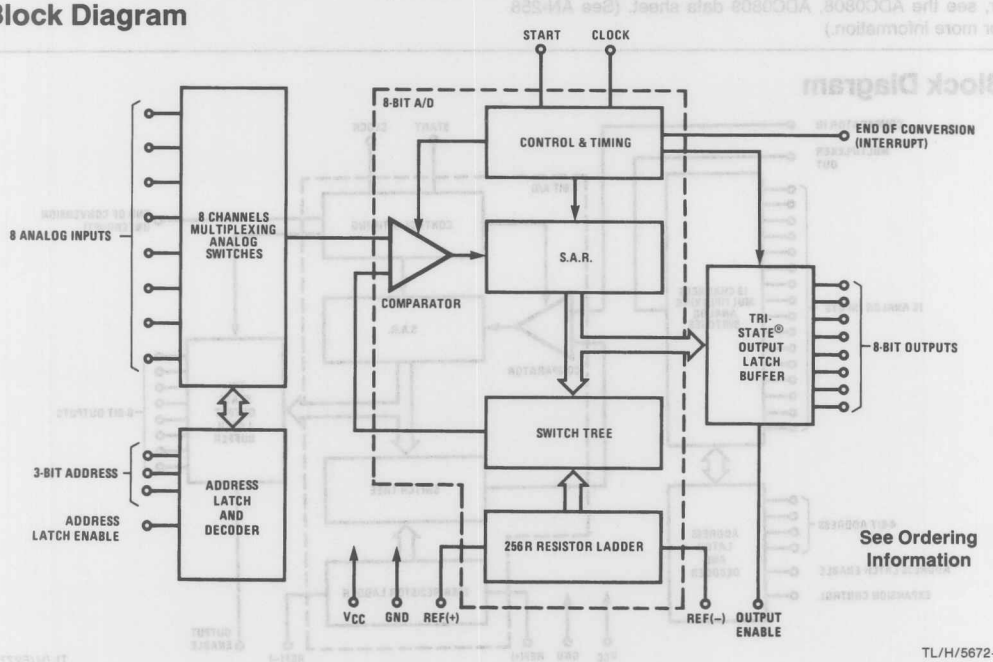
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 μs

Block Diagram



TL/H/5672–1

6

National Semiconductor

ADC0816, ADC0817 8-Bit μP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

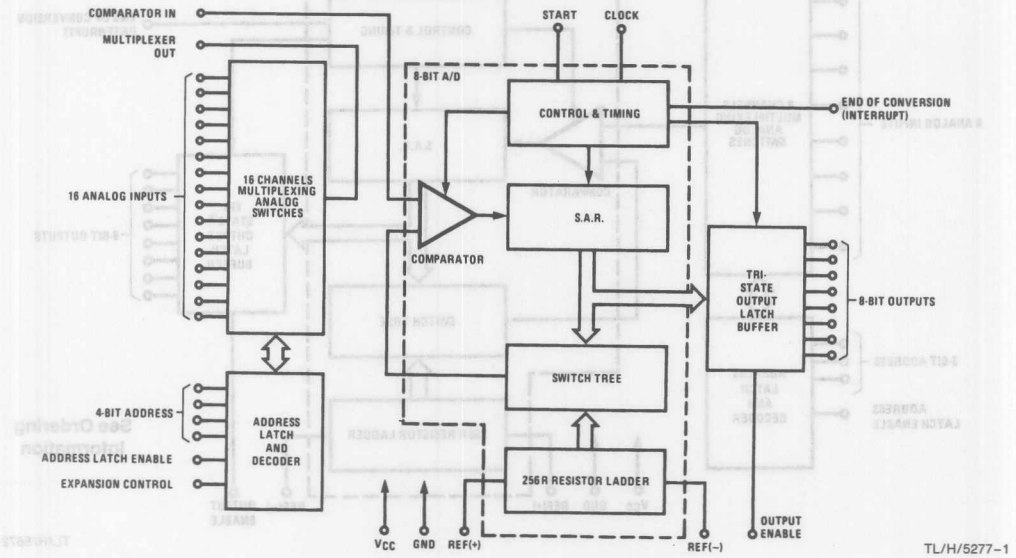
Features

- Easy interface to all microprocessors, or operates "stand alone"
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Outputs meet TTL voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Latched TRI-STATE output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning
- ADC0816 equivalent to MM74C948
- ADC0817 equivalent to MM74C948-1

Key Specifications

- Resolution 8 Bits
- Total Unadjusted Error ±½ LSB and ±1 LSB
- Single Supply 5 V_{DC}
- Low Power 15 mW
- Conversion Time 100 μs

Block Diagram



TL/H/5277–1

National Semiconductor

ADC0829 μP Compatible 8-Bit A/D with 11-Channel MUX/Digital Input

General Description

The ADC0829 is an 8-bit successive approximation A/D converter with an 11-channel multiplexer of which six can be used as digital inputs, as well as, analog inputs.

This A/D is designed to operate from the μP data bus using a single 5V supply.

Channel selection, conversion control, software configuration and bus interface logic are all contained on this monolithic CMOS device.

This device contains three 16-bit registers which are accessed via double byte instructions. The control register is a write only register which controls the start of a new conversion, selects the channel to be converted, configures the 8-bit I/O port as input or output, and provides information for the 8-bit output register.

The conversion results register is a read only register which contains the current status and most recent conversion results. The discrete input register is also a read only register which contains the four address bits of the selected channel, and the six discrete inputs which are connected to the analog multiplexer.

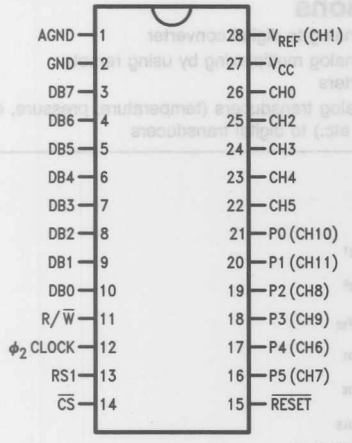
Features

- Easy interface to all microprocessors or operates "stand alone"
- Operates ratiometrically or with analog span adjusted voltage reference
- 11-Channel multiplexer with latched control logic of which six can be used as digital inputs
- 0 to 5V analog input range with single 5V supply
- TTL/MOS input/output compatible
- No zero or full scale adjusts required
- Standard 28-pin DIP
- Temperature range −40°C to +85°C
- ADC0829 equivalent to MM74C934

Key Specification

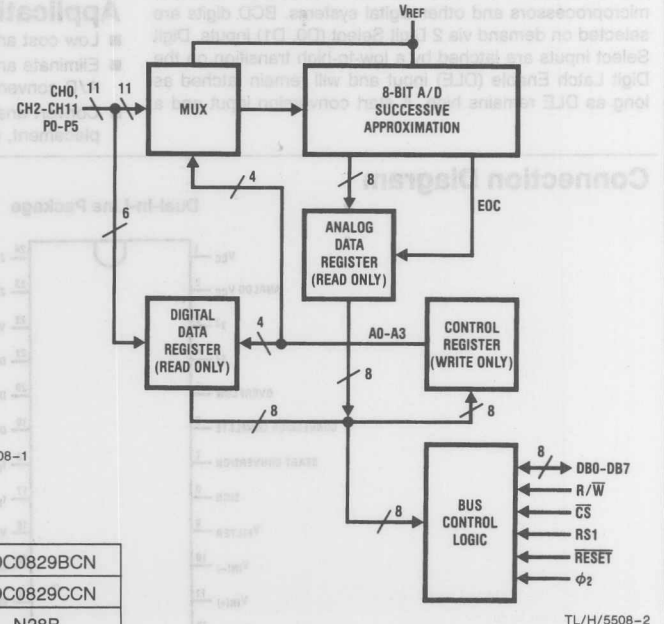
- Resolution 8 Bits
- Total Unadjusted Error ±½ LSB and ±1 LSB
- Conversion Time 256 μs
- Single Supply $5V_{DC}$
- Low Power 50 mW

Connection and Block Diagrams



TL/H/5508–1

Top View



TL/H/5508–2

Ordering Information

Error	± 1/2 Bit Unadjusted	ADC0829BCN
	± 1 Bit Unadjusted	ADC0829CCN
Package Outline		N28B

National Semiconductor

PRELIMINARY

ADC3511 3½-Digit Microprocessor Compatible A/D Converter
ADC3711 3¾-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

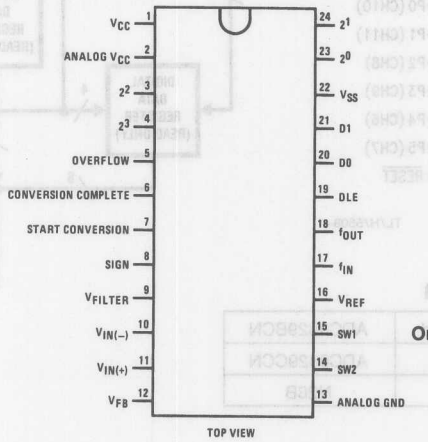
- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output
- ADC3511 equivalent to MM74C937
- ADC3711 equivalent to MM74C938-1

Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number ADC3511CCN or ADC3711CCN
NS Package N24A

TL/H/5678–1

National Semiconductor

ADD3501 3½ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3501 monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3501 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on all 4 versions of this product.

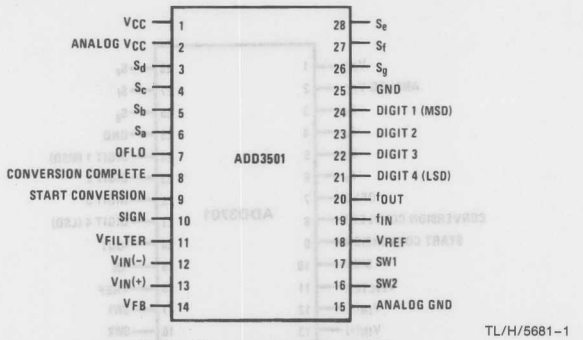
Features

- Operates from single 5V supply
- Converts 0V to ±1.999V
- Multiplexed 7-segment
- Drives segments directly
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed - 200ms/conversion
- Internal clock set with RC network or driven externally
- Overrange Indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts
- ADD3501 equivalent to MM74C935

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram



TL/H/5681–1

Order Number ADD3501CCN
See NS Package Number N28B

6

National Semiconductor

ADD3701 3¾ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3701 (MM74C936-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3701 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included.

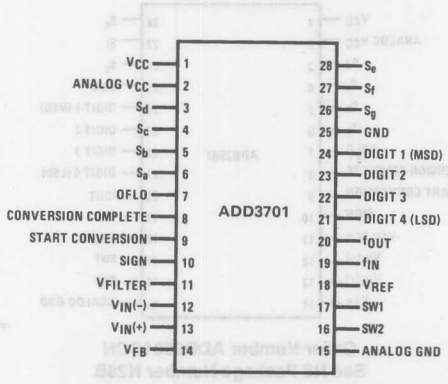
Features

- Operates from single 5V supply
- Converts 0 to ±3999 counts
- Multiplexed 7-segment
- Drives segments directly
- No external precision components necessary
- Accuracy specified over temperature
- Medium speed — 400 ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts
- ADD3701 equivalent to MM74C936-1

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers
- Indicators and displays requiring readout up to 3999 counts

Connection Diagram



TL/H/5682–1

Order Number ADD3701CCN
See NS Package Number N28B

National Semiconductor

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

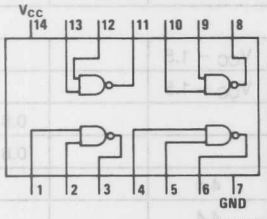
Features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power consumption	10 nW/package (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L

Connection Diagrams

Dual-In-Line Packages

MM54C00/MM74C00

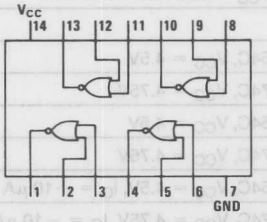


TL/F/5877–1

Top View

Order Number MM54C00* or MM74C00*

MM54C02/MM74C02

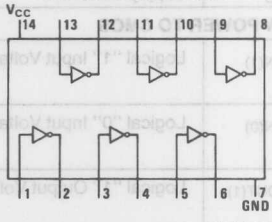


TL/F/5877–2

Top View

Order Number MM54C02* or MM74C02*

MM54C04/MM74C04

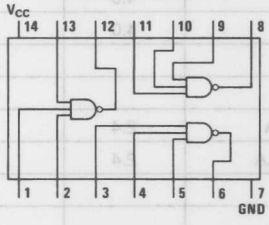


TL/F/5877–3

Top View

Order Number MM54C04* or MM74C04*

MM54C10/MM74C10

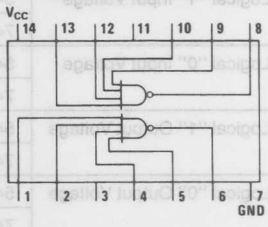


TL/F/5877–4

Top View

Order Number MM54C10* or MM74C10*

MM54C20/MM74C20



TL/F/5877–5

Top View

Order Number MM54C20* or MM74C20*

*Please look into Section 8, Appendix D for availability of various package types.

6

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
54C	$-55°C$ to $+125°C$
74C	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Operating V_{CC} Range	3.0V to 15V
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA
LOW POWER TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -10\ \mu A$	4.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -10\ \mu A$	4.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 10\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 10\ \mu A$			0.4	V
CMOS TO LOW POWER						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	4.0			V
		74C, $V_{CC} = 4.75V$	4.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			1.0	V
		74C, $V_{CC} = 4.75V$			1.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (see 54C/74C Family Characteristics Data Sheet) $T_A = 25°C$ (short circuit current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0V$, $V_{IN(0)} = 0V$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$, $V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0V$, $V_{IN(1)} = 5.0V$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$, $V_{OUT} = V_{CC}$	8.0			mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
C_{IN}	Input Capacitance	(Note 2)		6.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		60	100	ns
		$V_{CC} = 10V$		35	70	ns
C_{IN}	Input Capacitance	(Note 2)		7.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		18		pF
MM54C20/MM74C20						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		70	115	ns
		$V_{CC} = 10V$		40	80	ns
C_{IN}	Input Capacitance	(Note 2)		9		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		30		pF

*AC Parameters are guaranteed by DC correlated testing.

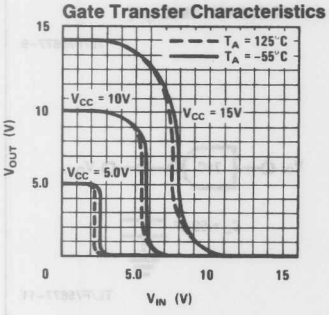
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

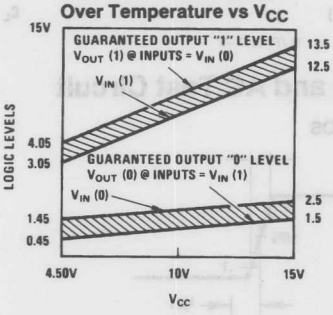
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

Typical Performance Characteristics

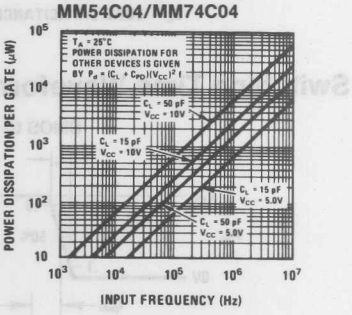
Gate Transfer Characteristics



Guaranteed Noise Margin Over Temperature vs V_{CC}



Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

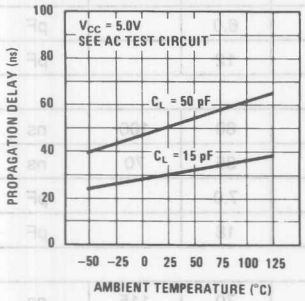


TL/F/5877–6

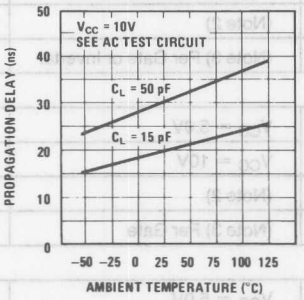
6

Typical Performance Characteristics (Continued)

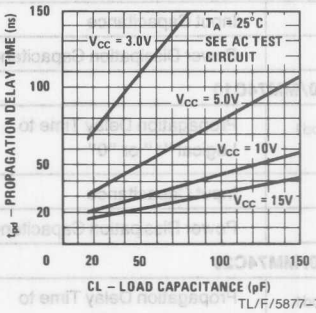
Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

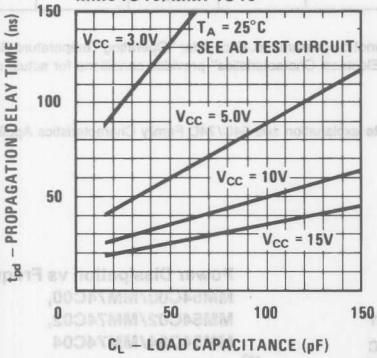


Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



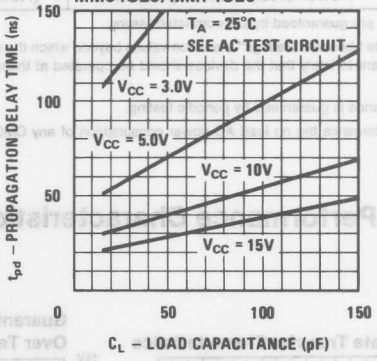
TL/F/5877–7

Propagation Delay Time vs Load Capacitance MM54C10/MM74C10



TL/F/5877–8

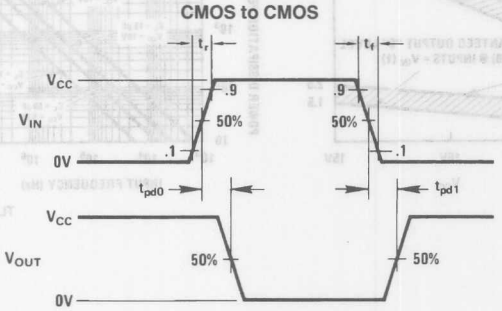
Propagation Delay Time vs Load Capacitance MM54C20/MM74C20



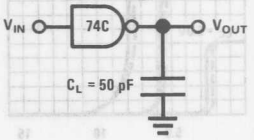
TL/F/5877–9

Switching Time Waveforms and AC Test Circuit

CMOS to CMOS



TL/F/5877–10



TL/F/5877–11

Note: Delays measured with input t_r, $t_f \leq 20$ ns.

National Semiconductor

MM54C08/MM74C08 Quad 2-Input AND Gate

General Description

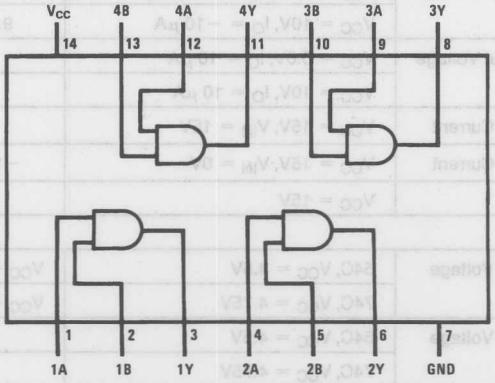
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L
■ Low power consumption	10 nW/package (typ.)

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5878–1

Top View

Order Number MM54C08* or MM74C08*

*Please look into Section 8, Appendix D for availability of various package types.

Inputs		Outputs
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Level L = Low Level

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin $-0.3V$ to $V_{CC} + 0.3V$

Operating Temperature Range
- MM54C08 $-55°C$ to $+125°C$
- MM74C08 $-40°C$ to $+85°C$

Storage Temperature Range $-65°C$ to $+150°C$

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Operating V_{CC} Range 3.0V to 15V

Absolute Maximum V_{CC} 18V

Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (see 54C/74C Family Characteristics Data Sheet) $T_A = 25°C$ (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$	-8.0	15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics*

(MM54C08/MM74C08) T_A = 25°C, C_L = 50 pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	V_{CC} = 5.0V		80	140	ns
		V_{CC} = 10V		40	70	ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		14		pF

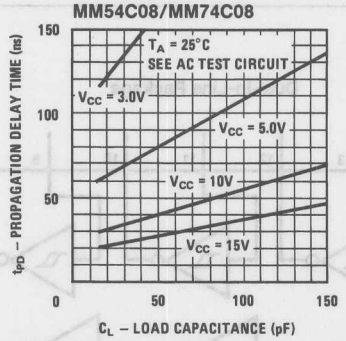
*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

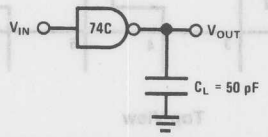
Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance MM54C08/MM74C08



TL/F/5878–2

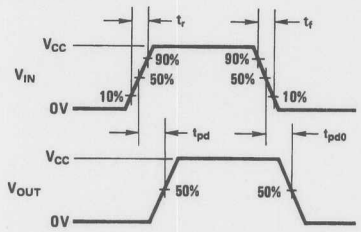
AC Test Circuit



TL/F/5878–3

Note: Delays measured with input t_r, t_f = 20 ns

Switching Time Waveforms



TL/F/5878–4

National Semiconductor

MM54C14/MM74C14 Hex Schmitt Trigger

General Description

The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ. 0.0005V/°C at V_{CC} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

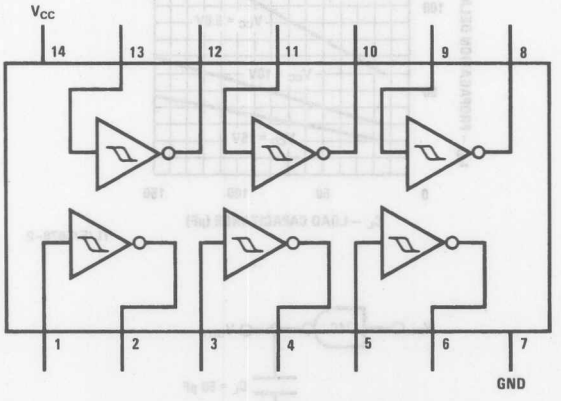
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} (typ.)
■ Low power	0.4 V_{CC} (typ.)
TTL compatibility	0.2 V_{CC} guaranteed
■ Hysteresis	0.4 V_{CC} (typ.)
	0.2 V_{CC} guaranteed

Connection Diagram

Dual-In-Line Package



TL/F/5879–1

Top View

Order Number MM54C14* or MM74C14*

*Please look into section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C14	$-55°C$ to $+125°C$
MM74C14	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

Min/Max limits apply across the guaranteed temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive Going Threshold Voltage	$V_{CC} = 5V$	3.0	3.6	4.3	V
		$V_{CC} = 10V$	6.0	6.8	8.6	V
		$V_{CC} = 15V$	9.0	10.0	12.9	V
V_{T-}	Negative Going Threshold Voltage	$V_{CC} = 5V$	0.7	1.4	2.0	V
		$V_{CC} = 10V$	1.4	3.2	4.0	V
		$V_{CC} = 15V$	2.1	5.0	6.0	V
$V_{T+} - V_{T-}$	Hysteresis	$V_{CC} = 5V$	1.0	2.2	3.6	V
		$V_{CC} = 10V$	2.0	3.6	7.2	V
		$V_{CC} = 15V$	3.0	5.0	10.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$, $V_{IN} = 0V/15V$		0.05	15	μA
		$V_{CC} = 5V$, $V_{IN} = 2.5V$ (Note 4)		20		μA
		$V_{CC} = 10V$, $V_{IN} = 5V$ (Note 4)		200		μA
		$V_{CC} = 15V$, $V_{IN} = 7.5V$ (Note 4)		600		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (see 54C/74C Family Characteristics Data Sheet) $T_A = 25°C$ (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$	8.0	16		mA

t_{PD0}, t_{PD1}	Propagation Delay from Input to Output	V_{CC} = 5V		220	400	ns
		V_{CC} = 10V		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

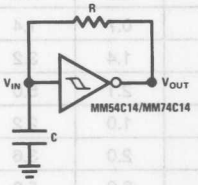
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

Note 4: Only one of the six inputs is at ½ V_{CC}; the others are either at V_{CC} or GND.

Typical Applications

Low Power Oscillator



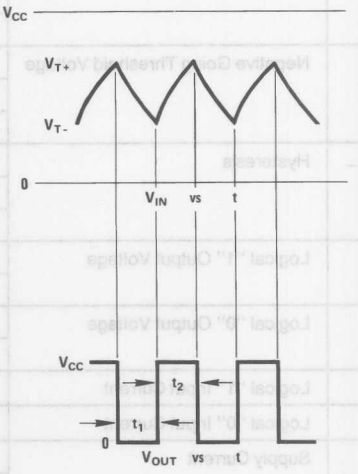
TL/F/5879–2

$$t_1 \approx RC \ell n \frac{V_{T+}}{V_{T-}}$$

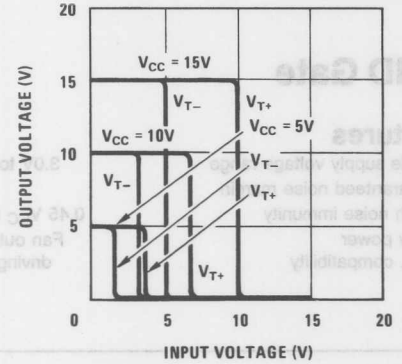
$$t_1 \approx RC \ell n \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ell n \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}} \approx \frac{1}{1.7\,RC}$$

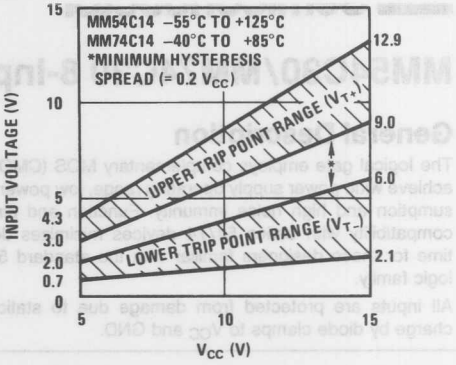
Note: The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$



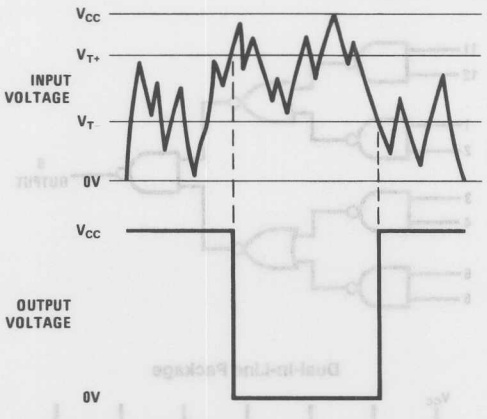
TL/F/5879–3



TL/F/5879–4



TL/F/5879–5



TL/F/5879–6

Note: For more information on output drive characteristics, power dissipation, and propagation delays, see AN-90.

National Semiconductor

MM54C30/MM74C30 8-Input NAND Gate

General Description

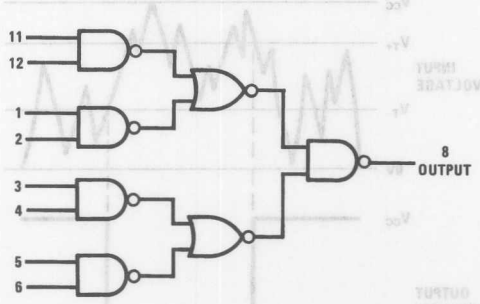
The logical gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

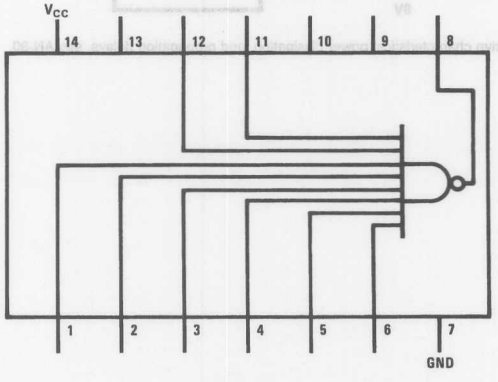
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L

Logic and Connection Diagrams



TL/F/5880–1

Dual-In-Line Package



TL/F/5880–2

Top View

Order Number MM54C30* or MM74C30*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	
MM54C30	$-55°C$ to $+125°C$
MM74C30	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5V$		125	180	ns
		$V_{CC} = 10V$		55	90	ns
C_{IN}	Input Capacitance	(Note 2)		4.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		26		pF

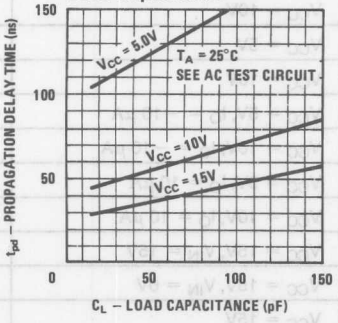
*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, application note—AN-90.

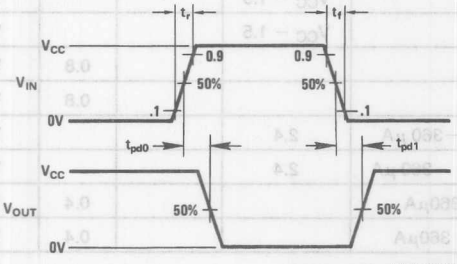
Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance



TL/F/5880–3

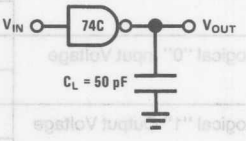
Switching Time Waveforms



TL/F/5880–4

Note: Delays Measured with Input t_r, t_f = 20 ns.

AC Test Circuit



TL/F/5880–5

National Semiconductor

MM54C32/MM74C32 Quad 2-Input OR Gate

General Description

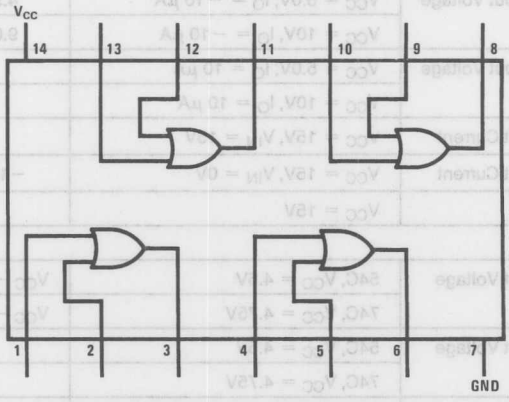
Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45V V_{CC} (typ.)
■ Low power	fan out of 2
TTL compatibility	driving 74L

Connection Diagram

Dual-In-Line Package



TL/F/5881–1

Top View

Order Number MM54C32* or MM74C32*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin $-0.3V$ to $V_{CC} + 0.3V$

Operating Temperature Range

MM54C32 $-55°C$ to $+125°C$

MM74C32 $-40°C$ to $+85°C$

Storage Temperature Range $-65°C$ to $+150°C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V_{CC} Range 3.0V to 15V

Absolute Maximum V_{CC} 18V

Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (see 54C/74C Family Characteristics Data Sheet) $T_A = 25°C$ (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

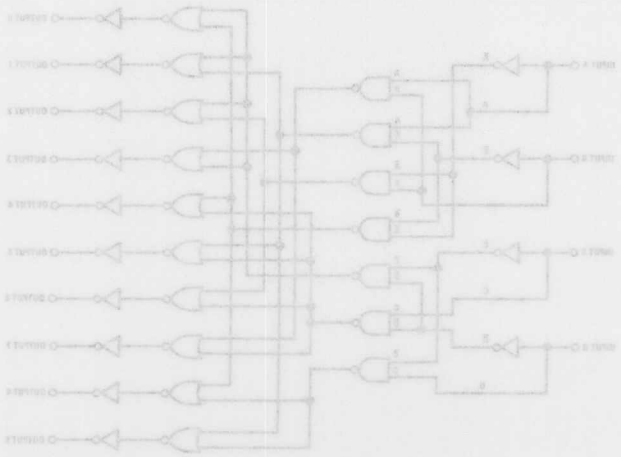
AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		80	150	ns
		$V_{CC} = 10V$		35	70	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 3)		15		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.



National Semiconductor

MM54C42/MM74C42 BCD-to-Decimal Decoder

General Description

The MM54C42/MM74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

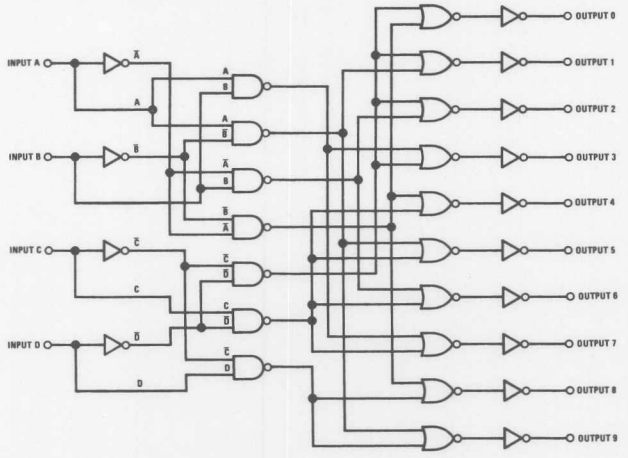
Features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Medium speed operation — 10 MHz (typ.) with 10V V_{CC}

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Schematic Diagram



TL/F/5882–1

Truth Table

Inputs				Outputs									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C42	$-55°C$ to $+125°C$
MM74C42	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0			μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (see 54C/74C Family Characteristics Data Sheet) $T_A = 25°C$ (short circuit current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5.0V$, $V_{IN(0)} = 0V$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$, $V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5.0V$, $V_{IN(1)} = 5.0V$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$, $V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "0" or "1"	$V_{CC} = 5.0V$		200	300	ns
		$V_{CC} = 10V$		90	140	ns
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		50		pF

*AC Parameters are guaranteed by DC correlated testing.

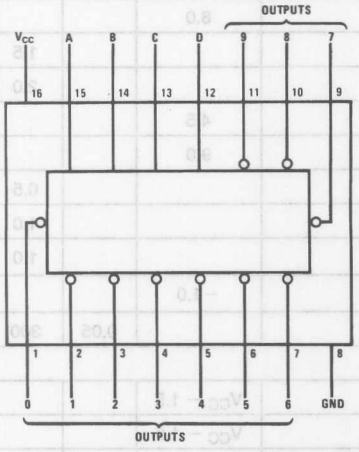
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

Connection Diagram

Dual-In-Line Package



TL/F/5882–2

Top View

Order Number MM54C42* or MM74C42*

*Please look into Section 8, Appendix D for availability of various package types.

National Semiconductor

MM54C48/MM74C48 BCD-to-7 Segment Decoder

General Description

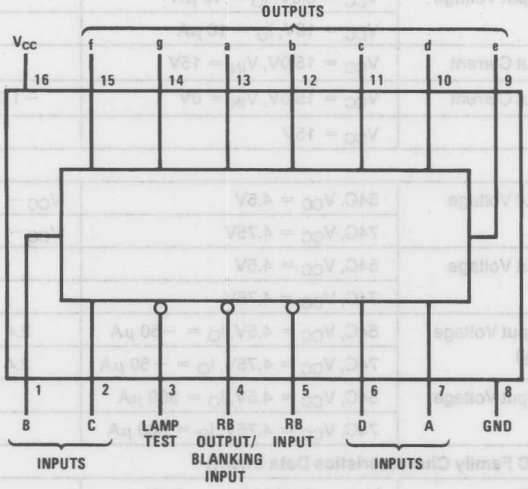
The MM54C48/MM74C48 BCD-to-7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test-blanking input/ripple-blanking output, and ripple-blanking inputs.

Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

Connection Diagram

Dual-In-Line Package



TL/F/5883–1

Top View

Order Number MM54C48* or MM74C48*

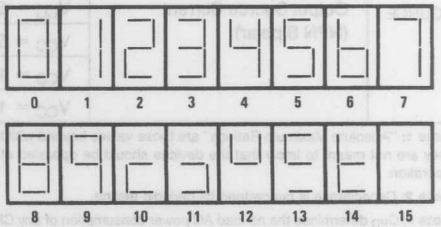
*Please look into Section 8, Appendix D for availability of various package types.

Segment Identification



TL/F/5883–2

Numerical Designations and Resultant Displays



TL/F/5883–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C48	$-55°C$ to $+125°C$
MM74C48	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15.0V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15.0V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	54C, $V_{CC} = 4.5V$, $I_O = -50\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -50\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel)(RB Output Only)	$V_{CC} = 4.75V$, $V_{OUT} = 0.4V$			-0.80	mA
		$V_{CC} = 10V$, $V_{OUT} = 0.5V$			-4.0	mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	8.0	16		mA
I_{SOURCE}	Output Source Current (NPN Bipolar)	$V_{CC} = 5.0V$, $V_{OUT} = 3.4V$	-20	-50		mA
		$V_{CC} = 5.0V$, $V_{OUT} = 3.0V$		-65		mA
		$V_{CC} = 10V$, $V_{OUT} = 8.4V$	-20	-50		mA
		$V_{CC} = 10V$, $V_{OUT} = 8.0V$		-65		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

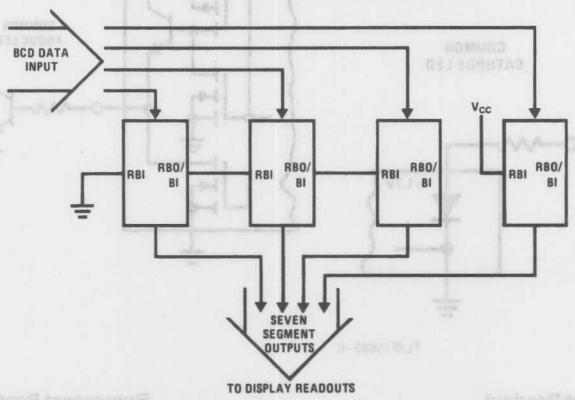
AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	$V_{CC} = 5.0V$		450	1500	ns
		$V_{CC} = 10V$		160	500	ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from RB Input	$V_{CC} = 5.0V$		500	1600	ns
		$V_{CC} = 10V$		180	550	ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from Blanking Input	$V_{CC} = 5.0V$		350	1200	ns
		$V_{CC} = 10V$		140	450	ns
t_{pd1}	Propagation Delay to a "1" on Segment Outputs from Lamp Test	$V_{CC} = 5.0V$		450	1500	ns
		$V_{CC} = 10V$		160	500	ns
t_{pd1}	Propagation Delay to a "1" on RB Output from RB Input	$V_{CC} = 5.0V$		600	2000	ns
		$V_{CC} = 10V$		250	800	ns
t_{pd0}	Propagation Delay to a "0" on RB Output from RB Input	$V_{CC} = 5.0V$		140	450	ns
		$V_{CC} = 10V$		50	150	ns

*AC Parameters are guaranteed by DC correlated testing.

Typical Applications

Typical Connection Utilizing the Ripple-Blanking Feature

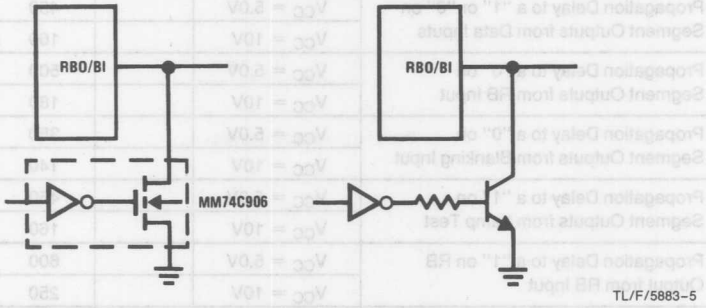


TL/F/5883–4

First three stages will blank leading zeros, the fourth stage will not blank zeros.

Typical Applications (Continued)

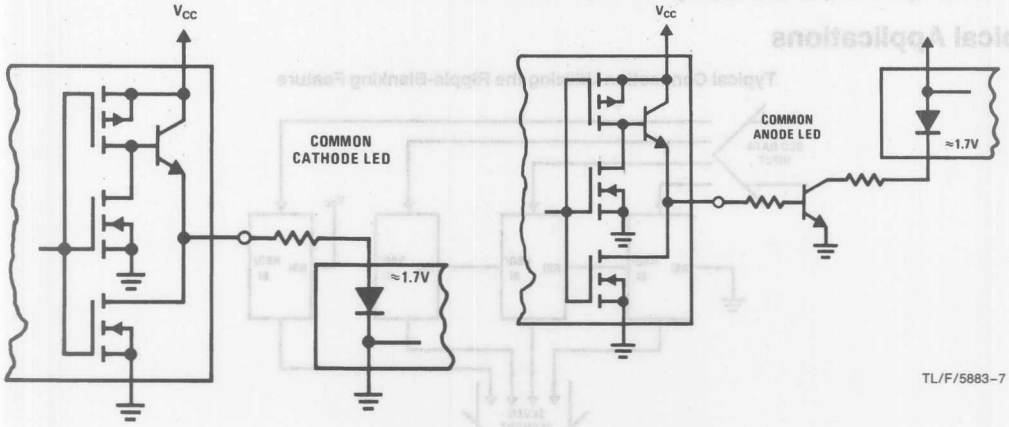
Blanking Input Connection Diagram



TL/F/5883–5

When RBO/BI is forced low, all segment outputs are off regardless of the state of any other input condition.

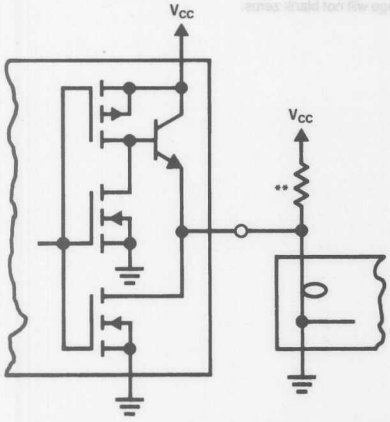
Light Emitting Diode (LED) Readout



TL/F/5883–6

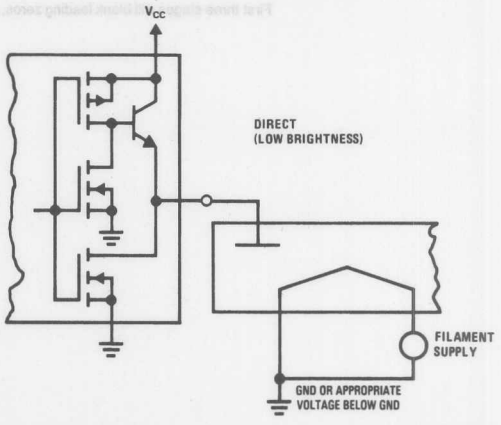
TL/F/5883–7

Incandescent Readout



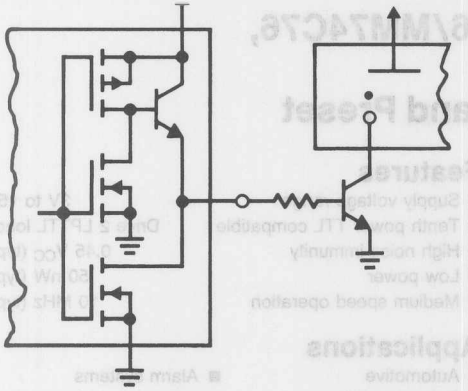
TL/F/5883–8

Fluorescent Readout

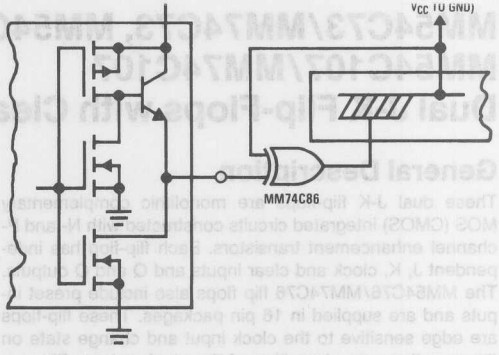


TL/F/5883–9

**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.



TL/F/5883–10



TL/F/5883–11

Direct DC drive of LC's not recommended for life of LC readouts.

Truth Table

Decimal or Function	Inputs						BI/RBO†	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

Note 1: The blanking input (BI) must be open when output functions 0–15 are desired. The ripple-blanking input (RBI) must be high, if blanking of a decimal zero is not desired.

Note 2: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

Note 3: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open and a low is applied to the lamp-test input, all segment outputs are high.

†One BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

National Semiconductor

MM54C73/MM74C73, MM54C76/MM74C76, MM54C107/MM74C107 Dual J-K Flip-Flops with Clear and Preset

General Description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and Q outputs. The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

Features

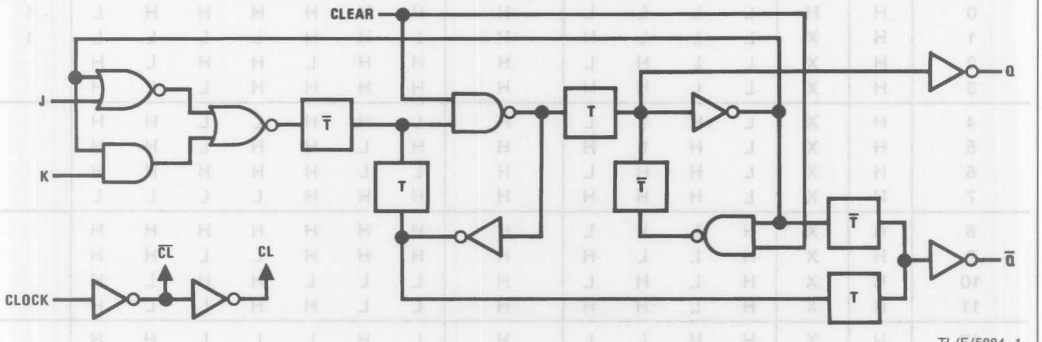
■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	Drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	10 MHz (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

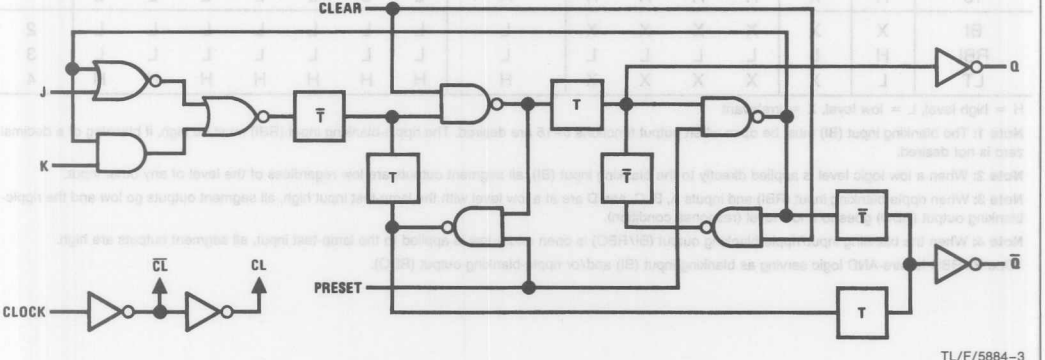
Logic Diagrams

MM54C73/MM74C73 and MM54C107/MM74C107



TL/F/5884–1

MM54C76/MM74C76



TL/F/5884–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

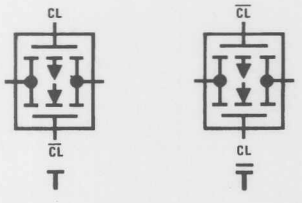
Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54CXX	$-55°C$ to $+125°C$
MM74CXX	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (Soldering, 10 sec.)	260°C
Operating V_{CC} Range	$+3V$ to $15V$
V_{CC} (Max)	18V

DC Electrical Characteristics Min/Max limits apply across temperature range unless othwerwise noted

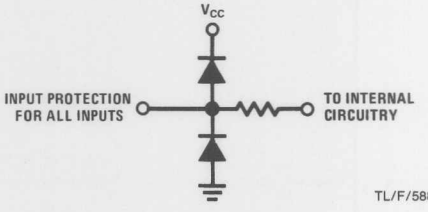
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$	4.5			V
		$V_{CC} = 10V$	9			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$			0.5	V
		$V_{CC} = 10V$			1	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$			1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1			μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.050	60	μA
LOW POWER TTL TO CMOS INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-8			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V$, $V_{IN(1)} = 5V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8			mA

Logic Diagrams (Continued)

Transmission Gate



TL/F/5884–2



TL/F/5884–4

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	Any Input		5		pF
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	$V_{CC} = 5V$		180	300	ns
		$V_{CC} = 10V$		70	110	ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5V$		200	300	ns
		$V_{CC} = 10V$		80	130	ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5V$		200	300	ns
		$V_{CC} = 10V$		80	130	ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5V$		110	175	ns
		$V_{CC} = 10V$		45	70	ns
t_H	Time after Clock Pulse that J and K must be Held	$V_{CC} = 5V$		−40	0	ns
		$V_{CC} = 10V$		−20	0	ns
t_{PW}	Minimum Clock Pulse Width $t_{WL} = t_{WH}$	$V_{CC} = 5V$		120	190	ns
		$V_{CC} = 10V$		50	80	ns
t_{PW}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5V$		90	130	ns
		$V_{CC} = 10V$		40	60	ns
t_{MAX}	Maximum Toggle Frequency	$V_{CC} = 5V$	2.5	4		MHz
		$V_{CC} = 10V$	7	11		MHz
t_r, t_f	Clock Pulse Rise and Fall Time	$V_{CC} = 5V$			15	μs
		$V_{CC} = 10V$			5	μs

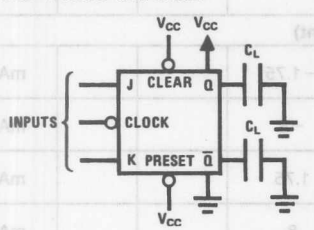
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note—AN-90.

AC Test Circuit



TL/F/5884–8

Truth Tables

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

t_n = bit time before clock pulse

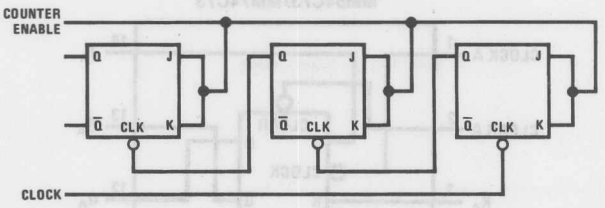
t_{n+1} = bit time after clock pulse

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

*No change in output from previous state

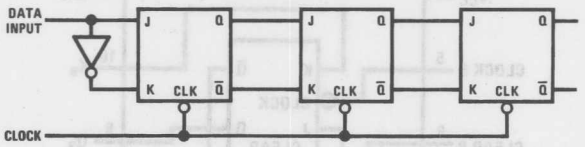
Typical Applications

Ripple Binary Counters



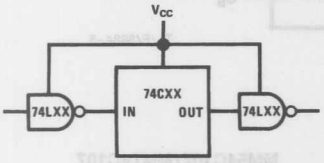
TL/F/5884–9

Shift Registers



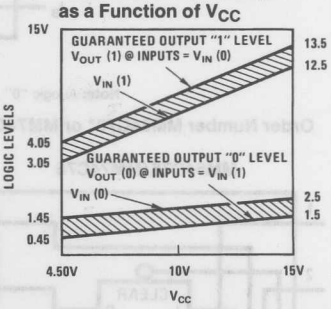
TL/F/5884–11

74C Compatibility



TL/F/5884–10

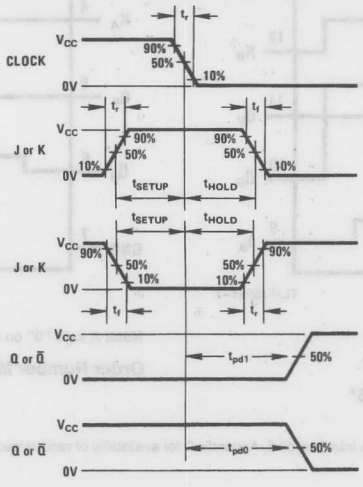
Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5884–12

Switching Time Waveforms

CMOS to CMOS

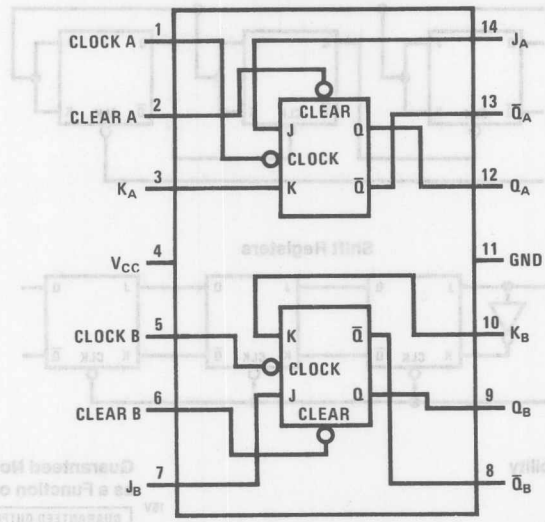


TL/F/5884–13

$t_r = t_f = 20$ ns

Connection Diagrams

MM54C73/MM74C73



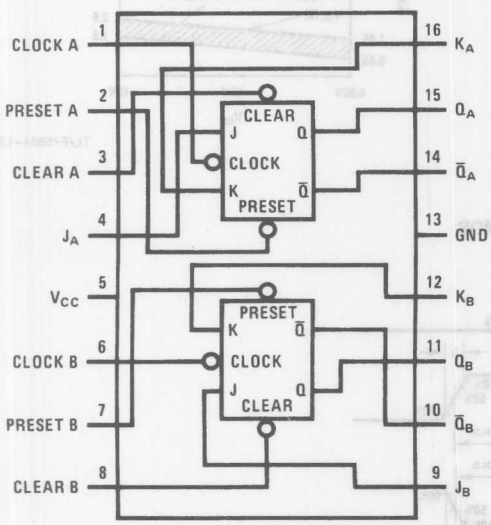
TL/F/5884–5

Top View

Note: A logic "0" on clear sets Q to logic "0".

Order Number MM54C73* or MM74C73*

MM54C76/MM74C76



TL/F/5884–7

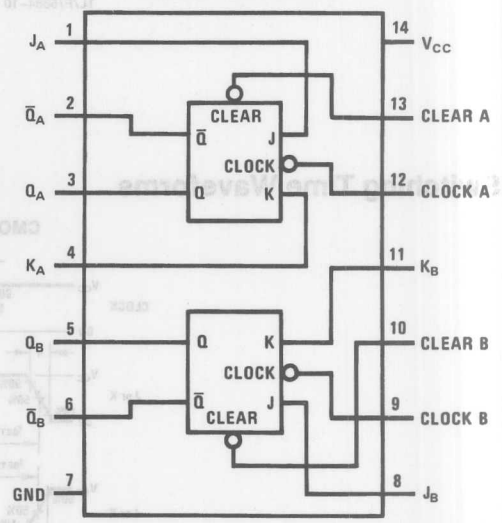
Top View

Note 1: A logic "0" on clear sets Q to a logic "0".

Note 2: A logic "0" on preset sets Q to a logic "1".

Order Number MM54C76* or MM74C76*

MM54C107/MM74C107



TL/F/5884–6

Top View

Note: A logic "0" on clear sets Q to logic "0".

Order Number MM54C107* or MM74C107*

*Please look into Section 8, Appendix D for availability of various package types.

National Semiconductor

MM54C74/MM74C74 Dual D Flip-Flop

General Description

The MM54C74/MM74C74 dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip-flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

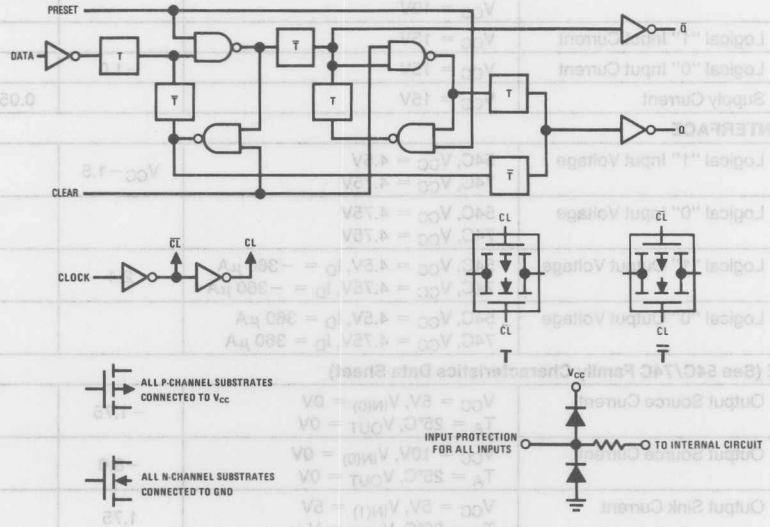
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	Drive 2 LPT^{2}L loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	10 MHz (typ.) with 10V supply

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Logic Diagram



TL/F/5885–1

Truth Table

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

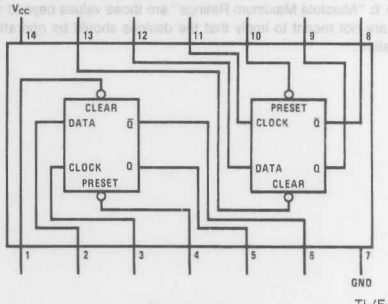
*No change in output from previous state.

Order Number MM54C74* or MM74C74*

*Please look into Section 8, Appendix D for availability of various package types.

Connection Diagram

Dual-In-Line Package



TL/F/5885–2

Top View

Note: A logic "0" on clear sets Q to logic "0".
A logic "0" on preset sets Q to logic "1".

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$	Small Outline	500 mW
Operating Temperature Range		Lead Temperature (Soldering, 10 seconds)	260°C
MM54C74	$-55°C$ to $+125°C$	Operating V_{CC} Range	3V to 15V
MM74C74	$-40°C$ to $+85°C$	V_{CC}(Max)	18V

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	80			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$	4.5			V
		$V_{CC} = 10V$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$			0.5	V
		$V_{CC} = 10V$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1.0			μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	60	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC}-1.5$			
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.75V$ 74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_D = -360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_D = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_D = 360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_D = 360\ \mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V$, $V_{IN(1)} = 5V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
t_{pd}	Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5V$ $V_{CC} = 10V$		250 100	400 150	ns ns
t_{S0}, t_{S1}	Time Prior to Clock Pulse that Data Must be Present t_{SETUP}	$V_{CC} = 5V$ $V_{CC} = 10V$	100 40	50 20		ns ns
t_{H0}, t_{H1}	Time after Clock Pulse that Data Must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$		−20 −8.0	0 0	ns ns
t_{PW1}	Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5V$ $V_{CC} = 10V$		100 40	250 100	ns ns
t_{PW2}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		100 40	160 70	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	15.0 5.0			μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.0 5.0	3.5 8.0		MHz MHz
C_{PD}	Power Dissipation Capacitance	(Note 3)		40		pF

*AC Parameters are guaranteed by DC correlated testing.

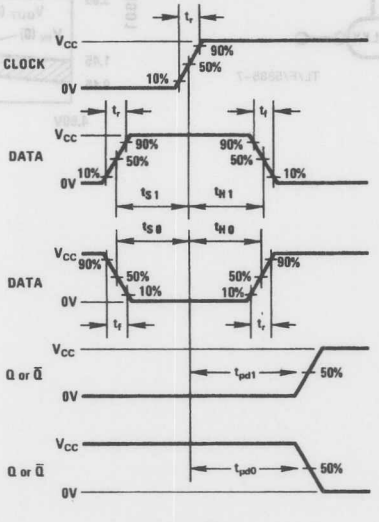
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

Switching Time Waveform

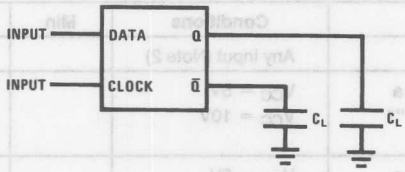
CMOS to CMOS



TL/F/5885–3

$t_r = t_f = 20$ ns

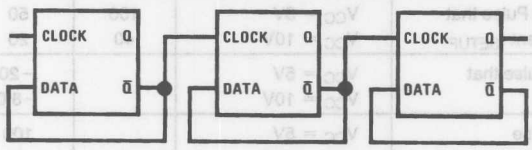
AC Test Circuit



TL/F/5885–4

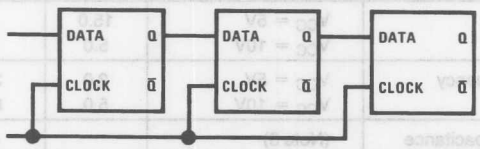
Typical Applications

Ripple Counter (Divide by 2^n)



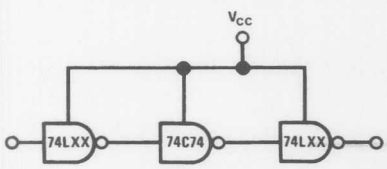
TL/F/5885–5

Shift Register



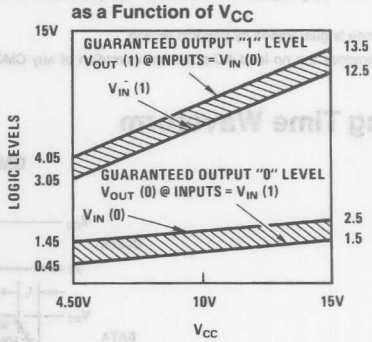
TL/F/5885–6

74C Compatibility



TL/F/5885–7

Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5885–8

National Semiconductor

MM54C83/MM74C83 4-Bit Binary Full Adder

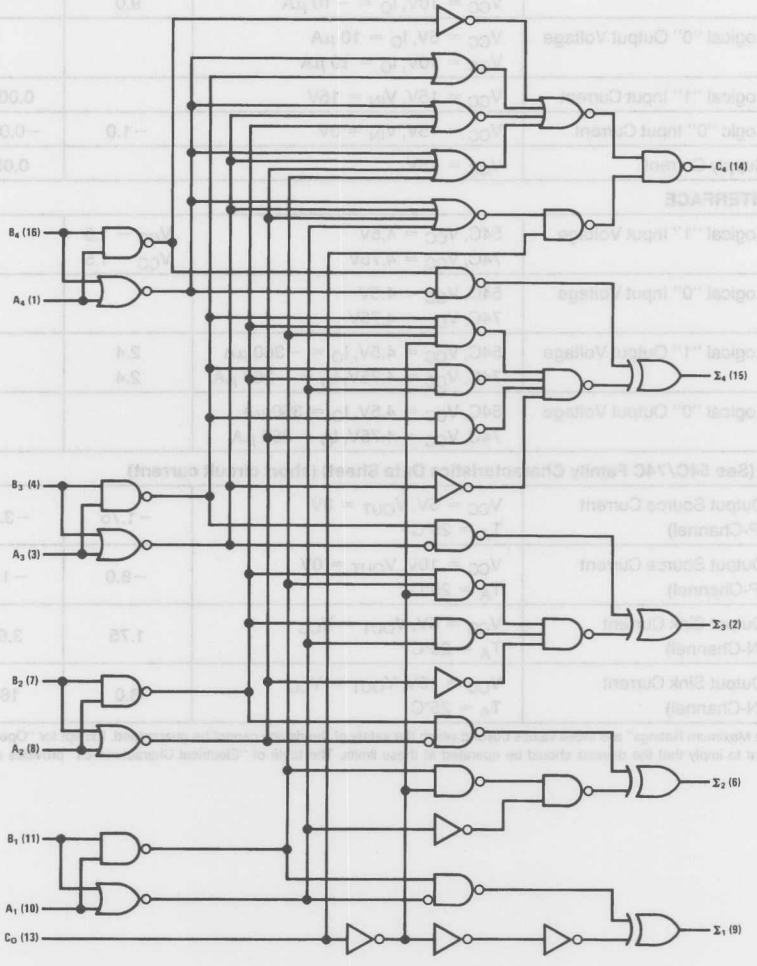
General Description

The MM54C83/MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers. A carry input (C_O) is included and the sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus, the end-around carry is accomplished without the need for level inversion.

Features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Fast carry ripple (C_O to C_4)	50 ns (typ.) at V_{CC} = 10V and C_L = 50 pF
■ Fast summing (Σ_{IN} to Σ_{OUT})	125 ns (typ.) at V_{CC} = 10V and C_L = 50 pF

Logic Diagram



TL/F/6035–1

contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	
MM54C83	$-55°C$ to $+125°C$
MM74C83	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10\ \mu A$ $V_{CC} = 10V, I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10\ \mu A$ $V_{CC} = 10V, I_O = 10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logic "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360\ \mu A$ 74C, $V_{CC} = 4.75V, I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V, I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay from C_0 to C_4	$V_{CC} = 5V$ $V_{CC} = 10V$		120 50	200 80	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to C_4	$V_{CC} = 5V$ $V_{CC} = 10V$		250 90	450 150	ns ns
t_{pd1}	Propagation Delay from C_0 to Sum Outputs	$V_{CC} = 5V$ $V_{CC} = 10V$		350 125	550 200	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to Sum Outputs	$V_{CC} = 5V$ $V_{CC} = 10V$		300 90	550 150	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		120		pF

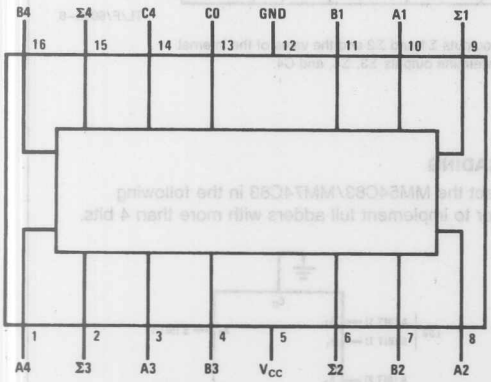
*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

Connection Diagram

Dual-In-Line Package

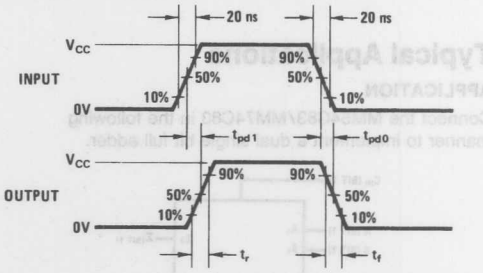


TL/F/6035–2

Order Number MM54C83* or MM74C83*

*Please look into Section 8, Appendix D for availability of various package types.

Switching Time Waveforms



TL/F/6035–3

Inputs must be tied to appropriate logic level.

Truth Table

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4	Σ1 Σ3	Σ2 Σ4	C2 C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	L	H	H	H	H	H	H

H = high level, L = low level

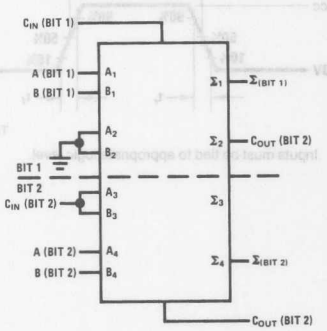
TL/F/6035–6

Note: Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Typical Applications

APPLICATION

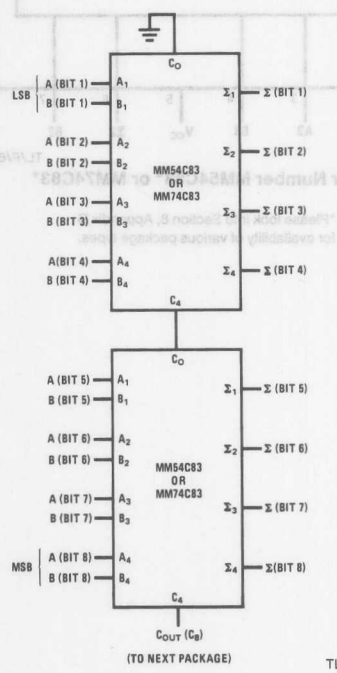
Connect the MM54C83/MM74C83 in the following manner to implement a dual single bit full adder.



TL/F/6035–4

CASCADING

Connect the MM54C83/MM74C83 in the following manner to implement full adders with more than 4 bits.



TL/F/6035–5

National Semiconductor

MM54C85/MM74C85 4-Bit Magnitude Comparator

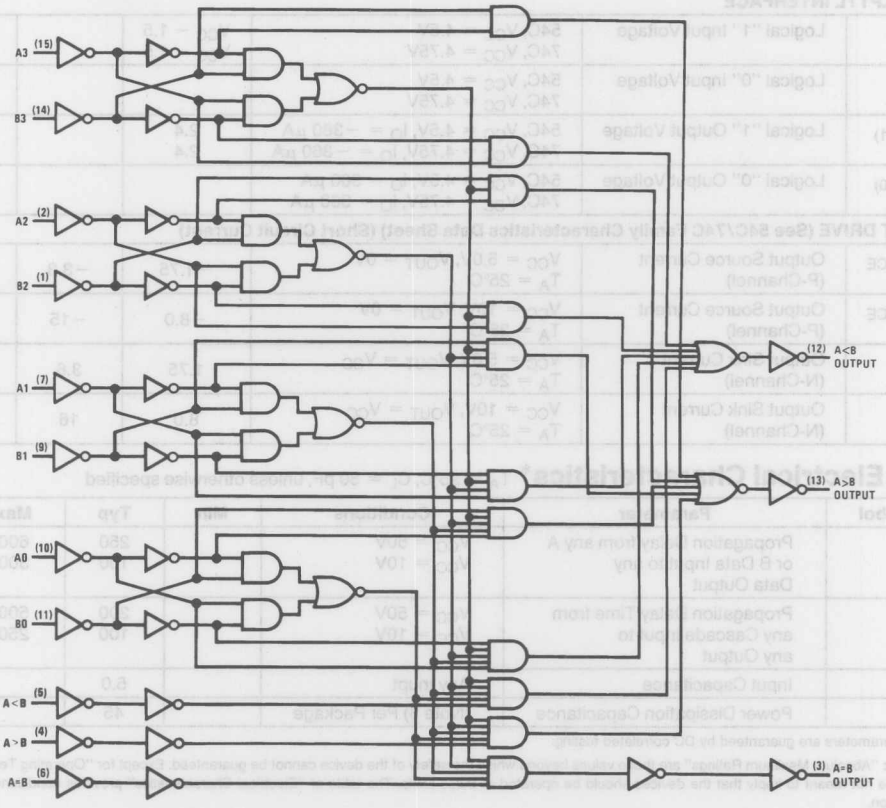
General Description

The MM54C85/MM74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A > B, A < B and A = B), and three outputs (A > B, A < B and A = B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A > B, A < B, and A = B) of the least significant stage to the cascade inputs (A > B, A < B and A = B) of the next-significant stage. In addition the least significant stage must have a high level voltage ($V_{IN(1)}$) applied to the A = B input and low level voltage ($V_{IN(0)}$) applied to A > B and A < B inputs.

Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.4 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- Expandable to 'N' stages
- Applicable to binary or BCD
- Low power pinout: 54L85/74L85

Logic Diagram



TL/F/5886–1

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C85	$-55°C$ to $+125°C$
MM74C85	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$ $V_{CC} = 10V$, $I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = +10\ \mu A$ $V_{CC} = 10V$, $I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay from any A or B Data Input to any Data Output	$V_{CC} = 50V$ $V_{CC} = 10V$		250 100	600 300	ns ns
t_{pd}	Propagation Delay Time from any Cascade Input to any Output	$V_{CC} = 50V$ $V_{CC} = 10V$		200 100	500 250	ns ns
C_{IN}	Input Capacitance	Any Inupt		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Package		45		pF

*AC Parameters are guaranteed by DC correlated testing.

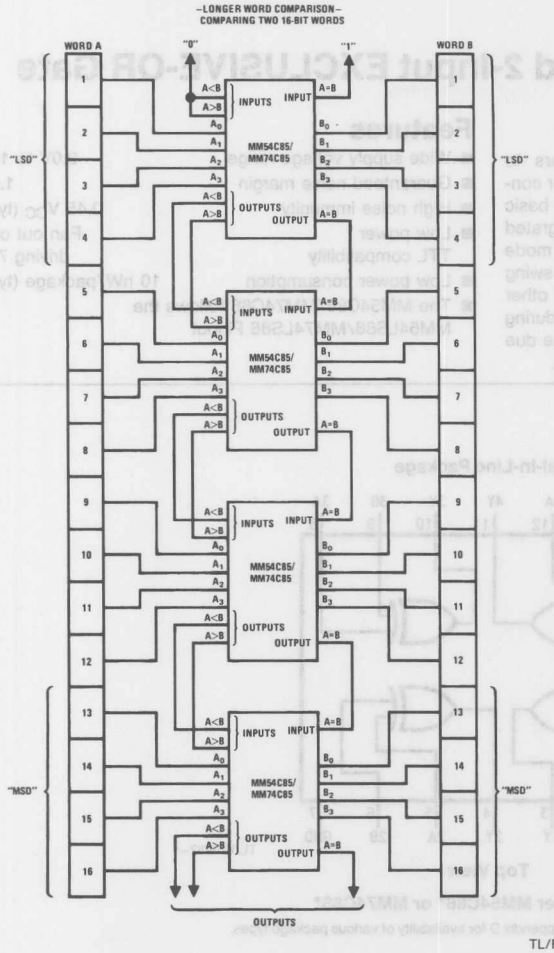
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Typical Applications

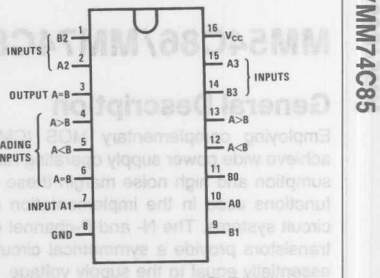
Four Digit Comparator



TL/F/5886–2

Connection Diagram

Dual-In-Line Package



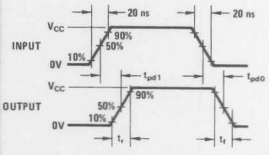
TL/F/5886–3

Top View

Order Number MM54C85* or MM74C85*

*Please look into Section 8, Appendix D for availability of various package types.

Switching Time Waveforms



TL/F/5886–4

Unused inputs must be tied to an appropriate logic level.

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate

General Description

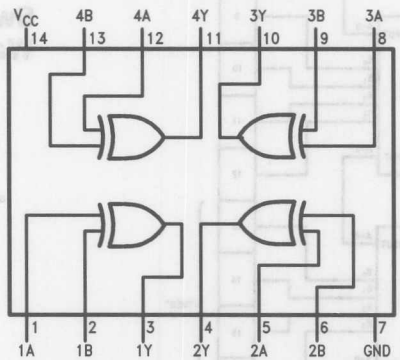
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L
- Low power consumption — 10 nW/package (typ.)
- The MM54C86/MM74C86 follows the MM54LS86/MM74LS86 Pinout

Connection Diagram

Dual-In-Line Package



TL/F/5887–1

Top View

Order Number MM54C86* or MM74C86*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Level L = Low Level

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin (Note 1)	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C86	$-55°C$ to $+125°C$
MM74C86	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line Package	700 mW
Small Outline	500 mW
Operating Range (V_{CC})	3.0V to 15V
Absolute Maximum (V_{CC})	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$ $V_{CC} = 10V$, $I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$, $I_O = +10\ \mu A$ $V_{CC} = 10V$, $I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.01	15	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* (MM54C86/MM74C86) $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Time to Logical "1" or "0"	$V_{CC} = 5.0V$		110	185	ns
		$V_{CC} = 10V$		50	90	ns
C_{IN}	Input Capacitance	Note 2		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

*AC Parameters are guaranteed by DC correlated testing.

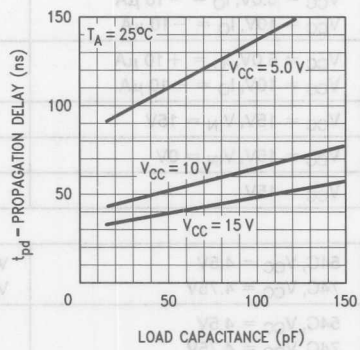
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note—AN-90.

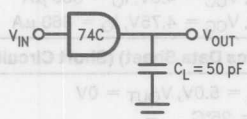
Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance MM54C86/MM74C86



TL/F/5887–2

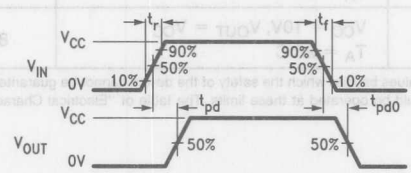
AC Test Circuit



TL/F/5887–3

Note: Delays Measured with Input t_r, t_f = 20 ns

Switching Time Waveforms



TL/F/5887–4

National Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE data output lines working in conjunction with the memory enable input provide for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

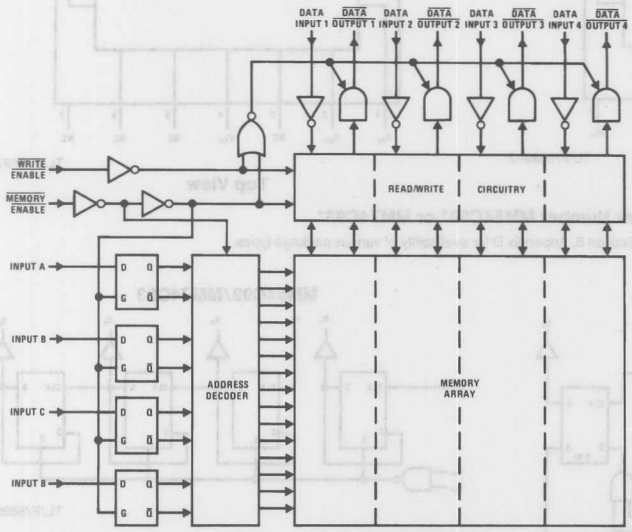
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

Features

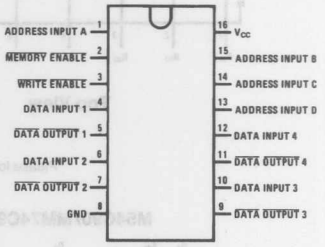
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	100 nW/package (typ.)
■ Fast access time	130 ns (typ.) at V_{CC} = 10V
■ TRI-STATE output	

Logic and Connection Diagrams



TL/F/5888–1

Dual-In-Line Package



Top View TL/F/5888–2

Order Number MM54C89* or MM74C89*

*Please look into Section 8, Appendix D for availability of various package types.

National Semiconductor

MM54C90/MM74C90 4-Bit Decade Counter
MM54C93/MM74C93 4-Bit Binary Counter

General Description

The MM54C90/MM74C90 decade counter and the MM54C93/MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}, and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

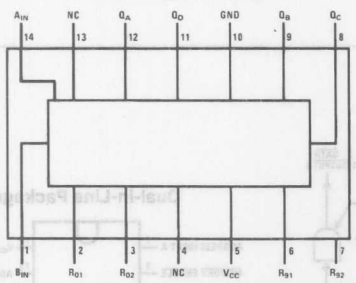
All inputs are protected against static discharge damage.

Features

- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatiblity — Fan out of 2 driving 74L
- The MM54C93/MM74C93 follows the MM54L93/MM74L93 Pinout

Connection and Logic Diagrams

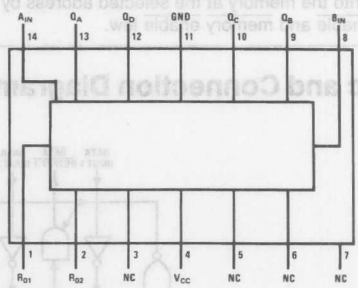
MM54C90/MM74C90
Dual-In-Line Package



TL/F/5889–2

Top View

MM54C93/MM74C93
Dual-In-Line Package



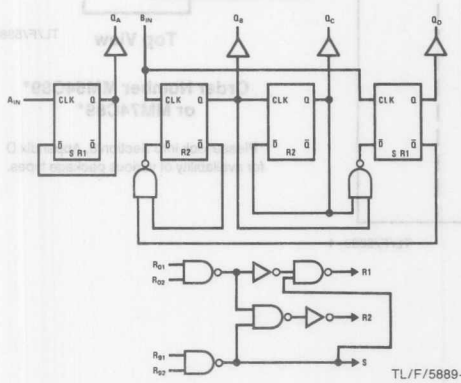
TL/F/5889–4

Top View

Order Number MM54C90* or MM74C93*

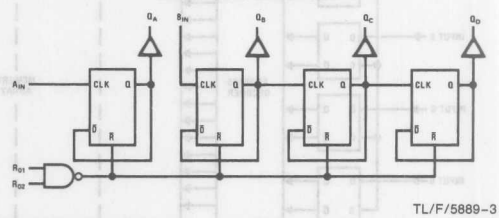
*Please look into Section 8, Appendix D for availability of various package types.

M54C90/MM74C90



TL/F/5889–1

MM54C93/MM74C93



TL/F/5889–3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (Note 1) $-0.3V$ to $V_{CC} + 0.3V$

Operating Temperature Range (T_A)

MM54C90, MM54C93 $-55°C$ to $+125°C$

MM74C90, MM74C93 $-40°C$ to $+85°C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V_{CC} Range 3V to 15V

Absolute Maximum V_{CC} 18V

Storage Temperature Range (T_S) $-65°C$ to $+150°C$

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10\ \mu A$ $V_{CC} = 10V, I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = +10\ \mu A$ $V_{CC} = 10V, I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC} = 4.5V$ $V_{CC} = 4.75V$	 $V_{CC} - 1.5$ $V_{CC} - 1.5$			 V V
$V_{IN(0)}$	Logical "0" Input Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC} = 4.5V$ $V_{CC} = 4.75V$			 0.8 0.8	 V V
$V_{OUT(1)}$	Logical "1" Output Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC} = 4.5V, I_O = -360\ \mu A$ $V_{CC} = 4.75V, I_O = -360\ \mu A$	 2.4 2.4			 V V
$V_{OUT(0)}$	Logical "0" Output Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC} = 4.5V, I_O = -360\ \mu A$ $V_{CC} = 4.75V, I_O = -360\ \mu A$			 0.4 0.4	 V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, V_{OUT} = 0V$ $T_A = 25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V$ $T_A = 25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, V_{OUT} = V_{CC}$ $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}$ $T_A = 25°C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C, C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_A	$V_{CC} = 5V$ $V_{CC} = 10$		200 80	400 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_B (MM54C93/MM74C93)	$V_{CC} = 5V$ $V_{CC} = 10V$		450 160	850 300	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_B (MM54C90/MM74C90)	$V_{CC} = 5V$ $V_{CC} = 10V$		450 160	800 300	ns ns

t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10		200	400	ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		500 200	1000 400	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		600 250	1200 500	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		450 160	800 300	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		150 75	300 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		200 75	400 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{91} or R_{92} to Q_A or Q_D (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		250 100	500 200	ns ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V	600 30	250 125		ns ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V	600 300	250 125		ns ns
t_{PW}	Min. R_{91} or R_{92} Pulse Width (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V	500 250	200 100		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	V_{CC} = 10V V_{CC} = 10V			15 5	μs μs
t_W	Minimum Clock Pulse Width	V_{CC} = 5V V_{CC} = 10V	250 100	100 50		ns ns
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5V V_{CC} = 10V	2 5			MHz MHz
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		45		pF

*AC Parameters are guaranteed by DC correlated testing.

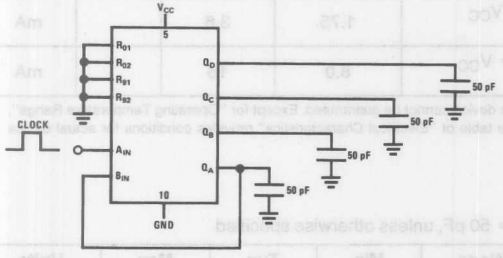
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note—AN-90.

AC Test Circuits

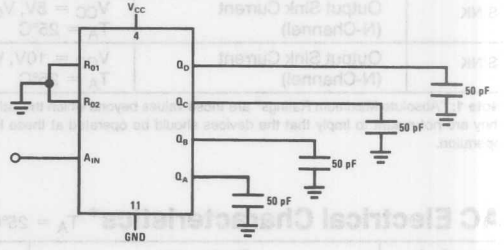
MM54C90/MM74C90



TL/F/5889–5

Clock rise and fall time $t_r = t_f = 20$ ns

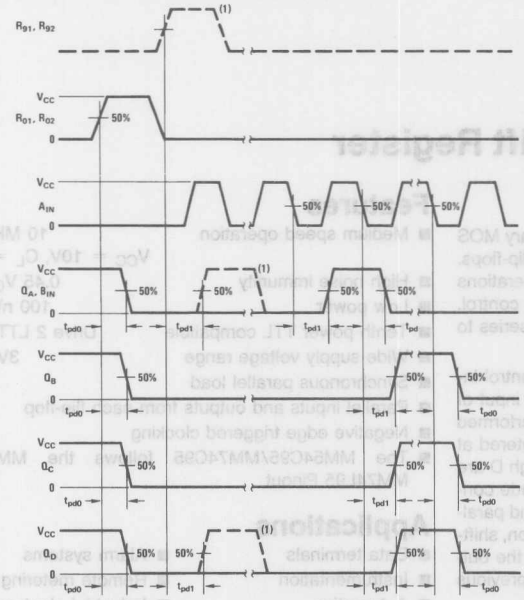
MM54C93/MM74C93



TL/F/5889–6

Clock rise and fall time $t_r = t_f = 20$ ns

Switching Time Waveforms



Note 1: MM54C90, MM74C90 and MM54C93, MM74C93 are solid line waveforms. Dashed line waveforms are for MM54C90/MM74C90 only.

TL/F/5889–7

Truth Table

MM54C90/MM74C90 4-Bit Decade Counter

BCD Count Sequence

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to Input B for BCD count.

H = High Level
L = Low Level
X = Irrelevant

Reset/Count Function Table

Reset Inputs				Output			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	Count			
L	X	L	X	Count			
L	X	X	L	Count			
X	L	L	X	Count			

MM54C93/MM74C93 4-Bit Binary Counter

Binary Count Sequence

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence.

H = High Level
L = Low Level
X = Irrelevant

Reset/Count Function Table

Reset Inputs		Output			
R_{01}	R_{02}	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	Count			
X	L	Count			

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National Semiconductor

MM54C95/MM74C95
4-Bit Right-Shift Left-Shift Register

General Description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip-flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift register.

When a logical "0" level is applied to the mode control input, the output of each flip-flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop and serial data is entered at input D.

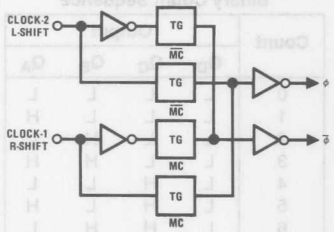
Features

- Medium speed operation — 10 MHz (typ.) V_{CC} = 10V, C_L = 50 pF
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 100 nW/(typ.)
- Tenth power TTL compatible — Drive 2 LTTL loads
- Wide supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Negative edge triggered clocking
- The MM54C95/MM74C95 follows the MM54L95/MM74L95 Pinout

Applications

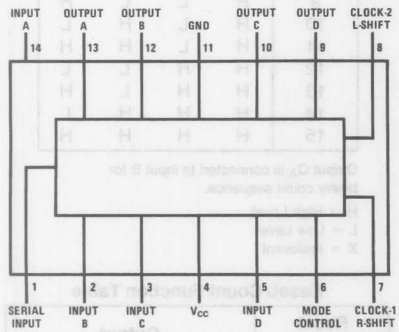
- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

Block and Connection Diagrams



TL/F/5890–1

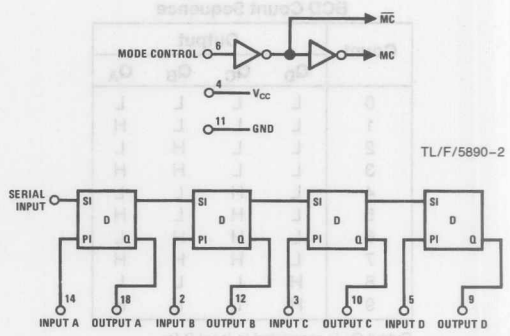
Dual-In-Line Package



TL/F/5890–4

Order Number MM54C95* or MM74C95*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5890–2

TL/F/5890–3

Mode Control = 0 for Right Shift

Mode Control = 1 for Left Shift or Parallel Load

contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin $-0.3V$ to $V_{CC}+0.3V$

Operating Temperature Range (T_A)
- MM54C95 $-55°C$ to $+125°C$
- MM74C95 $-40°C$ to $+85°C$

Maximum V_{CC} Voltage 18V

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Operating V_{CC} Range $+3V$ to $+15V$

Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1.0			μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.050	300	μA
LOW POWER TTL/CMOS INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V$, $V_{IN(1)} = 5V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	V_{CC} = 5V V_{CC} = 10V		200 80	400 160	ns ns
t_{S0}, t_{S1}	Time Prior to Clock Pulse that Data must be Preset	V_{CC} = 5V V_{CC} = 10V	60 25	30 10		ns ns
t_{H0}, t_{H1}	Time After Clock Pulse that Data must be Held	V_{CC} = 5V V_{CC} = 10V	25 10	10 50		ns ns
t_{PW}	Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5V V_{CC} = 10V		100 50		ns ns
t_{SM}	Time Prior to Clock Pulse that Mode Control must be Preset	V_{CC} = 5V V_{CC} = 10V	200 100	100 50		ns ns
f_{MAX}	Maximum Input Clock Frequency	V_{CC} = 5V V_{CC} = 10V	3 6.5	5 10		MHz MHz
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, Application Note AN-90.

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	c	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	L	H	X	X	X	X	X	Undefined			
↓	H	L	X	X	X	X	X	Operating Conditions			

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C or Q_D respectively, before the most recent transition of the clock.

National Semiconductor

MM54C150/MM74C150 16-Line to 1-Line Multiplexer MM72C19/MM82C19 TRI-STATE® 16-Line to 1-Line Multiplexer

General Description

The MM54C150/MM74C150 and MM72C19/MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

A strobe override places the output of MM54C150/MM74C150 in the logical "1" state and the output of MM72C19/MM82C19 in the high-impedance state.

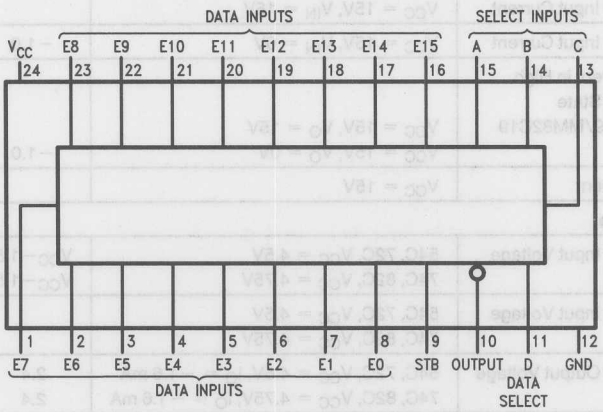
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Drive 1 TTL Load

Connection Diagram

Dual-In-Line Package



TL/F/5891–1

Order Number MM54C150*, MM74C150*, MM72C19* or MM82C19*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C150, MM72C19	$-55°C$ to $+125°C$
MM74C150, MM82C19	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature (soldering, 10 seconds)	260°C

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V, I_O = -10\ \mu A$ $V_{CC} = 10V, I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V, I_O = +10\ \mu A$ $V_{CC} = 10V, I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	V
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{OZ}	Output Current in High Impedance State MM72C19/MM82C19	$V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$	 -1.0	0.005 -0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, 72C, $V_{CC} = 4.5V$ 74C, 82C, $V_{CC} = 4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, 72C, $V_{CC} = 4.5V$ 74C, 82C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, 72C, $V_{CC} = 4.5V, I_O = -1.6$ mA 74C, 82C, $V_{CC} = 4.75V, I_O = -1.6$ mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, 72C, $V_{CC} = 4.5V, I_O = 1.6$ mA 74C, 82C, $V_{CC} = 4.75V, I_O = 1.6$ mA			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C$	-4.35	-8		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C$	-20	-40		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C$	4.35	8		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C$	20	40		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Inputs to Output	$V_{CC} = 5.0V$		250	600	ns
		$V_{CC} = 10V$		110	300	ns
		$V_{CC} = 5.0V$, $C_L = 150$ pF		290	650	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		120	330	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Select Inputs to Output	$V_{CC} = 5.0V$		290	650	ns
		$V_{CC} = 10V$		120	330	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe to Output MM54C150/MM74C150	$V_{CC} = 5.0V$		120	300	ns
		$V_{CC} = 10V$		55	150	ns
t_{1H}, t_{0H}	Delay from Strobe to High Impedance State MM72C19/MM82C19	$V_{CC} = 5.0V$, $R_L = 10k$, $C_L = 5$ pF		80	200	ns
		$V_{CC} = 10V$, $R_L = 10k$, $C_L = 5$ pF		60	150	ns
t_{H1}, t_{H0}	Delay from Strobe to Logical "1" Level or to Logical "0" Level (from High Impedance State) MM72C19/MM82C19	$V_{CC} = 5.0V$, $R_L = 10k$, $C_L = 5$ pF		80	250	ns
		$V_{CC} = 10V$, $R_L = 10k$, $C_L = 5$ pF		30	120	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance MM72C19/MM82C19	(Note 2)		11.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

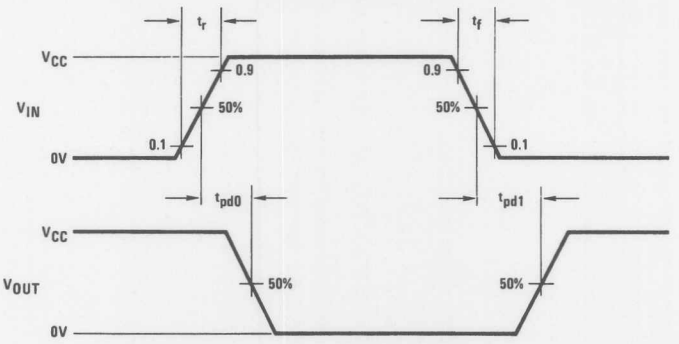
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, application note AN-90.

D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1*
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
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0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

*For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

Switching Time Waveforms

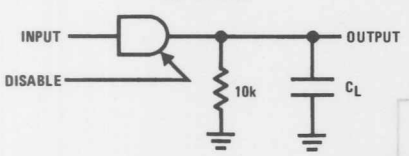
CMOS to CMOS



TL/F/5891–2

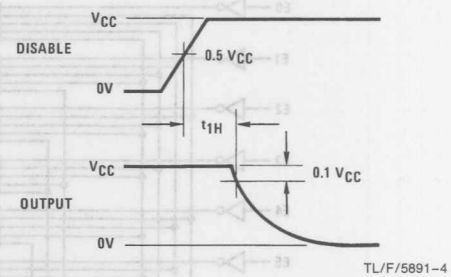
Switching Time Waveforms (Continued)

t_{1H} and t_{H1}



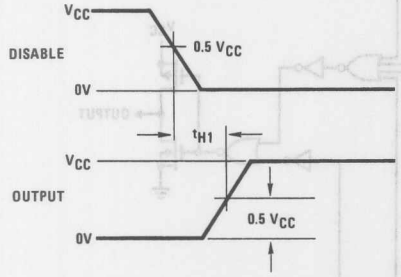
TL/F/5891–3

t_{1H}



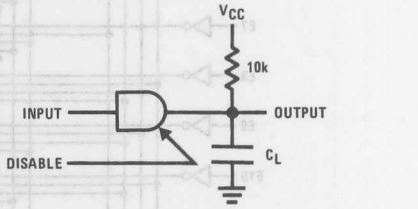
TL/F/5891–4

t_{H1}



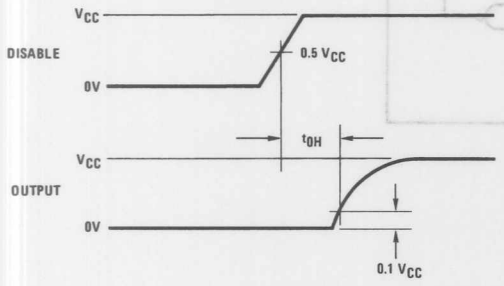
TL/F/5891–5

t_{0H} and t_{H0}



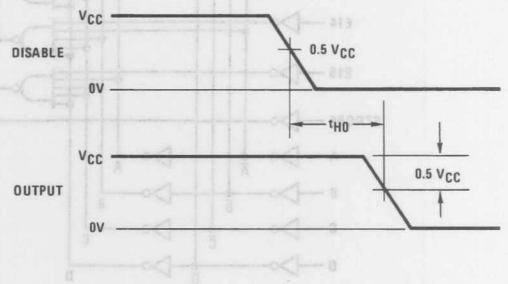
TL/F/5891–6

t_{0H}



TL/F/5891–7

t_{H0}

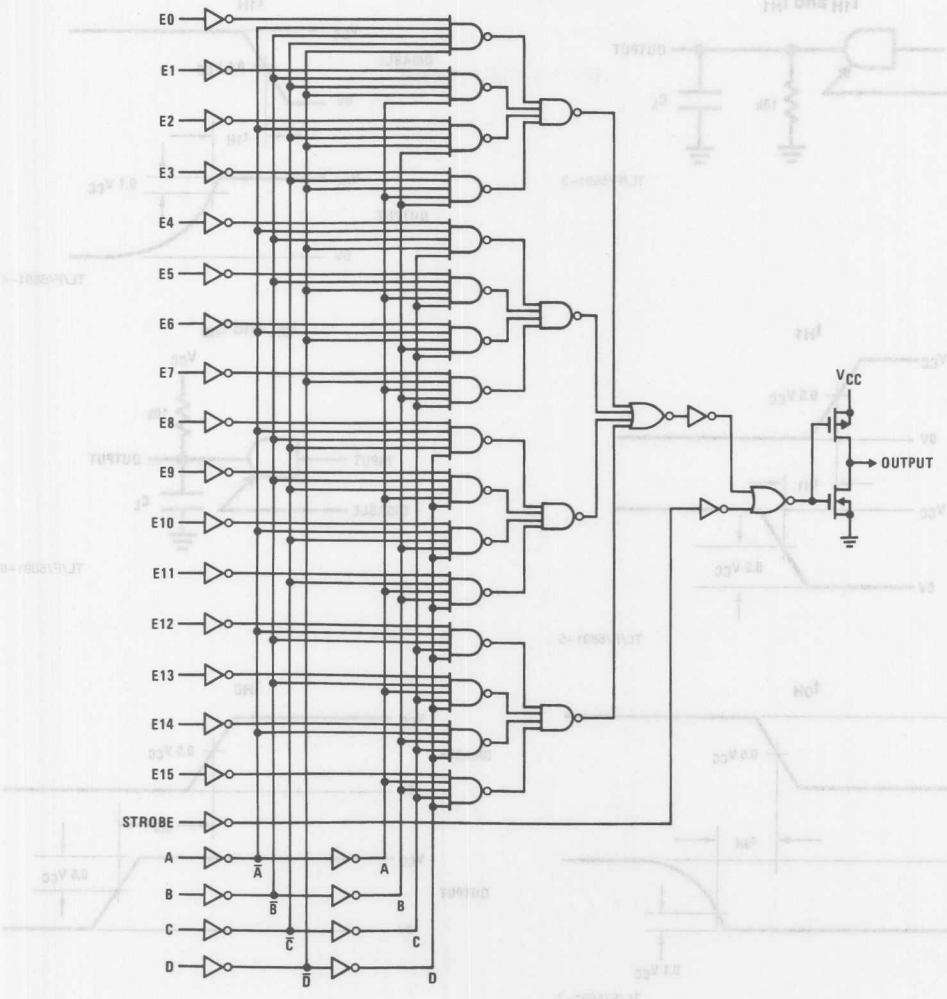


TL/F/5891–8

Note: Delays measured with input t_r, $t_f \leq 20$ ns.

Logic Diagrams

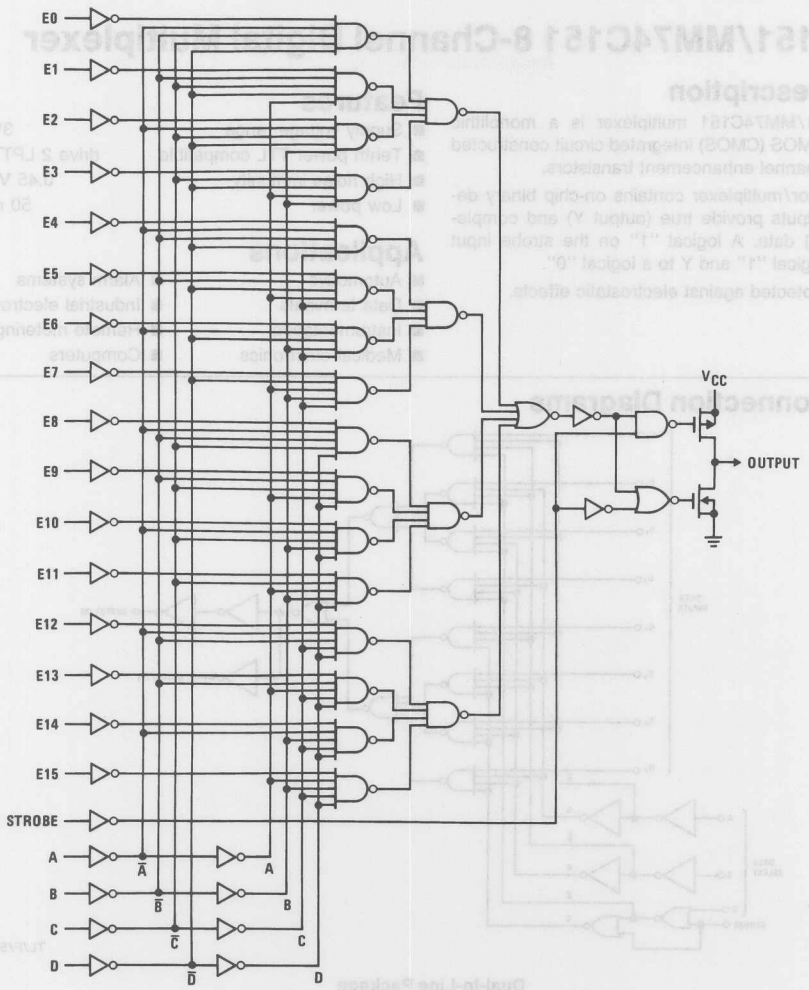
MM54C150/MM74C150



TL/F/5891–9

Logic Diagrams (Continued)

MM72C19/MM82C19



TL/F/5891–10

MM54C151/MM74C151 8-Channel Digital Multiplexer

General Description

The MM54C151/MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the strobe input forces W to a logical "1" and Y to a logical "0".

All inputs are protected against electrostatic effects.

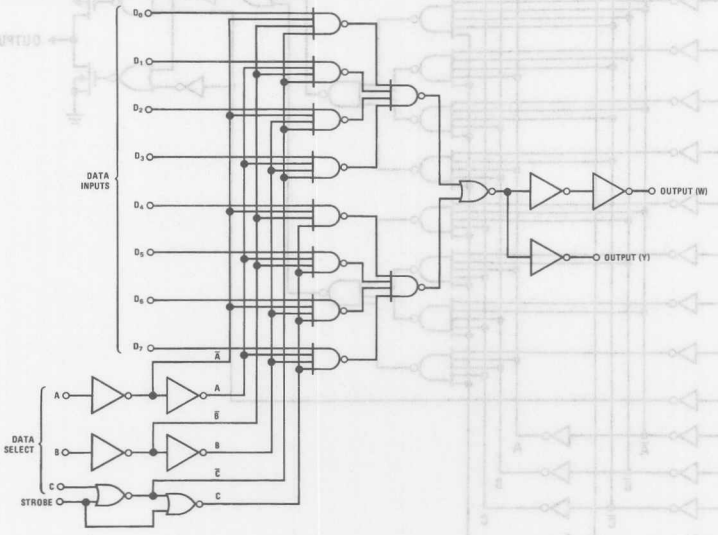
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)

Applications

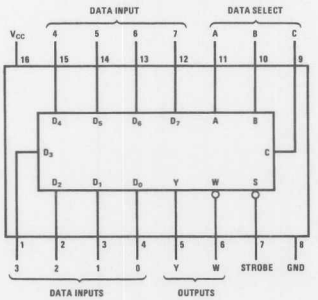
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic & Connection Diagrams



TL/F/5892–1

Dual-In-Line Package



TL/F/5892–2

Top View

Order Number MM54C151* or MM74C151*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C151	−55°C to +125°C
MM74C151	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18V
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA V_{CC} = 10V, I_O = 10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0			μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V mA
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA 74C V_{CC} = 4.75V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA 74C V_{CC} = 4.75V, I_O = 360 μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

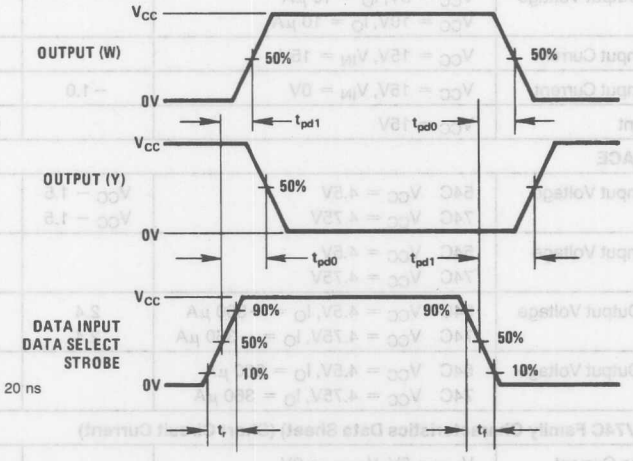
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y	$V_{CC} = 5V$, $V_{CC} = 10V$		170 80	270 130	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data to W	$V_{CC} = 5V$, $V_{CC} = 10V$		200 90	300 140	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y	$V_{CC} = 5V$, $V_{CC} = 10V$		240 110	360 170	ns ns
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		50		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

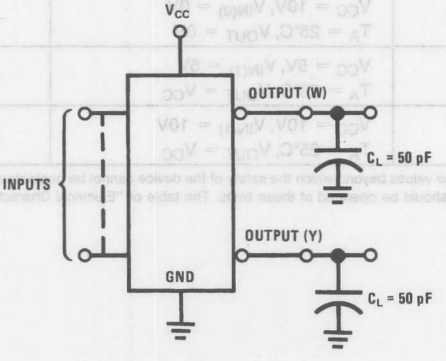
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

Switching Time Waveforms



TL/F/5892–3

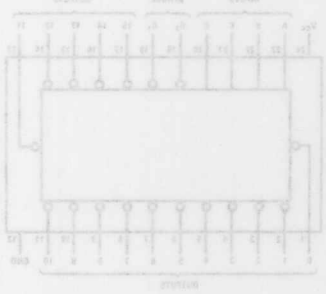
AC Test Circuit

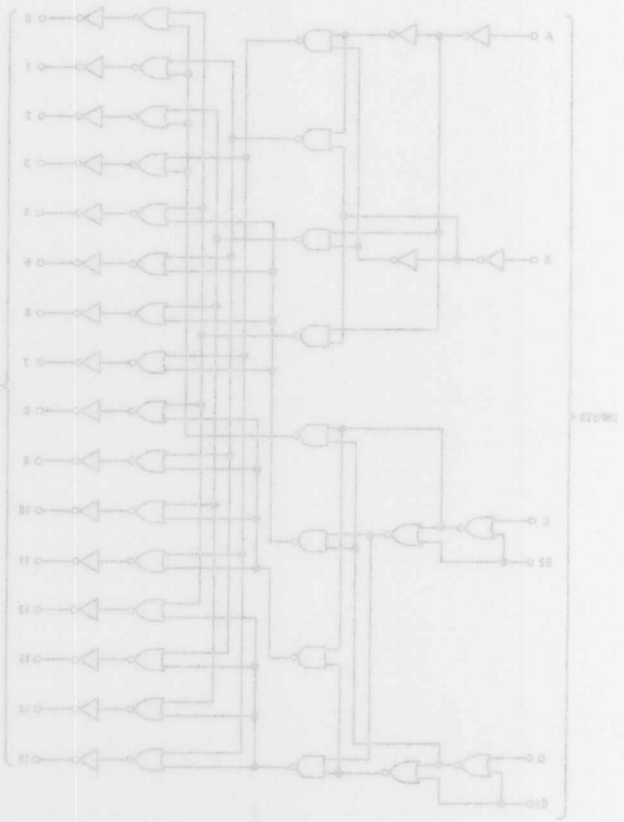


TL/F/5892–4

Truth Table

Inputs												Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0





MM54C154/MM74C154 4-Line to 16-Line Decoder/Demultiplexer

General Description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

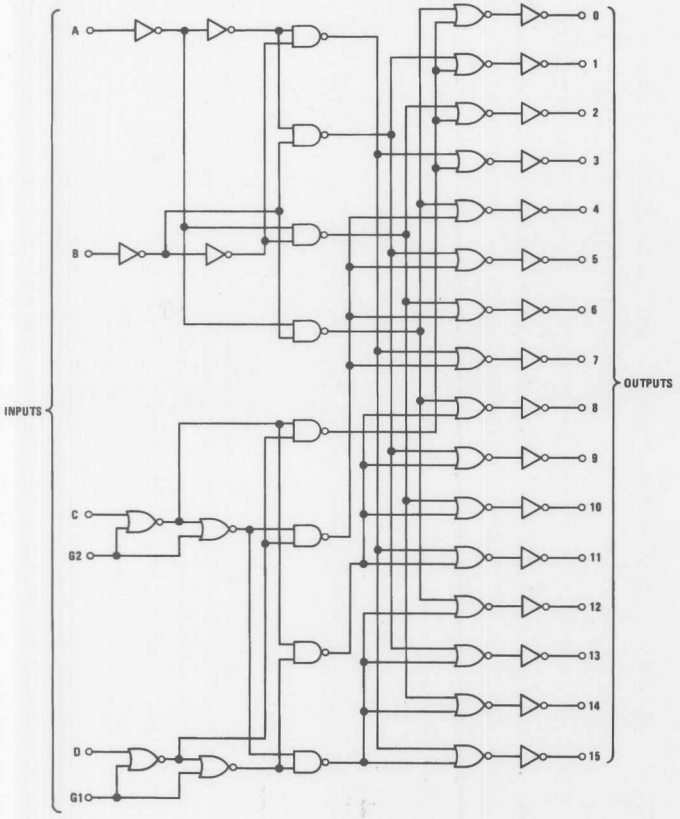
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	Drive 2 LPTTL loads
■ High noise margin	1V guaranteed
■ High noise immunity	0.45 V_{CC} (typ.)

Applications

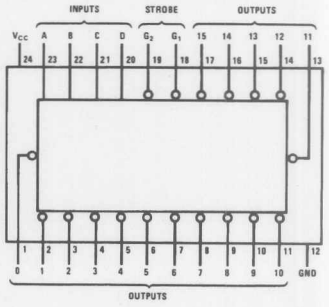
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic & Connection Diagrams



TL/F/5893–1

Dual-In-Line Package



TL/F/5893–2

Top View

Order Number MM54C154* or MM74C154*

*Please look into Section 8, Appendix D for availability of various package types.

Operating Temperature Range		Dual-In-Line	700 mW
MM54C154	−55°C to +125°C	Small Outline	500 mW
MM74C154	−40°C to +85°C	Operating V_{CC} Range	3V to 15V
		Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10μA V_{CC} = 10V, I_O = 10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −100 μA 74C V_{CC} = 4.75V, I_O = −100 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA 74C V_{CC} = 4.75V, I_O = 360 μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

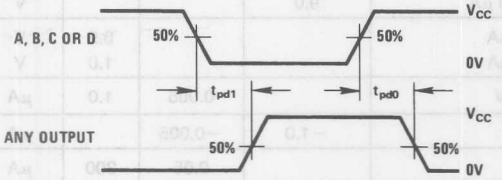
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" from Any Input to Any Output	$V_{CC} = 5.0V$		275	400	ns
		$V_{CC} = 10V$		100	200	ns
t_{pd0}	Propagation Delay to a Logical "0" from G1 or G2 to Any Output	$V_{CC} = 5.0V$		275	400	ns
		$V_{CC} = 10V$		100	200	ns
t_{pd0}	Propagation Delay to a Logical "0" from Any Input to Any Output	$V_{CC} = 5.0V$		265	400	ns
		$V_{CC} = 10V$		100	200	ns
t_{pd1}	Propagation Delay to a Logical "1" from G1 or G2 to Any Output	$V_{CC} = 5.0V$		265	400	ns
		$V_{CC} = 10V$		100	200	ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

*AC Parameters are guaranteed by DC correlated testing.

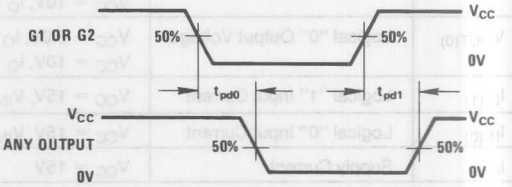
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

Switching Time Waveforms



TL/F/5893–3



TL/F/5893–4

$t_r = t_f = 20$ ns

Truth Table

Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

National Semiconductor

MM54C157/MM74C157 Quad 2-Input Multiplexers

General Description

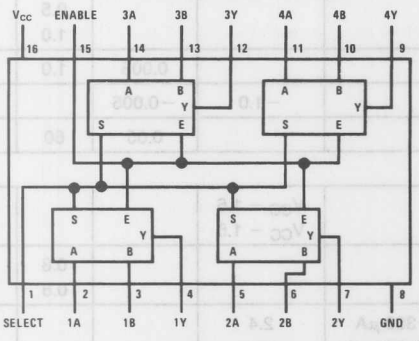
These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1", the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

Features

- Supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Tenth power TTL compatible — Drive 2 LPTTL loads

Logic & Connection Diagrams

Dual-In-Line Package

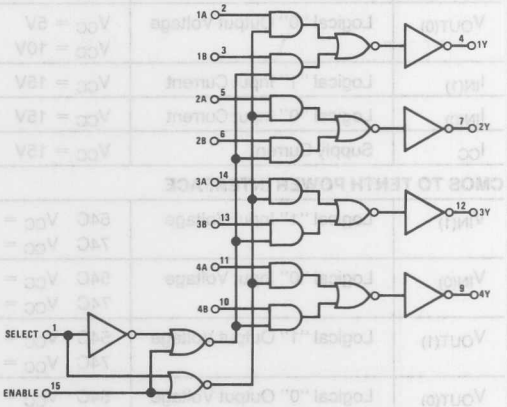


TL/F/5894–2

Top View

Order Number MM54C157* or MM74C157*

*Please look into Section 8, Appendix D for availability of various package types.

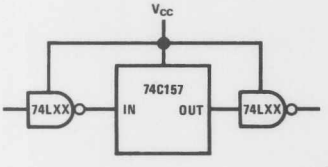


TL/F/5894–1

Truth Table

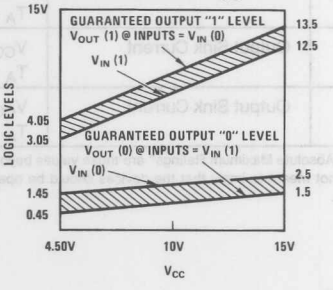
Enable	Select	A	B	Output Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

74L Compatibility



TL/F/5894–3

Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5894–4

Voltage at Any Pin $-0.3V$ to $V_{CC} + 0.3V$

Operating Temperature Range
- MM54C157 $-55°C$ to $+125°C$
- MM74C157 $-40°C$ to $+85°C$

Dual-In-Line 700 mW
Small Outline 500 mW
Operating V_{CC} Range 3V to 15V
Lead Temperature (Soldering, 10 sec.) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	60	μA
CMOS TO TENTH POWER INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -360\ \mu A$ 74C $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = 360\ \mu A$ 74C $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V$, $V_{IN(1)} = 5V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay from Data to Output	$V_{CC} = 5.0V$ $V_{CC} = 10V$		150 70	250 110	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Select to Output	$V_{CC} = 5V$ $V_{CC} = 10V$		180 80	300 130	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Enable to Output	$V_{CC} = 5V$ $V_{CC} = 10V$		180 80	300 130	ns ns
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		20		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, Application Note AN-90.

6

National Semiconductor

MM54C160/MM74C160 Decade Counter with Asynchronous Clear
MM54C161/MM74C161 Binary Counter with Asynchronous Clear
MM54C162/MM74C162 Decade Counter with Synchronous Clear
MM54C163/MM74C163 Binary Counter with Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits contructed with N- and P-channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear inputs sets all four outputs low regardless of the state of the clock.

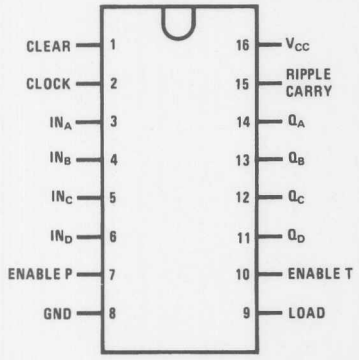
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- High noise margin — 1V guaranteed
- High noise immunity — 0.45 V_{CC} (typ.)
- Tenth power TTL compatible — Drives 2 LPTTL loads
- Wide supply voltage range — 3V to 15V
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable

Connection Diagram

Dual-In-Line Package



TL/F/5895–1

Order Number MM54C160*, MM74C160*, MM54C161*, MM74C161*, MM54C162*, MM74C162*, MM54C163* or MM74C163*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C160/1/2/3	−55°C to +125°C
MM74C160/1/2/3	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V	V_{CC}−1.5			V
		74C V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V			0.8	V
		74C V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA	2.4			V
		74C V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA			0.4	V
		74C V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

t_{pd}	Propagation Delay Time from Clock to Q	V_{CC} = 5V		250	400	ns
		V_{CC} = 10V		100	160	ns
t_{pd}	Propagation Delay Time from Clock to Carry Out	V_{CC} = 5V		290	450	ns
		V_{CC} = 10V		120	190	ns
t_{pd}	Propagation Delay Time from T Enable to Carry Out	V_{CC} = 5V		180	290	ns
		V_{CC} = 10V		70	120	ns
t_{pd}	Propagation Time from Clear to Q (C160 and C161 only)	V_{CC} = 5V		190	300	ns
		V_{CC} = 10V		80	150	ns
t_S	Time prior to Clock that Data or Load must be Present	V_{CC} = 5V			120	ns
		V_{CC} = 10V			30	ns
t_S	Time prior to Clock that Enable P or T must be Present	V_{CC} = 5V		170	280	ns
		V_{CC} = 10V		70	120	ns
t_S	Time prior to Clock that Clear must be Present (162, 163 only)	V_{CC} = 5V		120	190	ns
		V_{CC} = 10V		50	80	ns
t_W	Minimum Clock Pulses Width	V_{CC} = 5V		90	170	ns
		V_{CC} = 10V		35	70	ns
t_r, t_f	Maximum Clock Rise or Fall Time	V_{CC} = 5V			15	μs
		V_{CC} = 10V			5	μs
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5V	2.0	3		MHz
		V_{CC} = 10V	5.5	8.5		MHz
C_{PD}	Power Dissipation Capacitance	(Note 3)		95		pF
C_{IN}	Input Capacitance	(Note 2)		5		pF

*AC Parameters are guaranteed by DC correlated testing.

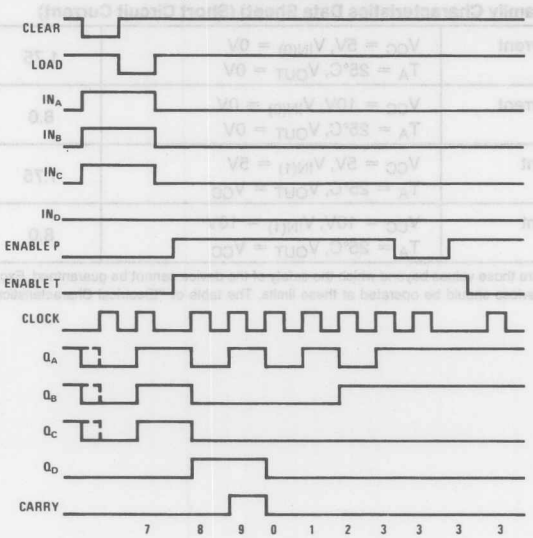
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

Logic Waveforms

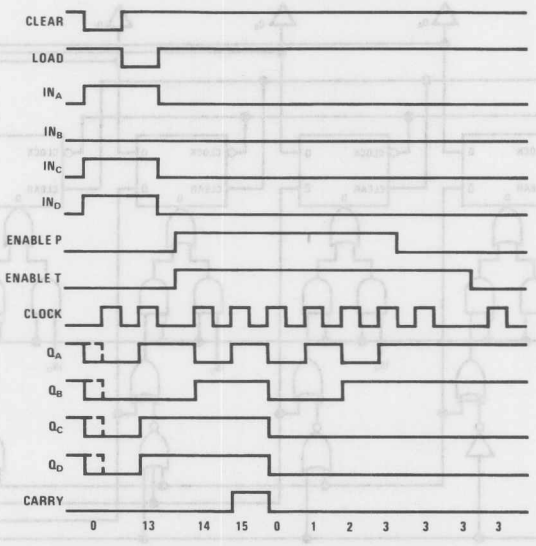
C160, C163 Decade Counters



TL/F/5895–2

Logic Waveforms (Continued)

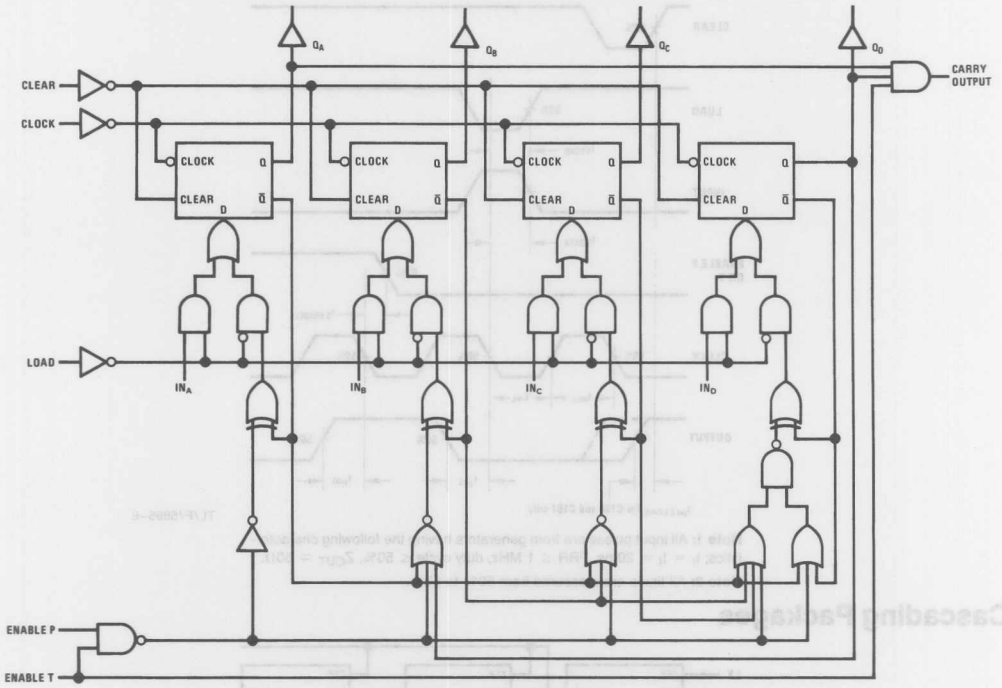
C161, . . . C163 Binary Counters



TL/F/5895–3

Logic Diagrams

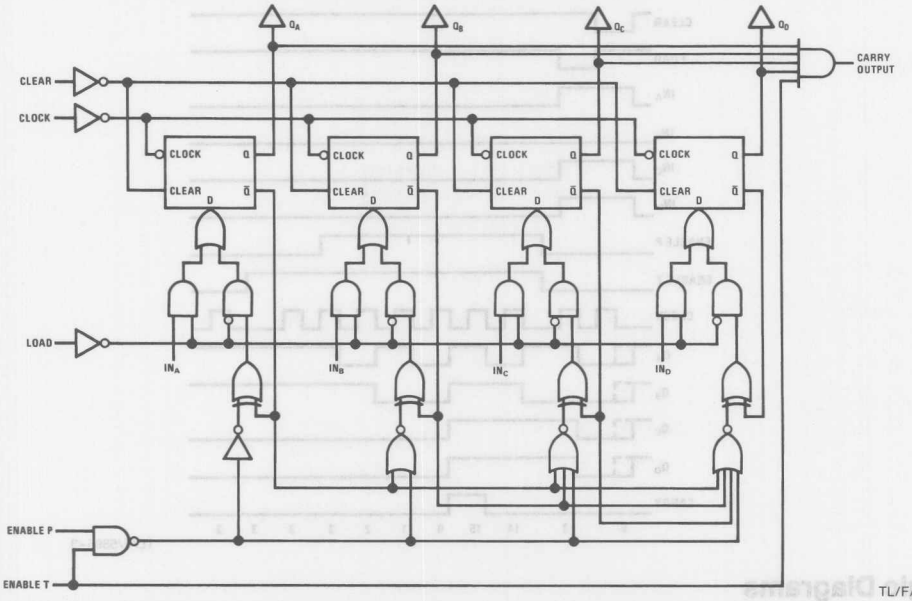
MM74C160, MM74C162; Clear is Synchronous for the MM74C162



TL/F/5895–4

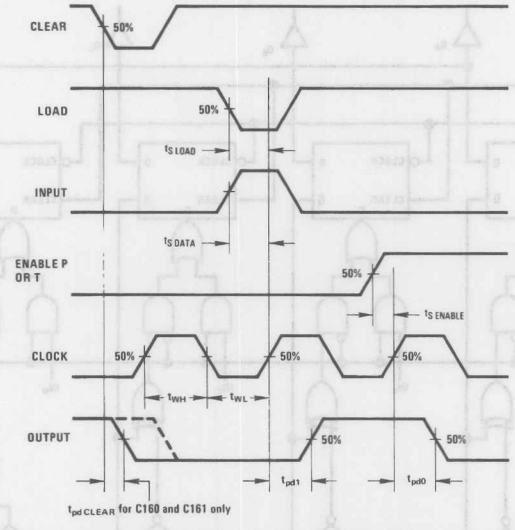
Logic Diagrams (Continued)

MM74C161, MM74C163; Clear is Synchronous for the MM74C163



TL/F/5895–5

Switching Time Waveforms

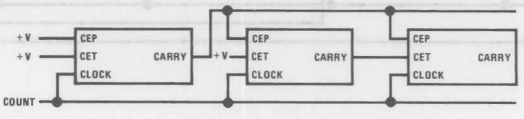


TL/F/5895–6

Note 1: All input pulses are from generators having the following characteristics; $t_r = t_f = 20$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages



TL/F/5895–7

National Semiconductor

MM54C164/MM74C164
8-Bit Parallel-Out Serial Shift Register

General Description

The MM54C164/MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. A high-level input enables the other input which will then determine the state of the flip-flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

Features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Medium speed operation — 0.8 MHz (typ.) with 10V supply

Applications

- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

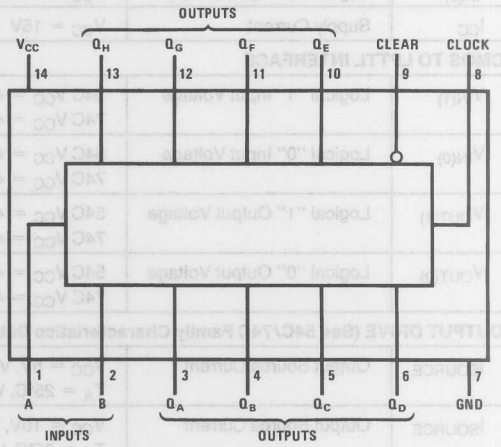
Truth Table

Serial Inputs A and B

Inputs t_n		Output t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

Connection Diagram

Dual-In-Line Package



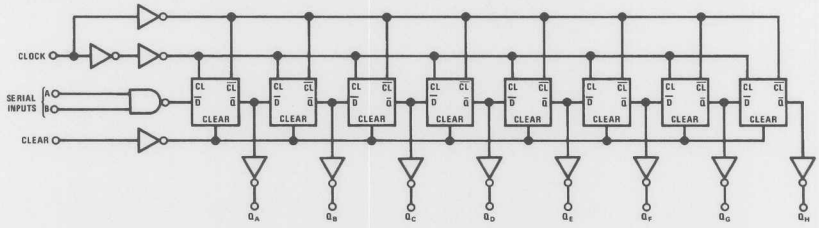
TL/F/5896–2

Top View

Order Number MM54C164* or MM74C164*

*Please look into Section 8, Appendix D for availability of various package types.

Block Diagram



TL/F/5896–1

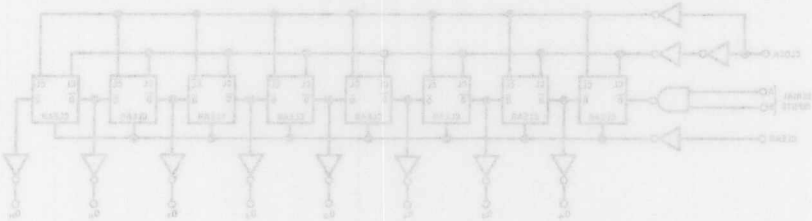
Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C164	$-55°C$ to $+125°C$
MM74C164	$-40°C$ to $+85°C$
Absolute Maximum V_{CC}	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10\ \mu A$ $V_{CC} = 10V, I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = +10\ \mu A$ $V_{CC} = 10V, I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V, I_O = -360\ \mu A$ 74C $V_{CC} = 4.75V, I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V, I_O = 360\ \mu A$ 74C $V_{CC} = 4.75V, I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25°C, V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25°C, V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25°C, V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25°C, V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.



AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

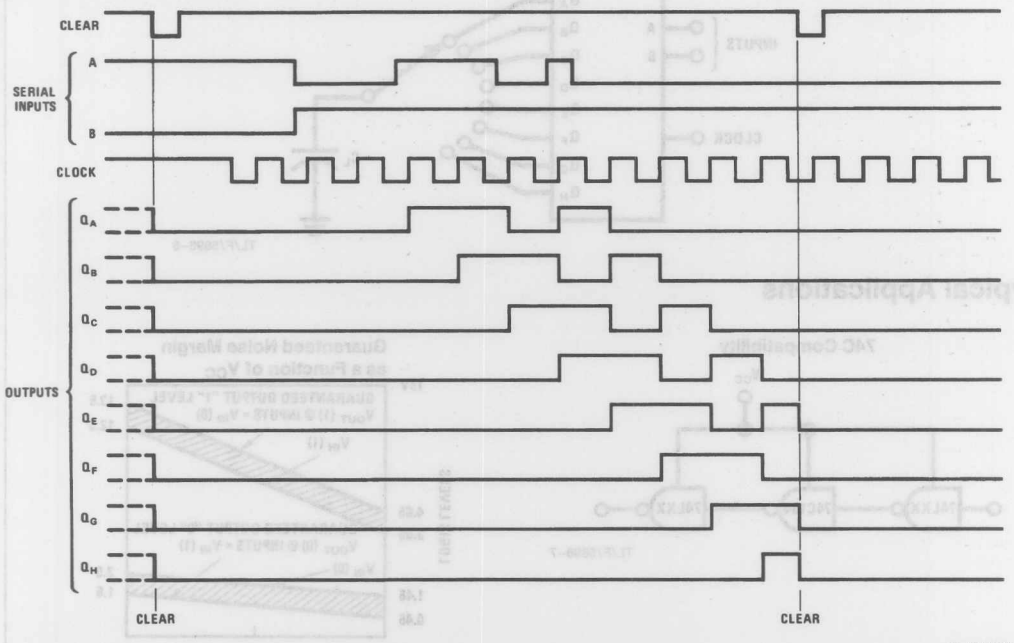
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay Time to a Logical "0" or a Logical "1" from Clock to Q	$V_{CC} = 5V$ $V_{CC} = 10V$		230 90	310 120	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5V$ $V_{CC} = 10V$		280 110	380 150	ns ns
t_S	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$	200 80	110 30		ns ns
t_H	Time After Clock Pulse that Data Must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$	0 0	0 0		ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.0 5.5	3 8		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		150 55	250 90	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	15 5			μs μs
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		140		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 2: Capacitance is guaranteed by periodic testing.

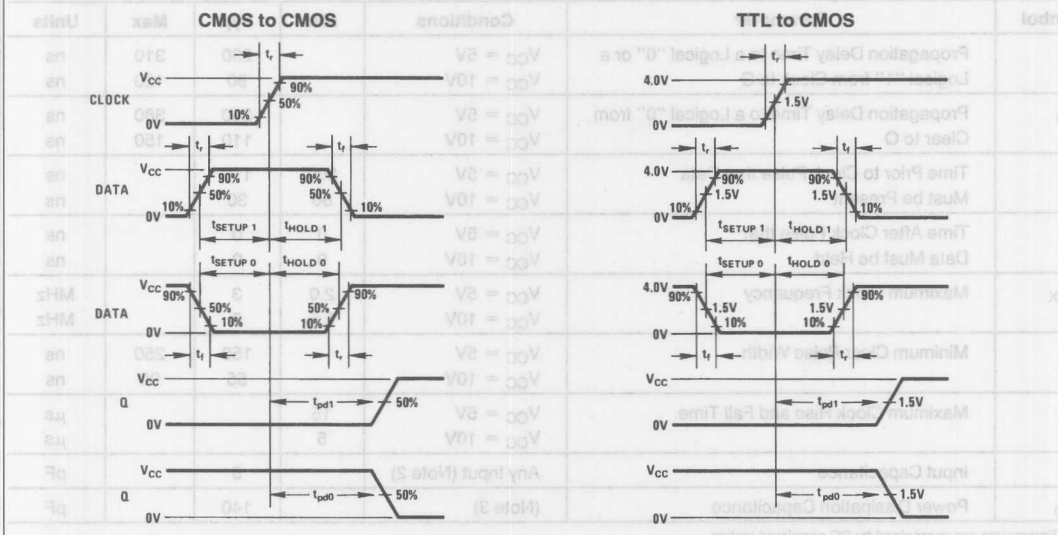
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Logic Waveforms



TL/F/5896–3

Switching Time Waveforms

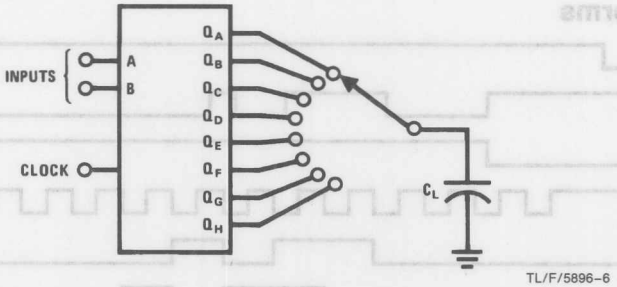


TL/F/5896–4

TL/F/5896–5

$t_r = t_f = 20$ ns

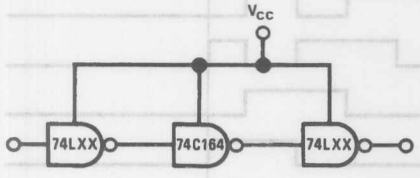
AC Test Circuit



TL/F/5896–6

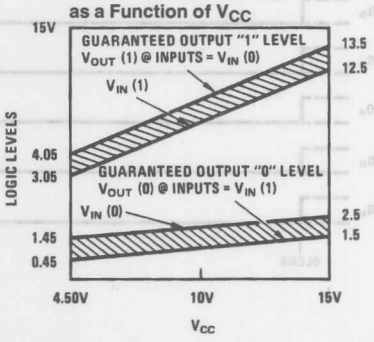
Typical Applications

74C Compatibility



TL/F/5896–7

Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5896–8

MM54C165/MM74C165
Parallel-Load 8-Bit Shift Register

General Description

The MM54C165/MM74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eighth bit.

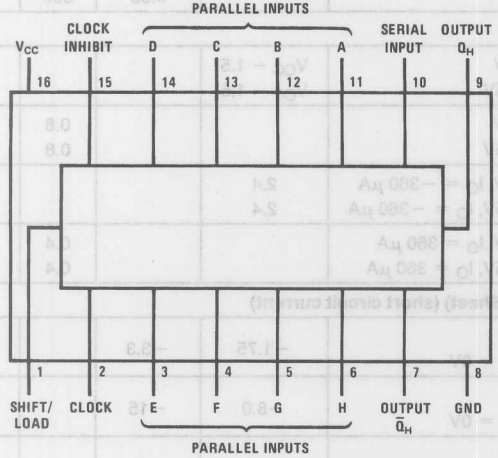
Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

Features

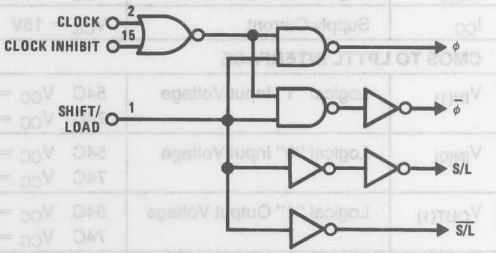
■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Direct overriding load	
■ Gated clock inputs	
■ Fully static operation	

Connection and Block Diagrams

Dual-In-Line Package



TL/F/5897–1

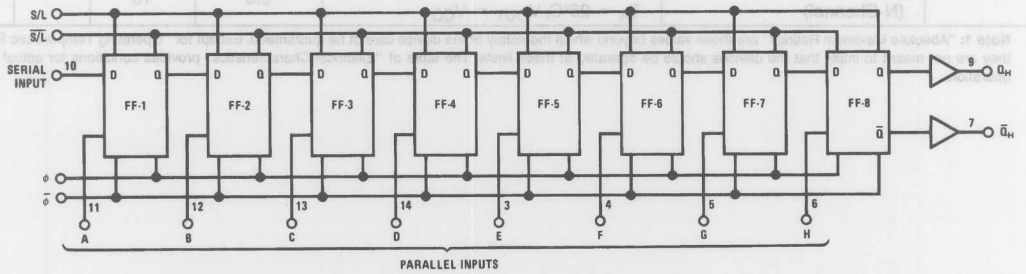


TL/F/5897–2

Order Number MM54C165* or MM74C165*

*Please look into Section 8, Appendix D for availability of various package types.

Top View



TL/F/5897–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C165	$-55°C$ to $+125°C$
MM74C165	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Absolute Maximum V_{CC}	18V
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10\ \mu A$ $V_{CC} = 10V, I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = +10\ \mu A$ $V_{CC} = 10V, I_O = +10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V, I_O = -360\ \mu A$ 74C $V_{CC} = 4.75V, I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V, I_O = 360\ \mu A$ 74C $V_{CC} = 4.75V, I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$ $T_A = 25°C, V_{OUT} = 0V$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$ $T_A = 25°C, V_{OUT} = 0V$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$ $T_A = 25°C, V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$ $T_A = 25°C, V_{OUT} = V_{CC}$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock or Load to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from H to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_S	Clock Inhibit Set-up Time	$V_{CC} = 5V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_S	Serial Input Set-up Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 30	25 15		ns ns
t_H	Serial Input Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_S	Parallel Input Set-Up Time	$V_{CC} = 5V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_H	Parallel Input Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		70 30	200 100	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		85 30	180 90	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.5 5	6 12		MHz MHz
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	10 5			μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		65		pF

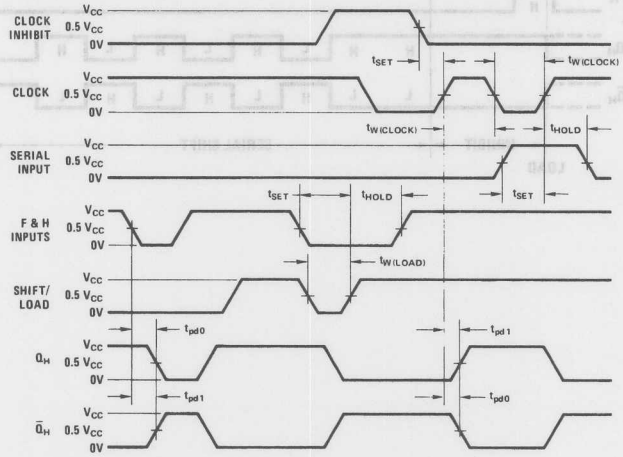
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



TL/F/5897–4

Note A: The remaining six data and the serial input are low.

Note B: Prior to test, high level data is loaded into H input.

Truth Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$

X = irrelevant

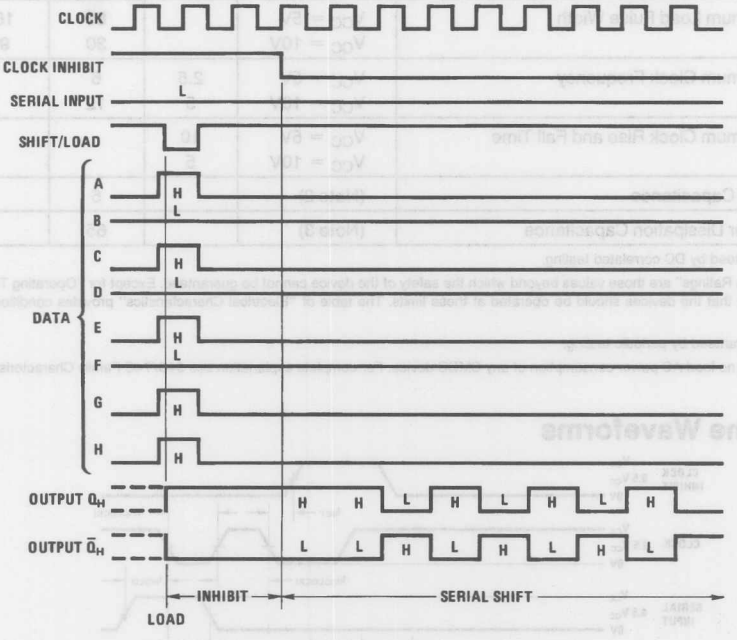
↑ = transition from $V_{IN(0)}$ to $V_{IN(1)}$

a . . . h = the level at data inputs A thru H

Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, before the indicated input conditions were established

Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock

Logic Waveforms



TL/F/5897–5

MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54C173/MM74C173 TRI-STATE quad D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The four D-type flip-flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus-organized systems.

The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip-flops to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive-going transition.

Features

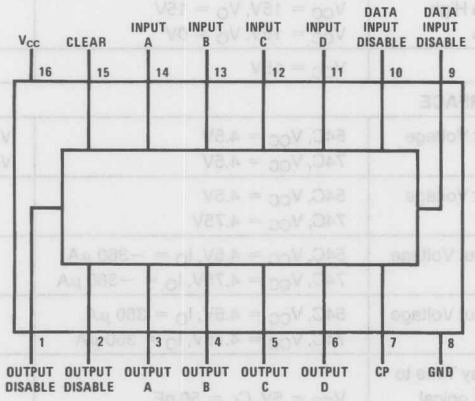
- Supply voltage range 3V to 15V
- Tenth power TTL compatible Drive 2 LPTTL loads
- High noise immunity 0.45 V_{CC} (typ.)
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disable without gating the clock

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line Package



TL/F/5898–2

Top View

Order Number MM54C173* or MM74C173*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

(Both Output Disables Low)

t_n		t_{n+1}
Data Input Disable	**Data Input**	**Output**
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C173	$-55°C$ to $+125°C$
MM74C173	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		-1.0	0.005		μA
I_{OZ}	Output Current in High Impedance State	$V_{CC} = 15V, V_O = 15V$ $V_{CC} = 15V, V_O = 0V$	 -1.0	0.001 0.001	1.0	μA μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	mA
LOW POWER TTL/CMOS INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.5V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360\ \mu A$ 74C, $V_{CC} = 4.75V, I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(1)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V, I_O = 360\ \mu A$			0.4 0.4	V V
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock	$V_{CC} = 5V, C_L = 50$ pF, $T_A = 25°C$		500		ns
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V, V_{IN(0)} = 0V$ $T_A = 25°C, V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V, V_{IN(0)} = 0V$ $T_A = 25°C, V_{OUT} = 0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V, V_{IN(1)} = 5V$ $T_A = 25°C, V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V, V_{IN(1)} = 10V$ $T_A = 25°C, V_{OUT} = V_{CC}$	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Output	$V_{CC} = 5V$ $V_{CC} = 10V$		220 80	400 200	ns ns
t_S	Input Data Set-up Time	$V_{CC} = 5V$ $V_{CC} = 10V$		40 15	80 30	ns ns
t_H	Input Data Hold Time	$V_{CC} = 5V$ $V_{CC} = 10V$		0 0	0 0	ns ns
t_S	Input Disable Set-up Time, $t_{S\ DISS}$	$V_{CC} = 5V$ $V_{CC} = 10V$		100 35	200 70	ns ns
t_H	Input Disable Hold Time, $t_{H\ DISS}$	$V_{CC} = 5V$ $V_{CC} = 10V$		0 0	0 0	ns ns
t_{1H}, t_{0H}	Delay from Output Disable to High Impedance State (from Logical "1" or Logical "0" Level)	$V_{CC} = 5V$, $R_L = 10k$ $V_{CC} = 10V$, $R_L = 10k$		170 70	340 140	ns ns
t_{H1}	Delay from Output Disable to Logical "1" Level (from High Impedance State)	$V_{CC} = 5V$ $V_{CC} = 10V$		170 70	340 140	ns ns
t_{H0}	Delay from Output Disable to Logical "0" Level (from High Impedance State)	$V_{CC} = 5V$ $V_{CC} = 10V$		170 70	340 140	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Clear to Output	$V_{CC} = 5V$ $V_{CC} = 10V$		240 90	490 180	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	3 7.0	4 12		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		150 70		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	10 5			μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)				

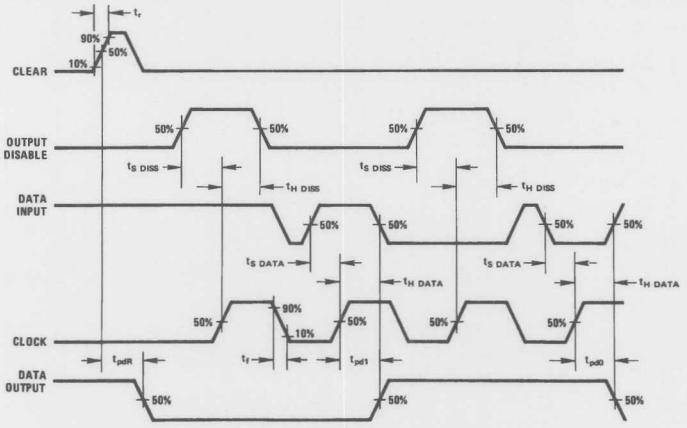
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guarantee.d Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

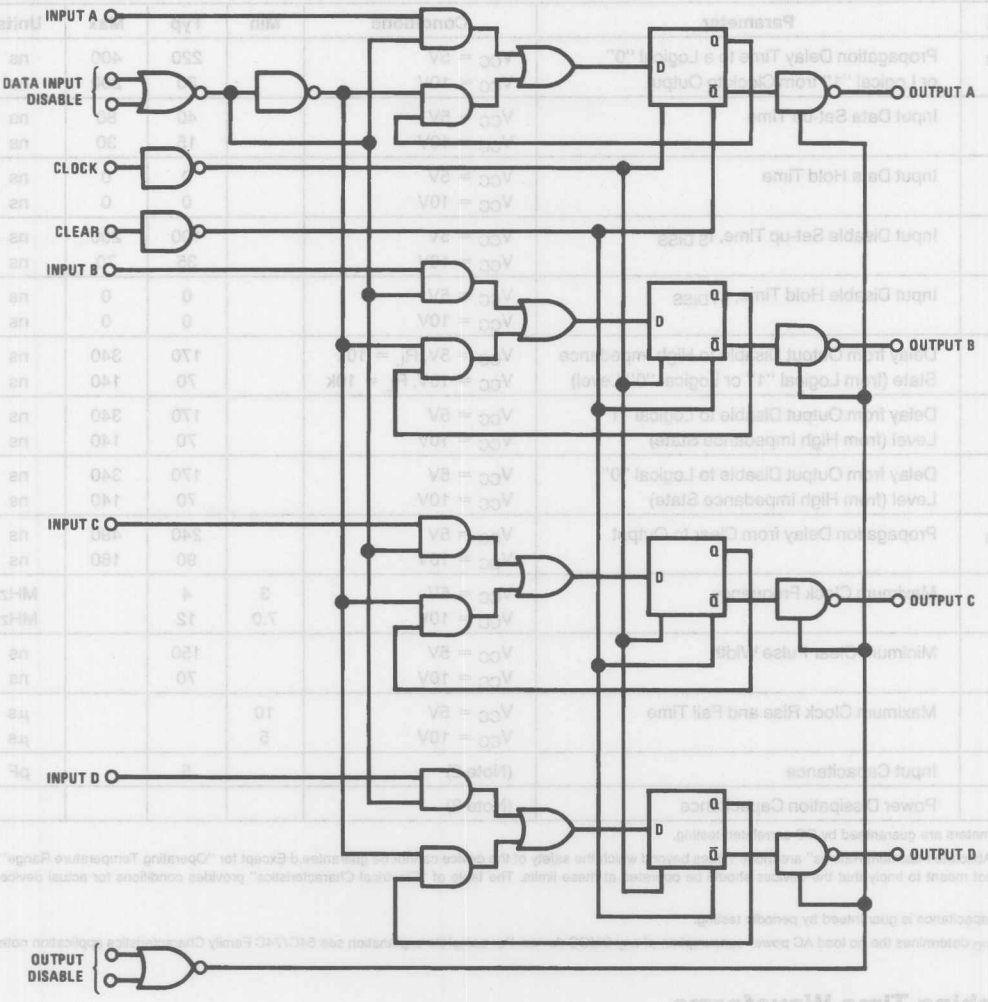
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



TL/F/5898–3

Logic Diagram



TL/F/5898–1

National Semiconductor

MM54C174/MM74C174 Hex D Flip-Flop

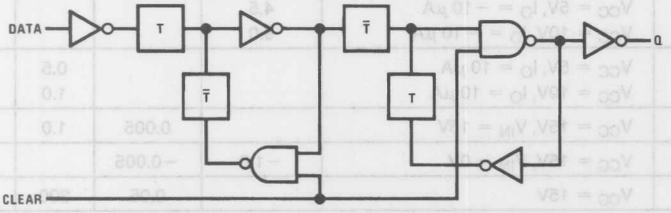
General Description

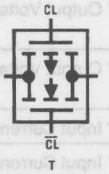
The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to V_{CC} and GND.

Features

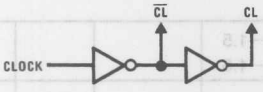
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L

Logic and Connection Diagrams

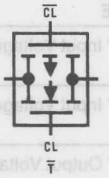




TL/F/5899–2

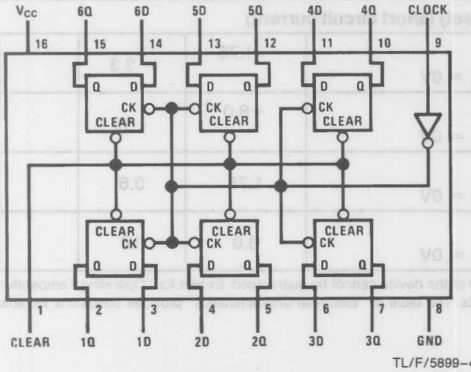


TL/F/5899–1



TL/F/5899–3

Dual-In-Line Package



TL/F/5899–4

Top View

Order Number MM54C174* or MM74C174*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

Voltage at Any Pin	−0.3V to V_{CC} +0.3V	Dual-In-Line	700 mW
		Small Outline	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C174	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C174	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA V_{CC} = 10V, I_O = 10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5 V_{CC}−1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360 μA 74C, V_{CC} = 4.75V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 360 μA 74C, V_{CC} = 4.75V, I_O = 360 μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V T_A = 25°C, V_{OUT} = 0V	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = 0V	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V T_A = 25°C, V_{OUT} = 0V	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V T_A = 25°C, V_{OUT} = 0V	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q	$V_{CC} = 5V$ $V_{CC} = 10V$		150 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Clear	$V_{CC} = 5V$ $V_{CC} = 10V$		110 50	300 110	ns ns
t_{S1}, t_{S0}	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$	75 25			ns ns
t_{H1}, t_{H0}	Time after Clock Pulse that Data Must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$	0 0	−10 −5.0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		50 35	250 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		65 35	140 70	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	15 5.0	>1200 >1200		μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.0 5.0	6.5 12		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		11 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		95		pF

*AC Parameters are guaranteed by DC correlated testing.

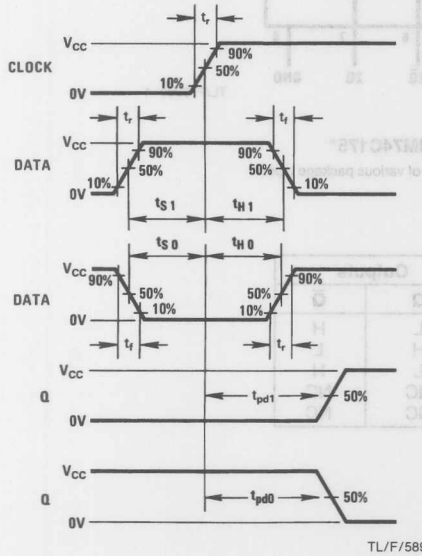
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

Switching Time Waveforms

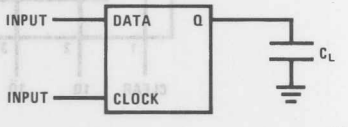
CMOS to CMOS



TL/F/5899–5

$t_r = t_f = 20$ ns

AC Test Circuit



TL/F/5899–6

National Semiconductor

MM54C175/MM74C175 Quad D Flip-Flop

General Description

The MM54C175/MM74C175 consists of four positive-edge triggered D type flip-flops implemented with monolithic CMOS technology. Both are true and complemented outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and Q's to logical "1".

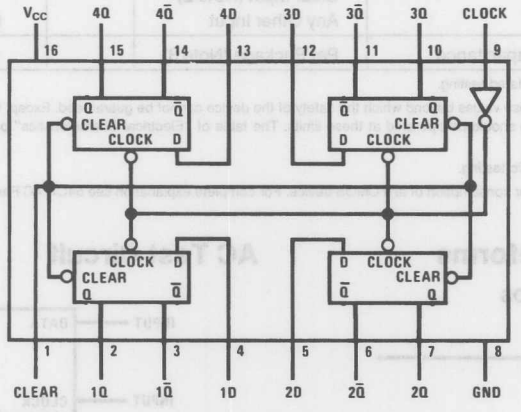
All inputs are protected from static discharge by diode clamps to V_{CC} and GND.

Features

- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — Fan out of 2 driving 74L

Connection Diagram & Truth Table

Dual-In-Line Package



TL/F/5900–1

Top View

Order Number MM54C175* or MM74C175*

*Please look into Section 8, Appendix D for availability of various package types.

Each Flip-Flop

Inputs			Outputs	
Clear	Clock	D	Q	$\bar{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C175	$-55°C$ to $+125°C$
MM74C175	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V, I_O = -10\ \mu A$ $V_{CC} = 10V, I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V, I_O = 10\ \mu A$ $V_{CC} = 10V, I_O = 10\ \mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V, V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$ 74C, $V_{CC} = 4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V, I_O = -360\ \mu A$ 74C, $V_{CC} = 4.75V, I_O = -360\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V, I_O = 360\ \mu A$ 74C, $V_{CC} = 4.75V, I_O = 360\ \mu A$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V, T_A = 25°C$, $V_{OUT} = 0V$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V, T_A = 25°C$, $V_{OUT} = 0V$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V, T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V, T_A = 25°C$, $V_{OUT} = V_{CC}$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

		Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	V_{CC} = 5V V_{CC} = 10V		190 75	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Clear to Q	V_{CC} = 5V V_{CC} = 10V		180 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "1" from Clear to Q	V_{CC} = 5V V_{CC} = 10V		230 90	400 150	ns ns
t_S	Time Prior to Clock Pulse that Data Must be Present	V_{CC} = 5V V_{CC} = 10V	100 40	45 16		ns ns
t_H	Time After Clock Pulse that Data Must be Held	V_{CC} = 5V V_{CC} = 10V	0 0	−11 −4		ns ns
t_W	Minimum Clock Pulse Width	V_{CC} = 5.0V V_{CC} = 10V		130 45	250 100	ns ns
t_W	Minimum Clear Pulse Width	V_{CC} = 5.0V V_{CC} = 10V		120 45	250 100	ns ns
t_r	Maximum Clock Rise Time	V_{CC} = 5V V_{CC} = 10V	15 5.0	450 125		μs μs
t_f	Maximum Clock Fall Time	V_{CC} = 5V V_{CC} = 10V	15 5.0	50 50		μs μs
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5V V_{CC} = 10V	2.0 5.0	3.5 10		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		10 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		130		pF

*AC Parameters are guaranteed by DC correlated testing.

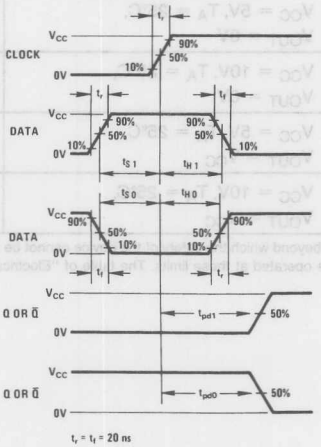
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

Switching Time Waveforms

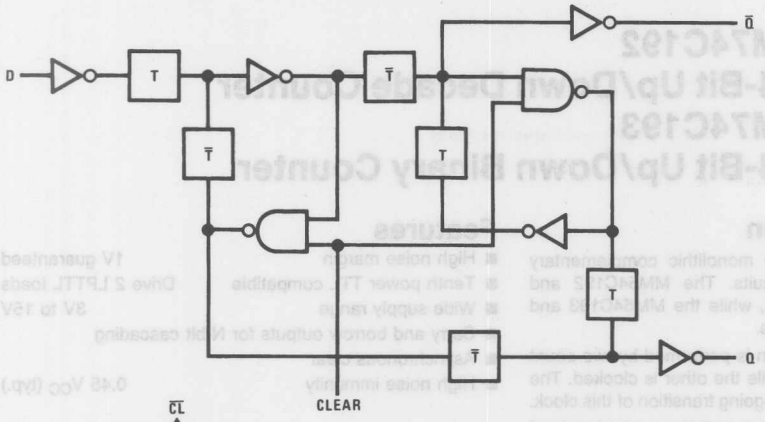
CMOS to CMOS



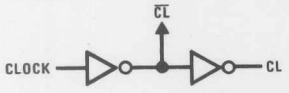
TL/F/5900–6

Logic Diagram

Typical One of Four



TL/F/5900–2



TL/F/5900–3



TL/F/5900–4



TL/F/5900–5

6

National Semiconductor

MM54C192/MM74C192
Synchronous 4-Bit Up/Down Decade Counter
MM54C193/MM74C193
Synchronous 4-Bit Up/Down Binary Counter

General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters, while the MM54C193 and MM74C193 are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

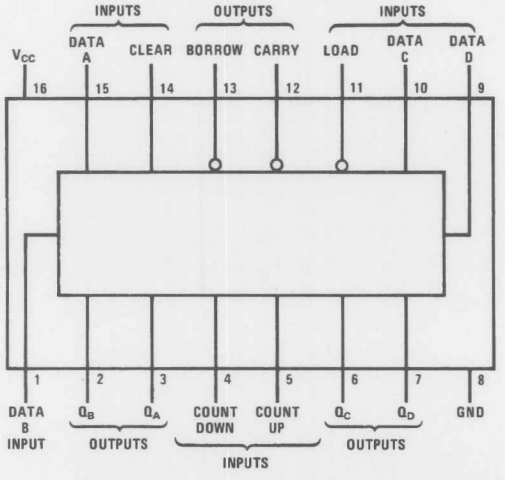
These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at a logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

Features

- High noise margin — 1V guaranteed
- Tenth power TTL compatible — Drive 2 LPTTL loads
- Wide supply range — 3V to 15V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 V_{CC} (typ.)

Connection Diagram

Dual-In-Line Package



TL/F/5901–1

Top View

Order Number MM54C192*, MM74C192*, MM54C193* or MM74C193*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	
MM54C154	$-55°C$ to $+125°C$
MM74C154	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Maximum V_{CC} Voltage	18V
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature (T_A) (Soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$			0.8	V
		74C $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -100\ \mu A$	2.4			V
		74C $V_{CC} = 4.75V$, $I_O = -100\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = 360\ \mu A$			0.4	V
		74C $V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{IN(0)} = 0V$ $T_A = 25°C$, $V_{OUT} = 0V$	-8			mA
I_{SINK}	Output Sink Current	$V_{CC} = 5V$, $V_{IN(1)} = 5V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC} = 10V$, $V_{IN(1)} = 10V$ $T_A = 25°C$, $V_{OUT} = V_{CC}$	8			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

	from Count Up or Down	V_{CC} = 10V		100	160	ns
t_{pd}	Propagation Delay Time to Q Borrow from Count Down	V_{CC} = 5V V_{CC} = 10V		120 50	200 80	ns ns
t_{pd}	Propagation Delay Time to Carry from Count Up	V_{CC} = 5V V_{CC} = 10V		120 50	200 80	ns ns
t_S	Time Prior to Load that Data Must be Present	V_{CC} = 5V V_{CC} = 10V		100 30	160 50	ns ns
t_W	Minimum Clear Pulse Width	V_{CC} = 5V V_{CC} = 10V		300 120	480 190	ns ns
t_W	Minimum Load Pulse Width	V_{CC} = 5V V_{CC} = 10V		100 40	160 65	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to Q from Load	V_{CC} = 5V V_{CC} = 10V		300 120	480 190	ns ns
t_W	Minimum Count Pulse Width	V_{CC} = 5V V_{CC} = 10V		120 35	200 80	ns ns
f_{MAX}	Maximum Count Frequency	V_{CC} = 5V V_{CC} = 10V	2.5 6	4 10		MHz MHz
t_r, t_f	Count Rise and Fall Time	V_{CC} = 5V V_{CC} = 10V			15 5	μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

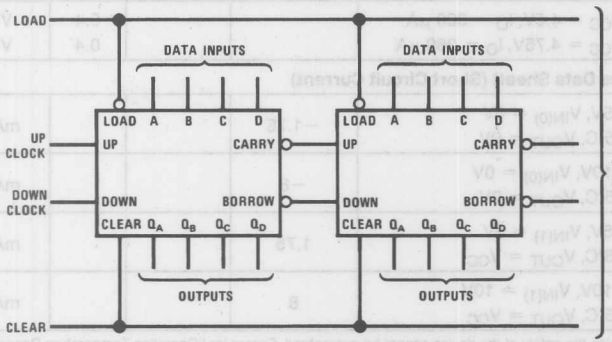
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

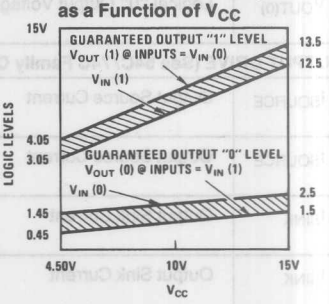
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics, Application Note AN-90.

Cascading Packages



TL/F/5901–2

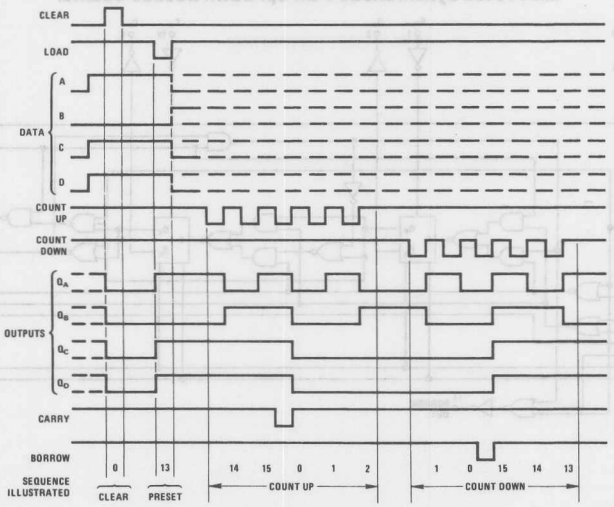
Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5901–3

Timing Diagrams

MM54C192/MM74C192



TL/F/5901–4

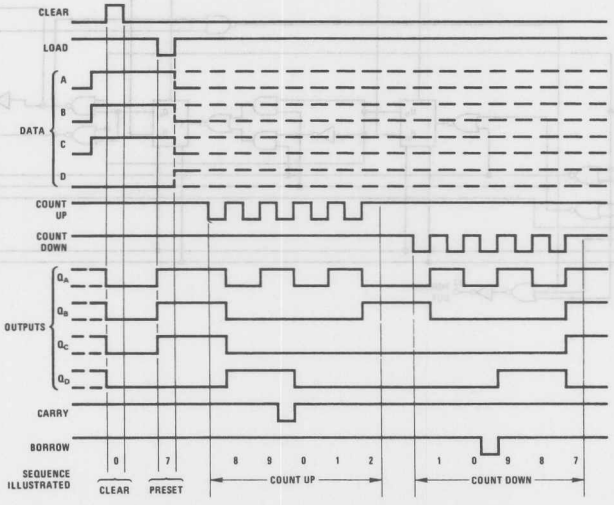
Note 1: Clear ouptuts to zero.

Note 2: Load (preset) to binary thirteen.

Note 3: Count up to fourteen, fifteen, carry, zero, one and two.

Note 4: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

MM54C193/MM74C193



TL/F/5901–5

Note 1: Clear ouptuts to zero.

Note 2: Load (preset) to BCD seven.

Note 3: Count up to eight, nine, carry, zero, one, and two.

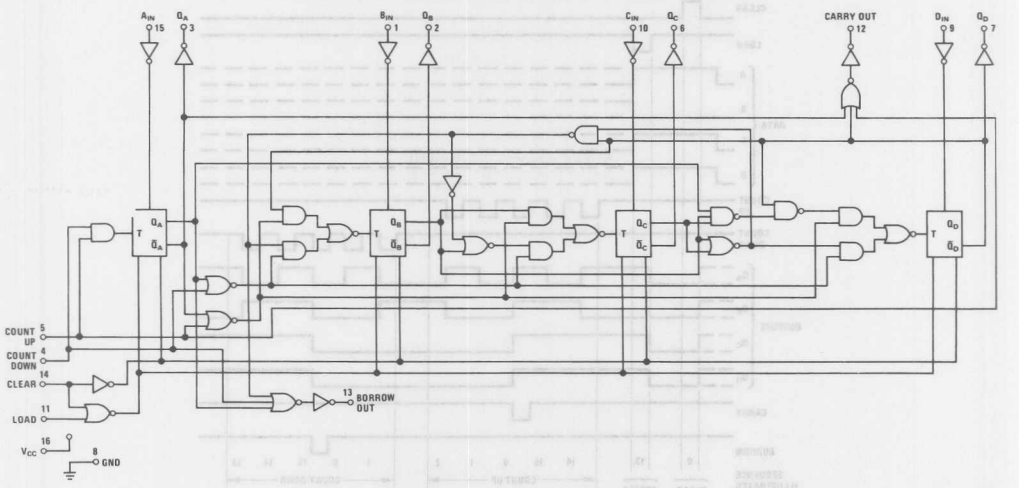
Note 4: Count down to one, zero, borrow, nine, eight, and seven.

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count down input must be high; when counting down, count-up input must be high.

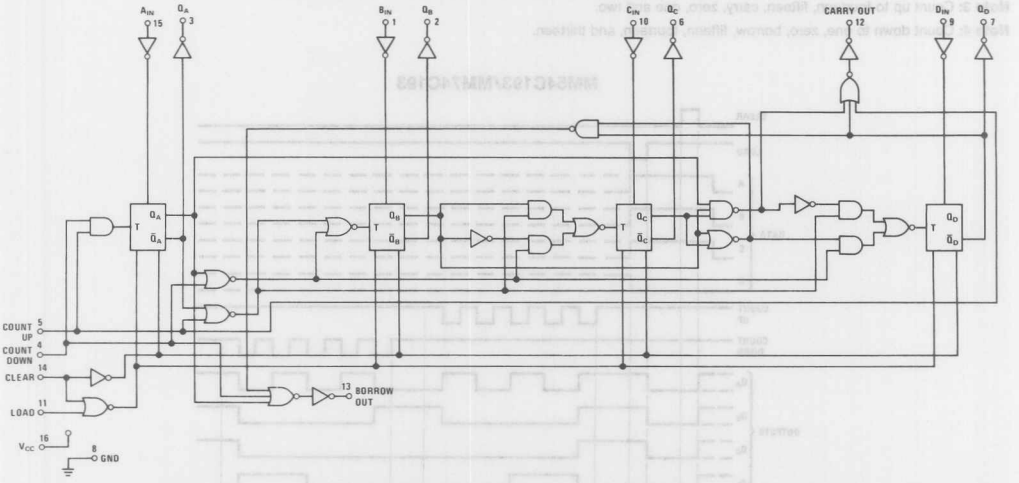
Schematic Diagrams

MM54C192 Synchronous 4-Bit Up/Down Decade Counter



TL/F/5901–6

MM54C193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5901–7

National Semiconductor

MM54C195/MM74C195 4-Bit Registers

General Description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible:

Parallel Load

Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control of input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K, D, or T-type flip flop as shown in the truth table.

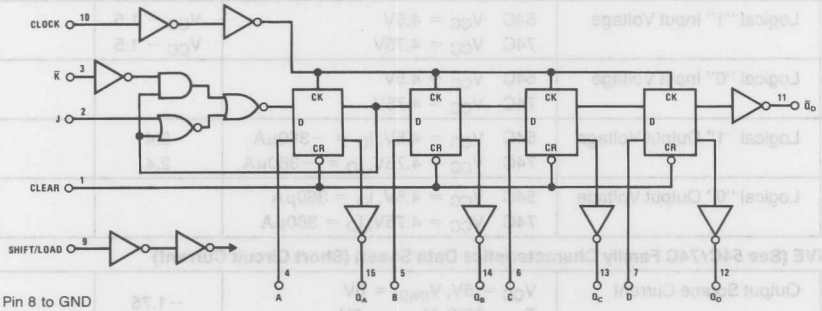
Features

- Medium speed operation — 8.5 MHz (typ.) with 10V supply and 50 pF load
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 100 nW (typ.)
- Tenth power TTL compatible — Drive 2 LPTTL loads
- Supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and K inputs to first stage
- Complementary outputs from last stage
- Positive-edge triggered clocking
- Diode clamped inputs to protect against static charge

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

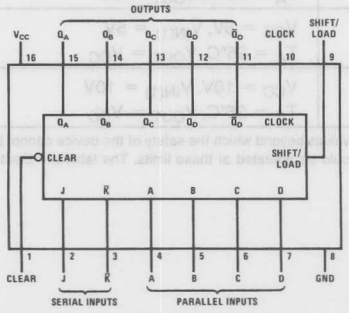
Schematic and Connection Diagrams



Pin 8 to GND
Pin 16 to V_{CC}

TL/F/5902–1

Dual-In-Line Package



TL/F/5902–2

Top View

Order Number MM54C195* or MM74C195*

*Please look into Section 8, Appendix D for availability of various package types.

Voltage at any Pin	−0.3V to V_{CC} +0.3V	Small Outline	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C195	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C195	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V V_{CC} = 10V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V V_{CC} = 10V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360μA 74C V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360μA 74C V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		150 75	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clear to Q or $\overline{Q}$	$V_{CC} = 5V$ $V_{CC} = 10V$		150 50	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$		80 35	200 70	ns ns
t_S	Time Prior to Clock Pulse that Shift/Load must be Present	$V_{CC} = 5V$ $V_{CC} = 10V$		110 60	150 90	ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5V$ $V_{CC} = 10V$		−10 −5.0	0 0	ns ns
t_W	Minimum Clear Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5V$ $V_{CC} = 10V$		100 50	200 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5V$ $V_{CC} = 10V$		90 40	130 60	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$ $V_{CC} = 10V$	5.0 2.0			μs μs
f_{MAX}	Maximum Input Clock Frequency	$V_{CC} = 5V$ $V_{CC} = 10V$	2.0 5.5	3.0 8.5		MHz MHz
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

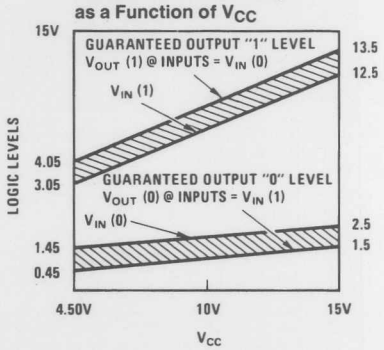
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Truth Table

Inputs AT t_n		Outputs AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

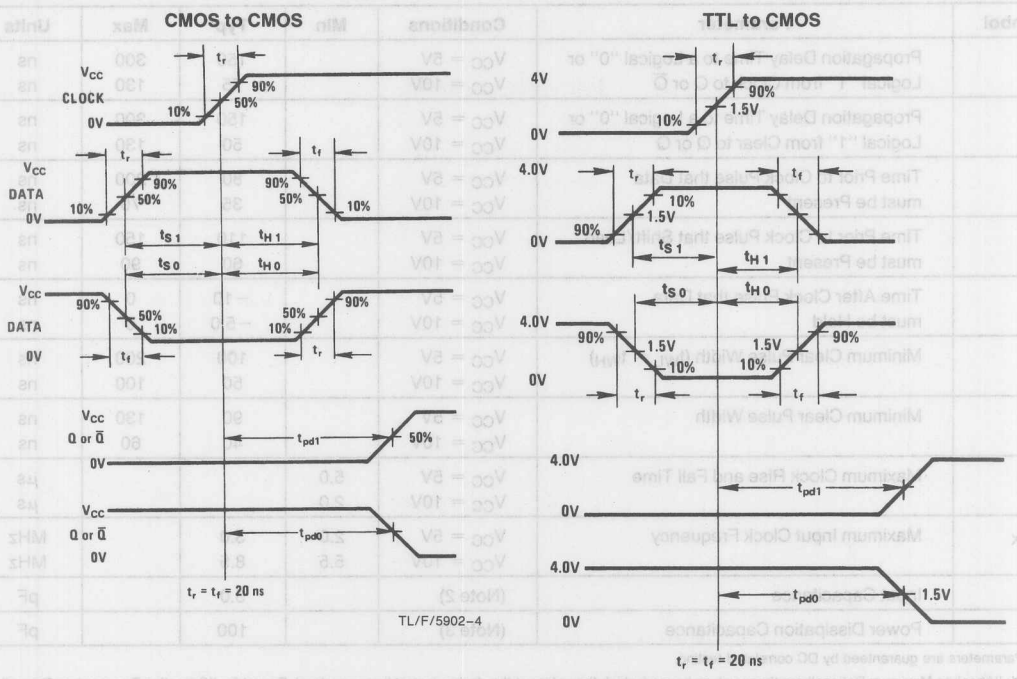
Note: H = High Level, L = Low Level
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n

Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5902–3

Switching Time Waveforms



National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line, working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the $\overline{CE}_3$ must occur for the memory to be selected.

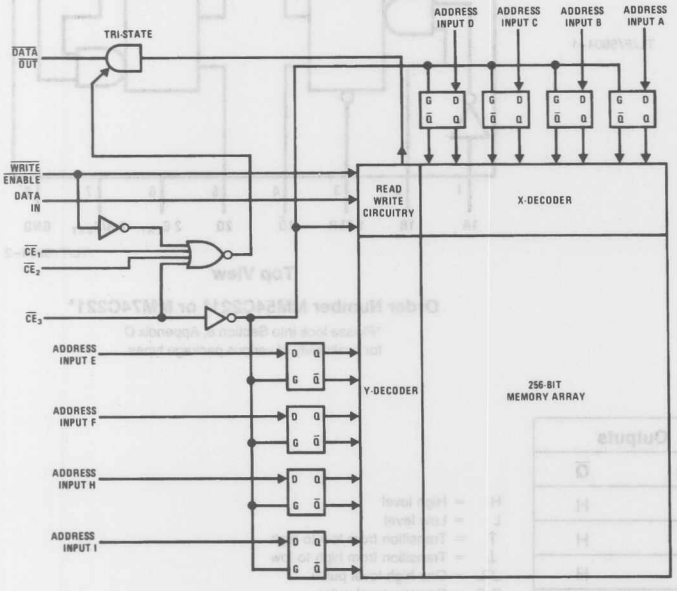
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{WE}$ high. Holding either $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus-organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control provides for fast access times by not totally disabling the chip.

Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{WE}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{WE}$ low.

Features

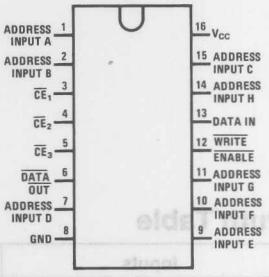
- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} (typ.)
- TTL compatibility — Fan out of 1 driving standard TTL
- Low power — 500 nW (typ.)
- Internal address register

Logic and Connection Diagrams



TL/F/5903–1

Dual-In-Line Package



TL/F/5903–2

Top View

Order Number MM54C200* or MM74C200*

*Please look into Section 8, Appendix D for availability of various package types.

National Semiconductor

MM54C221/MM74C221 Dual Monostable Multivibrator

General Description

The MM54C221/MM74C221 dual monostable multivibrator is a monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}.

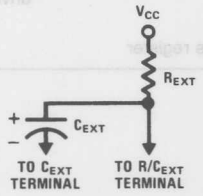
Pulse stability will be limited by the accuracy of external timing components. The pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT} R_{EXT}$. For further information and applications, see AN-138.

Features

- Wide supply voltage range — 4.5V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L

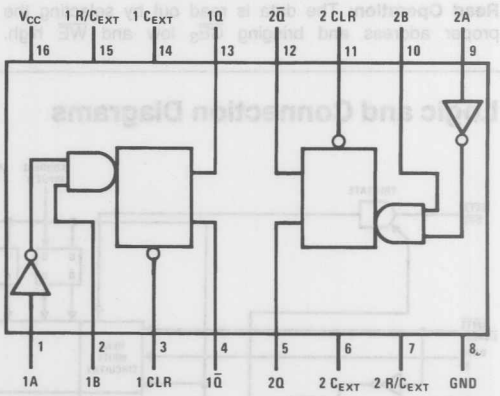
Connection Diagrams

Timing Component



TL/F/5904–1

Dual-In-Line Package



TL/F/5904–2

Top View

Order Number MM54C221* or MM74C221*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⎎ = One low level pulse
X = Irrelevant

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C221	−55°C to +125°C
MM74C221	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	4.5V to 15V
Absolute Maximum V_{CC}	18V
$R_{EXT} \geq 80\ V_{CC}$ (Ω)	
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Max/min limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA V_{CC} = 10V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = +10 μA V_{CC} = 10V, I_O = +10 μA			0.5 1	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current (Standby)	V_{CC} = 15V, R_{EXT} = ∞, Q1, Q2 = Logic "0" (Note 3)		0.05	300	μA
I_{CC}	Supply Current (During Output Pulse)	V_{CC} = 15V, Q1 = Logic "1", Q2 = Logic "0" *(Figure 4)*		15		mA
		V_{CC} = 5V, Q1 = Logic "1", Q2 = Logic "0" *(Figure 4)*		2		mA
	Leakage Current at R/C_{EXT} Pin	V_{CC} = 15V, V_{CEXT} = 5V		0.01	3.0	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5V, I_O = −360 μA 74C V_{CC} = 4.75V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5V, I_O = 360 μA 74C V_{CC} = 4.75V, I_O = 360 μA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = 0V	−8			mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V T_A = 25°C, V_{OUT} = V_{CC}	8			mA

$t_{pd\ A,\ B}$	Propagation Delay from Trigger Input (A, B) to Output Q, $\overline{Q}$	V_{CC} = 5V V_{CC} = 10V		250 120	500 250	ns ns
$t_{pd\ CL}$	Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$	V_{CC} = 5V V_{CC} = 10V		250 120	500 250	ns ns
t_S	Time Prior to Trigger Input (A, B) that Clear must be Set	V_{CC} = 5V V_{CC} = 10V	150 60	50 20		ns ns
$t_{W(A,\ B)}$	Trigger Input (A, B) Pulse Width	V_{CC} = 5V V_{CC} = 10V	150 70	50 30		ns ns
$t_{W(CL)}$	Clear Input (CL) Pulse Width	V_{CC} = 5V V_{CC} = 10V	150 70	50 30		ns ns
$t_{W(OUT)}$	Q or $\overline{Q}$ Output Pulse Width	V_{CC} = 5V, R_{EXT} = 10k, C_{EXT} = 0 pF		900		ns
		V_{CC} = 10V, R_{EXT} = 10k, C_{EXT} = 0 pF		350		ns
		V_{CC} = 15V, R_{EXT} = 10k, C_{EXT} = 0 pF		320		ns
		V_{CC} = 5V, R_{EXT} = 10k, C_{EXT} = 1000 pF *(Figure 1)*	9.0	10.6	12.2	μs
		V_{CC} = 10V, R_{EXT} = 10k, C_{EXT} = 1000 pF *(Figure 1)*	9.0	10	11	μs
		V_{CC} = 15V, R_{EXT} = 10k, C_{EXT} = 1000 pF *(Figure 1)*	8.9	9.8	10.8	μs
		V_{CC} = 5V, R_{EXT} = 10k, C_{EXT} = 0.1 μF *(Figure 2)*	900	1020	1200	μs
		V_{CC} = 10V, R_{EXT} = 10k, C_{EXT} = 0.1 μF *(Figure 2)*	900	1000	1100	μs
		V_{CC} = 15V, R_{EXT} = 10k, C_{EXT} = 0.1 μF *(Figure 2)*	900	990	1100	μs
R_{ON}	ON Resistance of Transistor between R/C_{EXT} to C_{EXT}	V_{CC} = 5V (Note 4) V_{CC} = 10V (Note 4) V_{CC} = 15V (Note 4)		50 25 16.7	150 65 45	Ω Ω Ω
	Output Duty Cycle	R = 10k, C = 1000 pF R = 10k, C = 0.1 μF (Note 5)			90 90	% %
C_{IN}	Input Capacitance	R/C_{EXT} Input (Note 2) Any Other Input (Note 2)		15 5	25	pF pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

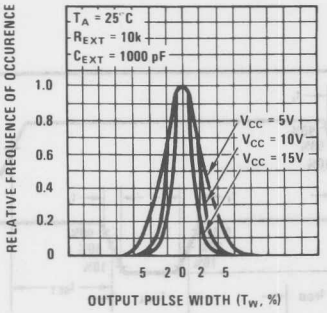
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: In Standby (Q = Logic "0") the power dissipated equals the leakage current plus V_{CC}/R_{EXT}.

Note 4: See AN-138 for detailed explanation R_{ON}.

Note 5: Maximum output duty cycle = R_{EXT}/R_{EXT} + 1000.

Typical Performance Characteristics



0% Point pulse width:

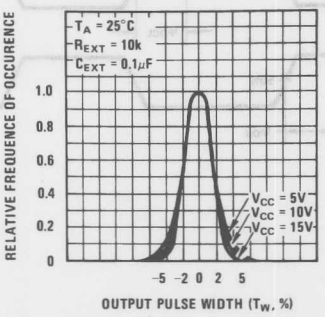
At V_{CC} = 5V, T_W = 10.6 μs
At V_{CC} = 10V, T_W = 10 μs
At V_{CC} = 15V, T_W = 9.8 μs

Percentage of units within ±4%:

At V_{CC} = 5V, 90% of units
At V_{CC} = 10V, 95% of units
At V_{CC} = 15V, 98% of units

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FIGURE 1. Typical Distribution of Units for Output Pulse Width



0% Point pulse width:

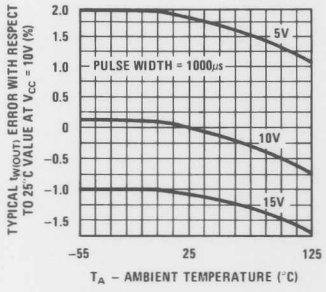
At V_{CC} = 5V, T_W = 1020 μs
At V_{CC} = 10V, T_W = 1000 μs
At V_{CC} = 15V, T_W = 982 μs

Percentage of units within ±4%:

At V_{CC} = 5V, 95% of units
At V_{CC} = 10V, 97% of units
At V_{CC} = 15V, 98% of units

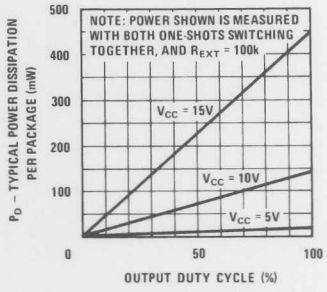
TL/F/5904–4

FIGURE 2. Typical Distribution of Units for Output Pulse Width



TL/F/5904–5

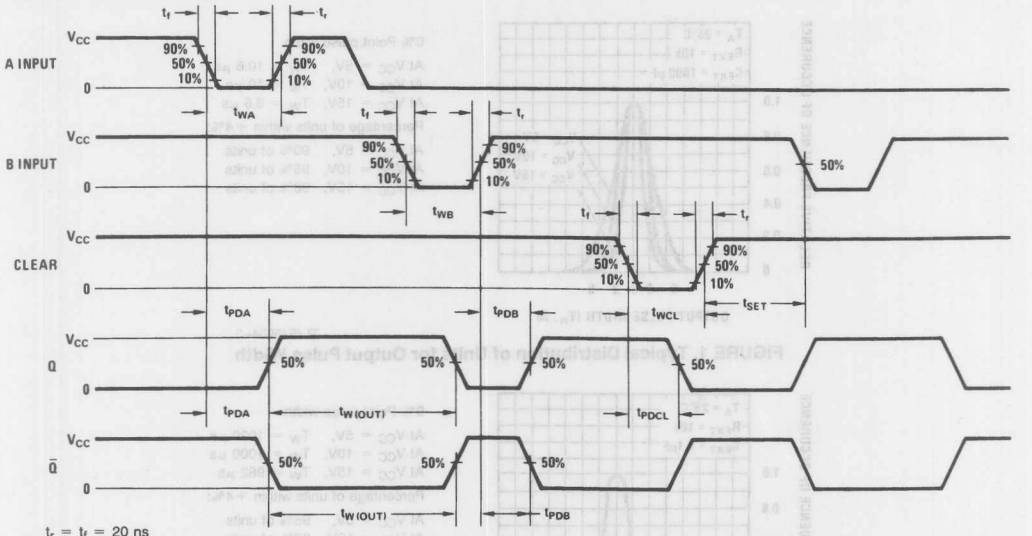
FIGURE 3. Typical Variation in Output Pulse Width vs Temperature



TL/F/5904–6

FIGURE 4. Typical Power Dissipation per Package

Switching Time Waveforms



TL/F/5904–7

National Semiconductor

MM54C240/MM74C240 Inverting MM54C244/MM74C244 Non-Inverting Octal Buffers and Line Drivers with TRI-STATE® Outputs

General Description

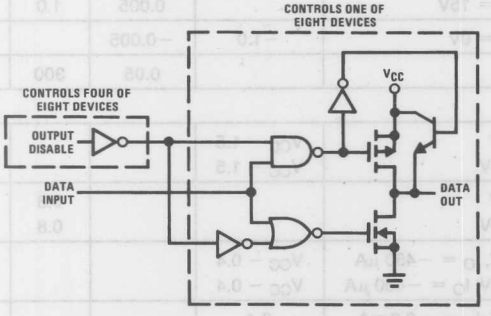
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state. For improved TTL input compatibility see MM74C941.

Features

- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45 V_{CC} typ)
- Low power consumption
- High capacitive load drive capability
- TRI-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns (typ.) @ 10V, 50 pF (MM74C244)

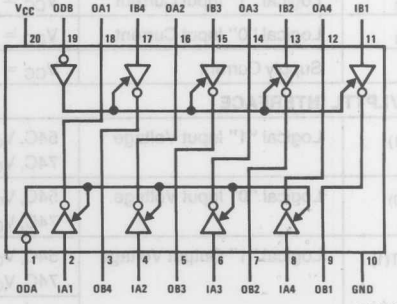
Logic and Connection Diagrams

MM54C240/MM74C240



TL/F/5905–1

MM54C240/MM74C240 Dual-In-Line Package

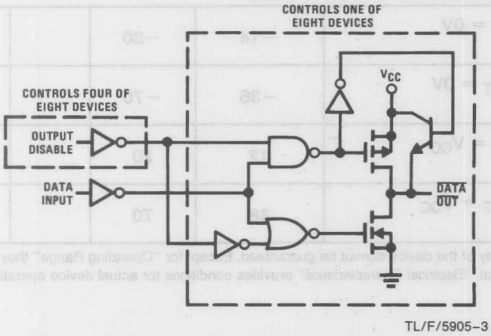


TL/F/5905–2

Top View

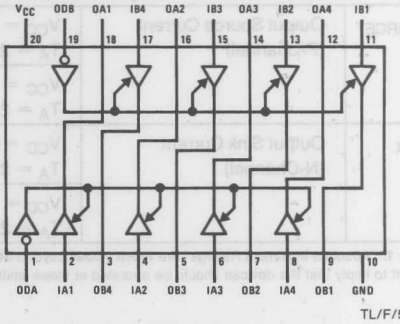
Order Number MM54C240* or MM74C240*

MM54C244/MM74C244



TL/F/5905–3

MM54C244/MM74C244 Dual-In-Line Package



TL/F/5905–4

Top View

Order Number MM54C244* or MM74C244*,

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C240, MM54C244	$-55°C$ to $+125°C$
MM74C240, MM74C244	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
I_{OZ}	TRI-STATE Output Current	$V_{CC} = 10V$, OD = V_{IH}			±10	μA
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -450\ \mu A$	$V_{CC} - 0.4$			V
		74C, $V_{CC} = 4.75V$, $I_O = -450\ \mu A$	$V_{CC} - 0.4$			V
		54C, $V_{CC} = 4.5V$, $I_O = -2.2$ mA	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -2.2$ mA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = 2.2$ mA			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = 2.2$ mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$, $T_A = 25°C$	−14	−30		mA
		$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	−36	−70		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	12	20		mA
		$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	48	70		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PD(1)}$, $t_{PD(0)}$	Propagation Delay (Data In to Out)					
	MM54C240/MM74C240	$V_{CC} = 5V$, $C_L = 50$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		40	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		80	110	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		60	90	ns
	MM54C244/MM74C244	$V_{CC} = 5V$, $C_L = 50$ pF		45	70	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		25	50	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	70	ns
t_{1H}, t_{0H}	Propagation Delay Output Disable to High Impedance State (from a Logic Level)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		45	80	ns
		$V_{CC} = 10V$		35	60	ns
t_{H1}, t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
$t_{T(HL)}$, $t_{T(LH)}$	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		45	80	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		30	60	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		75	140	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		50	100	ns
C_{PD}	Power Dissipation Capacitance (Output Enabled per Buffer)	(Note 3)				
	MM54C240/MM74C240			100		pF
	MM54C244/MM74C244			100		pF
	(Output Disabled per Buffer)					
	MM54C240/MM74C240			10		pF
	MM54C244/MM74C244			0		pF
C_{IN}	Input Capacitance (Any Input)	$V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$		10		pF
C_O	Output Capacitance (Output Disabled)	$V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$		10		pF

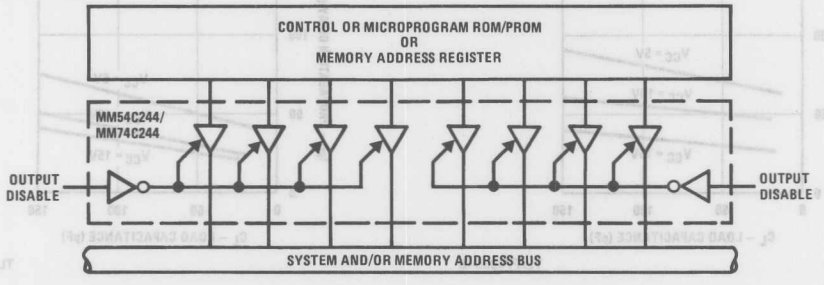
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

Typical Application



TL/F/5905–5

1	X	Z
1	X	Z
0	0	1
0	1	0

1	X	Z
1	X	Z
0	0	1
0	1	0

MM54C244/MM74C244

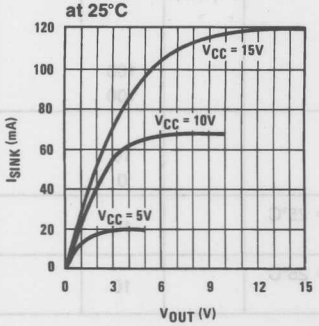
ODA	IA	OA
1	X	Z
1	X	Z
0	0	0
0	1	1

ODB	IB	OB
1	X	Z
1	X	Z
0	0	0
0	1	1

1 = High
0 = Low
X = Don't Care
Z = TRI-STATE

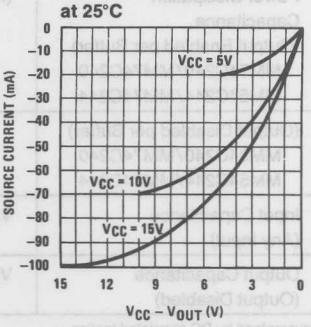
Typical Performance Characteristics

N-Channel Output Drive at 25°C



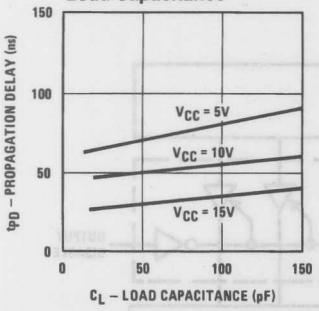
TL/F/5905–6

P-Channel Output Drive at 25°C



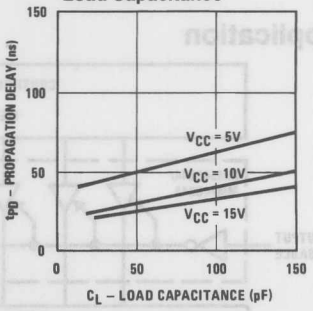
TL/F/5905–7

MM54C240/MM74C240 Propagation Delay vs. Load Capacitance



TL/F/5905–8

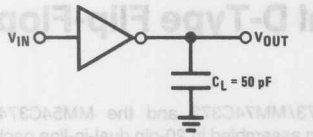
MM54C244/MM74C244 Propagation Delay vs. Load Capacitance



TL/F/5905–9

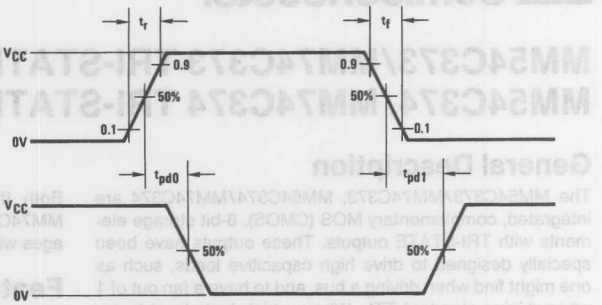
AC Test Circuits and Switching Time Waveforms

t_{pd0}, t_{pd1}



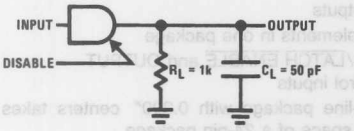
TL/F/5905–10

CMOS to CMOS



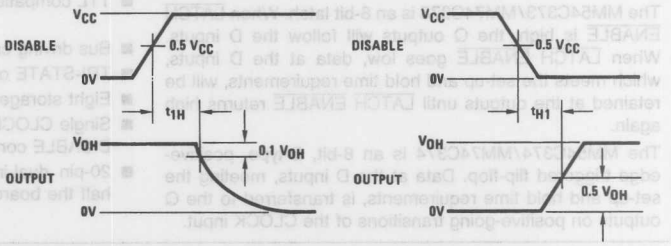
TL/F/5905–11

t_{1H} and t_{H1}



TL/F/5905–12

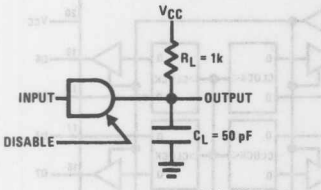
t_{1H} t_{H1}



TL/F/5905–13

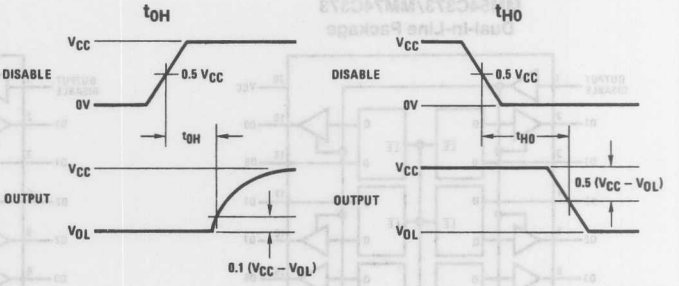
Note: V_{OH} is defined as the DC output high voltage when the device is loaded with a 1 kΩ resistor to ground.

t_{0H} and t_{H0}



TL/F/5905–14

t_{0H} t_{H0}



TL/F/5905–15

Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a 1 kΩ resistor to V_{CC}.

Note: Delays measured with input t_r, $t_f \leq 20$ ns.

National Semiconductor

MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch
MM54C374/MM74C374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE outputs. These outputs have been specially designed to drive high capacitive loads, such as one might find when driving a bus, and to have a fan out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high, the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

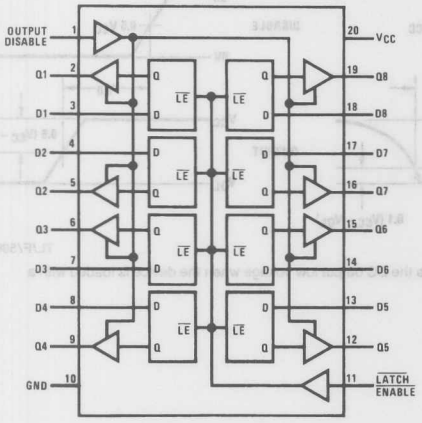
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300″ pin centers.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power consumption
- TTL compatibility — Fan out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single CLOCK/$\overline{\text{LATCH ENABLE}}$ and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300″ centers takes half the board space of a 24-pin package

Connection Diagrams

MM54C373/MM74C373
Dual-In-Line Package

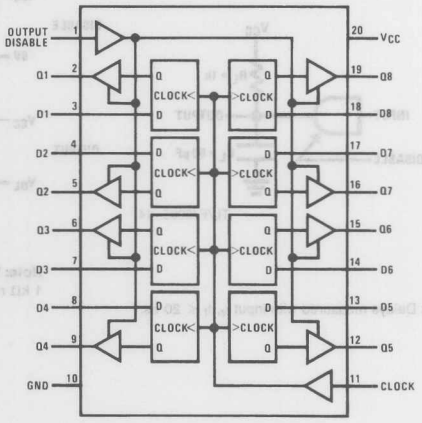


TL/F/5906–1

Top View

Order Number MM54C373* or MM74C373*

MM54C374/MM74C374
Dual-In-Line Package



TL/F/5906–2

Top View

Order Number MM54C374* or MM74C374*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	
MM54C373	$-55°C$ to $+125°C$
MM74C373	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{OZ}	TRI-STATE Leakage Current	$V_{CC} = 15V$, $V_O = 15V$		0.005	1.0	μA
		$V_{CC} = 15V$, $V_O = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$			0.8	V
		54C $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	$V_{CC} - 0.4$			V
		74C $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	$V_{CC} - 0.4$			V
		54C $V_{CC} = 4.5V$, $I_O = -1.6$ mA	2.4			V
		74C $V_{CC} = 4.75V$, $I_O = -1.6$ mA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = 1.6$ mA			0.4	V
		74C $V_{CC} = 4.75V$, $I_O = 1.6$ mA			0.4	V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$ (Note 4)	-12	-24		mA
I_{SOURCE}	Output Source Current	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$ (Note 4)	-24	-48		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$ (Note 4)	6	12		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$ (Note 4)	24	48		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

t_{pd0}, t_{pd1}	Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output	V_{CC} = 5V, C_L = 50 pF		165	330	ns
		V_{CC} = 10V, C_L = 50 pF		70	140	ns
		V_{CC} = 5V, C_L = 150 pF		195	390	ns
		V_{CC} = 10V, C_L = 150 pF		85	170	ns
t_{pd0}, t_{pd1}	Propagation Delay Data In to Output	$\overline{\text{LATCH ENABLE}}$ = V_{CC}				
		V_{CC} = 5V, C_L = 50 pF		155	310	ns
		V_{CC} = 10V, C_L = 50 pF		70	140	ns
		V_{CC} = 5V, C_L = 150 pF		185	370	ns
		V_{CC} = 10V, C_L = 150 pF		85	170	ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	t_{HOLD} = 0 ns				
		V_{CC} = 5V		70	140	ns
		V_{CC} = 10V		35	70	ns
f_{MAX}	Maximum $\overline{\text{LATCH ENABLE}}$ Frequency					
		V_{CC} = 5V	3.5	6.7		MHz
		V_{CC} = 10V	4.5	9.0		MHz
t_{PWH}	Minimum $\overline{\text{LATCH ENABLE}}$ Pulse Width	V_{CC} 5V		75	150	ns
		V_{CC} = 10V		55	110	ns
t_r, t_f	Maximum $\overline{\text{LATCH ENABLE}}$ Rise and Fall Time	V_{CC} = 5V		NA		μs
		V_{CC} = 10V		NA		μs
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	R_L = 10k, C_L = 5 pF				
		V_{CC} = 5V		105	210	ns
		V_{CC} = 10V		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	R_L = 10k, C_L = 50 pF				
		V_{CC} = 5V		105	210	ns
		V_{CC} = 10V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{CC} = 5V, C_L = 50 pF		65	130	ns
		V_{CC} = 10V, C_L = 50 pF		35	70	ns
		V_{CC} = 5V, C_L = 150 pF		110	220	ns
		V_{CC} = 10V, C_L = 150 pF		70	140	ns
C_{LE}	Input Capacitance	$\overline{\text{LE}}$ Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		200		pF

*AC Parameters are guaranteed by DC correlated testing.

t_{pd0}, t_{pd1}	Propagation Delay, CLOCK to Output	V_{CC} = 5V, C_L = 50 pF		150	300	ns
		V_{CC} = 10V, C_L = 50 pF		65	130	ns
		V_{CC} = 5V, C_L = 150 pF		180	360	ns
		V_{CC} = 10V, C_L = 150 pF		80	160	ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/LATCH ENABLE	t_{HOLD} = 0 ns				
		V_{CC} = 5V		70	140	ns
		V_{CC} = 10V		35	70	ns
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width	V_{CC} = 5V		70	140	ns
		V_{CC} = 10V		50	100	ns
f_{MAX}	Maximum CLOCK Frequency	V_{CC} = 5V	3.5	7.0		MHz
		V_{CC} = 10V	5	10		MHz
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	R_L = 10k, C_L = 50 pF				
		V_{CC} = 5V		105	210	ns
		V_{CC} = 10V		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	R_L = 10k, C_L = 50 pF				
		V_{CC} = 5V		105	210	ns
		V_{CC} = 10V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{CC} = 5V, C_L = 50 pF		65	130	ns
		V_{CC} = 10V, C_L = 50 pF		35	70	ns
		V_{CC} = 5V, C_L = 150 pF		110	220	ns
		V_{CC} = 10V, C_L = 150 pF		70	140	ns
t_r, t_f	Maximum CLOCK Rise and Fall Time	V_{CC} = 5V	15	>2000		μs
		V_{CC} = 10V	5	>2000		μs
C_{CLK}	Input Capacitance	CLOCK Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		250		pF

*AC Parameters are guaranteed by DC correlated testing.

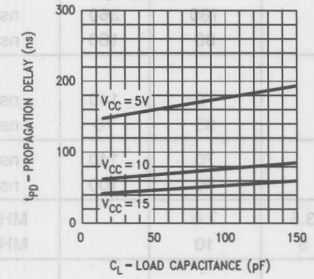
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note AN-90.

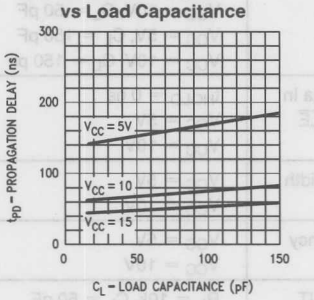
Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

Typical Performance Characteristics $T_A = 25°C$

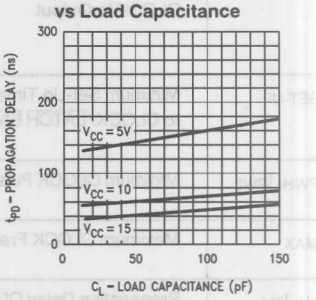
MM54C373/MM74C373 Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output vs Load Capacitance



MM54C373/MM74C373 Propagation Delay, Data In to Output vs Load Capacitance

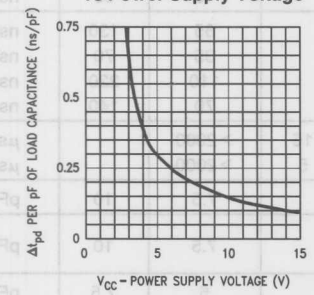


MM54C374/MM74C374 Propagation Delay, CLOCK to Output vs Load Capacitance

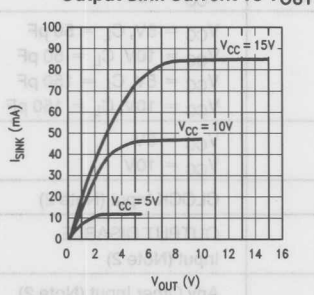


TL/F/5906–3

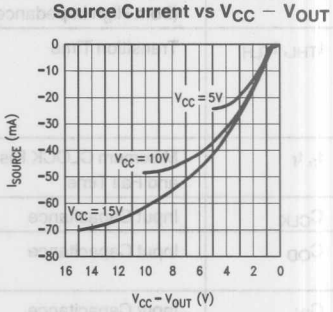
MM54C373/MM74C373, MM54C374/MM74C374 Change in Propagation Delay per pF of Load Capacitance (Δt_{PD}/pF) vs Power Supply Voltage



MM54C373/MM74C373, MM54C374/MM74C374 Output Sink Current vs V_{OUT}



MM54C373/MM74C373, MM54C374/MM74C374 Output Source Current vs $V_{CC} - V_{OUT}$



TL/F/5906–4

Truth Table

MM54C373/MM74C373

Output Disable	$\overline{\text{LATCH ENABLE}}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

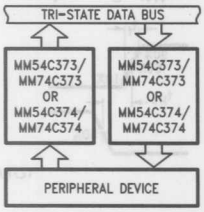
MM54C374/MM74C374

Output Disable	Clock	D	Q
L	⌐‾	H	H
L	⌐‾	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

L = Low logic level
H = High logic level
X = Irrelevant
⌐‾ = Low to high logic level transition
Q = Preexisting output level
Hi-Z = High impedance output state

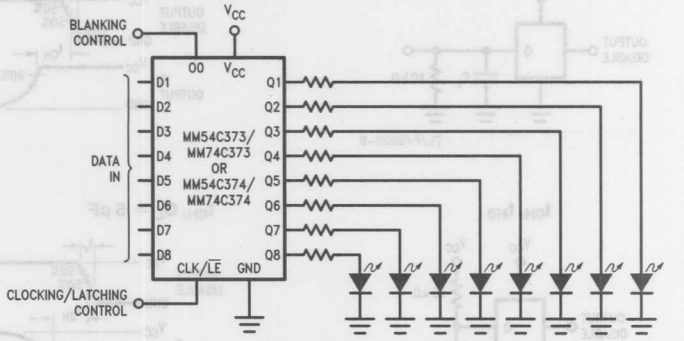
Typical Applications

Data Bus Interfacing Element



TL/F/5906–5

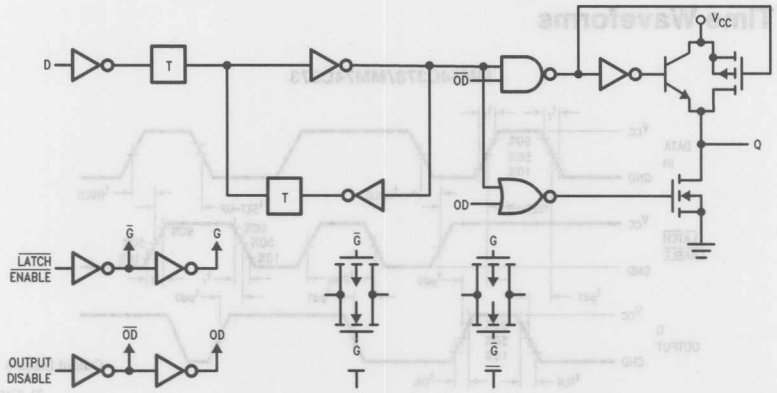
Simple, Latching, Octal, LED Indicator Driver with Blanking for Use as Data Display, Bus Monitor, μP Front Panel Display, Etc.



TL/F/5906–6

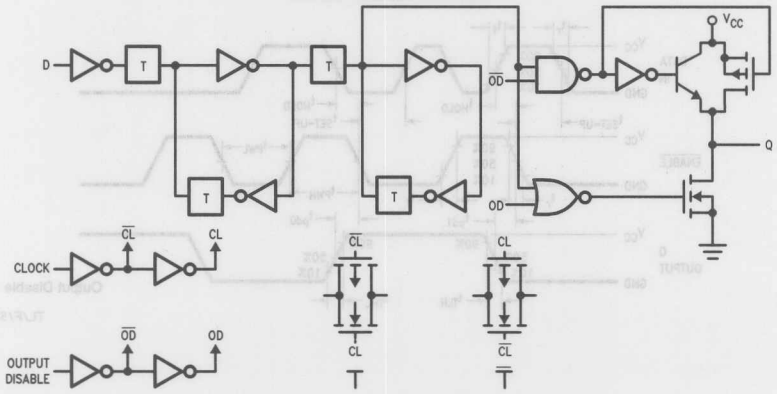
Logic Diagrams

MM54C373/MM74C373 (1 of 8 Latches)

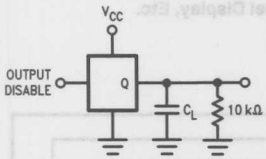


TL/F/5906–7

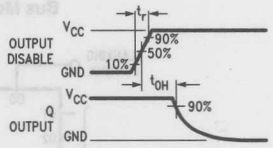
MM54C374/MM74C374 (1 of 8 Flip-Flops)

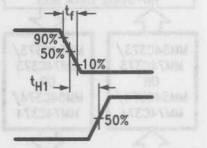


TL/F/5906–8



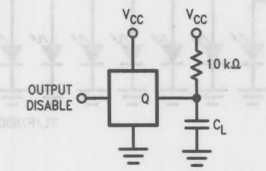
TL/F/5906–9





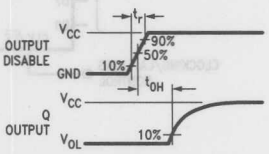
TL/F/5906–10

t_{0H}, t_{H0}

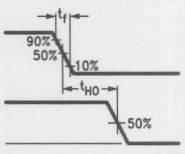


TL/F/5906–11

t_{0H}, C_L = 5 pF



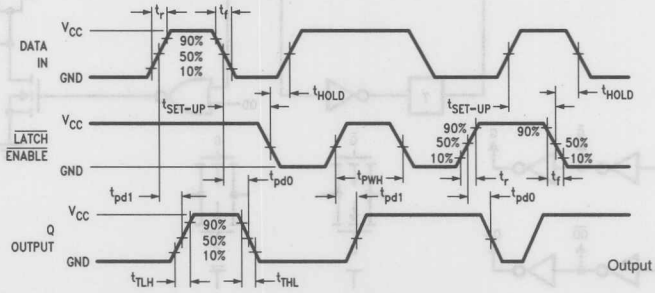
t_{H0}, C_L = 50 pF



TL/F/5906–12

Switching Time Waveforms

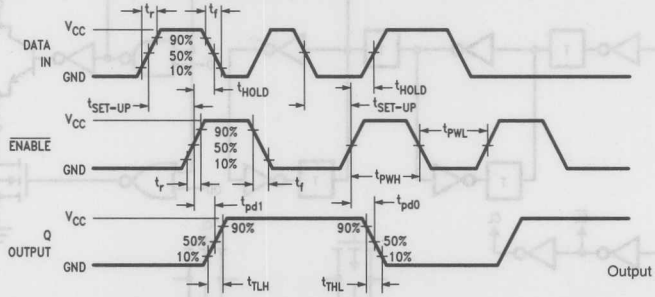
MM54C373/MM74C373



Output Disable = GND

TL/F/5906–13

MM54C374/MM74C374



Output Disable = GND

TL/F/5906–14

National Semiconductor

MM54C901/MM74C901 Hex Inverting TTL Buffer
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer
MM54C903/MM74C903 Hex Inverting CMOS Buffer
MM54C904/MM74C904 Hex Non-Inverting CMOS Buffer

General Description

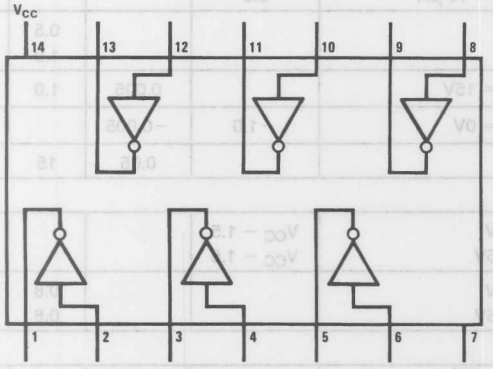
These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, and high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Fan out of 2 driving standard TTL

Connection Diagrams

Dual-In-Line Package
MM54C901/MM74C901
MM54C903/MM74C903

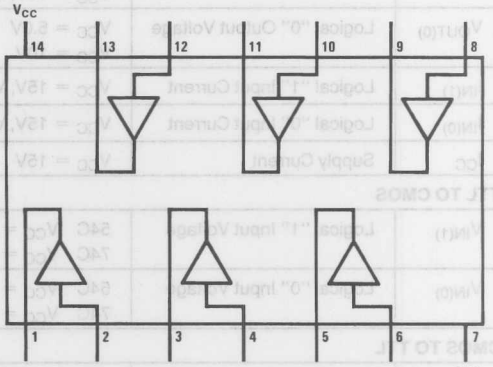


TL/F/5909–1

Top View

Order Number MM54C901*, MM74C901*, MM54C903* or MM74C903*

Dual-In-Line Package
MM54C902/MM74C902
MM54C904/MM74C904



TL/F/5909–2

Top View

Order Number MM54C902*, MM74C902*, MM54C904* or MM74C904*

*Please look into Section 8, Appendix D for availability of various package types.

6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin $-0.3V$ to $V_{CC} + 0.3V$

Voltage at Any Input Pin
- MM54C901/MM74C901 $-0.3V$ to $+15V$
- MM54C902/MM74C902 $-0.3V$ to $+15V$
- MM54C903/MM74C903 $V_{CC} - 17V$ to $V_{CC} + 0.3V$
- MM54C904/MM74C904 $V_{CC} - 17V$ to $V_{CC} + 0.3V$

Storage Temperature Range (T_S) $-65°C$ to $+150°C$

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Operating Temperature Range (T_A)
- MM54C901, MM54C902, MM54C903, MM54C904 $-55°C$ to $+125°C$
- MM74C901, MM74C902, MM74C903, MM74C904 $-40°C$ to $+85°C$

Operating V_{CC} Range 3.0V to 15V

Absolute Maximum V_{CC} 18V

Lead Temperature (T_L) (Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5.0V$, $I_O = -10\ \mu A$ $V_{CC} = 10V$, $I_O = -10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5.0V$ $V_{CC} = 10V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$		0.05	15	μA
TTL TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$	$V_{CC} - 1.5$ $V_{CC} - 1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC} = 4.5V$ 74C $V_{CC} = 4.75V$			0.8 0.8	V V
CMOS TO TTL						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5V$	4.0			V
	MM54C902, MM54C904	$V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
	MM74C901, MM74C903	$V_{CC} = 4.75V$	4.25			V
	MM74C902, MM74C904	$V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5V$			1.0	V
	MM54C902, MM54C904	$V_{CC} = 4.5V$			1.5	V
	MM74C901, MM74C903	$V_{CC} = 4.75V$			1.0	V
	MM74C902, MM74C904	$V_{CC} = 4.75V$			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC} = 4.5V$, $I_O = -800\ \mu A$ 74C $V_{CC} = 4.75V$, $I_O = -800\ \mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C901, MM54C903	$V_{CC} = 4.5V$, $I_O = 2.6$ mA			0.4	V
	MM54C902, MM54C904	$V_{CC} = 4.5V$, $I_O = 3.2$ mA			0.4	V
	MM74C901, MM74C903	$V_{CC} = 4.75V$, $I_O = 2.6$ mA			0.4	V
	MM74C902, MM74C904	$V_{CC} = 4.75V$, $I_O = 3.2$ mA			0.4	V

DC Electrical Characteristics (Continued)

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current) (MM54C901/MM74C901, MM54C903/MM74C903)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = 0V$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = 0V$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$, $V_{IN} = V_{CC}$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0.4V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	3.8			mA
(MM54C902/MM74C902, MM54C904/MM74C904)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$, $V_{IN} = 0V$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0V$, $V_{OUT} = 0.4V$ $T_A = 25°C$, $V_{IN} = 0V$	3.8			mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

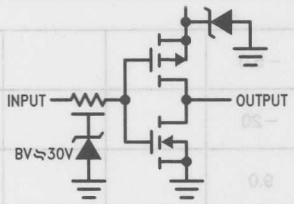
Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM54C901/MM74C901, MM54C903/MM74C903						
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		38 22	70 30	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		21 13	35 20	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		14		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF
MM54C902/MM74C902, MM54C904/MM74C904						
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		57 27	90 40	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0V$ $V_{CC} = 10V$		54 25	90 40	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		50		pF

*AC Parameters are guaranteed by DC correlated testing.

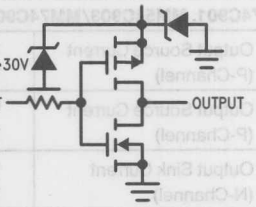
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

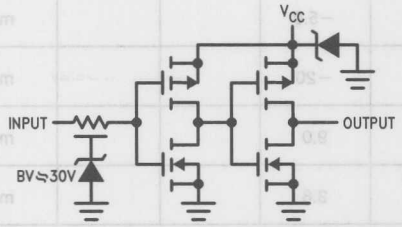


TL/F/5909-3



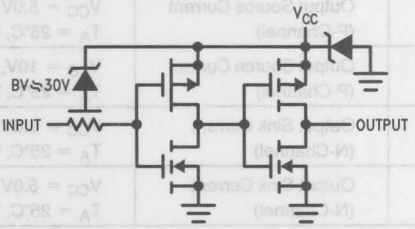
TL/F/5909-4

MM54C902/MM74C902
CMOS to TTL Buffer



TL/F/5909-5

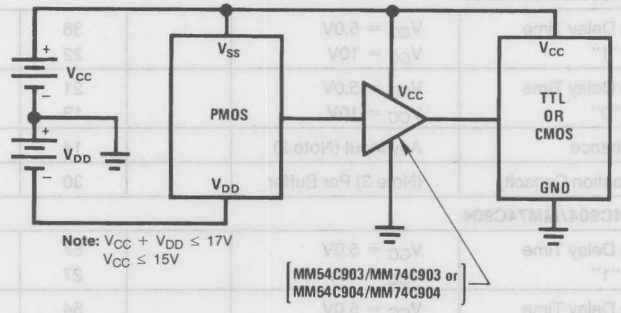
MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



TL/F/5909-6

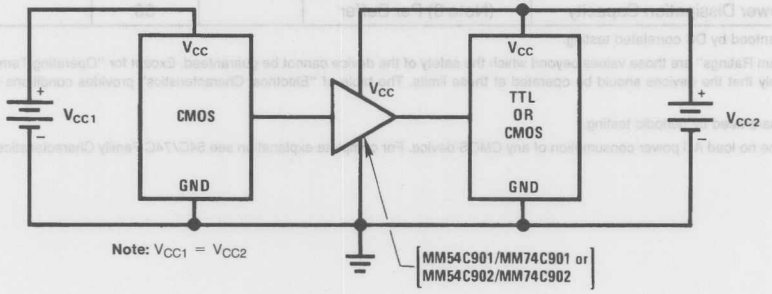
Typical Applications

PMOS to CMOS or TTL Interface



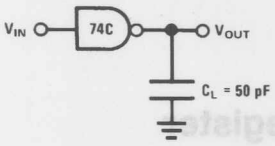
TL/F/5909-7

CMOS to TTL or CMOS at a Lower V_{CC}



TL/F/5909-8

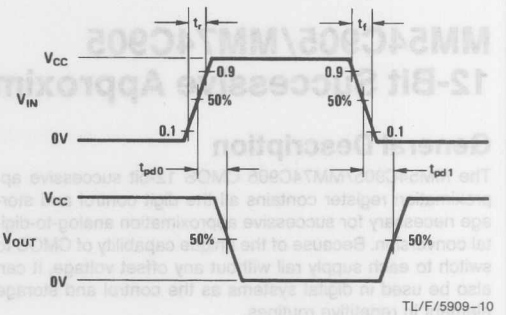
AC Test Circuit and Switching Time Waveforms



TL/F/5909–9

Note: Delays measured with input t_r, t_f = 20 ns.

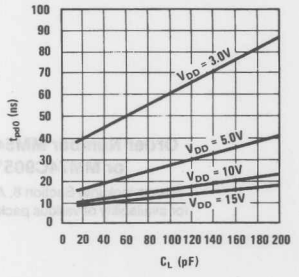
CMOS to CMOS



TL/F/5909–10

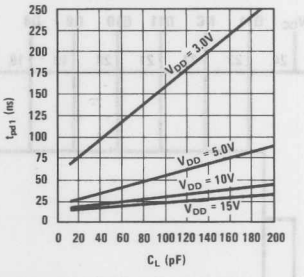
Typical Performance Characteristics

Typical Propagation Delay to a Logical "0" for the MM54C901/MM74C901 and MM54C903/MM74C903



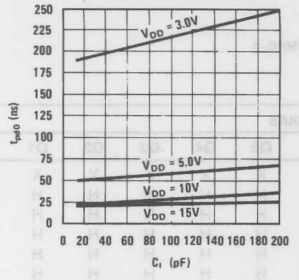
TL/F/5909–11

Typical Propagation Delay to a Logical "1" for the MM54C901/MM74C901 and M54C903/MM74C903



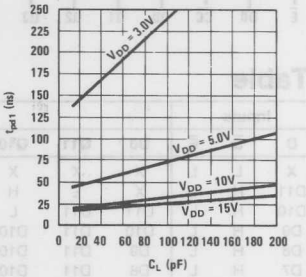
TL/F/5909–13

Typical Propagation Delay to a Logical "0" for the MM54C902/MM74C902 and MM54C904/MM74C904



TL/F/5909–14

Typical Propagation Delay to a Logical "1" for the MM54C902/MM74C902 and MM54C904/MM74C904



TL/F/5909–12

6

National Semiconductor

PRELIMINARY

MM54C905/MM74C905
12-Bit Successive Approximation Register

General Description

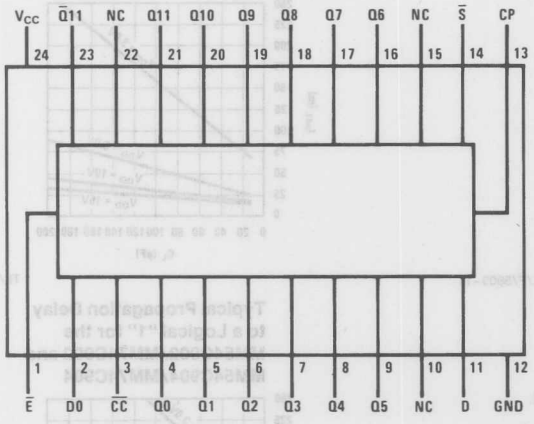
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} (typ)
- Low power TTL compatibility — Fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram

Dual-In-Line Package



TL/F/5910–1

Order Number MM54C905* or MM74C905*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Table

Time	Inputs			Outputs													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High Level L = Low Level X = Don't Care NC = No Change

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin −0.3V to V_{CC} +0.3V

Operating Temperature Range (T_A)

MM54C905 −55°C to +125°C

MM74C905 −40°C to +85°C

Storage Temperature Range (T_S) −65°C to +150°C

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V_{CC} Range 3.0V to 15V

Absolute Maximum V_{CC} 16V

Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C905	V_{CC} = 4.5V	V_{CC} − 1.5			V
	MM74C905	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C905	V_{CC} = 4.5V			0.8	V
	MM74C905	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage					
	MM54C905	V_{CC} = 4.5V, I_O = −360 μA	2.4			V
	MM74C905	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C905	V_{CC} = 4.5V, I_O = 360 μA			0.4	V
	MM74C905	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C, V_{CC} = 10V ±5%	8.0	16		mA
R_{SOURCE}	Q11–Q0 Outputs	V_{OUT} = V_{CC} − 0.3V, T_A = 25°C	150		350	Ω
R_{SINK}	Q11–Q0 Outputs	V_{CC} = 10V ±5%, V_{OUT} = 0.3V, T_A = 25°C	80		230	Ω

	Clock Input to Outputs (Q0–Q11) ($t_{pd(Q)}$)	V_{CC} = 10V		80	150	ns
t_{pd}	Propagation Delay Time from Clock Input to D0 ($t_{pd(D0)}$)	V_{CC} = 5.0V V_{CC} = 10V		180 70	325 125	ns ns
t_{pd}	Propagation Delay Time from Register Enable (E) to Output (Q11) ($t_{pd(E)}$)	V_{CC} = 5.0V V_{CC} = 10V		190 75	350 150	ns ns
t_{pd}	Propagation Delay Time from Clock to CC ($t_{pd(CC)}$)	V_{CC} = 5.0V V_{CC} = 10V		190 75	350 0.50	ns ns
t_S	Data Input Set-Up Time	V_{CC} = 5.0V V_{CC} = 10V	80 30			ns ns
t_S	Start Input Set-Up Time	V_{CC} = 5.0V V_{CC} = 10V	80 30			ns ns
t_W	Minimum Clock Pulse Width	V_{CC} = 5.0V V_{CC} = 10V	250 100	125 50		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	V_{CC} = 5.0V V_{CC} = 10V			15 5.0	μs μs
f_{MAX}	Maximum Clock Frequency	V_{CC} = 5.0V V_{CC} = 10V	2.0 5.0	4.0 10		MHz MHz
C_{CK}	Clock Input Capacitance	Clock Input (Note 2)		10		pF
C_{IN}	Input Capacitance	Any other Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

*AC Parameters are guaranteed by DC correlated testing.

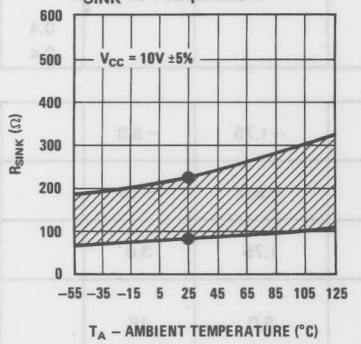
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics Application Note—AN-90.

Typical Performance Characteristics

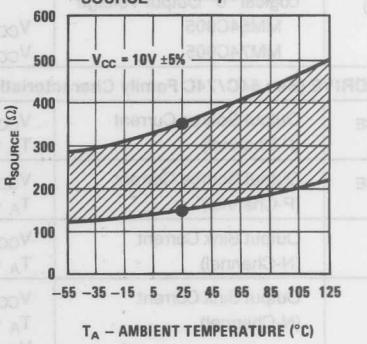
R_{SINK} vs Temperature



TL/F/5910–2

• These points are guaranteed by automatic testing.

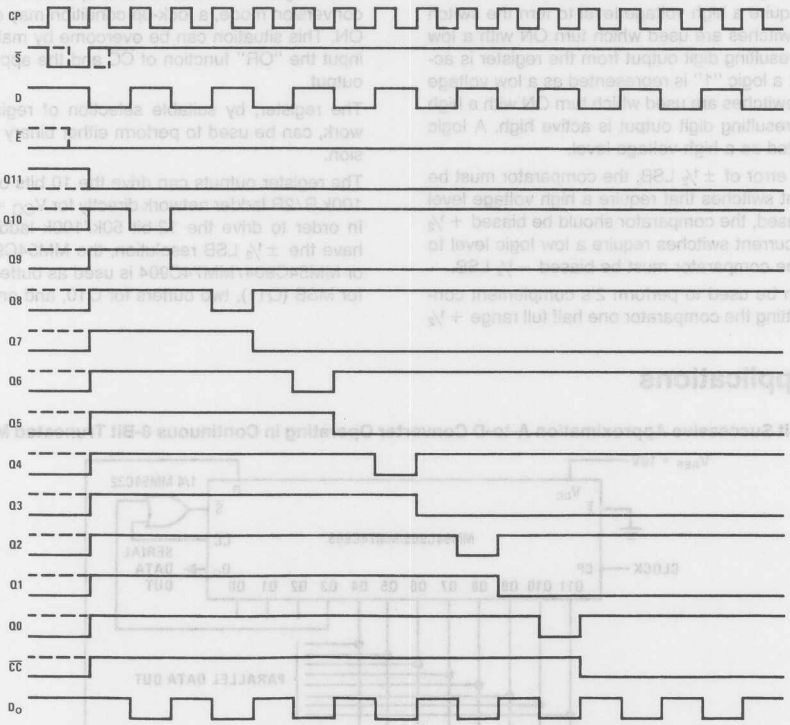
R_{SOURCE} vs Temperature



TL/F/5910–3

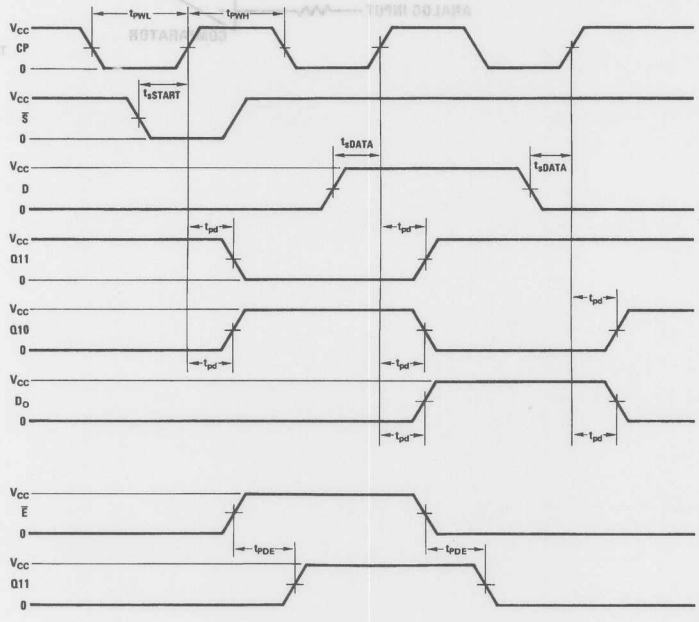
• These points are guaranteed by automatic testing.

Timing Diagram



TL/F/5910–4

Switching Time Waveforms



TL/F/5910–5

USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of $\pm\frac{1}{2}$ LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased $+\frac{1}{2}$ LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased $-\frac{1}{2}$ LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range $+\frac{1}{2}$ LSB and using the complement of the MSB Q11 as the sign bit.

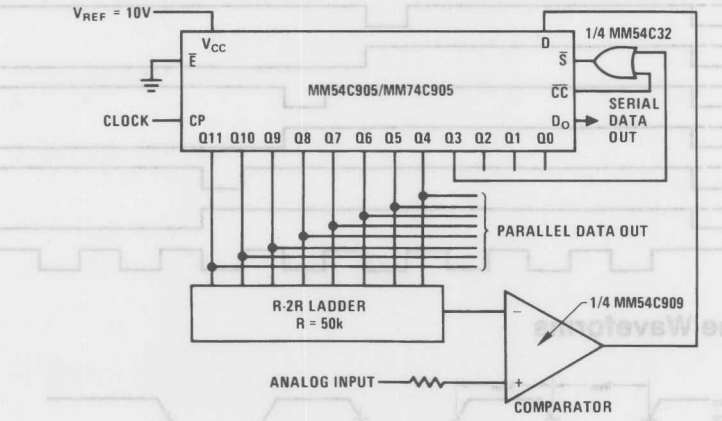
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for $V_{CC} = 10V$ or higher. In order to drive the 12-bit 50k/100k ladder network and have the $\pm\frac{1}{2}$ LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

Typical Applications

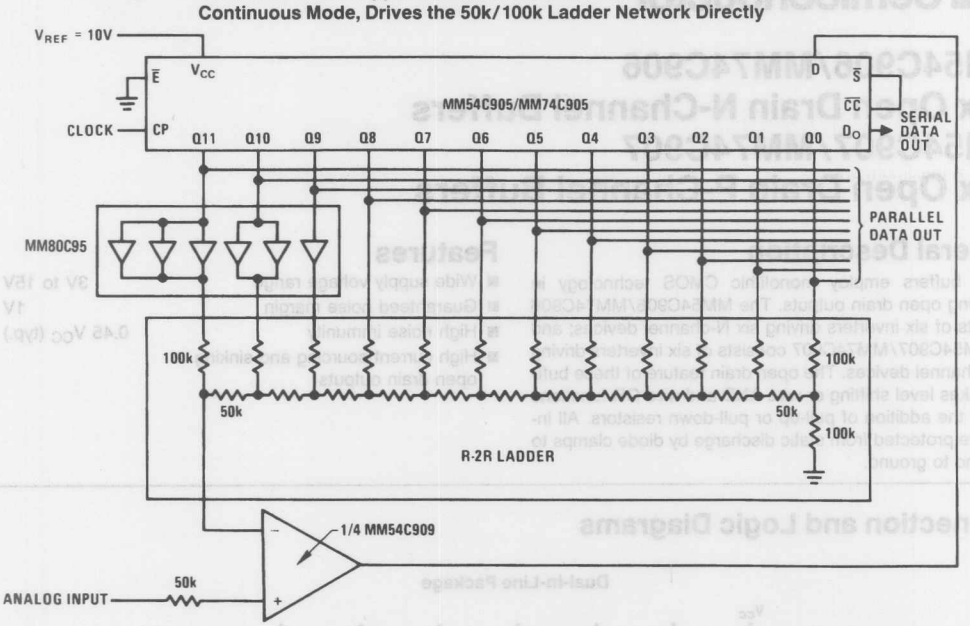
12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



TL/F/5910–6

Typical Applications (Continued)

12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



TL/F/5910–7

Definition of Terms

CP: Register *clock* input.

CC: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q}$11: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

National Semiconductor

MM54C906/MM74C906
Hex Open Drain N-Channel Buffers
MM54C907/MM74C907
Hex Open Drain P-Channel Buffers

General Description

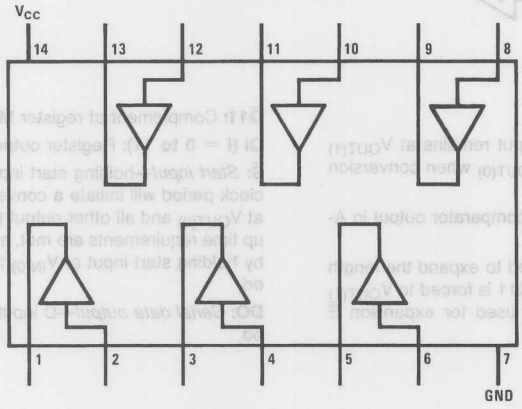
These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

Features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ High current sourcing and sinking open drain outputs	

Connection and Logic Diagrams

Dual-In-Line Package



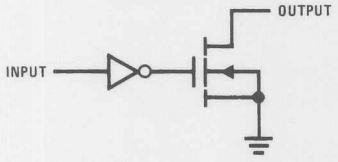
TL/F/5911–1

Top View

Order Number MM54C906*, MM54C907*, MM74C906* or MM74C907*

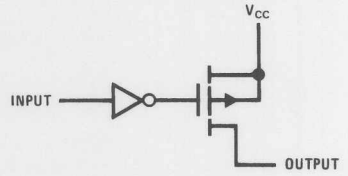
*Please look into Section 8, Appendix D for availability of various package types.

MM54C906/MM74C906



TL/F/5911–2

MM54C907/MM74C907



TL/F/5911–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Input Pin	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Any Output Pin	
MM54C906/MM74C906	$-0.3V$ to $+18V$
MM54C907/MM74C907	$V_{CC} - 18$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C906/MM54C907	$-55°C$ to $+125°C$
MM74C906/MM74C907	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 15V$, Output Open		0.05	15	μA
	Output Leakage					
	MM54C906	$V_{CC} = 4.5V$, $V_{IN} = V_{CC} - 1.5V$				
		$V_{CC} = 4.5V$, $V_{OUT} = 18V$		0.005	5	μA
	MM74C906	$V_{CC} = 4.75V$, $V_{IN} = V_{CC} - 1.5V$				
		$V_{CC} = 4.75V$, $V_{OUT} = 18V$		0.005	5	μA
	MM54C907	$V_{CC} = 4.5V$, $V_{IN} = 1V + 0.1\ V_{CC}$				
		$V_{CC} = 4.5V$, $V_{OUT} = V_{CC} - 18V$		0.005	5	μA
	MM74C907	$V_{CC} = 4.75V$, $V_{IN} = 1V + 0.1\ V_{CC}$				
		$V_{CC} = 4.75V$, $V_{OUT} = V_{CC} - 18V$		0.005	5	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5V$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5V$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE CURRENT						
	MM54C906	$V_{CC} = 4.5V$, $V_{IN} = 1V + 0.1\ V_{CC}$				
		$V_{CC} = 4.5V$, $V_{OUT} = 0.5V$	2.1	8.0		mA
		$V_{CC} = 4.5V$, $V_{OUT} = 1.0V$	4.2	12.0		mA
	MM74C906	$V_{CC} = 4.75V$, $V_{IN} = 1V + 0.1\ V_{CC}$				
		$V_{CC} = 4.75V$, $V_{OUT} = 0.5V$	2.1	8.0		mA
		$V_{CC} = 4.75V$, $V_{OUT} = 1.0V$	4.2	12.0		mA
	MM54C907	$V_{CC} = 4.5V$, $V_{IN} = V_{CC} - 1.5V$				
		$V_{CC} = 4.5V$, $V_{OUT} = V_{CC} - 0.5V$	-1.05	-1.5		mA
		$V_{CC} = 4.5V$, $V_{OUT} = V_{CC} - 1V$	-2.1	-3.0		mA
	MM74C907	$V_{CC} = 4.75V$, $V_{IN} = V_{CC} - 1.5V$				
		$V_{CC} = 4.75V$, $V_{OUT} = V_{CC} - 0.5V$	-1.05	-1.5		mA
		$V_{CC} = 4.75V$, $V_{OUT} = V_{CC} - 1V$	-2.1	-3.0		mA
	MM54C906/MM74C906	$V_{CC} = 10V$, $V_{IN} = 2V$				
		$V_{CC} = 10V$, $V_{OUT} = 0.5V$	4.2	-20		mA
		$V_{CC} = 10V$, $V_{OUT} = 1V$	8.4	-30		mA
	MM54C907/MM74C907	$V_{CC} = 10V$, $V_{IN} = 8V$				
		$V_{CC} = 10V$, $V_{OUT} = 9.5V$	-2.1	-4.0		mA
		$V_{CC} = 10V$, $V_{OUT} = 9V$	-4.2	-8.0		mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, R = 10k			150	ns
		$V_{CC} = 10V$, R = 10k			75	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$ (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$ (Note 4)			75 + 0.7 RC	ns
t_{pd}	Propagation Delay Time to a Logical "1"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$ (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$ (Note 4)			75 + 0.7 RC	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, R = 10k			150	ns
		$V_{CC} = 10V$, R = 10k			75	ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{OUT}	Output Capacity	(Note 2)		20		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

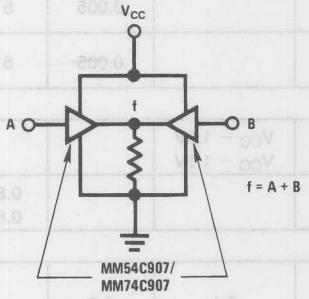
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90. (Assumes outputs are open).

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

Typical Applications

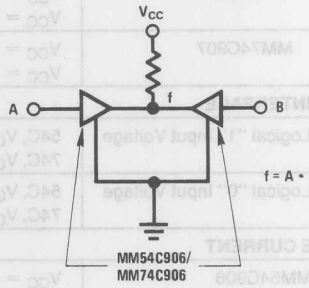
Wire OR Gate



TL/F/5911–4

Note: Can be extended to more than 2 inputs.

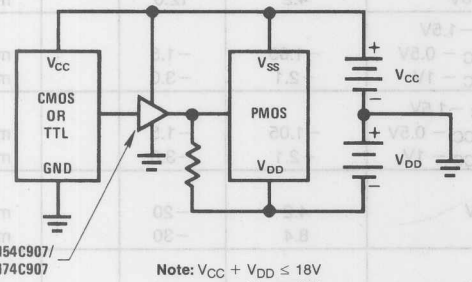
Wire AND Gate



TL/F/5911–5

Note: Can be extended to more than 2 inputs.

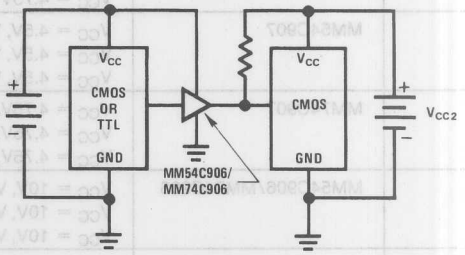
CMOS or TTL to PMOS Interface



Note: $V_{CC} + V_{DD} \leq 18V$
$V_{CC} \leq 15V$

TL/F/5911–6

CMOS or TTL to CMOS at a Higher V_{CC}



TL/F/5911–7

National Semiconductor

MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4-bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{WE}$, and a $\overline{ME}$ line. The six address lines are internally decoded to select one of the 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{ME}$. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{ME}$, and (t_{HA}) after the positive to negative transition of $\overline{ME}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{WE}$ goes low while $\overline{ME}$ is low. $\overline{WE}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{WE}$ returns high.

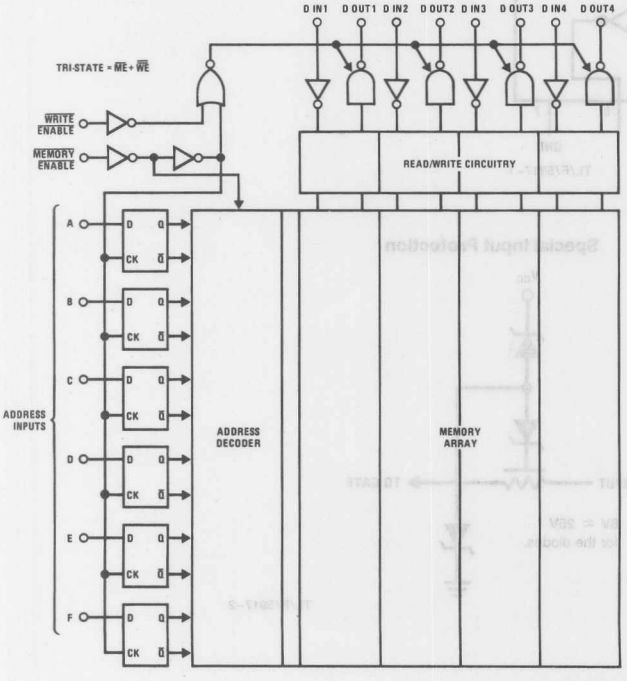
Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{WE}$ held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

Features

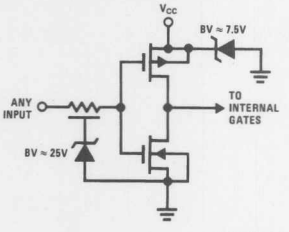
■ Supply voltage range	3.0V to 5.5V
■ High noise immunity	$0.45V_{CC}$ (typ.)
■ TTL compatible fan out	1 TTL load
■ Input address register	
■ Low power consumption	250 nW/package (typ.) (chip enabled or disabled)
■ Fast access time	250 ns (typ.) at 5.0V
■ TRI-STATE outputs	
■ High voltage inputs	

Logic Diagrams



TL/F/5914–1

Input Protection



TL/F/5914–2

National Semiconductor

MM54C914/MM74C914 Hex Schmitt Trigger with Extended Input Voltage

General Description

The MM54C914/MM74C914 is a monolithic CMOS Hex Schmitt trigger with special input protection scheme. This scheme allows the input voltage levels to exceed V_{CC} or ground by at least 10V (V_{CC} − 25V to GND + 25V), and is valuable for applications involving voltage level shifting or mismatched power supplies.

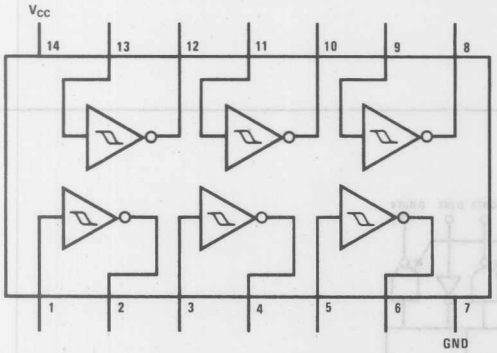
The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{CC} = 10V). And the hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

Features

■ Hysteresis	0.45 V_{CC} (typ.) 0.2 V_{CC} guaranteed
■ Special input protection	Extended Input Voltage Range
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.7 V_{CC} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L

Connection Diagram

Dual-In-Line Package



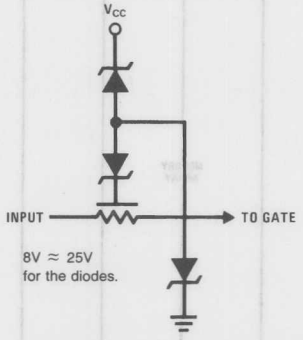
TL/F/5917–1

Top View

Order Number MM54C914* or MM74C914*

*Please look into Section 8, Appendix D for availability of various package types.

Special Input Protection



TL/F/5917–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Input Pin	V_{CC} − 25V to GND + 25V
Voltage at any other Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range (T_A)	
MM54C914	−55°C to +125°C
MM74C914	−40°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum (V_{CC})	18V
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive Going Threshold Voltage	V_{CC} = 5V	3.0	3.6	4.3	V
		V_{CC} = 10V	6.0	6.8	8.6	V
		V_{CC} = 15V	9.0	10	12.9	V
V_{T-}	Negative Going Threshold Voltage	V_{CC} = 5V	0.7	1.4	2.0	V
		V_{CC} = 10V	1.4	3.2	4.0	V
		V_{CC} = 15V	2.1	5	6.0	
$V_{T+} - V_{T-}$	Hysteresis	V_{CC} = 5V	1.0	2.2	3.6	V
		V_{CC} = 10V	2.0	3.6	7.2	V
		V_{CC} = 15V	3.0	5	10.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = +10 μA			0.5	V
		V_{CC} = 10V, I_O = +10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 25V		0.005	5.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = −10V	−100	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V, V_{IN} = − 10V/25V		0.05	300	μA
		V_{CC} = 5V, V_{IN} = − 2.5V (Note 4)		20		μA
		V_{CC} = 10V, V_{IN} = 5V (Note 4)		200		μA
		V_{CC} = 15V, V_{IN} = 7.5V (Note 4)		600		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360 μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 360 μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay from Input to Output	$V_{CC} = 5V$		220	400	ns
		$V_{CC} = 10V$		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

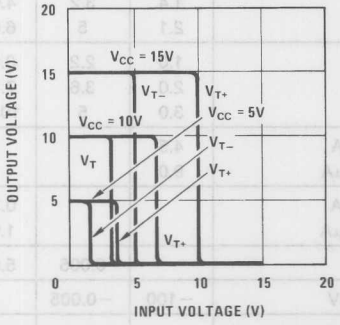
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

Note 4: Only one input is at ½ V_{CC}, the others are either at V_{CC} or GND.

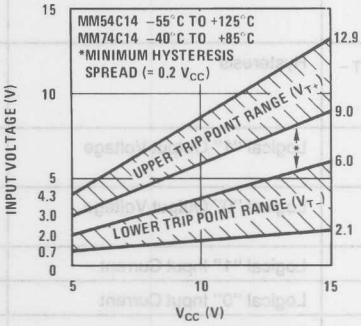
Typical Performance Characteristics

Typical Transfer Characteristics

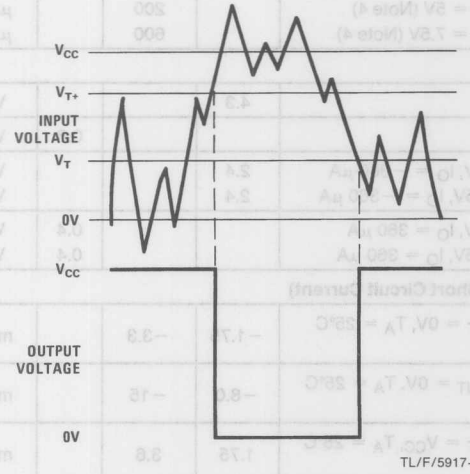


TL/F/5917–4

Guaranteed Trip Point Range

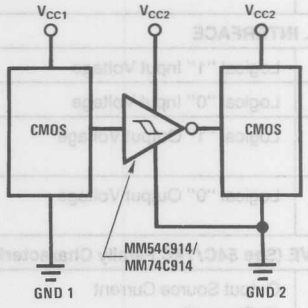


TL/F/5917–5



TL/F/5917–6

Typical Application



TL/F/5917–3

Note: $V_{CC1} = V_{CC2}$
GND1 = GND2

MM54C915/MM74C915 7-Segment-to-BCD Converter

General Description

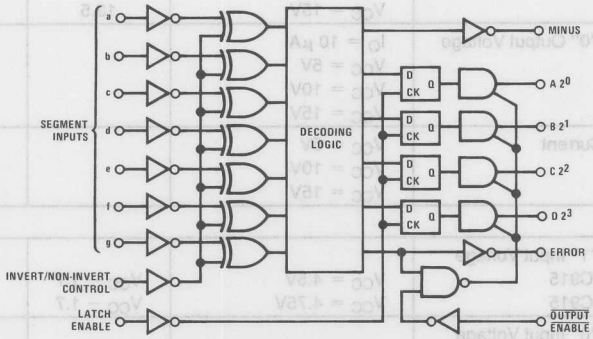
The MM54C915/MM74C915 is a monolithic complementary MOS (CMOS) integrated circuit, constructed with N- and P-channel enhancement-mode transistors. This circuit accepts 7-segment information and converts it into BCD information. The true state of the Segment inputs can be selected by use of the Invert/Non-Invert control pin. A logical "0" on the Invert/Non-Invert control pin selects active high true decoding at the Segment inputs. A logical "1" on the Invert/Non-Invert control pin selects active low true decoding at the Segment inputs. In addition to 4 TTL compatible BCD outputs, an Error output and Minus output are available. The Error output goes to an active "1" whenever a non-standard 7-segment code appears at the Segment input. The BCD outputs are forced into a TRI-STATE® condition when an error is detected. This allows the user to program his own error code by tying the BCD outputs to V_{CC} or Ground via high value resistors (~ 500k). The BCD outputs may also be forced into TRI-STATE by a logical "1" on output enable ($\overline{OE}$).

The Minus output goes to a logical "1" whenever a minus code is detected and is useful as a microprocessor interrupt. The BCD outputs are in a flow-through condition when Latch Enable (LE) is at a logical "0" and latched when LE is at a logical "1". The inputs will not clamp signals to the positive supply, allowing simple level translation from MOS to TTL.

Features

- Wide supply range — 3V–15V
- High noise immunity — 0.45 V_{CC} (typ.)
- TTL compatible fan out — 1 TTL load
- Selectable active true inputs
- TRI-STATE outputs
- On-chip latch
- Error output
- Minus output

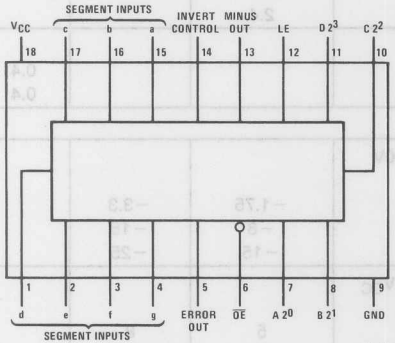
Logic Diagram



TL/F/5918–1

Connection Diagram

Dual-In-Line Package



TL/F/5918–2

Top View

Order Number MM54C915* or MM74C915*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Output: $-0.3V$ to $V_{CC} + 0.3V$

Voltage at Any Input: $-0.3V$ to $18V$

Operating Temperature Range

MM54C915: $-55°C$ to $+125°C$

MM74C915: $-40°C$ to $+85°C$

Storage Temperature Range: $-65°C$ to $+150°C$

Power Dissipation

Dual-In-Line: 700 mW

Small Outline: 500 mW

Operating V_{CC} Range: 4.0V to 15V

Maximum V_{CC}: 18V

Lead Temperature (Soldering, 10 seconds): 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.5			V
		$V_{CC} = 10V$	8.0			V
		$V_{CC} = 15V$	12.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
		$V_{CC} = 10V$			2.0	V
		$V_{CC} = 15V$			2.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN} = 0V$	-1.0	-0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = 10\ \mu A$				
		$V_{CC} = 5V$	4.5			V
		$V_{CC} = 10V$	9.0			V
		$V_{CC} = 15V$	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 10\ \mu A$				
		$V_{CC} = 5V$			0.5	V
		$V_{CC} = 10V$			1.0	V
		$V_{CC} = 15V$			1.5	V
I_{CC}	Supply Current	$V_{CC} = 5V$		0.25	1	mA
		$V_{CC} = 10V$		0.75	2.5	mA
		$V_{CC} = 15V$		1.00	3.0	mA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C915	$V_{CC} = 4.5V$	$V_{CC} - 1.7$			V
	MM74C915	$V_{CC} = 4.75V$	$V_{CC} - 1.7$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C915	$V_{CC} = 4.5V$			0.8	V
	MM74C915	$V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O = -360\ \mu A$				
	MM54C915	$V_{CC} = 4.5V$	2.4			V
	MM74C915	$V_{CC} = 4.75V$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O = 1.6$ mA				
	MM54C915	$V_{CC} = 4.5V$			0.4	V
	MM74C915	$V_{CC} = 4.75V$			0.4	V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current P-Channel	$T_A = 25°C$, $V_O = 0V$ (Note 2)				
		$V_{CC} = 5V$	-1.75	-3.3		mA
		$V_{CC} = 10V$	-8	-15		mA
		$V_{CC} = 15V$	-15	-25		mA
I_{SINK}	Output Sink Current N-Channel	$T_A = 25°C$, $V_O = V_{CC}$ (Note 2)				
		$V_{CC} = 5V$	5	8		mA
		$V_{CC} = 10V$	20	30		mA
		$V_{CC} = 15V$	30	50		mA

AC Electrical Characteristics* $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1"	$C_L = 50$ pF				
		$V_{CC} = 5V$		500	1000	ns
		$V_{CC} = 10V$		300	600	ns
		$V_{CC} = 15V$		300	600	ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	$R_L = 10k$, $C_L = 10$ pF				
		$V_{CC} = 5V$		110	200	ns
		$V_{CC} = 10V$		75	130	ns
		$V_{CC} = 15V$		60	110	ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	$R_L = 10k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		150	250	ns
		$V_{CC} = 10V$		80	140	ns
		$V_{CC} = 15V$		70	125	ns
t_s	Input Data Set-Up Time	$C_L = 50$ pF				
		$V_{CC} = 5V$		500	1000	ns
		$V_{CC} = 10V$		300	600	ns
		$V_{CC} = 15V$		300	600	ns
t_H	Input Data Hold Time	$C_L = 50$ pF				
		$V_{CC} = 5V$		−150	0	ns
		$V_{CC} = 10V$		−100	0	ns
		$V_{CC} = 15V$		−100	0	ns
C_{IN}	Input Capacitance	Any Input (Note 3)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output (Note 3)		10		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply to transient operation. It is not meant to imply that the device should be operated at these limits in sustained operation.

Note 3: Capacitance is guaranteed by periodic testing.

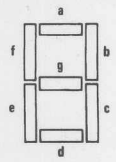
Truth Table

CHARACTER AT SEGMENT INPUTS	BCD OUTPUTS D 2^3	C 2^2	B 2^1	A 2^0	NON-BCD OUTPUTS ERROR	MINUS
0	0	0	0	0	0	0
1	0	0	0	1	0	0
-	0	0	0	1	0	0
2	0	0	1	0	0	0
3	0	0	1	1	0	0
4	0	1	0	0	0	0
5	0	1	0	1	0	0
6	0	1	1	0	0	0
6	0	1	1	0	0	0
7	0	1	1	1	0	0
8	1	0	0	0	0	0
9	1	0	0	1	0	0
9	1	0	0	1	0	0
	1	1	1	1	0	0
-	X	X	X	X	1	1
All other input combinations	X	X	X	X	1	0

X = represents TRI-STATE condition

TL/F/5918–3

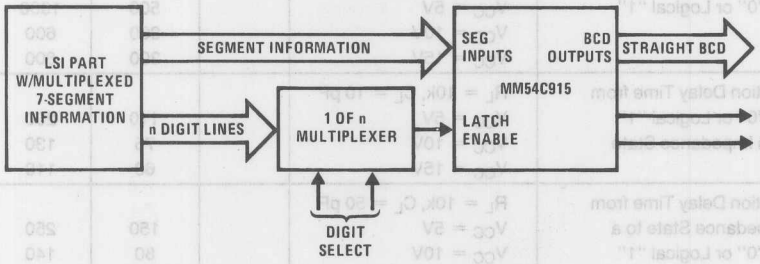
Segment Identification



TL/F/5918–4

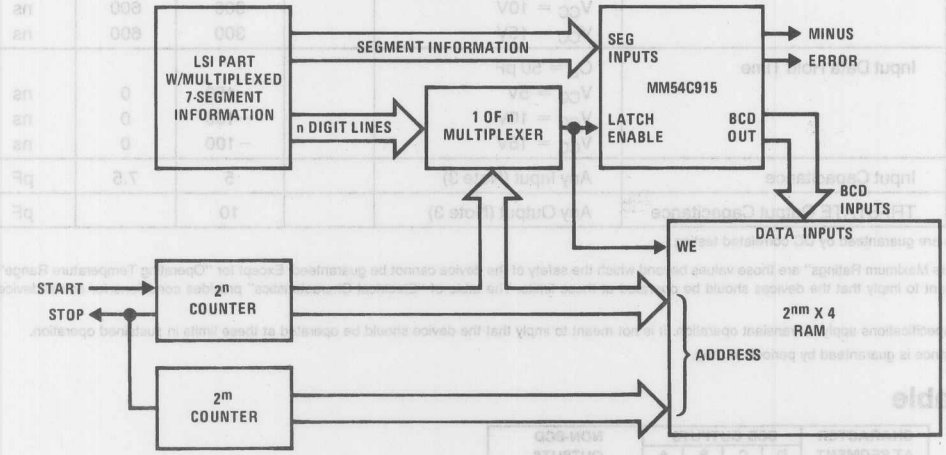
Typical Applications

Multiplex 7-Segment to Straight BCD



TL/F/5918–5

Memory Expansion from 7-Segment Outputs



TL/F/5918–6

National Semiconductor

MM54C922/MM74C922 16-Key Encoder
MM54C923/MM74C923 20-Key Encoder

General Description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two-key rollover is provided between any two switches.

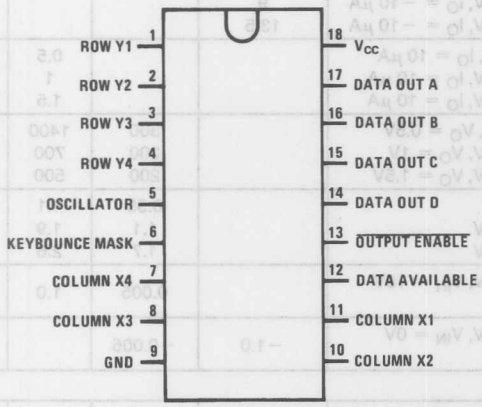
An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On-chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outpust LPTTL compatible
- Wide supply range — 3V to 15V
- Low power consumption

Connection Diagrams

Dual-In-Line Package

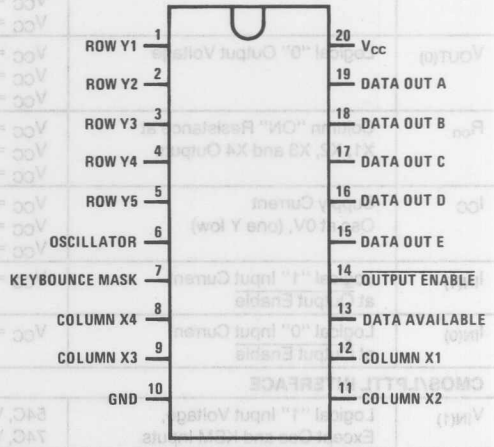


TL/F/6037–1

Top View

Order Number MM54C922* or MM74C922*

Dual-In-Line Package



TL/F/6037–2

Top View

Order Number MM54C923* or MM74C923*

*Please look into Section 8, Appendix D for availability of various package types.

6

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin $V_{CC} - 0.3V$ to $V_{CC} + 0.3V$

Operating Temperature Range

MM54C922, MM54C923 $-55°C$ to $+125°C$

MM74C922, MM74C923 $-40°C$ to $+85°C$

Storage Temperature Range $-65°C$ to $+150°C$

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Operating V_{CC} Range 3V to 15V

V_{CC} 18V

Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V$, $I_{IN} \geq 0.7$ mA	3.0	3.6	4.3	V
		$V_{CC} = 10V$, $I_{IN} \geq 1.4$ mA	6.0	6.8	8.6	V
		$V_{CC} = 15V$, $I_{IN} \geq 2.1$ mA	9.0	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	$V_{CC} = 5V$, $I_{IN} \geq 0.7$ mA	0.7	1.4	2.0	V
		$V_{CC} = 10V$, $I_{IN} \geq 1.4$ mA	1.4	3.2	4.0	V
		$V_{CC} = 15V$, $I_{IN} \geq 2.1$ mA	2.1	5	6.0	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V$	3.5	4.5		V
		$V_{CC} = 10V$	8.0	9		V
		$V_{CC} = 15V$	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	$V_{CC} = 5V$		0.5	1.5	V
		$V_{CC} = 10V$		1	2	V
		$V_{CC} = 15V$		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	$V_{CC} = 5V$, $V_{IN} = 0.1\ V_{CC}$		-2	-5	μA
		$V_{CC} = 10V$		-10	-20	μA
		$V_{CC} = 15V$		-22	-45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
		$V_{CC} = 10V$, $I_O = -10\ \mu A$	9			V
		$V_{CC} = 15V$, $I_O = -10\ \mu A$	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC} = 5V$, $I_O = 10\ \mu A$			0.5	V
		$V_{CC} = 10V$, $I_O = 10\ \mu A$			1	V
		$V_{CC} = 15V$, $I_O = 10\ \mu A$			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	$V_{CC} = 5V$, $V_O = 0.5V$		500	1400	Ω
		$V_{CC} = 10V$, $V_O = 1V$		300	700	Ω
		$V_{CC} = 15V$, $V_O = 1.5V$		200	500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	$V_{CC} = 5V$		0.55	1.1	mA
		$V_{CC} = 10V$		1.1	1.9	mA
		$V_{CC} = 15V$		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at Output Enable	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at Output Enable	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, $V_{CC} = 4.5V$	$V_{CC} - 1.5$			V
		74C, $V_{CC} = 4.75V$	$V_{CC} - 1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, $V_{CC} = 4.5V$			0.8	V
		74C, $V_{CC} = 4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$	2.4			V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC} = 4.5V$, $I_O = -360\ \mu A$			0.4	V
		74C, $V_{CC} = 4.75V$, $I_O = -360\ \mu A$			0.4	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise specified (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$, $T_A = 25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	8	16		mA

AC Electrical Characteristics*

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

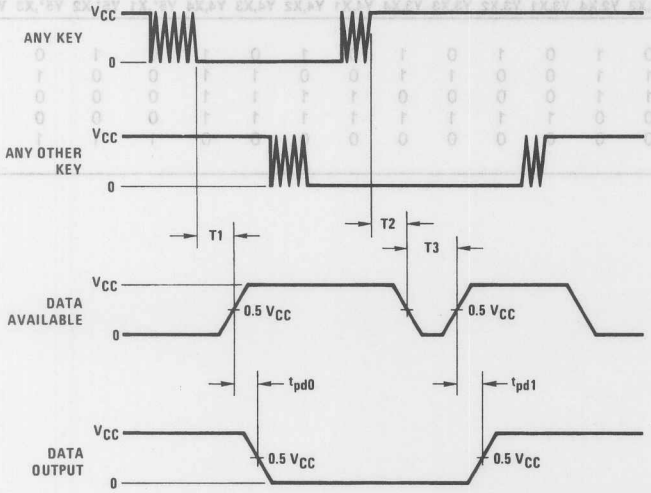
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	$C_L = 50$ pF *(Figure 1)*				
		$V_{CC} = 5V$		60	150	ns
		$V_{CC} = 10V$		35	80	ns
		$V_{CC} = 15V$		25	60	ns
t_{0H}, t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	$R_L = 10k$, $C_L = 10$ pF *(Figure 2)*				
		$V_{CC} = 5V$, $R_L = 10k$		80	200	ns
		$V_{CC} = 10V$, $C_L = 10$ pF		65	150	ns
		$V_{CC} = 15V$		50	110	ns
t_{H0}, t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	$R_L = 10k$, $C_L = 50$ pF *(Figure 2)*				
		$V_{CC} = 5V$, $R_L = 10k$		100	250	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		55	125	ns
		$V_{CC} = 15V$		40	90	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output (Note 2)		10		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

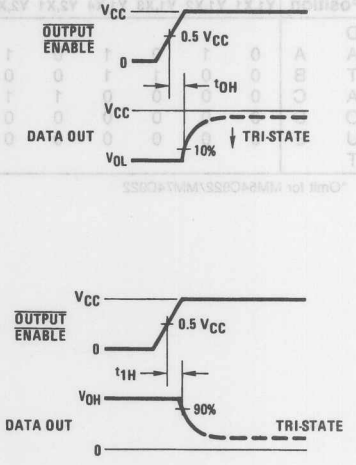
Switching Time Waveforms



TL/F/6037–3

T1 ≈ T2 ≈ RC, T3 ≈ 0.7 RC, where R ≈ 10k and C is external capacitor at KBM input.

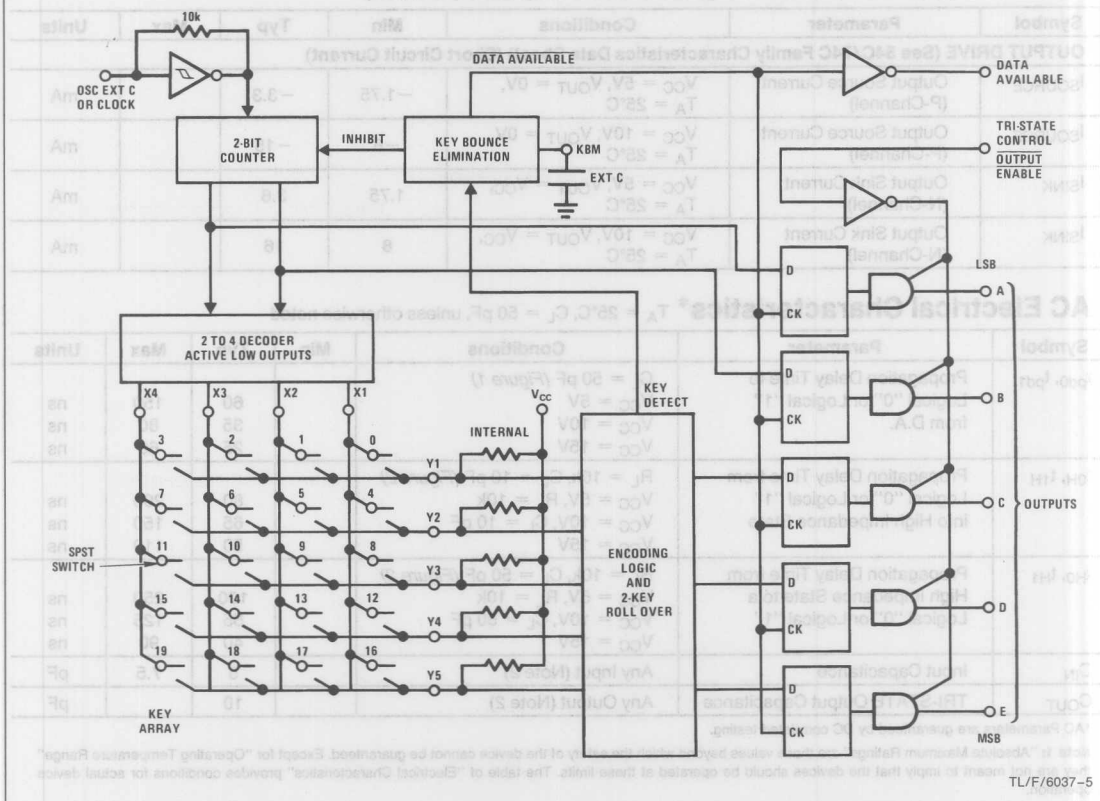
FIGURE 1



TL/F/6037–4

FIGURE 2

Block Diagram

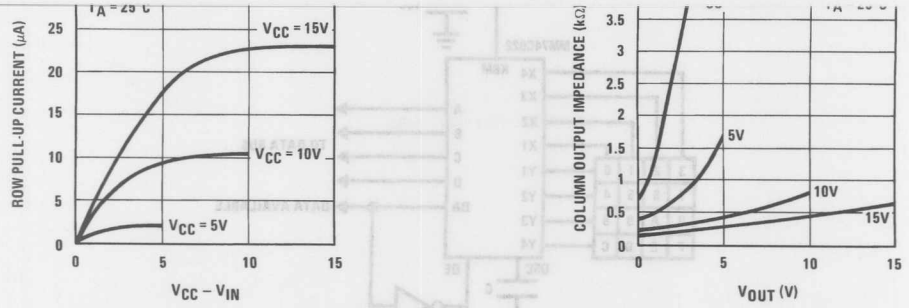


TL/F/6037–5

Truth Table

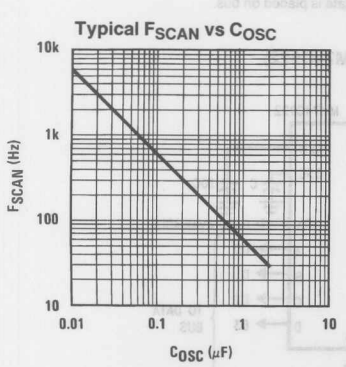
Switch Position		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
DATA OUT	A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
	D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

*Omit for MM54C922/MM74C922

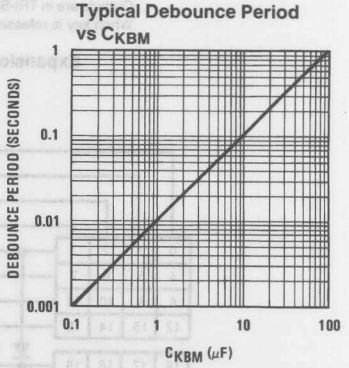


TL/F/6037–6

TL/F/6037–7



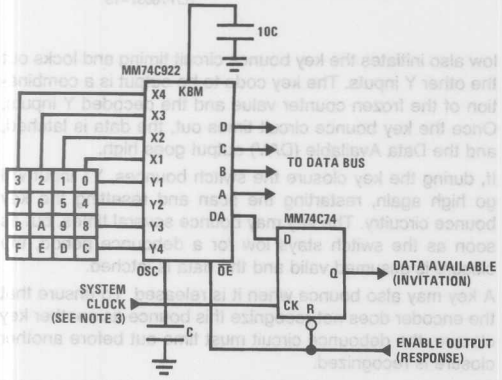
TL/F/6037–8



TL/F/6037–9

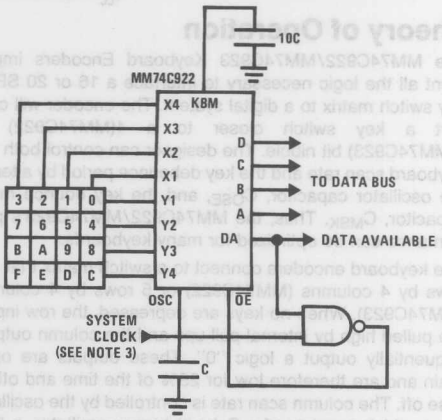
Typical Applications

Synchronous Handshake (MM74C922)



TL/F/6037–10

Synchronous Data Entry Onto Bus (MM74C922)



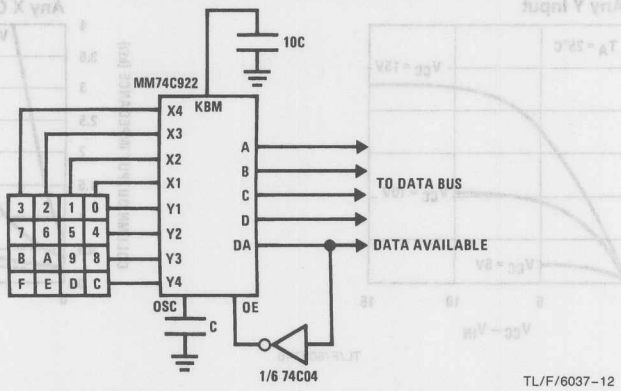
TL/F/6037–11

Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

Typical Applications (Continued)

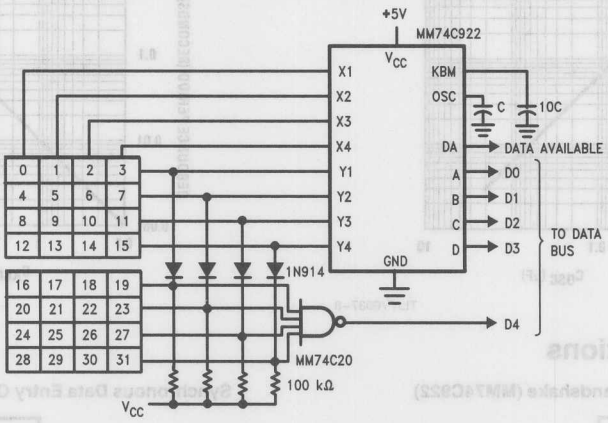
Asynchronous Data Entry Onto Bus (MM74C922)



TL/F/6037–12

Outputs are in TRI-STATE until key is pressed, then data is placed on bus.
When key is released, outputs return to TRI-STATE.

Expansion to 32 Key Encoder (MM74C922)



TL/F/6037–13

Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM74C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2–4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be output is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two-key roll-over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed TRI-STATE, which is enabled when the Output Enable ($\overline{OE}$) input is taken low.

National Semiconductor

MM54C932/MM74C932 Phase Comparator

General Description

The MM74C932/MM54C932 consists of two independent output phase comparator circuits. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

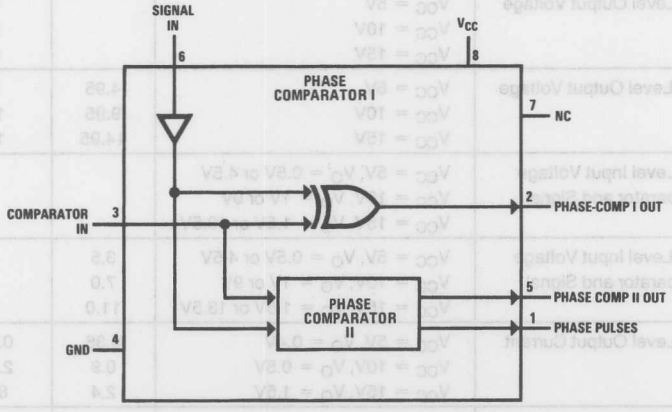
Phase comparator I, an exclusive-OR gate, provides a digital error signal (phase comp. I out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II out) and lock in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

Features

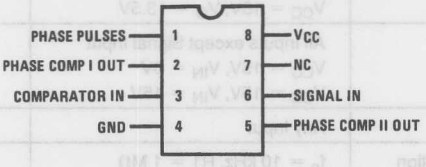
- Wide supply voltage range
- Convenient mini-DIP package
- TRI-STATE® phase-comparator output (comparator II)
- 200 mV input voltage (signal in) sensitivity (typical)

Block and Connection Diagrams



TL/F/5921–1

Dual-In-Line Package



TL/F/5921–2

Top View

Order Number MM54C932* or MM74C932*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range	
MM54C932	$-55°C$ to $+125°C$
MM74C932	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics

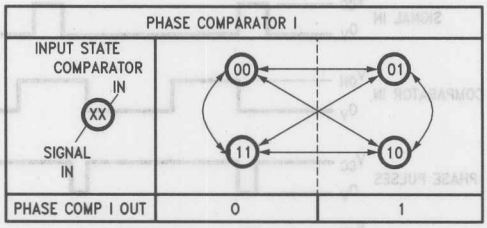
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Device Current	PIN 5 = V_{CC}, PIN 8 = V_{CC}, PIN 3 = 0V				
		V_{CC} = 5V		0.005	150	μA
		V_{CC} = 10V		0.01	300	μA
		V_{CC} = 15V		0.015	600	μA
		PIN 6 = Open, PIN 3 = GND				
		V_{CC} = 5V		5	205	μA
		V_{CC} = 10V		20	710	μA
		V_{CC} = 15V		50	1800	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 5V		0	0.05	V
		V_{CC} = 10V		0	0.05	V
		V_{CC} = 15V		0	0.05	V
V_{OH}	High Level Output Voltage	V_{CC} = 5V	4.95	5		V
		V_{CC} = 10V	9.95	10		V
		V_{CC} = 15V	14.95	15		V
V_{IL}	Low Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V			1.5	V
		V_{CC} = 10V, V_O = 1V or 9V			3.0	V
		V_{CC} = 15V, V_O = 1.5V or 13.5V			4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V	3.5			V
		V_{CC} = 10V, V_O = 1V or 9V	7.0			V
		V_{CC} = 15V, V_O = 1.5V or 13.5V	11.0			V
I_{OL}	Low Level Output Current	V_{CC} = 5V, V_O = 0.4V	0.36	0.88		mA
		V_{CC} = 10V, V_O = 0.5V	0.9	2.25		mA
		V_{CC} = 15V, V_O = 1.5V	2.4	8.8		mA
I_{OH}	High Level Output Current	V_{CC} = 5V, V_O = 4.6V	−0.36	−0.88		mA
		V_{CC} = 10V, V_O = 9.5V	−0.9	−2.25		mA
		V_{CC} = 15V, V_O = 13.5V	−2.4	−8.8		mA
I_{IN}	Input Current	All Inputs except Signal Input				
		V_{CC} = 15V, V_{IN} = 0V		-10^{-5}	−1.0	μA
		V_{CC} = 15V, V_{IN} = 15V		10^{-5}	1.0	μA
C_{IN}	Input Capacitance	Any Input			7.5	pF
P_D	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO_{IN} = $V_{CC}/2$				
		V_{CC} = 5V		0.07		mW
		V_{CC} = 10V		0.6		mW
		V_{CC} = 15V		2.4		mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

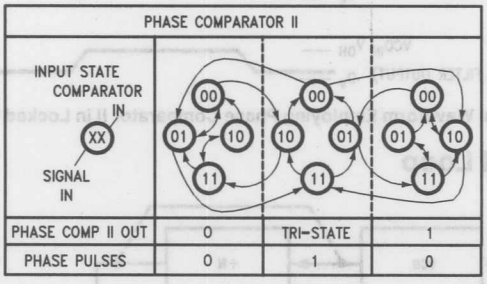
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{IN}	Phase Comparators					
	Input Resistance Signal Input	V_{CC} = 5V	1.0	3.0		MΩ
		V_{CC} = 10V	0.2	0.7		MΩ
		V_{CC} = 15V	0.1	0.3		MΩ
	Comparator Input	V_{CC} = 5V		10^6		MΩ
		V_{CC} = 10V		10^6		MΩ
		V_{CC} = 15V		10^6		MΩ
	AC Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000 pF f = 50 kHz				
		V_{CC} = 5V		200	400	mV
		V_{CC} = 10V		400	800	mV
		V_{CC} = 15V		700	1400	mV

Phase Comparator State Diagrams



TL/F/5921–3



TL/F/5921–4

FIGURE 1

Typical Waveforms

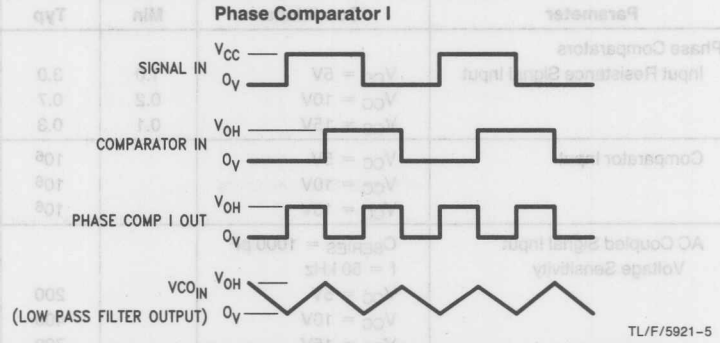


FIGURE 2. Typical Waveform Employing Phase Comparator I in Locked Condition

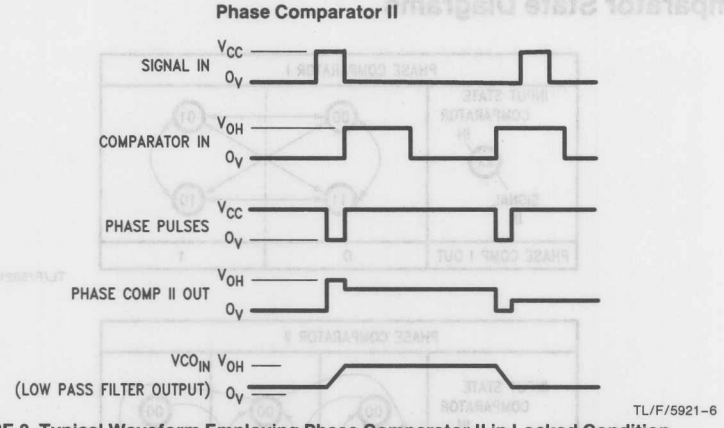
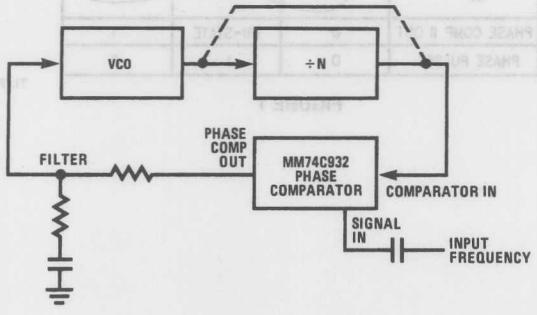


FIGURE 3. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Phase Locked Loop



National Semiconductor

MM54C941/MM74C941 Octal Buffers/Line Receivers/ Line Drivers with TRI-STATE® Outputs

General Description

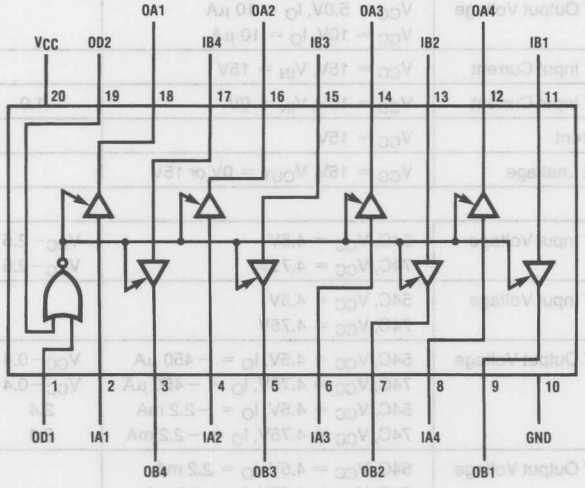
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. When V_{CC} = 5V, inputs can accept true TTL high and low logic levels.

Features

- Wide supply voltage range (3V to 15V)
- Low power consumption
- TTL compatibility (Improved on the inputs)
- High capacitive load
- TRI-STATE outputs
- Input protection
- 20-pin dual-in-line package
- High output drive

Connection and Logic Diagrams

Dual-In-Line Package

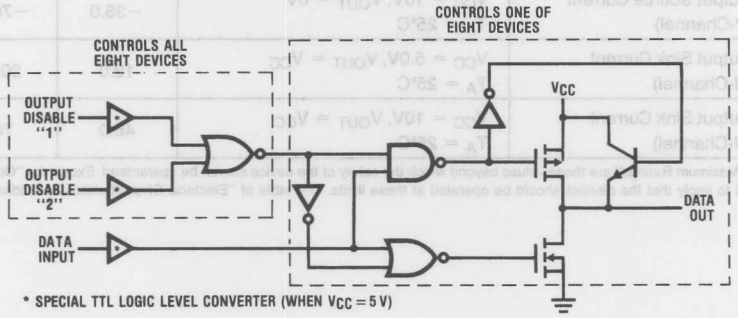


TL/F/5923–1

Top View

Order Number MM54C941* or MM74C941*

*Please look into Section 8, Appendix D for availability of various package types.



TL/F/5923–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin 0.3V to V_{CC} + 0.3V

Operating Temperature Range (T_A)
- MM54C941 −55°C to +125°C
- MM74C941 −40°C to +85°C

Storage Temperature Range (T_S) −65°C to +150°C

Power Dissipation (P_D)
- Dual-In-Line 700 mW
- Small Outline 500 mW

Operating V_{CC} Range 3V to 15V

V_{CC} 18V

Lead Temperature (T_L)
(Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	2.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			0.8 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA V_{CC} = 10V, I_O = 10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 15V, V_{OUT} = 0V or 15V			±10	μA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−2.5 V_{CC}−2.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −450 μA 74C, V_{CC} = 4.75V, I_O = −450 μA 54C, V_{CC} = 4.5V, I_O = −2.2 mA 74C, V_{CC} = 4.75V, I_O = −2.2 mA	V_{CC}−0.4 V_{CC}−0.4 2.4 2.4			V V V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 2.2 mA 74C, V_{CC} = 4.75V, I_O = 2.2 mA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−14.0	−30.0		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−36.0	−70.0		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	12.0	20.0		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	48.0	70		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}, t_{pd0}	Propagation Delay (Data IN to OUT)	$V_{CC} = 5.0V$, $C_L = 50$ pF		70	140	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		35	70	ns
		$V_{CC} = 5.0V$, $C_L = 150$ pF		90	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		45	90	ns
t_{1H}, t_{OH}	Propagation Delay Output Disable to Logic Level (from High Impedance State) (from a Logic Level)	$R_L = 1$ kΩ, $C_L = 50$ pF				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 210V$		55	110	ns
t_{H1}, t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1$ kΩ, $C_L = 50$ pF				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 10V$		55	110	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0V$, $C_L = 50$ pF		50	100	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		30	60	ns
		$V_{CC} = 5.0V$, $C_L = 150$ pF		80	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		50	100	ns
C_{PD}	Power Dissipation Capacitance	(Note 3)				
	(Output Enabled per Buffer)			100		pF
	(Output Disabled per Buffer)			10		pF
C_{IN}	Input Capacitance (Any Input)	(Note 2) $V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$		10		pF
C_O	(Output Capacitance) (Output Disabled)	$V_{IN} = 0V$, f = 1 MHz, $T_A = 25°C$		10		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics Application Note, AN-90.

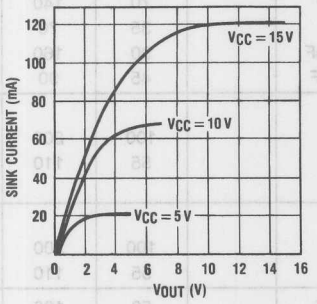
Truth Table

OD1	OD2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	Z
1	0	X	Z
1	1	X	Z

1 = High
0 = Low
X = Don't Care
Z = TRI-STATE

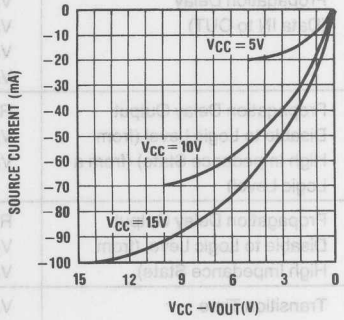
Typical Performance Characteristics

N-Channel Output Drive @ 25°C



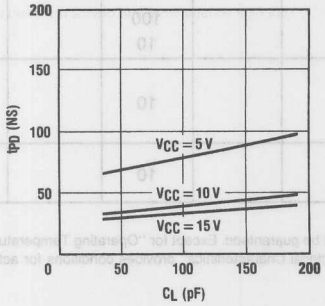
TL/F/5923–3

P-Channel Output Drive @ 25°C



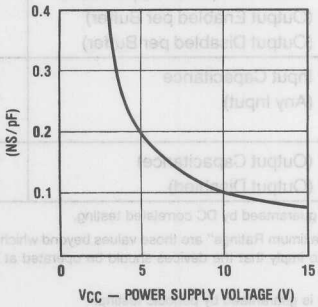
TL/F/5923–4

Propagation Delay vs Load Capacitance



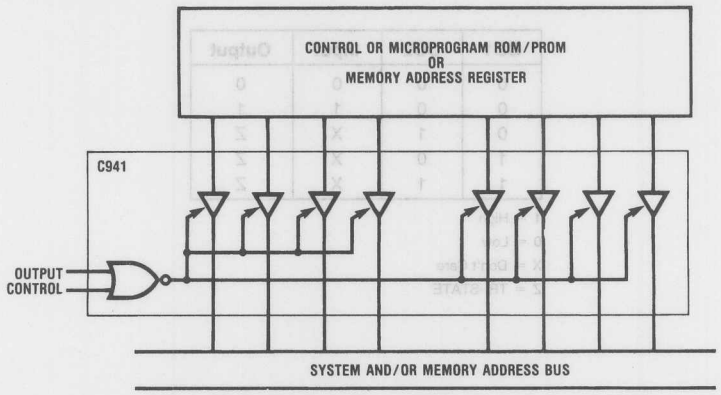
TL/F/5923–5

Δt_{PD} per pF of Load Capacitance

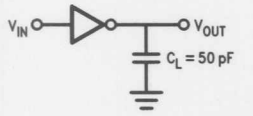


TL/F/5923–6

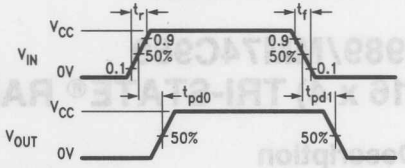
Typical Application



TL/F/5923–7

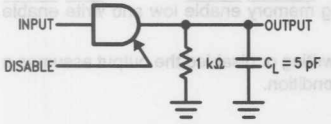


TL/F/5923–8

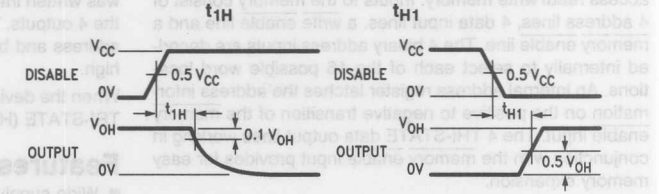


TL/F/5923–9

t_{1H} and t_{H1}



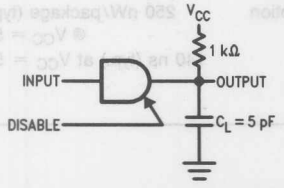
TL/F/5923–10



TL/F/5923–11

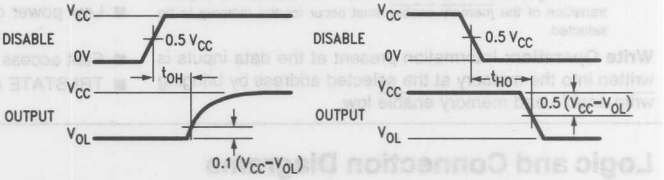
Note: V_{OH} is defined as the DC output high voltage when the device is loaded with a 1 kΩ resistor to ground.

t_{0H} and t_{H0}



TL/F/5923–12

Note: Delays measured with input t_r, $t_f \leq 20$ ns.



TL/F/5923–13

Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a 1 kΩ resistor to V_{CC}.

National Semiconductor

MM54C989/MM74C989
64-Bit (16 x 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines. a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

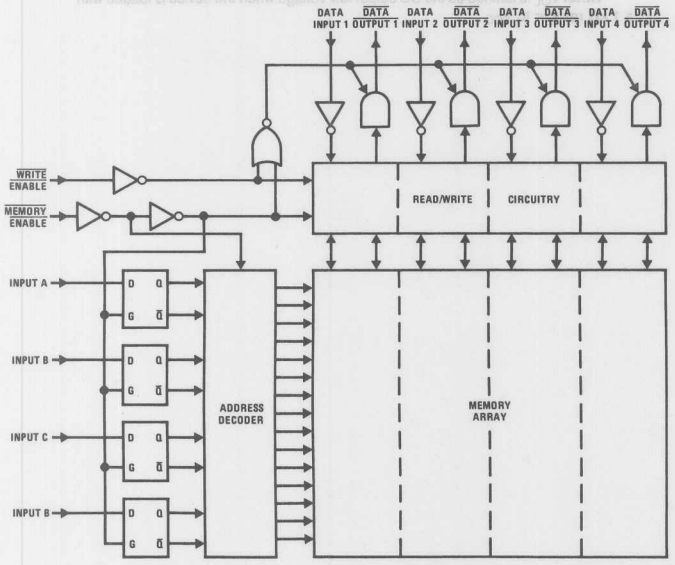
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-Z) condition.

Features

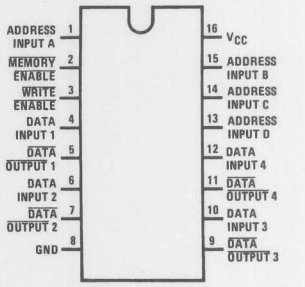
■ Wide supply voltage range	3.0V to 5.5V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	Fan out of 2 driving 74L
■ Input address register	
■ Low power consumption	250 nW/package (typ.) @ V_{CC} = 5V
■ Fast access time	140 ns (typ.) at V_{CC} = 5V
■ TRI-STATE output	

Logic and Connection Diagrams



TL/F/5925–1

Dual-In-Line Package



TL/F/5925–2

Top View

Order Number
MM54C989* or MM74C989*

*Please look into Section 8, Appendix D
*for availability of various package types.

National Semiconductor

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE Hex Inverters

General Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

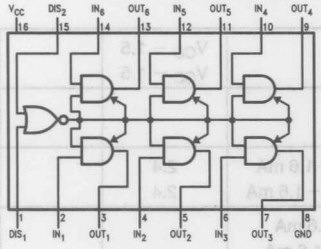
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatible	Drive 1 TTL Load

Applications

■ Bus drivers	Typical propagation delay into 150 pF load is 40 ns

Connection Diagrams (Dual-In-Line Packages)

MM70C95/MM80C95

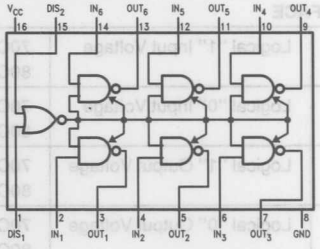


TL/F/5907–1

Top View

Order Number MM70C95* or MM80C95*

MM70C96/MM80C96

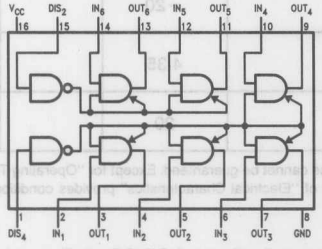


TL/F/5907–2

Top View

Order Number MM70C96* or MM80C96*

MM70C97/MM80C97

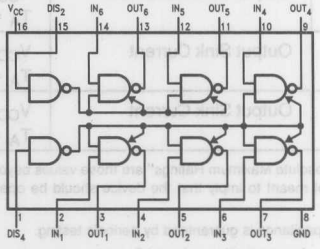


TL/F/5907–3

Top View

Order Number MM70C97* or MM80C97*

MM70C98/MM80C98



TL/F/5907–4

Top View

Order Number MM70C98* or MM80C98*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin −0.3V to V_{CC} + 0.3V

Operating Temperature Range

MM70CXX −55°C to +125°C

MM80CXX −40°C to +85°C

Storage Temperature Range −65°C to +150°C

Power Dissipation (P_D)

Dual-In-Line 700 mW

Small Outline 500 mW

Power Supply Voltage (V_{CC}) 18V

Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V V_{CC} = 10V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V V_{CC} = 10V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V V_{CC} = 10V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V V_{CC} = 10V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V V_{CC} = 15V, V_O = 0V	−1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	V_{CC} = 15V		0.01	15	μA
TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	70C V_{CC} = 4.5V 80C V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	70C V_{CC} = 4.5V 80C V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	70C V_{CC} = 4.5V, I_O = −1.6 mA 80C V_{CC} = 4.75V, I_O = −1.6 mA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	70C V_{CC} = 4.5V, I_O = 1.6 mA 80C V_{CC} = 4.75V, I_O = 1.6 mA			0.4 0.4	V V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, $V_{IN(1)}$ = 5V T_A = 25°C, V_{OUT} = 0V	−4.35			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = 0V	−20			mA
I_{SINK}	Output Sink Current	V_{CC} = 5V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = V_{CC}	4.35			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = V_{CC}	20			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$		60	100	ns
		$V_{CC} = 10V$		25	40	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$		70	150	ns
		$V_{CC} = 10V$		35	75	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$, $C_L = 150$ pF		85	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	80	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$, $C_L = 150$ pF		95	210	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		45	110	ns
t_{1H}, t_{0H}	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0")	$R_L = 10k$, $C_L = 5$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		80	135	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		100	180	ns
		$V_{CC} = 10V$		70	125	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		70	125	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		90	170	ns
		$V_{CC} = 10V$		70	125	ns
t_{H1}, t_{H0}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		130	225	ns
		$V_{CC} = 10V$		60	110	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		95	175	ns
		$V_{CC} = 10V$		40	80	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance TRI-STATE	Any Output (Note 2)		11		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

*AC Parameters are guaranteed by DC correlated testing.

Truth Tables

MM70C95/MM80C95

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

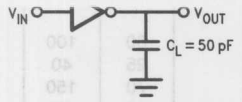
MM70C97/MM80C97

Disable DIS_4	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

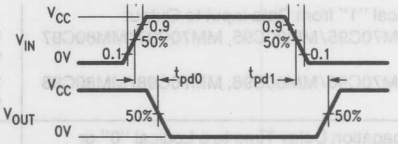
MM70C98/MM80C98

Disable DIS_4	Input DIS_2	Input	Output
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

*Output 5–6 only
**Output 1–4 only
X = Irrelevant

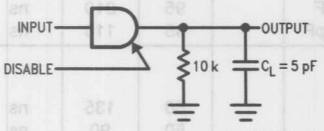


TL/F/5907–13



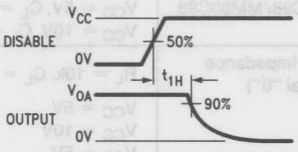
TL/F/5907–14

t_{1H} and t_{H1}



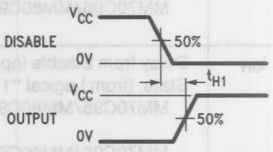
TL/F/5907–15

t_{1H}



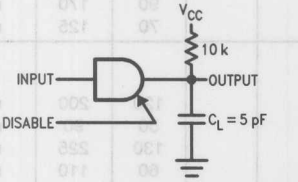
TL/F/5907–16

t_{H1}



TL/F/5907–17

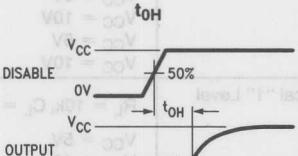
t_{0H} and t_{H0}



TL/F/5907–18

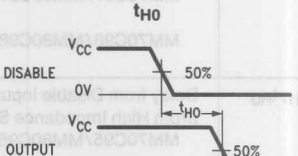
Note: Delays measured with input t_r, $t_f \leq 20$ ns.

t_{0H}

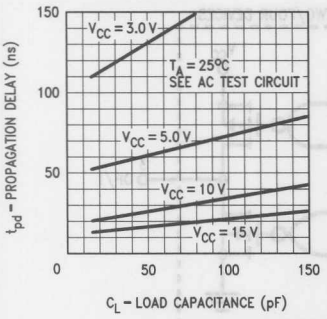


TL/F/5907–19

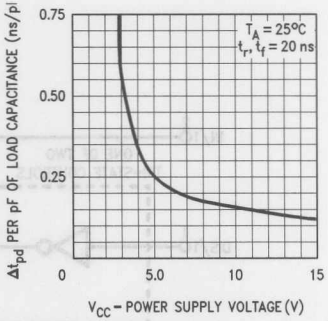
t_{H0}



TL/F/5907–20

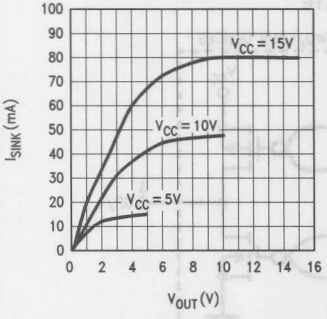


TL/F/5907–5



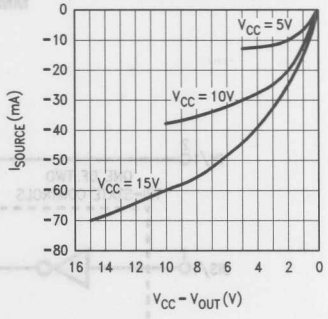
TL/F/5907–6

N-Channel Output Drive at 25°C



TL/F/5907–7

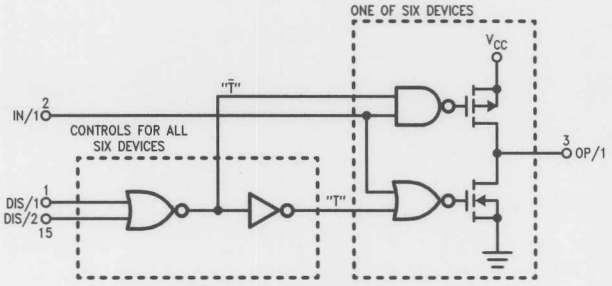
P-Channel Output Drive at 25°C



TL/F/5907–8

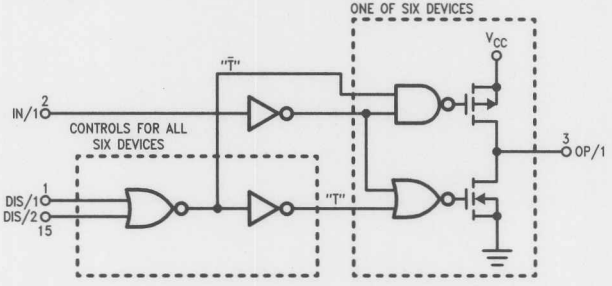
Schematic Diagrams

MM70C95/MM80C95 TRI-STATE



TL/F/5907–9

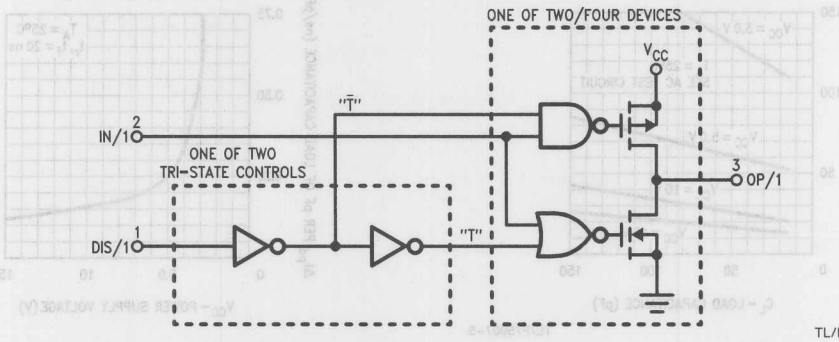
MM70C96/MM80C96 TRI-STATE



TL/F/5907–10

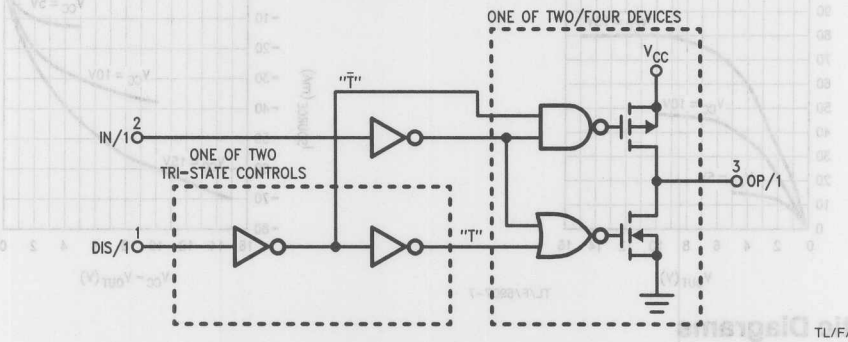
Schematic Diagrams (Continued)

MM70C97/MM80C97 TRI-STATE



TL/F/5907–11

MM70C98/MM80C98 TRI-STATE



TL/F/5907–12

National Semiconductor

MM74C908/MM74C918 Dual CMOS 30V Relay Driver

General Description

The MM74C908 and MM74C918 are general purpose dual high voltage drivers, each capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_J = 65°C$.

The MM74C908 and MM74C918 consist of two CMOS NAND gates driving an emitter follower Darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of −30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

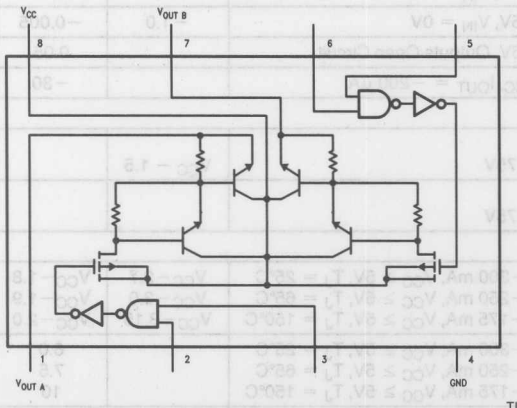
Features

■ Wide supply voltage range	3V to 18V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low output "ON" resistance	8Ω (typ.)
■ High voltage	−30V
■ High current	250 mA

Connection Diagrams

Dual-In-Line Package

MM74C908



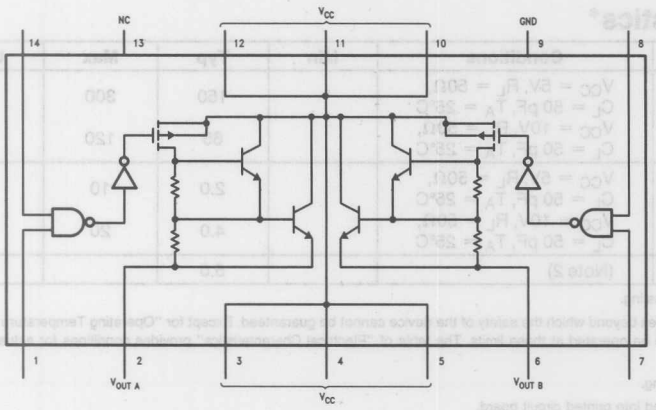
TL/F/5912–1

Top View

Order Number MM74C908*

Dual-In-Line Package

MM74C918



TL/F/5912–2

Top View

Order Number MM74C918*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Input Pin	$-0.3V$ to $V_{CC}+0.3V$
Voltage at any Output Pin	32V
Operating Temperature Range MM74C908/MM74C918	$-40°C$ to $+85°C$
Operating V_{CC} Range	4V to 18V
Absolute Maximum V_{CC}	19V
I_{SOURCE}	500 mA
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
Power Dissipation (P_D)	Refer to Maximum Power Dissipation vs Ambient Temperature Graph

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5V$ $V_{CC}=10V$			1.5 2.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V, V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V, V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$, Outputs Open Circuit		0.05	15	μA
	Output "OFF" Voltage	$V_{IN}=V_{CC}, I_{OUT}=-200\ \mu A$		-30		V
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage MM74C908/MM74C918	$V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage MM74C908/MM74C918	$V_{CC}=4.75V$			0.8	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage	$I_{OUT}=-300$ mA, $V_{CC}\geq 5V$, $T_J=25°C$ $I_{OUT}=-250$ mA, $V_{CC}\geq 5V$, $T_J=65°C$ $I_{OUT}=-175$ mA, $V_{CC}\geq 5V$, $T_J=150°C$	$V_{CC}-2.7$ $V_{CC}-3.0$ $V_{CC}-3.15$	$V_{CC}-1.8$ $V_{CC}-1.9$ $V_{CC}-2.0$		V V V
R_{ON}	Output Resistance	$I_{OUT}=-300$ mA, $V_{CC}\geq 5V$, $T_J=25°C$ $I_{OUT}=-250$ mA, $V_{CC}\geq 5V$, $T_J=65°C$ $I_{OUT}=-175$ mA, $V_{CC}\geq 5V$, $T_J=150°C$		6.0 7.5 10	9.0 12 18	Ω Ω Ω
	Output Resistance Coefficient			0.55	0.80	%/°C
θ_{JA}	Thermal Resistance MM74C908/MM74C918	(Note 3) (Note 3)		100 45	110 55	°C/W °C/W

AC Electrical Characteristics*

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logical "1"	$V_{CC}=5V, R_L=50\Omega$, $C_L=50$ pF, $T_A=25°C$		150	300	ns
		$V_{CC}=10V, R_L=50\Omega$, $C_L=50$ pF, $T_A=25°C$		65	120	ns
t_{pd0}	Propagation Delay to a Logic "0"	$V_{CC}=5V, R_L=50\Omega$, $C_L=50$ pF, $T_A=25°C$		2.0	10	μs
		$V_{CC}=10V, R_L=50\Omega$, $C_L=50$ pF, $T_A=25°C$		4.0	20	μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: θ_{JA} measured in free air with device soldered into printed circuit board.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$		60	100	ns
		$V_{CC} = 10V$		25	40	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$		70	150	ns
		$V_{CC} = 10V$		35	75	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$, $C_L = 150$ pF		85	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	80	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$, $C_L = 150$ pF		95	210	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		45	110	ns
t_{1H}, t_{0H}	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0")	$R_L = 10k$, $C_L = 5$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		80	135	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		100	180	ns
		$V_{CC} = 10V$		70	125	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		70	125	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		90	170	ns
		$V_{CC} = 10V$		70	125	ns
t_{1H}, t_{0H}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$R_L = 10k$, $C_L = 5$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		130	225	ns
		$V_{CC} = 10V$		60	110	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		95	175	ns
		$V_{CC} = 10V$		40	80	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance TRI-STATE®	Any Output (Note 2)		11		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

*AC Parameters are guaranteed by DC correlated testing.

Truth Tables

MM70C95/MM80C95

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

Disable DIS_1	Input DIS_2	Input	Output
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

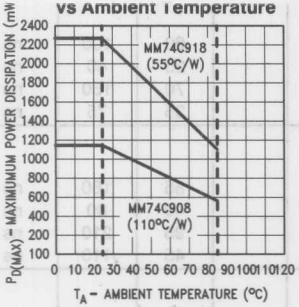
Disable DIS_4	Input DIS_2	Input	Output
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

MM70C98/MM80C98

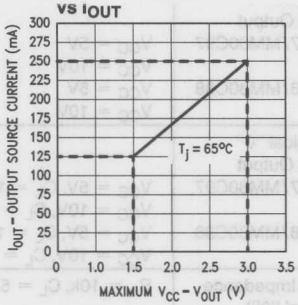
Disable DIS_4	Input DIS_2	Input	Output
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

*Output 5–6 only
**Output 1–4 only
X = Irrelevant

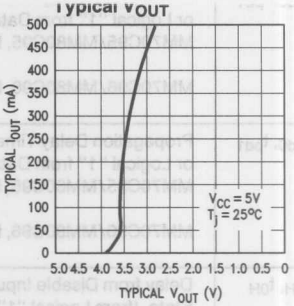
vs Ambient Temperature



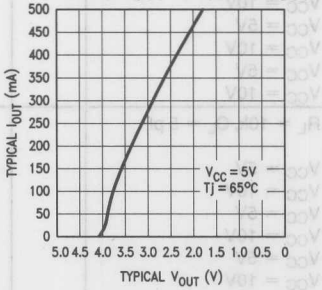
vs I_{OUT}



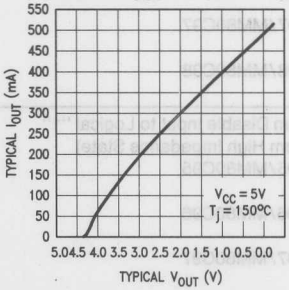
Typical V_{OUT}



Typical I_{OUT} vs Typical V_{OUT}

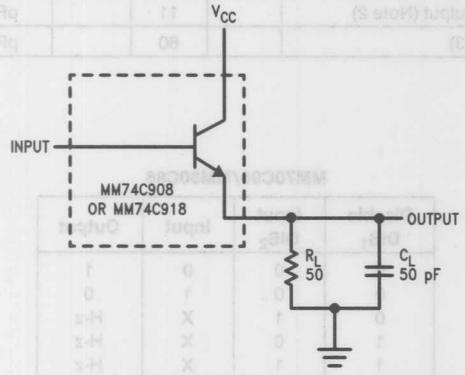


Typical I_{OUT} vs Typical V_{OUT}



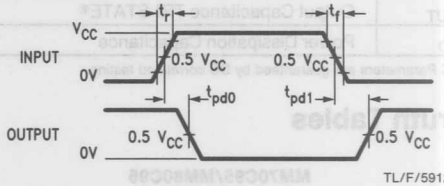
TL/F/5912–3

AC Test Circuit



TL/F/5912–4

Switching Time Waveforms



TL/F/5912–5

$t_r = t_f = 20$ ns

Power Considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_J, and is given by:

$$R_{ON} = 9\,(T_J - 25)\,(0.008) + 9 \quad (1)$$

and T_J is given by:

$$T_J = T_A + P_{DAV}\,\theta_{JA}, \quad (2)$$

where T_A = ambient temperature, θ_{JA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B. P_D is given by:

$$P_D = I_{OA}^2\,R_{ON} + I_{OB}^2\,R_{ON}, \quad (3)$$

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L} \quad (4)$$

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$$P_{DAV} = I_{OA}^2\,R_{ON}\,(\text{Duty Cycle}_A) + I_{OB}^2\,R_{ON}\,(\text{Duty Cycle}_B) \quad (5)$$

where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

$$T_J = T_A + \theta_{JA}\,[9\,(T_J - 25)\,(0.008) + 9]\,[I_{OA}^2\,(\text{Duty Cycle}_A) + I_{OB}^2\,(\text{Duty Cycle}_B)] \quad (6a)$$

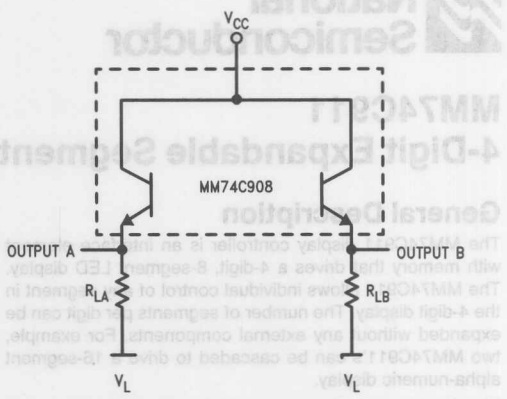
simplifying:

$$T_J = \frac{T_A + 7.2\,\theta_{JA}\,[I_{OA}^2\,(\text{Duty Cycle}_A) + I_{OB}^2\,(\text{Duty Cycle}_B)]}{1 - 0.072\,\theta_{JA}\,[I_{OA}^2\,(\text{Duty Cycle}_A) + I_{OB}^2\,(\text{Duty Cycle}_B)]}$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.

Applications

(See AN-177 for applications)



TL/F/5912–6

For example, let $V_{CC} = 15V$, $R_{LA} = 100\Omega$, $R_{LB} = 100\Omega$, $V_L = 0V$, $T_A = 25°C$, $\theta_{JA} = 110°C/W$, Duty Cycle$_A$ = 50%, Duty Cycle$_B$ = 75%.

Assuming $R_{ON} = 11\Omega$, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\text{ mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\text{ mA}$$

and

$$T_J = \frac{T_A + 7.2\,\theta_{JA}\,[I_{OA}^2\,(\text{Duty Cycle}_A) + I_{OB}^2\,(\text{Duty Cycle}_B)]}{1 - 0.072\,\theta_{JA}\,[I_{OA}^2\,(\text{Duty Cycle}_A) + I_{OB}^2\,(\text{Duty Cycle}_B)]}$$

$$T_J = \frac{25 + (7.2)\,(110)\,[(0.1351)^2\,(0.5) + (0.1351)^2\,(0.75)]}{1 - (0.072)\,(110)\,[(0.1351)^2\,(0.5) + (0.1351)^2\,(0.75)]}$$

$$T_J = 52.6°C$$

and $R_{ON} = 9\,(T_J - 25)\,(0.008) + 9$

$= 9(52.6 - 25)\,(0.008) + 9 = 11\Omega$

National Semiconductor

MM74C911
4-Digit Expandable Segment Display Controller

General Description

The MM74C911 display controller is an interface element with memory that drives a 4-digit, 8-segment LED display. The MM74C911 allows individual control of any segment in the 4-digit display. The number of segments per digit can be expanded without any external components. For example, two MM74C911's can be cascaded to drive a 16-segment alpha-numeric display.

The display controllers receive data information through 8 data lines a, b . . . DP, and digit information through 2 address inputs K1 and K2. The input data is written into the register selected by the address information when CHIP ENABLE, $\overline{CE}$, and WRITE ENABLE, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required.

A self-contained internal oscillator sequentially presents the stored data to high drive (100 mA typ.) TRI-STATE® output drivers which directly drive the LED display. The drivers are active when the control pin labeled SEGMENT OUTPUT ENABLE, $\overline{SOE}$, is low and go into TRI-STATE when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control, or for disabling the output drive for power conservation.

The digit outputs directly drive the base of the digit transistor when the control pin labeled DIGIT INPUT OUTPUT, $\overline{DIO}$, is low. When $\overline{DIO}$ is high, the digit lines turn into inputs and the internal scanning multiplexer is disabled.

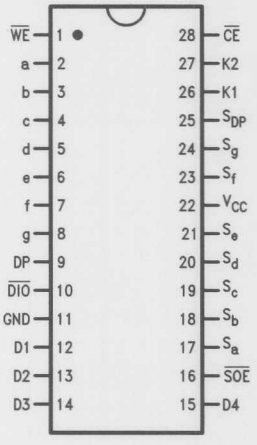
When any digit line is forced high by an external device, usually another MM74C911, the data information for that digit is presented to the output. In this manner, 16-segment alpha-numeric displays, 24- or 32-segment displays, or an array of discrete LED's can be controlled by the simple cascading of expandable segment display controllers. All inputs except digit inputs are TTL compatible and do not clamp input voltages above V_{CC}.

Features

- Direct segment drive (100 mA typ.) TRI-STATE
- 4 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor
- Segment expandability without external components
- TTL compatible inputs
- Power saver mode—5 μW (typ.)

Connection Diagram

Dual-In-Line Package



TL/F/5915–1

Top View

Order Number MM74C911*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

Input Control

$\overline{CE}$	Digit Address		$\overline{WE}$	Operation
	K2	K1		
0	0	0	0	Write Digit 1
0	0	0	1	Latch Digit 1
0	0	1	0	Write Digit 2
0	0	1	1	Latch Digit 2
0	1	0	0	Write Digit 3
0	1	0	1	Latch Digit 3
0	1	1	0	Write Digit 4
0	1	1	1	Latch Digit 4
1	X	X	X	Disable Writing

Output Control

$\overline{DIO}$	$\overline{SOE}$	Digit Lines				Operation
		D4	D3	D2	D1	
0	0	R	R	R	R	Refresh Display
0	1	R	R	R	R	Disable Segment Outputs
1	0	0	0	0	0	Digits Are Now Inputs
1	0	0	0	0	1	Display Digit 1
1	0	0	0	1	0	Display Digit 2
1	0	0	1	0	0	Display Digit 3
1	0	1	0	0	0	Display Digit 4
1	1	0	0	0	0	Power Saver Mode

R = Refresh (digit lines sequentially pulsed)

X = Don't Care

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin except Inputs	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Any Input except Digits	$-0.3V$ to $+15V$
Operating Temperature Range, (T_A)	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Power Dissipation (P_D)	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply at $-40°C \le T_J \le +85°C$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V, V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V, V_{IN} = 0V$	−1.0	−0.005		μA
I_{CC}	Supply Current (Normal)	$V_{CC} = 5V$, Outputs Open		0.50	2.5	mA
I_{CC}	Supply Current (Power Saver)	$V_{CC} = 5V$, $\overline{SOE}$, $\overline{DIO}$ = "1", D1, D2, D3, D4 = "0"		1	600	μA
I_{OUT}	TRI-STATE Output Current	$V_O = 5V$ $V_O = 0V$	 −10	0.03 −0.03	10	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} - 2$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	$V_{CC} = 5V, V_O = 3.4V$ $T_J = 25°C$ $T_J = 100°C$	 −60 −40	 −100 −60		 mA mA
I_{DH}	High Level Digit Current	$V_{CC} = 5V, V_O = 3V$ $T_J = 25°C$ $T_J = 100°C$ $V_{CC} = 5V, V_O = 1V$ $T_J = 25°C$ $T_J = 100°C$	 −10 −7 −15 −10	 −20 −10 −40 −15		 mA mA mA mA
$V_{OUT(1)}$	Logical "1" Output Voltage, Any Digit	$V_{CC} = 5V, I_O = -360\ \mu A$	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage, Any Output	$V_{CC} = 5V, I_O = 360\ \mu A$			0.4	V
θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltage reference to ground.

Note 3: θ_{JA} measured in free-air with device soldered into printed circuit board.

AC Electrical Characteristics* $V_{CC} = 5V, t_r = t_f = 20$ ns, $C_L = 50$ pF

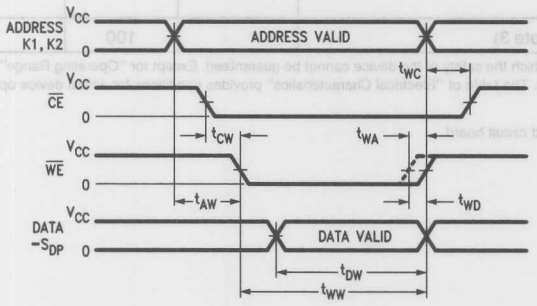
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CW}	Chip Enable to Write Enable Set-Up Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{AW}	Address to Write Enable Set-Up Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{WW}	Write Enable Width	$T_J = 25°C$	400	225		ns
		$T_J = 125°C$	450	250		ns
t_{DW}	Data to Write Enable Set-Up Time	$T_J = 25°C$	390	225		ns
		$T_J = 125°C$	430	250		ns
t_{WD}	Write Enable to Data Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	$T_J = 25°C$	55	30		ns
		$T_J = 125°C$	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels into TRI-STATE	$R_L = 10k, C_L = 10$ pF				
		$T_J = 25°C$		275	500	ns
		$T_J = 125°C$		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" or	$R_L = 10k, C_L = 10$ pF				
	Logical "0" Levels	$T_J = 25°C$		325	600	ns
		$T_J = 125°C$		375	700	ns
t_{D1}, t_{D0}	Propagation Delay from Digit Input to	$T_J = 25°C$		500	1000	ns
	Segment Output	$T_J = 125°C$		700	1400	ns
t_{IB}	Interdigit Blanking Time	$T_J = 25°C$	5	10		μs
		$T_J = 125°C$	10	20		μs
f_{MUX}	Multiplex Scan Frequency	$T_J = 25°C$		525		Hz
		$T_J = 125°C$		375		Hz
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		30	50	pF

*AC Parameters are guaranteed by DC correlated testing.

Note 4: Capacitance guaranteed by periodic testing.

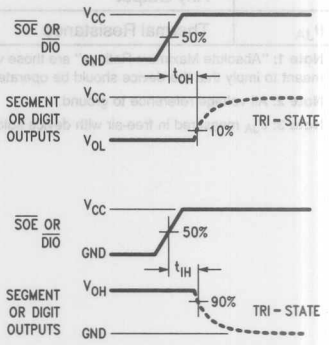
Switching Time Waveforms

Write Data Waveforms



TL/F/5915–2

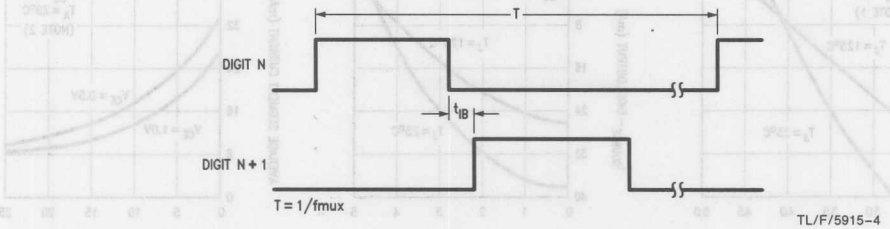
TRI-STATE Waveforms



TL/F/5915–3

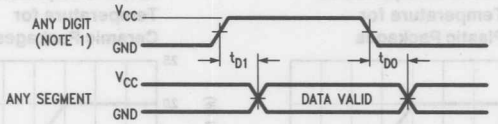
Switching Time Waveforms (Continued)

Multiplexing Output Waveforms



TL/F/5915–4

Read Data Waveforms



TL/F/5915–5

Note 1: All other digit lines are at a low level. $\overline{DIO}$ at a high level.

Functional Description

The MM74C911 display controller is manufactured on standard metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin to suppress current transients.

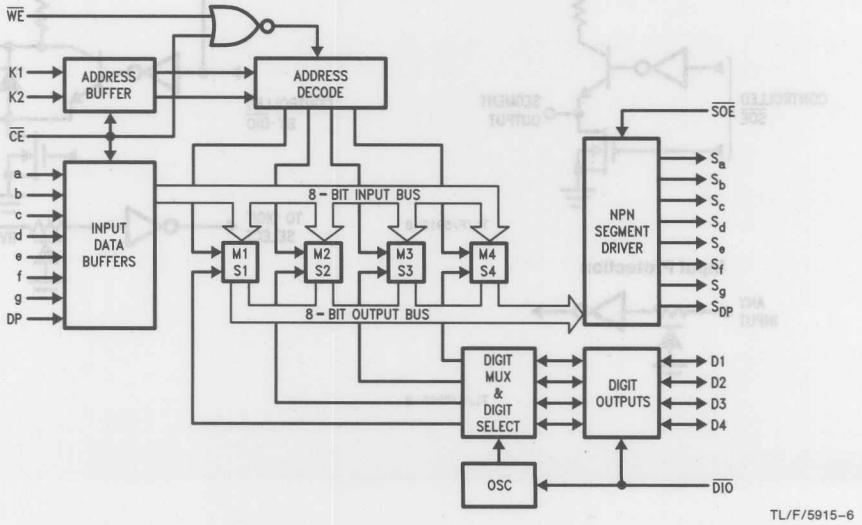
The digit outputs directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration. If an MM74C911 is driving a digit transistor and also supplying digit information to a cascaded MM74C911, base resistors are needed in the digit transistors to provide an adequate high level to the digit inputs of the cascaded MM74C911.

As seen in the block diagram, these display controllers contain four 8-bit registers; any one may be randomly written into. In normal operation, the internal multiplexer scans the registers and refreshes the display. In cascaded operation, 1 MM74C911 serves as a master refresh device and cascaded MM74C911's are slaved to it through digit lines operating as inputs.

The MM74C911 appears to a microprocessor as memory and to the user as a self-scan display. Since every segment is under microprocessor control, great versatility is obtained.

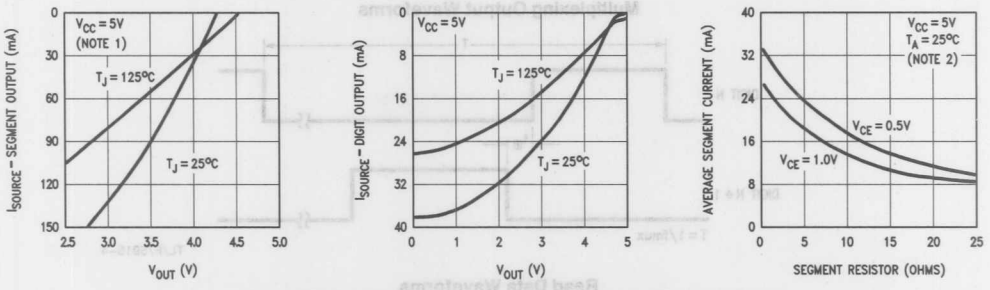
Low power standby operation occurs with both $\overline{SOE}$ and $\overline{DIO}$ inputs high. This condition forces the MM74C911 to a quiescent state typically drawing less than 1 μA of supply current with a standby supply voltage as low as 3V.

Block Diagram

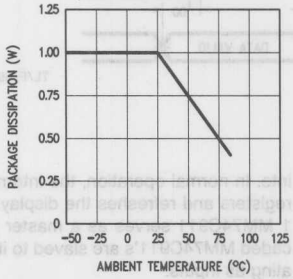


TL/F/5915–6

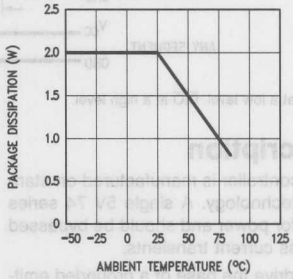
Typical Performance Characteristics



Power Dissipation vs Temperature for Plastic Packages



Power Dissipation vs Temperature for Ceramic Packages



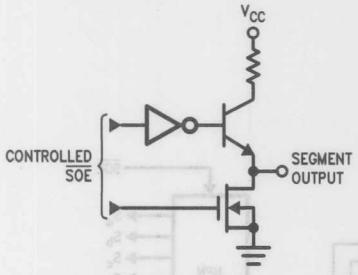
TL/F/5915–7

Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

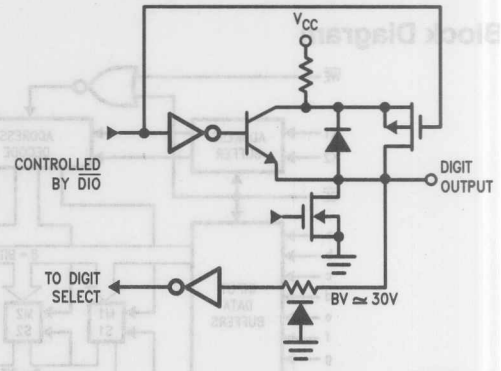
Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

Applications

Segment Output Structure

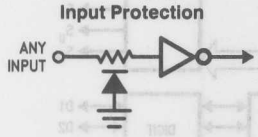


Digit Output Structure



TL/F/5915–10

Input Protection

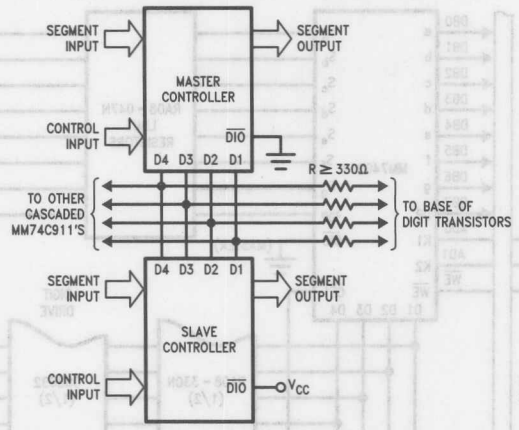


TL/F/5915–8

TL/F/5915–9

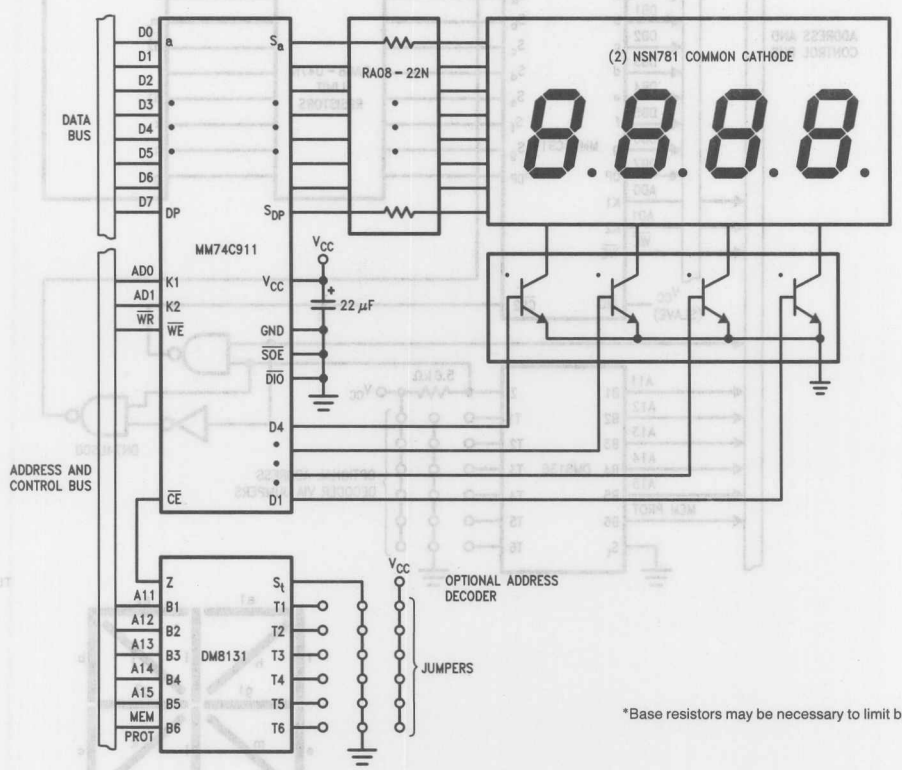
Applications (Continued)

Segment Expansion



TL/F/5915–11

Typical Application

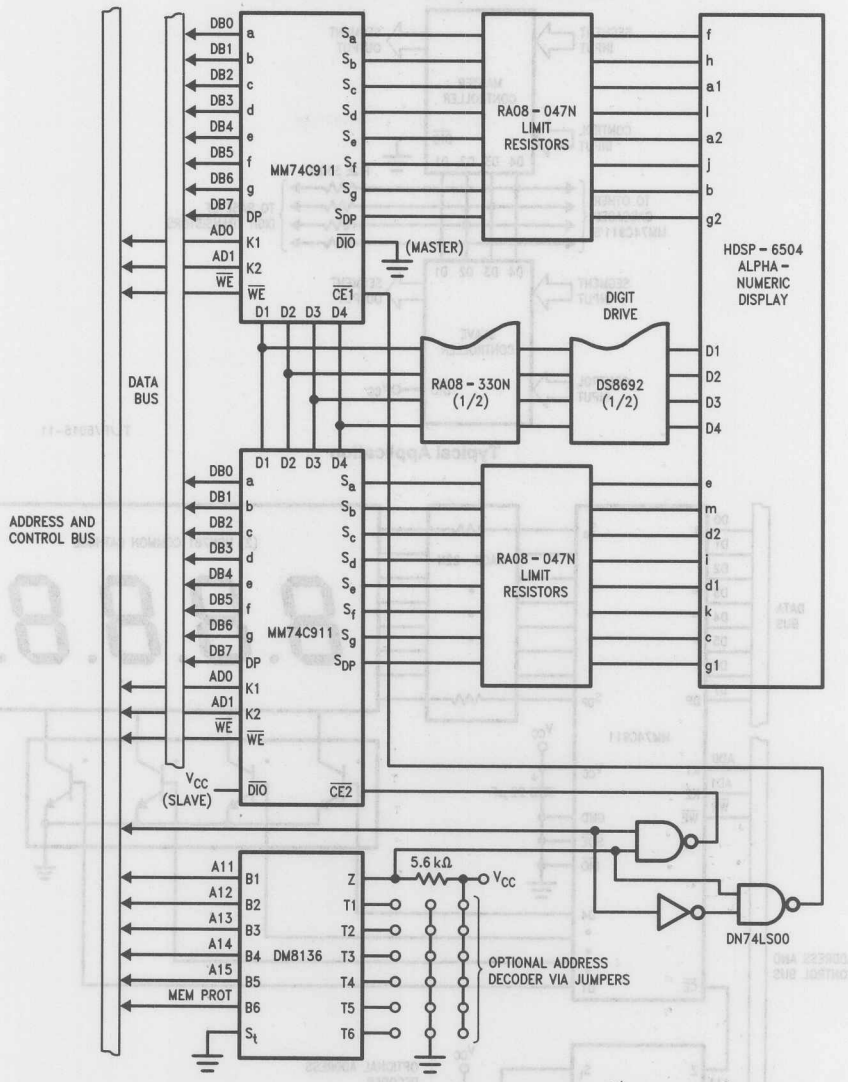


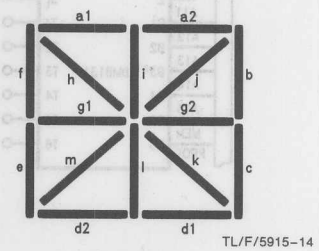
*Base resistors may be necessary to limit base current.

TL/F/5915–12

Applications (Continued)

4-Digit, 16-Segment Alpha-Numeric Display





TL/F/5915–14

Segment Identification

National Semiconductor

MM74C912 6-Digit BCD Display Controller/Driver
MM74C917 6-Digit Hex Display Controller/Driver

General Description

The MM74C912, MM74C917 display controllers are interface elements, with memory, that drive a 6-digit, 8-segment LED display.

The display controllers receive data information through 5 data inputs A, B, C, D and DP, and digit information through 3 address inputs K1, K2 and K3.

The input data is written into the register selected by the address information when CHIP ENABLE, $\overline{CE}$, and WRITE ENABLE, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required. A self-contained internal oscillator sequentially presents the stored data to a decoder where 4 data bits control the format of the displayed character and 1 bit controls the decimal point. The internal oscillator is controlled by a control input labeled OSCILLATOR ENABLE, $\overline{OSE}$, which is tied low in normal operation. A high level at $\overline{OSE}$ prevents automatic refresh of the display.

The 7-segment plus decimal point output information directly drives an LED display through high drive (100 mA typ.) output drivers. The drivers are active when the control pin labeled SEGMENT OUTPUT ENABLE, $\overline{SOE}$, is low and go into TRI-STATE® when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control and for disabling the output drivers for power conservation.

The MM74C912 segment decoder converts BCD data into 7-segment format. The MM74C917 converts binary data into hex format.

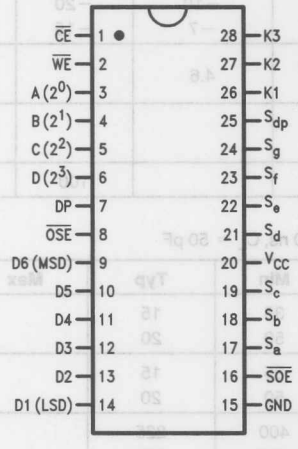
All inputs are TTL compatible and do not clamp to the V_{CC} supply.

Features

- Direct segment drive (100 mA typ.) TRI-STATE
- 6 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor (20 mA typ.)
- Internal segment decoder
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5916–1

Top View

Order Number MM74C912* or MM74C917*

*Please look into Section 8, Appendix D for availability of various package types.

Truth Tables

Input Control

$\overline{CE}$	Digit Address			$\overline{WE}$	Operation
	K3	K2	K1		
0	0	0	0	0	Write Digit 1
0	0	0	0	1	Latch Digit 1
0	0	0	1	0	Write Digit 2
0	0	0	1	1	Latch Digit 2
0	0	1	0	0	Write Digit 3
0	0	1	0	1	Latch Digit 3
0	0	1	1	0	Write Digit 4
0	0	1	1	1	Latch Digit 4
0	1	0	0	0	Write Digit 5
0	1	0	0	1	Latch Digit 5
0	1	0	1	0	Write Digit 6
0	1	0	1	1	Latch Digit 6
0	1	1	0	0	Write Null Digit
0	1	1	0	1	Latch Null Digit
0	1	1	1	0	Write Null Digit
0	1	1	1	1	Latch Null Digit
1	X	X	X	X	Disable Writing

X = Don't Care

Output Control

$\overline{SOE}$	$\overline{OSE}$	Operation
0	0	Refresh Display
0	1	Stop Oscillator*
1	0	Disable Segment Outputs
1	1	Standby Mode

*Segment drive may exceed maximum display dissipation.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin Except Inputs	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Any Input	$-0.3V$ to $+15V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	Refer to $P_{D\,MAX}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
Absolute Maximum (V_{CC})	6.5V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply at $40°C \le T_J \le 85°C$, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 5V$, Outputs Open		0.5	2	mA
I_{OUT}	TRI-STATE Output Current	$V_{CC} = 5V$, $V_O = 5V$ $V_{CC} = 5V$, $V_O = 0V$	 -10	0.03 -0.03	10	μA μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC} - 2.0$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	$V_{CC} = 5V$, $V_O = 3.4V$ $T_J = 25°C$ $T_J = 100°C$	 -60 -40	 -100 -60		 mA mA
I_{DH}	High Level Digit Current	$V_{CC} = 5V$, $V_O = 1V$ $T_J = 25°C$ $T_J = 100°C$	 -10 -7	 -20 -15		 mA mA
$V_{OUT(1)}$	Logical "1" Output Voltage Any Digit	$V_{CC} = 5V$, $I_O = -360\mu A$	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage Any Digit	$V_{CC} = 5V$, $I_O = 360\mu A$			0.4	V
θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

AC Electrical Characteristics* $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{CW}	Chip Enable to Write Enable Setup Time	$T_J = 25°C$ $T_J = 125°C$	35 50	15 20		ns ns
t_{AW}	Address to Write Enable Setup Time	$T_J = 25°C$ $T_J = 125°C$	35 50	15 20		ns ns
t_{WW}	Write Enable Width	$T_J = 25°C$ $T_J = 125°C$	400 450	225 250		ns ns
t_{DW}	Data to Write Enable Setup Time	$T_J = 25°C$ $T_J = 125°C$	390 430	225 250		ns ns
t_{WD}	Write Enable to Data Hold Time	$T_J = 25°C$ $T_J = 125°C$	0 0	-10 -15		ns ns

	Hold Time	$T_J = 125°C$	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	$T_J = 25°C$ $T_J = 125°C$	50 75	30 40		ns ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels into TRI-STATE	$R_L = 10k$, $T_J = 25°C$ $C_L = 10$ pF, $T_J = 125°C$		275 325	500 600	ns ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" to Logical "0" Level	$R_L = 10k$, $T_J = 25°C$ $C_L = 50$ pF, $T_J = 125°C$		325 375	600 700	ns ns
t_{IB}	Interdigit Blanking Time	$T_J = 25°C$ $T_J = 125°C$	5 10	10 20		μs μs
f_{MUX}	Multiplex Scan Frequency	$T_J = 25°C$ $T_J = 125°C$		350 250		Hz Hz
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		30	50	pF

*AC Parameters are guaranteed by DC correlated testing.

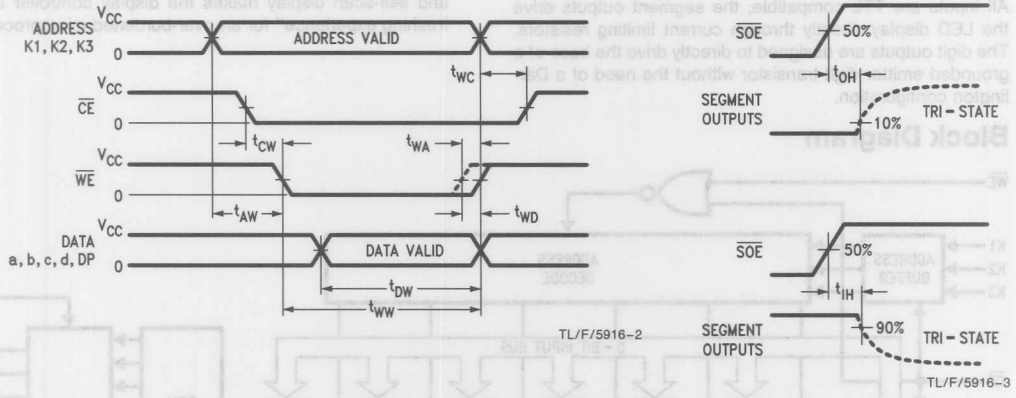
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages reference to ground.

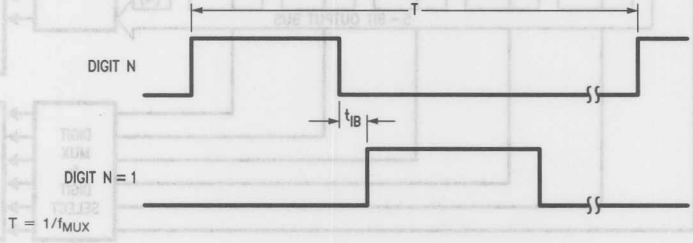
Note 3: θ_{JA} measured in free air with device soldered into printed circuit board.

Note 4: Capacitance is guaranteed by periodic testing.

Switching Time Waveforms



Multiplexing Output Waveforms



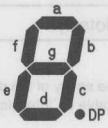
Functional Description

Character Font

		0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	F.
MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	R	b	C	d	E	F	F.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	o	°	-	-	_		.
Input A 2^0	X	0	1	0	1	0	0	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	1	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
OUTPUT ENABLE $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TL/F/5916–5

Segment Identification



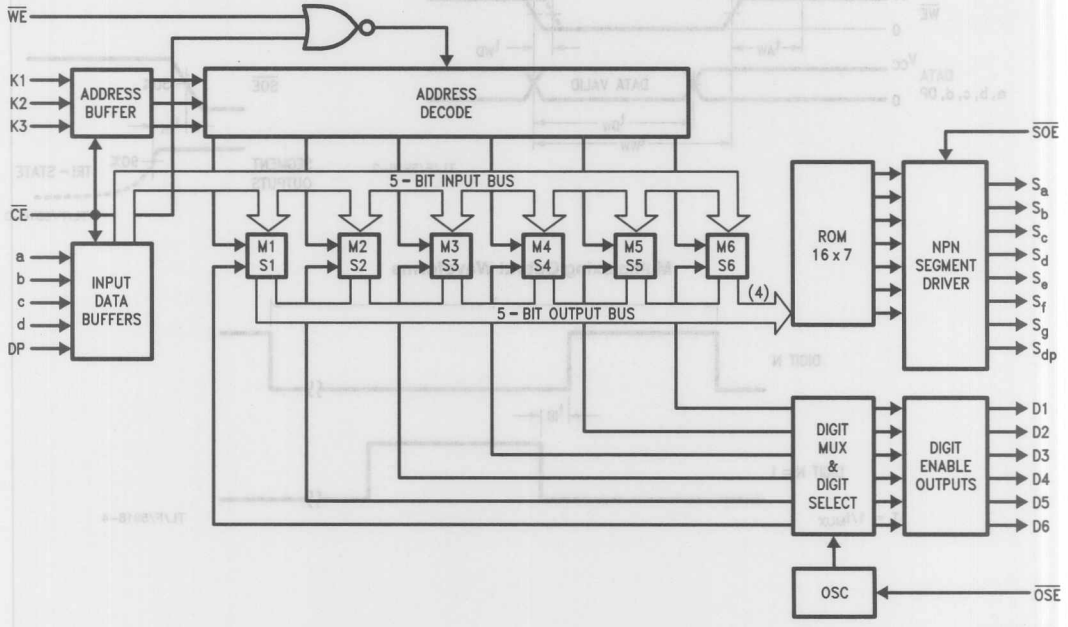
TL/F/5916–6

The MM74C912, MM74C917 display controllers are manufactured using metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin.

All inputs are TTL compatible; the segment outputs drive the LED display directly through current limiting resistors. The digit outputs are designed to directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration.

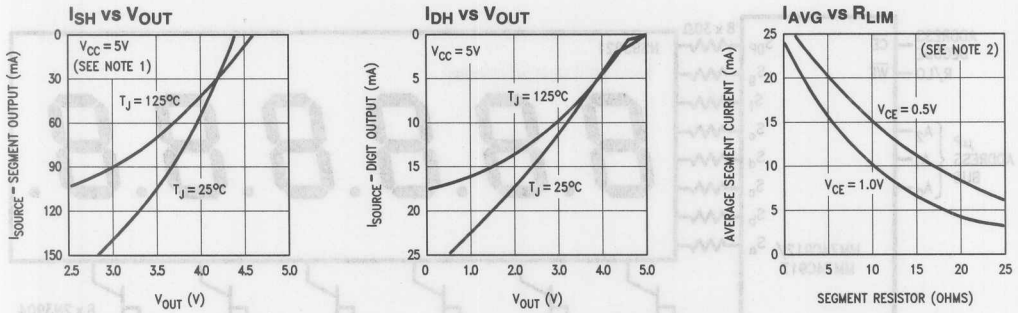
As seen in the block diagram, these display controllers contain six 5-bit registers; any one of which may be randomly written. The internal multiplexer scans the registers and refreshes the display. This combination of write only memory and self-scan display makes the display controller a "refreshing experience" for an over-burdened microprocessor.

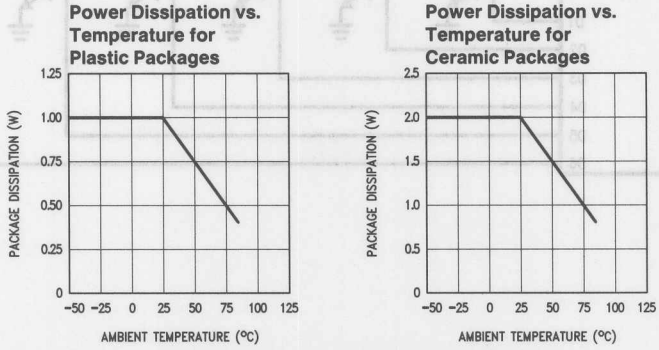
Block Diagram



TL/F/5916–7

Typical Performance Characteristics





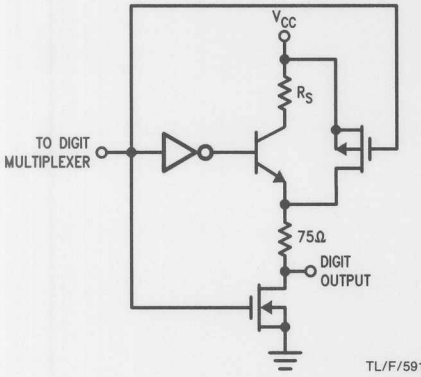
TL/F/5916–8

Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

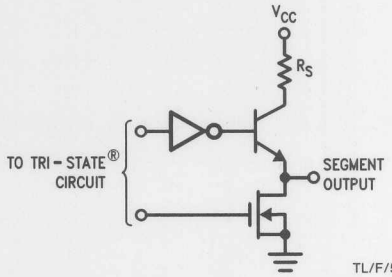
Typical Applications

Digit Output Structure



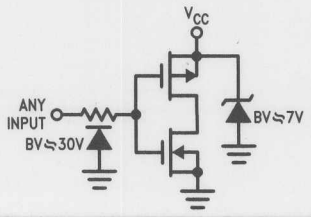
TL/F/5916–9

Segment Output Structure



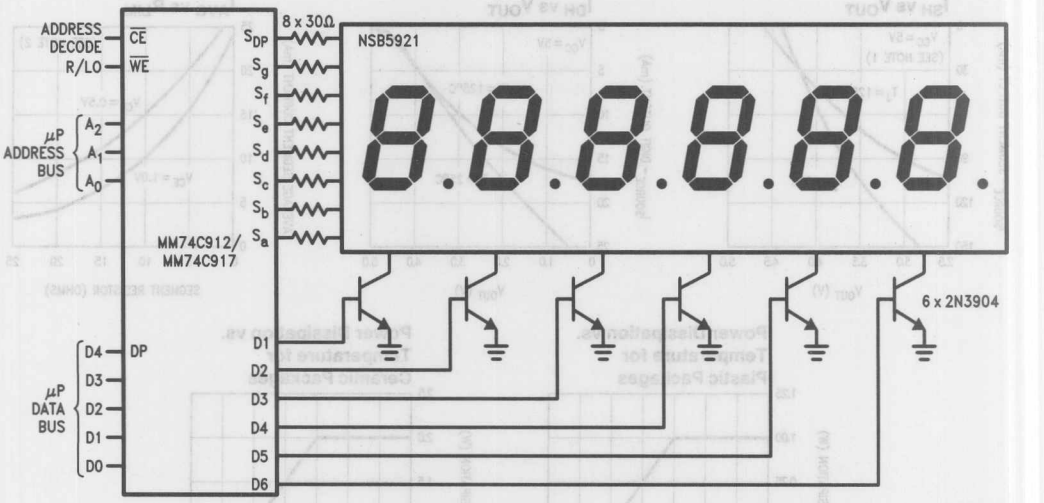
TL/F/5916–10

Input Protection



TL/F/5916–11

Typical Application



TL/F/5916–12

National Semiconductor

MM74C925, MM74C926, MM74C927, MM74C928 4-Digit Counters with Multiplexed 7-Segment Output Drivers

General Description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a $3\frac{1}{2}$-digit counter.

Features

- Wide supply voltage range — 3V to 6V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} (typ.)
- High segment sourcing current — 40 mA @ $V_{CC} - 1.6V$, $V_{CC} = 5V$
- Internal multiplexing circuitry

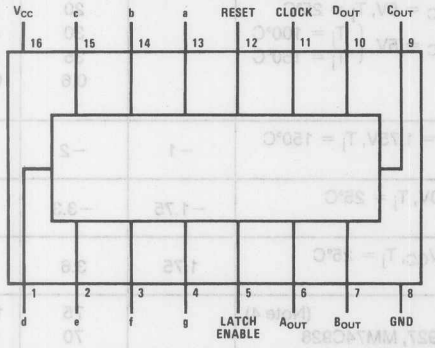
Design Considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DS75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

Connection Diagrams

Dual-In-Line Package

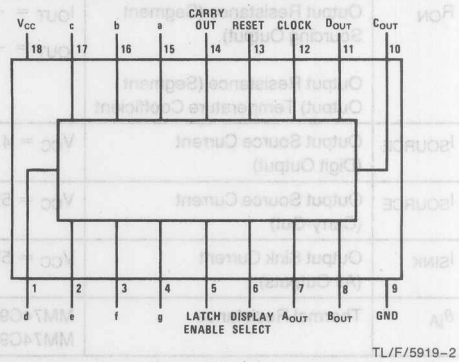


TL/F/5919–1

Top View

Order Number MM74C925*

Dual-In-Line Package



TL/F/5919–2

Top View

Order Number MM74C926*, MM74C927* or MM74C928*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Output Pin	GND − 0.3V to V_{CC} + 0.3V
Voltage at Any Input Pin	GND − 0.3V to +15V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply at −40°C ≤ T_j ≤ +85°C, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 5V, I_O = −10 μA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5V, V_{IN} = 15V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5V, V_{IN} = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 2			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C	V_{CC} − 2	V_{CC} − 1.3		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C	V_{CC} − 1.6	V_{CC} − 1.2		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C	V_{CC} − 2	V_{CC} − 1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		20	32	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C		30	40	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-Out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	−1.75	−3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{jA}	Thermal Resistance	MM74C925 (Note 4)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: θ_{jA} measured in free-air with device soldered into printed circuit board.

AC Electrical Characteristics* $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$,	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5V$				15	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	$V_{CC} = 5V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK, LE)}$	Clock to Latch Enable Set-Up Time	$V_{CC} = 5V$	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset Wait Time	$V_{CC} = 5V$	$T_j = 25°C$	0	−100		ns
			$T_j = 100°C$	0	−100		ns
$t_{SET(R, LE)}$	Reset to Latch Enable Set-Up Time	$V_{CC} = 5V$	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	$V_{CC} = 5V$			1000		Hz
C_{IN}	Input Capacitance	Any Input (Note 2)			5		pF

*AC Parameters are guaranteed by DC correlated testing.

Functional Description

Reset — Asynchronous, active high

Display Select — High, displays output of counter
Low, displays output of latch

Latch Enable — High, flow through condition
Low, latch condition

Clock — Negative edge sensitive

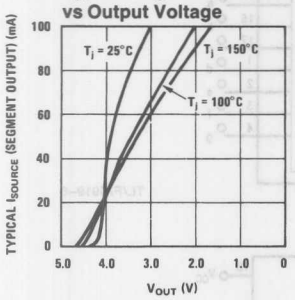
Segment Output — Current sourcing with 40 mA @$V_{OUT} = V_{CC} - 1.6V$ (typ.) Also, sink capability = 2 LTTL loads

Digit Output — Current sourcing with 1 mA @V_{OUT} = 1.75V. Also, sink capability = 2 LTTL loads

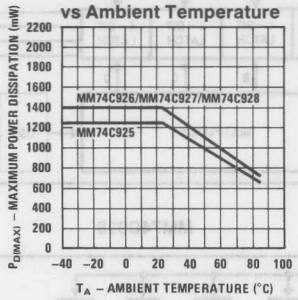
Carry-Out — 2 LTTL loads. See carry-out waveforms.

Typical Performance Characteristics

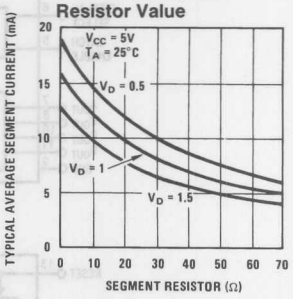
Typical Segment Current vs Output Voltage



Maximum Power Dissipation vs Ambient Temperature

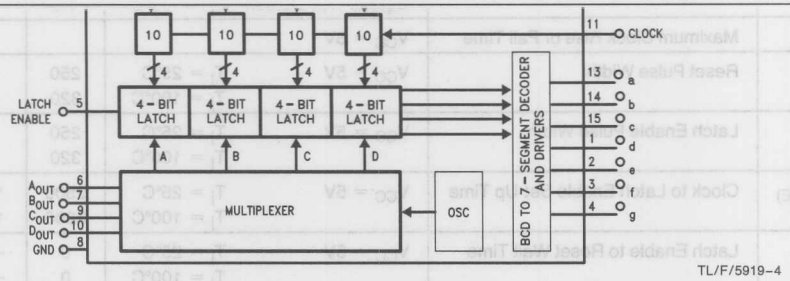


Typical Average Segment Current vs Segment Resistor Value



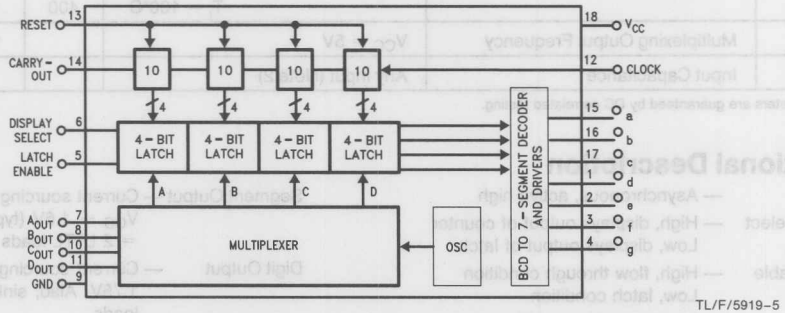
TL/F/5919–3

Note: V_D = Voltage across digit driver



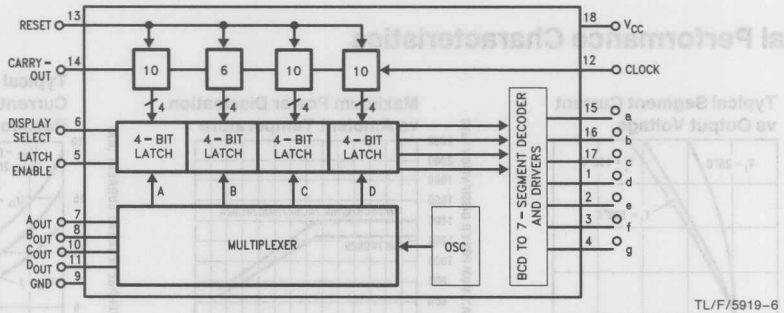
TL/F/5919–4

MM74C926



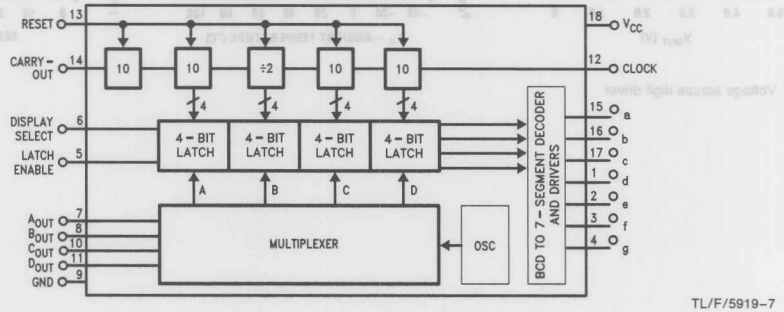
TL/F/5919–5

MM74C927



TL/F/5919–6

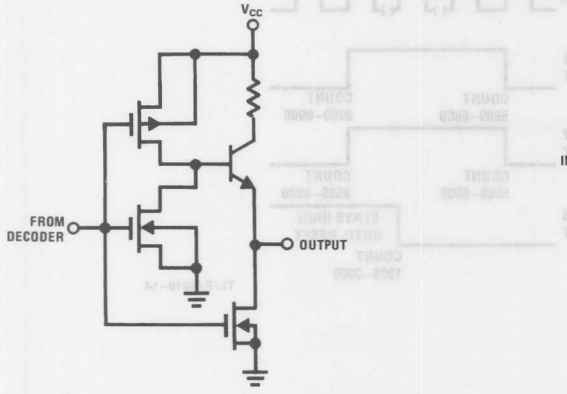
MM74C928



TL/F/5919–7

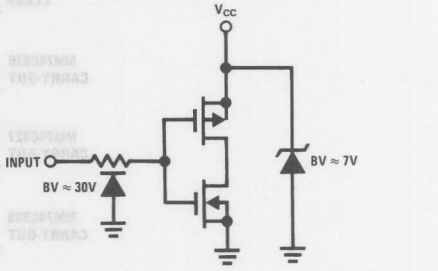
Logic and Block Diagrams (Continued)

Segment Output Driver



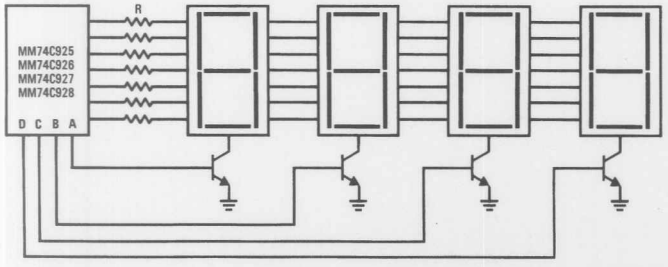
TL/F/5919–8

Input Protection



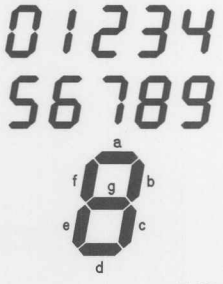
TL/F/5919–9

Common Cathode LED Display



TL/F/5919–10

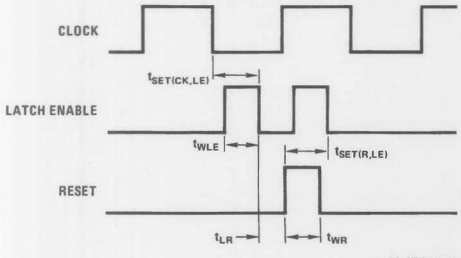
Segment Identification



TL/F/5919–11

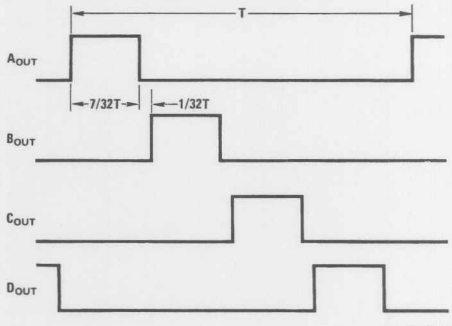
Switching Time Waveforms

Input Waveforms



TL/F/5919–12

Multiplexing Output Waveforms

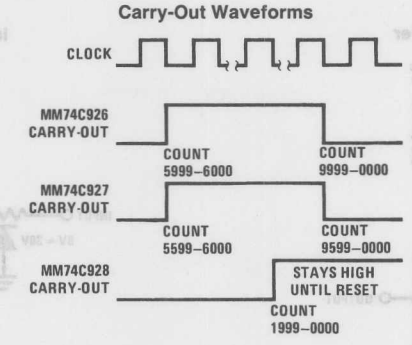


TL/F/5919–13

$T = 1/f_{MUX}$

Switching Time Waveforms (Continued)

Carry-Out Waveforms



TL/F/5919–14

National Semiconductor

PRELIMINARY

MM74C945, MM74C947 4-Digit Up/Down Counter/Latch/Decoder Driver

General Description

The MM74C945, MM74C947 are 4-digit counters for directly driving LCD displays. The MM74C945 contains a 4-decade up/down counter, output latches, counter/latch select multiplexer and 7-segment decoders. Also included are the backplane oscillator/driver, segment drivers and display blanking circuitry.

The MM74C947 differs from the MM74C945 in that it has no counter/latch multiplexer, but provides true leading zero blanking. All leading zeroes are automatically blanked except the least significant digit, which can be optionally blanked.

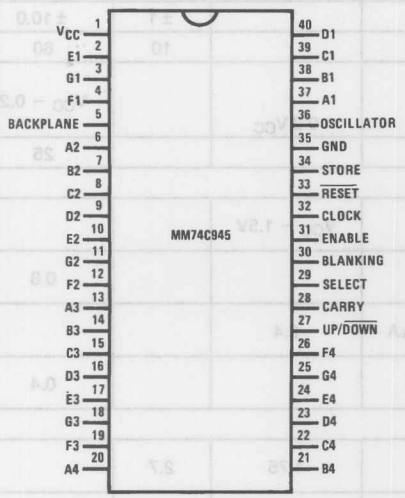
Both devices provide 28-segment outputs to drive a 4-digit display. Segment and backplane waveforms are generated internally, but can also be slaved to an external signal. This facilitates cascading of multiple displays.

Features

- 4-decade up/down count
- Direct 4-digit drive for high contrast and long display life
- Carry/borrow out for cascading counters
- Schmitt trigger clock input
- MM74C945 has display select to allow viewing of counter or latch
- Store and reset inputs allow operation as frequency or period counter
- MM74C947 has true ripple blanking; least significant digit may be optionally blanked

Connection Diagrams

Dual-In-Line Package

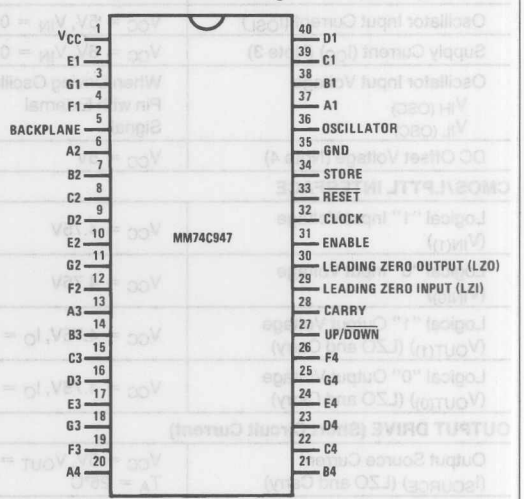


TL/F/5098–1

Top View

Order Number MM74C945*

Dual-In-Line Package



TL/F/5098–2

Top View

Order Number MM74C947*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	
MM74C945/MM74C947	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	500 mW
Operating V_{CC} Range	3.0V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Only)	$V_{CC} = 5V$, V_{IN} (0 ⟶ 5) V	2.5	2.9	3.25	V
V_{T-} Negative Going Threshold Voltage (Clock Only)	$V_{CC} = 5V$, V_{IN} (0 ⟶ 5) V	1.5	2.2	2.4	V
Hysteresis ($V_{T+} - V_{T-}$) (Clock Only)	$V_{CC} = 5V$	0.1	0.7	1.75	V
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 5V$, $I_O = +10\ \mu A$			0.5	V
Clock Input Current $\lvert I_{IN} \rvert$	$V_{CC} = 5V$, $V_{IN} = 5V/0V$		0.005	1.0	μA
Input Current @ Pins 29, 31, 33 and 34 (Note 2)	$V_{CC} = 5V$, $V_{IN} = 0V$	-2.0	-12	-25	μA
Oscillator Input Current (I_{OSL})	$V_{CC} = 5V$, $V_{IN} = 0V/5V$		± 1	± 10.0	μA
Supply Current (I_{CC}) (Note 3)	$V_{CC} = 5V$, $V_{IN} = 0V/5V$		10	60	μA
Oscillator Input Voltage $V_{IH\ (OSC)}$ $V_{IL\ (OSC)}$	When Driving Oscillator Pin with External Signal	 $0.2\ V_{CC}$		$V_{CC} - 0.2$	 V V
DC Offset Voltage (Note 4)	$V_{CC} = 5V$			25	mV
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 4.75V$	$V_{CC} - 1.5V$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V
OUTPUT DRIVE (Short Circuit Current)					
Output Source Current (I_{SOURCE}) (LZO and Carry)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	1.75	2.7		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	1.75	3.2		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	1.4	2.0		mA
Output Sink Current (I_{SINK}) (Segment Output)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	1.4	2.2		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	12.6	15.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	12.6	20.0		mA

AC Electrical Characteristics* $T_J = 25°C$, $C_L = 50$ pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry	$V_{CC} = 5.0V$		375	600	ns
f_{CLK}	Maximum Clock Frequency	$V_{CC} = 5.0V$	2	3		MHz
t_r, t_f	Clock Input Rise or Fall Time	$V_{CC} = 5.0V$			No Limit	MHz
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	180	120		ns
t_{WS}	Store Pulse Width	$V_{CC} = 5.0V$	150	80		ns
$t_{SU\ (CK, S)}$	Clock to Store Set-Up Time	$V_{CC} = 5.0V$	500	270		ns
t_{SR}	Store to Reset Wait Time	$V_{CC} = 5.0V$	280	170		ns
$t_{SU\ (E, CK)}$	Enable to Clock Set-Up Time	$V_{CC} = 5.0V$	140	80		ns
t_{RR}	Reset Removal	$V_{CC} = 5.0V$	50	0		ns
$t_{SU\ (U/D, CK)}$	Up/Down to Clock Set-Up Time	$V_{CC} = 5.0V$	300	190		ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating, $V_{CC} = 5.0V$		85		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 2)		5		pF
t_{rfs}	Segment Rise/Fall Time	$C_{load} = 200$ pF		0.5		μs
t_{rfb}	Backplane Rise/Fall time	$C_{load} = 5000$ pF		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating, $V_{CC} = 5.0V$		11		kHz

*AC Parameters are guaranteed by DC correlated testing.

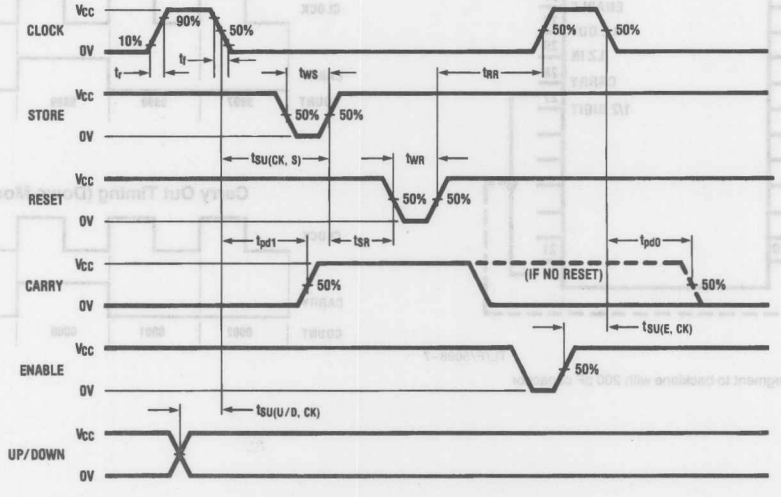
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Does not apply to backplane and oscillator pins.

Note 3: Display blanked. See Test Circuit.

Note 4: DC offset voltage is the effective DC voltage the LCD will have between any segment and the backplane.

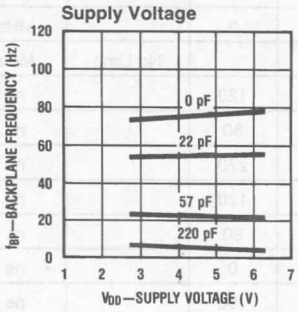
AC Waveforms



TL/F/5098–3

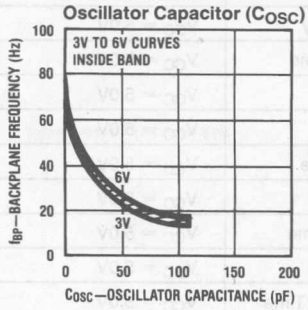
Typical Characteristics

Backplane Frequency as a Function of Supply Voltage



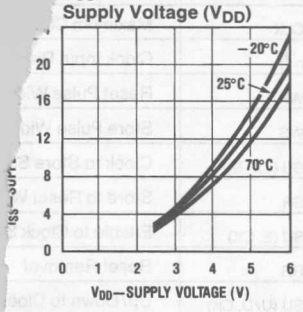
TL/F/5098–4

Backplane Frequency as a Function of Oscillator Capacitor (C_{OSC})



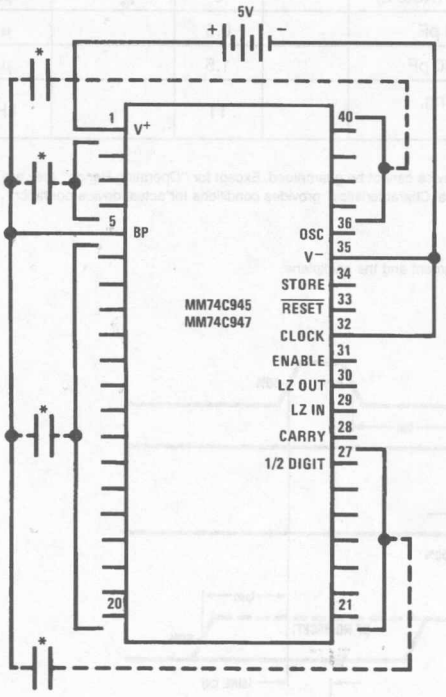
TL/F/5098–5

Operating Supply Current (I_{SS}) as a Function of Supply Voltage (V_{DD})



TL/F/5098–6

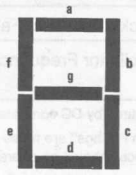
Test Circuit



TL/F/5098–7

*Each segment to backlane with 200 pF capacitor.

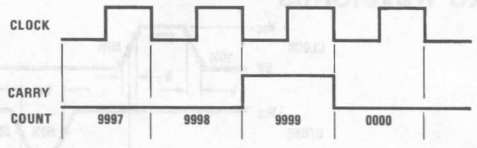
Segment Identification



TL/F/5098–8

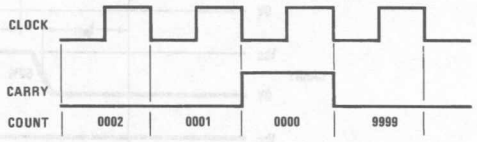
Timing Diagrams

Carry Out Timing (Up Mode)



TL/F/5098–9

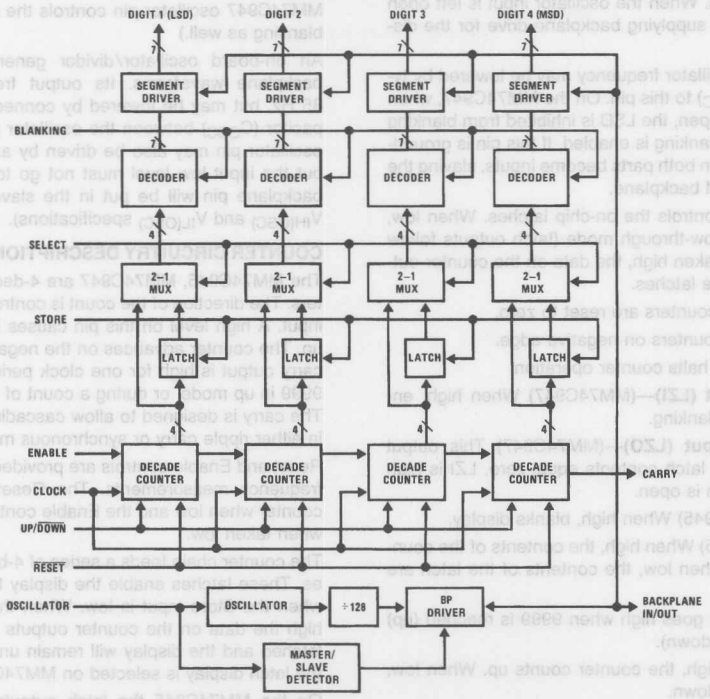
Carry Out Timing (Down Mode)



TL/F/5098–10

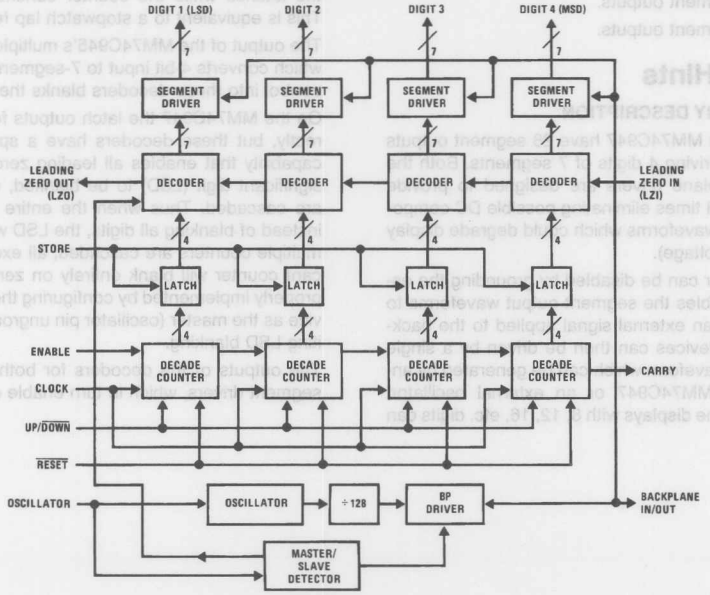
Block Diagrams

MM74C945



TL/F/5098–11

MM74C947



TL/F/5098–12

Pin Description

Backplane In/Out—When the oscillator input is grounded this pin is an input allowing an external device to generate a backplane waveform. When the oscillator input is left open this pin is an output supplying backplane drive for the display.

Oscillator—The oscillator frequency may be lowered by tying a capacitor (C_{OSC}) to this pin. On the MM74C947, when the oscillator pin is open, the LSD is inhibited from blanking when leading zero blanking is enabled. If this pin is grounded, the backplanes on both parts become inputs, slaving the device to an external backplane.

Store—This input controls the on-chip latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high, the data on the counter outputs are stored in the latches.

$\overline{\text{Reset}}$—When low, counters are reset to zero.

Clock—Advances counters on negative edge.

Enable—When low, halts counter operation.

Leading Zero Input (LZI)—(MM74C947) When high, enables leading zero blanking.

Leading Zero Output (LZO)—(MM74C947) This output goes high when the latch contents equal zero, LZI is high and the oscillator pin is open.

Blanking—(MM74C945) When high, blanks display.

Select—(MM74C945) When high, the contents of the counter are displayed. When low, the contents of the latch are displayed.

Carry—This outputs goes high when 9999 is reached (up) or 0000 is reached (down).

Up/$\overline{\text{Down}}$—When high, the counter counts up. When low, the counter counts down.

A1–G1—Digit 1 segment outputs.

A2–G2—Digit 2 segment outputs.

A3–G3—Digit 3 segment outputs.

A4–G4—Digit 4 segment outputs.

Application Hints

DISPLAY CIRCUITRY DESCRIPTION

The MM74C945 and MM74C947 have 28 segment outputs capable of directly driving 4 digits of 7 segments. Both the segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life (i.e., DC offset voltage).

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. Several devices can then be driven by a single master backplane waveform which can be generated by another MM74C945, MM74C947 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven with several counters. The maximum fanout of a master backplane driver is limited by its total capacitive load, which is the sum of the slaved backplane input capacitances and the display backplane capacitance. (The MM74C947 oscillator pin controls the least significant digit blanking as well.)

An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency is typically 85 Hz, but may be lowered by connecting an external capacitor (C_{OSC}) between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane pin will be put in the slave (input) mode (see $V_{IH(OSC)}$ and $V_{IL(OSC)}$ specifications).

COUNTER CIRCUITRY DESCRIPTION

The MM74C945, MM74C947 are 4-decade up/down counters. The direction of the count is controlled by the up/$\overline{\text{down}}$ input. A high level on this pin causes the counter to count up. The counter advances on the negative clock edge. The carry output is high for one clock period during a count of 9999 in up mode, or during a count of 0000 in down mode. The carry is designed to allow cascading of several circuits in either ripple carry or synchronous modes.

Reset and Enable controls are provided to allow period and frequency measurements. The Reset control clears the counter when low and the Enable control disables counting when taken low.

The counter chain feeds a series of 4-bit flow-through latches. These latches enable the display to follow the counter when the Store input is low. When the Store pin is taken high the data on the counter outputs at this time become latched and the display will remain unchanged. (Assuming the latch display is selected on MM74C945.)

On the MM74C945 the latch outputs feed a multiplexer which selects either the latch outputs or counter outputs for display. This allows an intermediate count to be stored in the latches while the counter continues to be displayed. This is equivalent to a stopwatch lap feature.

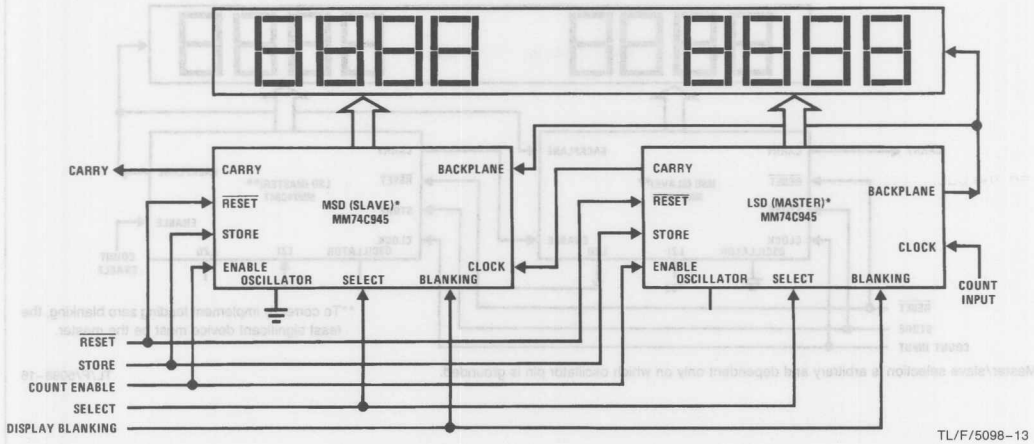
The output of the MM74C945's multiplexer feeds a decoder which converts 4-bit input to 7-segment outputs. A blanking control into these decoders blanks the display.

On the MM74C947 the latch outputs feed the decoders directly, but these decoders have a special ripple blanking capability that enables all leading zeroes except the least significant digit (LSD) to be blanked, even when counters are cascaded. Thus when the entire counter reads zero, instead of blanking all digits, the LSD will remain on. (When multiple counters are cascaded, all except the least significant counter will blank entirely on zeroes.) This feature is properly implemented by configuring the least significant device as the master (oscillator pin ungrounded) thereby inhibiting LSD blanking.

The outputs of the decoders for both devices control the segment drivers, which in turn enable display operation.

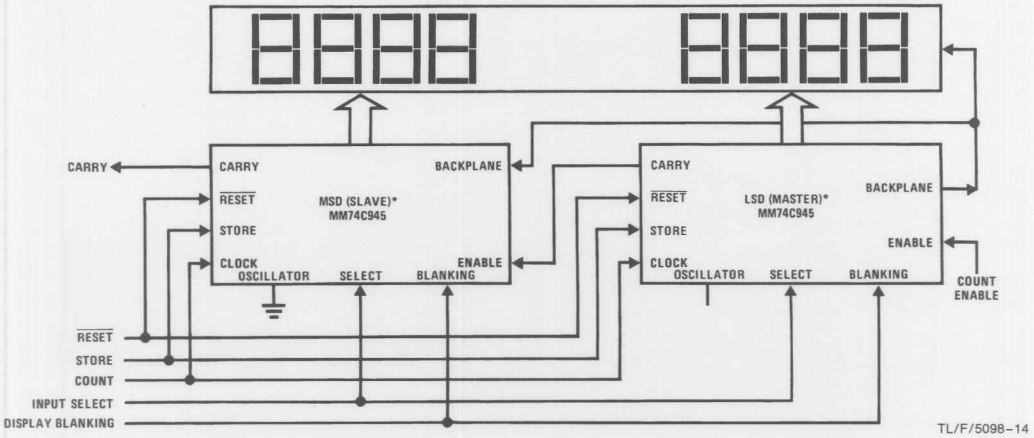
Typical Applications

Ripple Carry Cascading—MM74C945



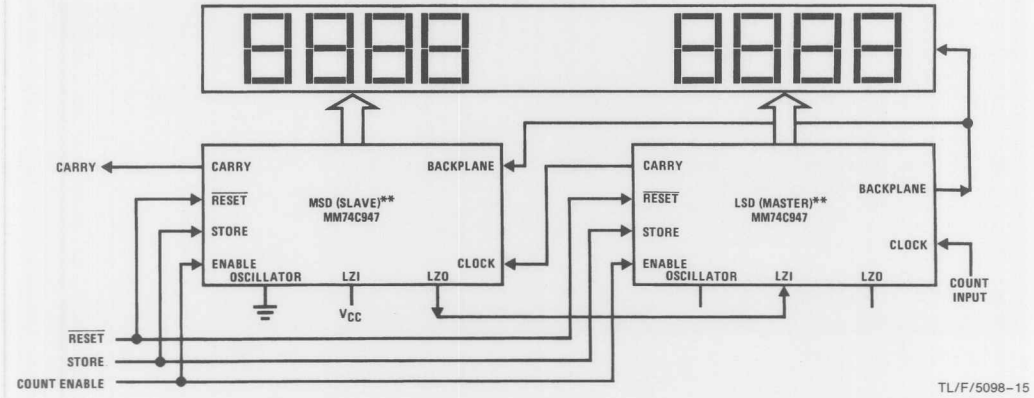
TL/F/5098–13

Synchronous Cascading—MM74C945



TL/F/5098–14

Ripple Cascading—MM74C947

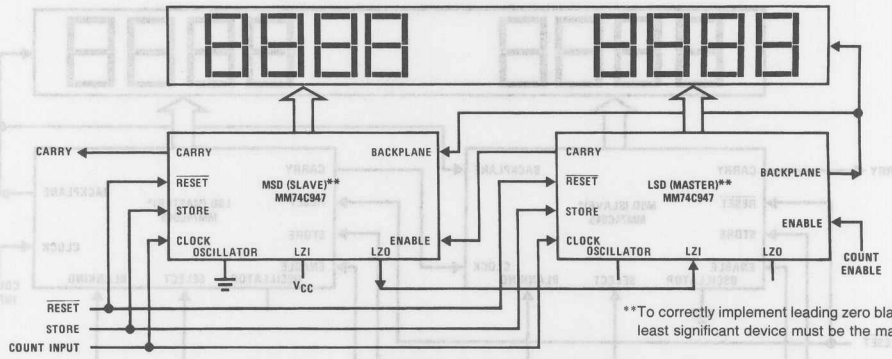


TL/F/5098–15

6

Typical Applications (Continued)

Synchronous Cascading—MM74C947



*Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.

**To correctly implement leading zero blanking, the least significant device must be the master.

TL/F/5098–16

National Semiconductor

PRELIMINARY

MM74C946
4½-Digit Counter/Decoder/Driver for LCD Displays

General Description

The MM74C946 is a 4½-digit CMOS counter which contains a counter chain, decoders, output latches, LCD segment drivers, count inhibit and backplane oscillator/driver circuitry. This device also contains leading zero blanking and a carry output to increase flexibility and facilitate cascading of multiple 4-digit sections.

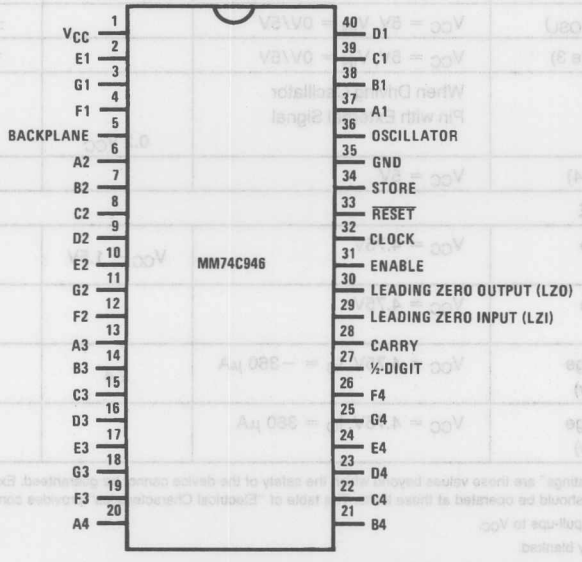
This device provides 29 segment outputs to drive a standard 4½-digit liquid crystal display. An on-chip backplane oscillator/driver is also provided. This can be disabled by grounding the oscillator pin, thus allowing the device to be slaved to an external backplane signal via the backplane pin.

Features

- Low power operation—less than 100 μW quiescent
- Direct 4½-digit 7-segment display drive for higher contrast and long display life
- Pin compatible to Intersil's ICM7224
- Store and $\overline{\text{RESET}}$ inputs permit operation as frequency or period counter
- True count inhibit disables first counter stage
- Carry output for cascading 4-digit blocks
- Schmitt trigger on the clock input allows operation in noisy environments or with slowly changing inputs
- Leading zero blanking input and output for correct leading zero blanking with cascaded devices
- On-chip backplane oscillator/driver which can be disabled to permit slaving of multiple devices to an external backplane signal

Connection Diagram

Dual-In-Line Package



TL/F/5102–1

Top View

Order Number MM74C946*

*Please look into Section 8, Appendix D for availability of various package types.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A) MM74C946	$-40°C$ to $+85°C$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	500 mW
Operating V_{CC} Range	3V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (T_L) (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/Max limits apply across temperature range, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Input)	$V_{CC} = 5V$, V_{IN} (0 → 5)V	2.5	2.9	3.25	V
V_{T-} Negative Going Threshold Voltage (Clock Input)	$V_{CC} = 5V$, V_{IN}(5 → 0)V	1.5	2.2	2.4	V
Hysteresis ($V_{T+} - V_{T-}$) (Clock Input)	$V_{CC} = 5V$	0.1	0.7	1.75	V
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 5V$, $I_O = -10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 5V$, $I_O = 10\ \mu A$			0.5	V
Clock Input Current $\lvert I_{IN} \rvert$	$V_{CC} = 5V$, $V_{IN} = 5V/0V$		0.005	1	μA
Input Current @ Pins 29, 31, 33 and 34 (Note 2)	$V_{CC} = 5V$, $V_{IN} = 0V$	-2	-12	-25	μA
Oscillator Input Current (I_{OSL})	$V_{CC} = 5V$, $V_{IN} = 0V/5V$		± 1	± 10	μA
Supply Current (I_{CC}) (Note 3)	$V_{CC} = 5V$, $V_{IN} = 0V/5V$		10	60	μA
Oscillator Input Voltage $V_{IH(OSC)}$ $V_{IL(OSC)}$	When Driving Oscillator Pin with External Signal	$0.2\ V_{CC}$		$V_{CC} - 0.2$	V V
DC Offset Voltage (Note 4)	$V_{CC} = 5V$			25	mV
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 4.75V$	$V_{CC} - 1.5V$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC} = 4.75V$, $I_O = -360\ \mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC} = 4.75V$, $I_O = 360\ \mu A$			0.4	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These input pins have pull-ups to V_{CC}.

Note 3: See test circuit. Display blanked.

Note 4: DC offset voltage is the effective DC voltage the LCD will have between any segment and the backplane.

DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted (Continued)

Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (Short Circuit Current)					
Output Source Current (I_{SOURCE}) (LZO and Carry)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	1.75	2.7		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	V_{CC} = 5V, V_{OUT} = 5V, T_A = 25°C	1.75	3.2		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	1.4	2		mA
Output Sink Current (I_{SINK}) (Segment Outputs)	V_{CC} = 5V, V_{OUT} = 5V, T_A = 25°C	1.4	2.2		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	12.6	15		mA
Output Sink Current (I_{SINK}) (Backplane Output)	V_{CC} = 5V, V_{OUT} = 5V, T_A = 25°C	12.6	20		mA
Output Source Current (I_{SOURCE}) (½-Digit)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	2.8	3.4		mA
Output Source Current (I_{SINK}) (½-Digit)	V_{CC} = 5V, V_{OUT} = 5V, T_A = 25°C	2.8	5		mA

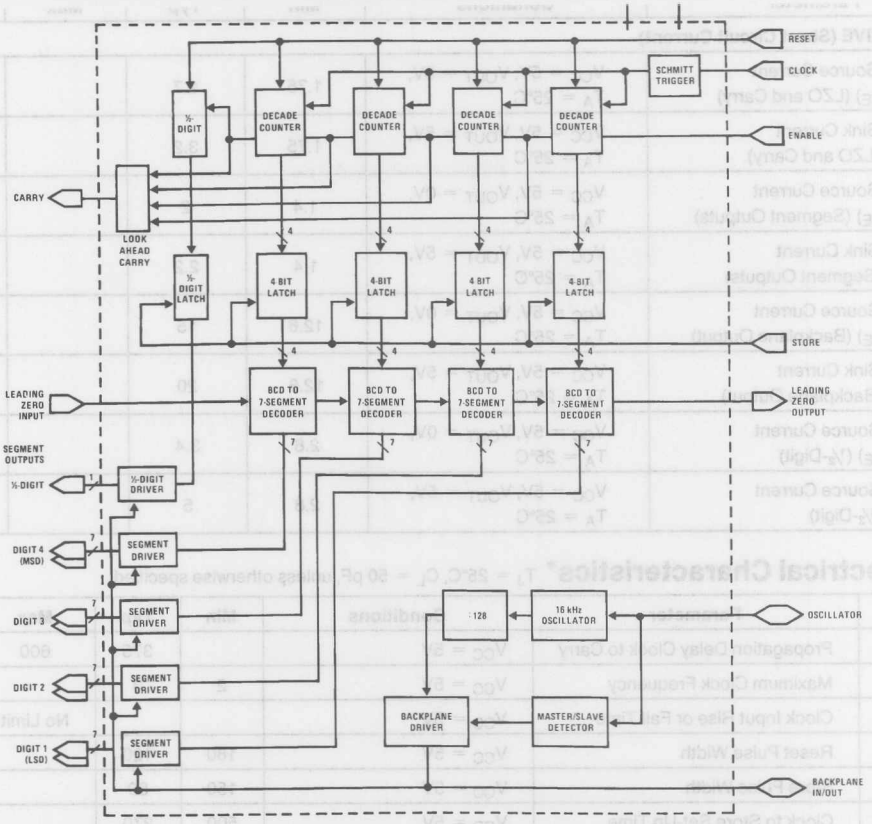
AC Electrical Characteristics*

T_J = 25°C, C_L = 50 pF, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry	V_{CC} = 5V		375	600	ns
f_{CLK}	Maximum Clock Frequency	V_{CC} = 5V	2	3		MHz
t_r, t_f	Clock Input Rise or Fall Time	V_{CC} = 5V			No Limit	
t_{WR}	Reset Pulse Width	V_{CC} = 5V	180	120		ns
t_{WS}	Store Pulse Width	V_{CC} = 5V	150	80		ns
$t_{SU(CK,S)}$	Clock to Store Set-Up Time	V_{CC} = 5V	500	270		ns
t_{SR}	Store to Reset Wait Time	V_{CC} = 5V	280	170		ns
$t_{SU(E,CK)}$	Enable to Clock Set-Up Time	V_{CC} = 5V	140	80		ns
t_{RR}	Reset Removal	V_{CC} = 5V	50	0		ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating, V_{CC} = 5V		85		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 5)		5		pF
t_{rfs}	Segment Rise/Fall Time	C_{load} = 200 pF		0.5		μs
t_{rfb}	Backplane Rise/Fall Time	C_{load} = 5000 pF		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating, V_{CC} = 5V		11		kHz

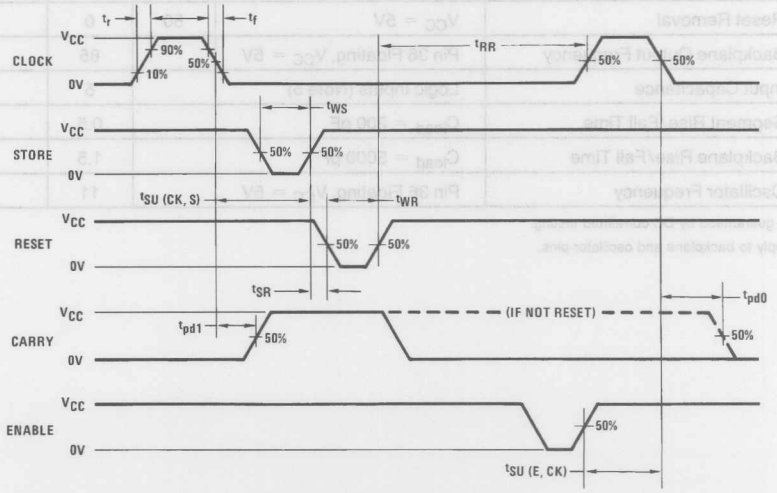
*AC Parameters are guaranteed by DC correlated testing.

Note 5: Does not apply to backplane and oscillator pins.



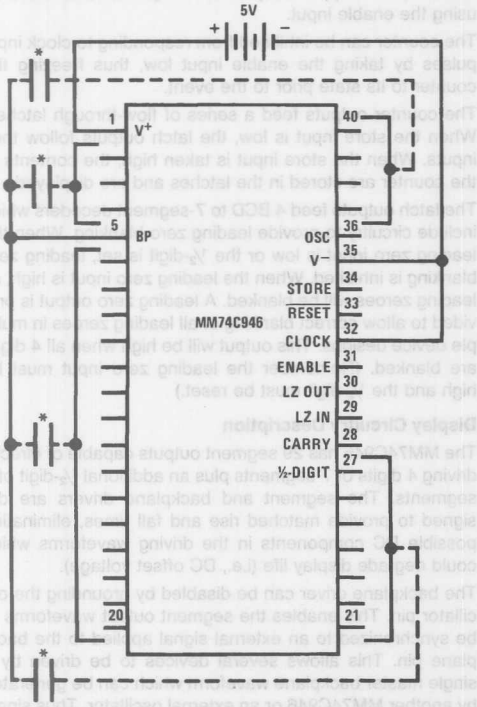
TL/F/5102–2

AC Waveforms



TL/F/5102–3

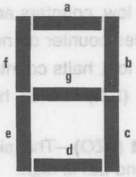
Test Circuit



TL/F/5102–4

*Each segment to backplane with 200 pF capacitor

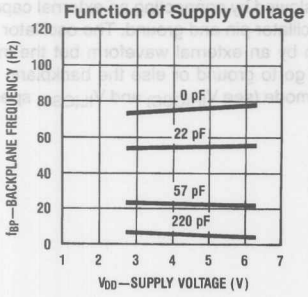
Segment Identification



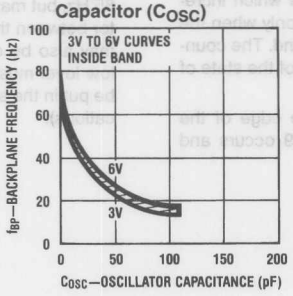
TL/F/5102–5

Typical Characteristics

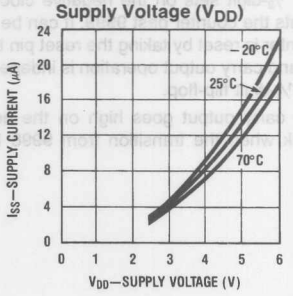
Backplane Frequency as a Function of Supply Voltage



Backplane Frequency as a Function of Oscillator Capacitor (C_{OSC})



Operating Supply Current (I_{SS}) as a Function of Supply Voltage (V_{DD})



TL/F/5102–6

6

Control Pin Description

Backplane In/Out—When the oscillator pin is grounded this pin is an input allowing an external device to generate the backplane waveform. When the oscillator pin is left open this pin is an output supplying backplane drive for an LCD.

Oscillator—The oscillator frequency may be lowered by tying a capacitor (C_{OSC}) between this pin and ground. If this pin is grounded the backplane pin becomes an input.

Store Input—This controls the latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high data on counter outputs is stored in latches and displayed.

$\overline{\text{RESET}}$ Input—When low, counters are reset to zero.

Clock Input—Advances counter on negative edge.

Enable Input—When low, halts counter operation.

Leading Zero Input (LZI)—When high, enables leading zero blanking.

Leading Zero Output (LZO)—This signal goes high when counter equals zero and LZI is high.

Carry Output—Goes high for one clock period when count of 9999 is reached.

A1–G1—Digit 1 segment outputs.

A2–G2—Digit 2 segment outputs.

A3–G3—Digit 3 segment outputs.

A4–G4—Digit 4 segment outputs.

½-Digit Output—Goes high when count goes from 9999 to 0000 and stays high until $\overline{\text{RESET}}$ goes low.

Application Hints

Counter Circuitry Description

The MM74C946 contains a 4-digit resettable synchronous counter with a Schmitt trigger on the clock input. An additional D flip-flop clocked by the counter carry out provides a true ½-digit, or it can be used to indicate an overflow condition. The counters increment on the negative clock edge. The ½-digit sets on the negative clock edge which increments the counter past 9999. It can be reset only when the counter is reset by taking the reset pin to ground. The counter and carry output operation is independent of the state of the ½-digit flip-flop.

The carry output goes high on the negative edge of the clock when the transition from 9998 to 9999 occurs and then goes low on the next count. Thus counters may be cascaded in a ripple carry mode or synchronous mode by using the enable input.

The counter can be inhibited from responding to clock input pulses by taking the enable input low, thus freezing the counter to its state prior to the event.

The counter outputs feed a series of flow-through latches. When the store input is low, the latch outputs follow their inputs. When the store input is taken high, the contents of the counter are stored in the latches and are displayed.

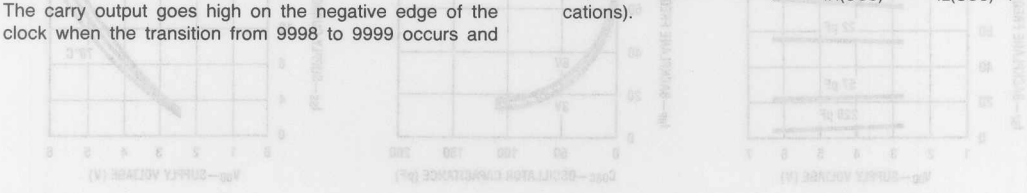
The latch outputs feed 4 BCD to 7-segment decoders which include circuitry to provide leading zero blanking. When the leading zero input is low or the ½-digit is set, leading zero blanking is inhibited. When the leading zero input is high, all leading zeroes will be blanked. A leading zero output is provided to allow correct blanking of all leading zeroes in multiple device designs. This output will be high when all 4 digits are blanked. (Remember the leading zero input must be high and the ½-digit must be reset.)

Display Circuitry Description

The MM74C946 has 29 segment outputs capable of directly driving 4 digits of 7 segments plus an additional ½-digit of 2 segments. The segment and backplane drivers are designed to provide matched rise and fall times, eliminating possible DC components in the driving waveforms which could degrade display life (i.e., DC offset voltage).

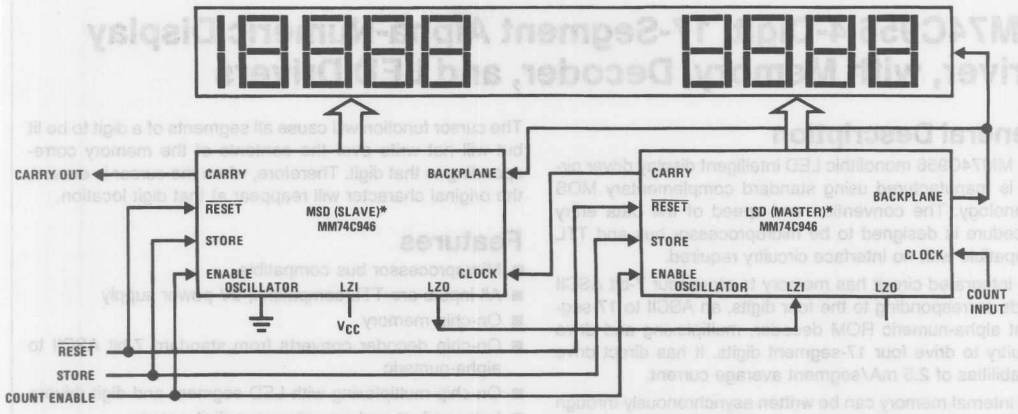
The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. This allows several devices to be driven by a single master backplane waveform which can be generated by another MM74C946 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc., digits can be driven by multiple counters. The maximum fanout of a master backplane driver is limited by its total capacitive load, which is the sum of the slaved backplane input capacitances and the display backplane capacitance.

An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency typically is 85 Hz, but may be slowed by connecting an external capacitor between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane will be put in the slave mode (see $V_{IH(OSC)}$ and $V_{IL(OSC)}$ specifications).



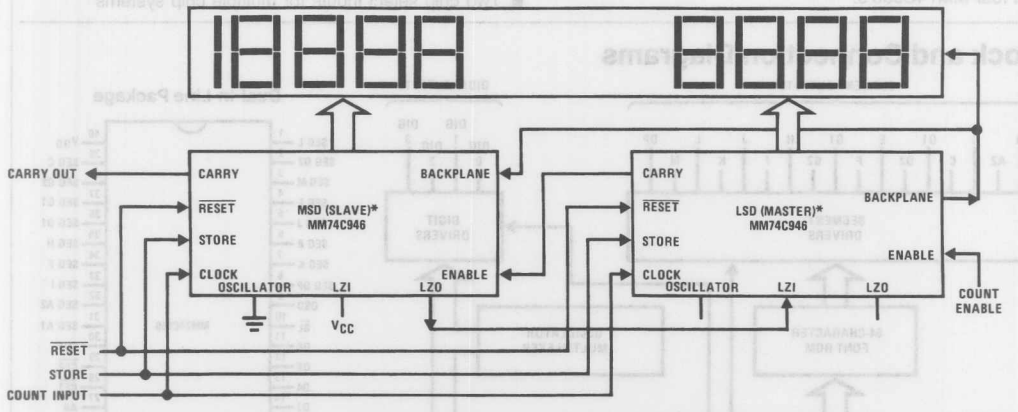
Typical Applications

Ripple Carry Cascading



TL/F/5102–7

Synchronous Cascading



TL/F/5102–8

*Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.

National Semiconductor

MM74C956 4-Digit, 17-Segment Alpha-Numeric Display Driver, with Memory, Decoder, and LED Drivers

General Description

The MM74C956 monolithic LED intelligent display driver circuit is manufactured using standard complementary MOS technology. The convention and speed of the data entry procedure is designed to be microprocessor bus and TTL compatible with no interface circuitry required.

The integrated circuit has memory to store four 7-bit ASCII words corresponding to the four digits, an ASCII to 17-segment alpha-numeric ROM decoder, multiplexing and drive circuitry to drive four 17-segment digits. It has direct drive capabilities of 2.5 mA/segment average current.

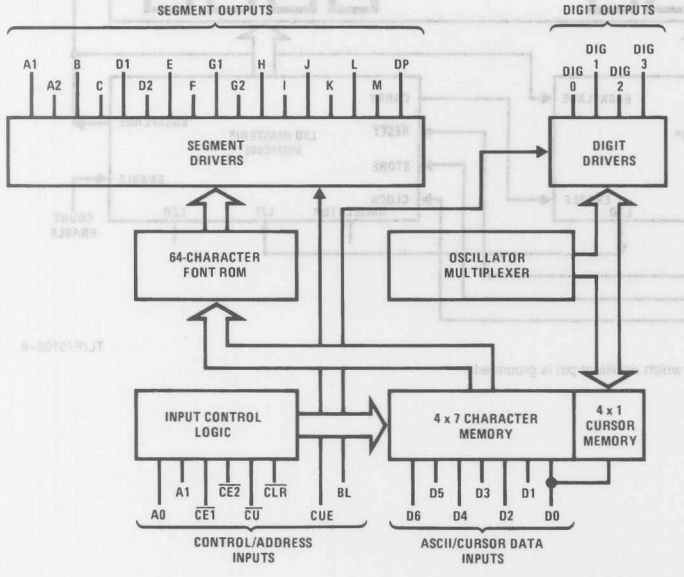
The internal memory can be written asynchronously through the 7-bit data bus (D0–D6) into the digit location addressed by the 2-bit address bus (A0, A1). For multiple chip circuits, two chip select inputs ($\overline{CE1}$, $\overline{CE2}$) can be decoded or a one-of-n decoder can be used for displays incorporating more than four MM74C956's.

The cursor function will cause all segments of a digit to be lit but will not write over the contents of the memory corresponding to that digit. Therefore, when the cursor is erased, the original character will reappear at that digit location.

Features

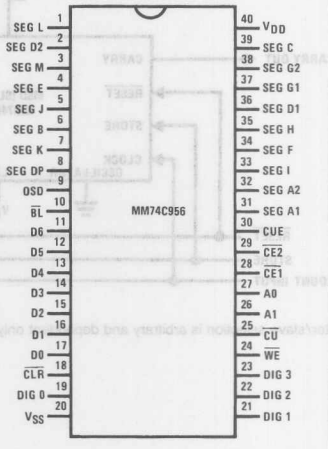
- Microprocessor bus compatible
- All inputs are TTL compatible; 5V power supply
- On-chip memory
- On-chip decoder converts from standard 7-bit ASCII to alpha-numeric
- On-chip multiplexing with LED segment and digit drivers
- Independent and asynchronous digit access
- Independent cursor function: can be disabled
- Display clear function
- Display blank function
- Two chip select inputs for multiple chip systems

Block and Connection Diagrams



TL/F/5924–1

Dual-In-Line Package



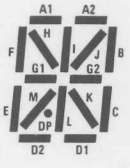
TL/F/5924–2

Top View

Order Number MM74C956*

*Please look into Section 8, Appendix D for availability of various package types.

Segment Designation



TL/F/5924–3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM74C956	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation (P_D)	700 mW
Operating V_{CC} Range	4.5V to 5.5V
V_{CC}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics T_A = 25°C

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	2.4			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5V, V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5V, V_{IN} = 0V	−100	25		μA
I_{CC}	Supply Current	V_{CC} = 5V @ T_A = 25°C All Outputs Open All Inputs @ 5V		0.5	1	mA
Output Drive (Notes 2 and 3)						
I_{SOURCE}	Peak Output Source Current (P-Channel Segment Driver with 1 Segment On)	V_{CC} = 5V, V_{OUT} = 1.9V T_A = 25°C			14.8	mA
I_{SOURCE}	Peak Output Source Current (P-Channel Segment Driver with 17 Segments On)	V_{CC} = 10V, V_{OUT} = 3.3V T_A = 25°C	4.2			mA
I_{SINK}	Peak Output Sink Current (N-Channel Digit Driver with 3 Segments On)	V_{CC} = 5V, V_{OUT} = 0.25V T_A = 25°C	18.5			mA
I_{SINK}	Peak Output Sink Current (N-Channel Digit Driver with 17 Segments On)	V_{CC} = 10V, V_{OUT} = 1.3V T_A = 25°C			172	mA

AC Electrical Characteristics* T_A = 25°C, V_{CC} = 5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_W	Write Pulse Width	All Inputs Swing from 0V–4V	240			ns
t_{DS}	Data Set-Up Time	All Inputs Swing from 0V–4V	100			ns
t_{DH}	Data Hold Time	All Inputs Swing from 0V–4V	50			ns
t_{AS}	Address Set-Up Time	All Inputs Swing from 0V–4V	300			ns
t_{AH}	Address Hold Time	All Inputs Swing from 0V–4V	0			ns
t_{CLR}	Clear Time	All Inputs Swing from 0V–4V	1			μs

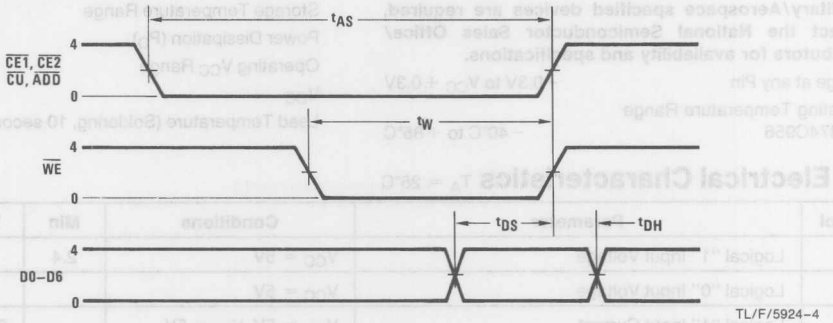
*AC Parameters are guaranteed by DC correlated testing.

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Average drive current ≈ peak drive current ÷ 4.

Note 3: Current/segment is dependent upon total number of segments on. Maximum current occurs with 1 segment on; minimum current occurs with 17 segments on.

Timing Diagram for data access



TL/F/5924–4

Functional Description

Entry into Data Memory

To enter an ASCII code, the $\overline{CE1}$ and $\overline{CE2}$ inputs must be low, $\overline{CU}$ must be high. When the address is set up at A0 and A1, the $\overline{WE}$ can go low, at which time the internal RAM will respond to the data inputs (D0–D6). Note that the data need not be set up prior to the $\overline{WE}$ transition.

All digits can be cleared by holding the $\overline{CLR}$ input low for the specified interval.

Entry into Cursor Memory

This is accomplished by setting the $\overline{CE1}$ and $\overline{CE2}$ inputs as well as the $\overline{CU}$ input low. The cursor memory consists of 4 bits corresponding to the four digits, each one addressable by way of the A0 and A1 inputs. Once the address is stable, the $\overline{WE}$ input must go low and the cursor memory will respond to the D0 input. That is, if D0 is high, a cursor will be written and if D0 is low, the cursor will be erased. $\overline{CLR}$ will not erase a cursor. A cursor will only be displayed when CUE is high and the cursor function can be bypassed by tying CUE low. A flashing cursor can be implemented by pulsing CUE; this results in alternately displaying the cursor and the character originally written in that digit. CUE will not alter the contents of either the cursor or data memory.

Blanking the Display

Display blanking can be realized by using the $\overline{BL}$ input. By taking $\overline{BL}$ low, the display will be disabled while leaving the contents of the data and cursor memory unchanged. A flashing display will occur if $\overline{BL}$ is pulsed. The display is blanked by $\overline{BL}$ regardless of whether a cursor or character is being displayed.

Illegal Code

If an illegal ASCII code is entered into the data memory (i.e., D6 = D5) the display will automatically be blanked for the corresponding digit.

OSD Pin

Taking the OSD pin high disables the internal oscillator and prohibits normal multiplex scanning. This pin is pulled low internally and is primarily meant to be used in testing the part only. This pin should be grounded or left open in normal operation.

Clearing the Display

Pulsing the $\overline{CLR}$ pin low for the specified time will clear all internal data memories while leaving the cursor memories unchanged.

Functional Description (Continued)

TABLE I. Data and Cursor Entry Function Example

Assume initially D6 = 1 and D5 − D0 = 0 for all internal digit memories. Cursor memory is cleared. Table is intended to be read in sequence.

	$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WE}$	$\overline{CLR}$	A1	A0	D6	D5	D4	D3	D2	D1	D0	DIG 3	DIG 2	DIG 1	DIG 0
DATA ENTRY FUNCTION	0	X	X	X	X	1	1	X	X	X	X	X	X	X	X	X				
	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X				
	1	0	1	X	X	X	1	X	X	X	X	X	X	X	X	X				
	1	0	0	X	X	1	1	X	X	X	X	X	X	X	X	X				
	1	0	0	X	1	0	1	0	0	1	0	0	0	1	1	1				
	1	0	0	X	1	0	1	1	0	0	1	1	0	1	0	0				
	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X				
	1	0	0	X	1	0	1	0	0	1	0	0	0	0	0	1				
	1	0	0	X	1	0	1	0	1	1	0	0	0	0	1	0				
	1	0	0	X	1	0	1	1	0	1	0	0	0	0	1	1				
	1	0	0	X	1	0	1	1	1	1	0	0	0	1	0	0				
CURSOR ENTRY FUNCTION	1	0	0	1	0	0	1	0	0	X	X	X	X	X	X	1				
	1	0	0	1	0	0	1	0	1	X	X	X	X	X	X	1				
	1	0	0	1	0	0	1	1	1	X	X	X	X	X	X	1				
	1	0	0	1	0	0	1	1	0	X	X	X	X	X	X	1				
	1	X	X	0	1	1	1	X	X	X	X	X	X	X	X	X				
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X				
	1	0	0	1	0	0	1	0	0	X	X	X	X	X	X	0				
	1	0	0	0	0	0	1	1	0	X	X	X	X	X	X	0				
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X				
	0	X	X	X	1	1	1	X	X	X	X	X	X	X	X	X				
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X				
	1	X	X	1	1	X	0	X	X	X	X	X	X	X	X	X				
	1	0	0	1	0	0	1	1	1	X	X	X	X	X	X	0				
	1	0	0	1	0	0	1	0	1	X	X	X	X	X	X	0				

X = don't care

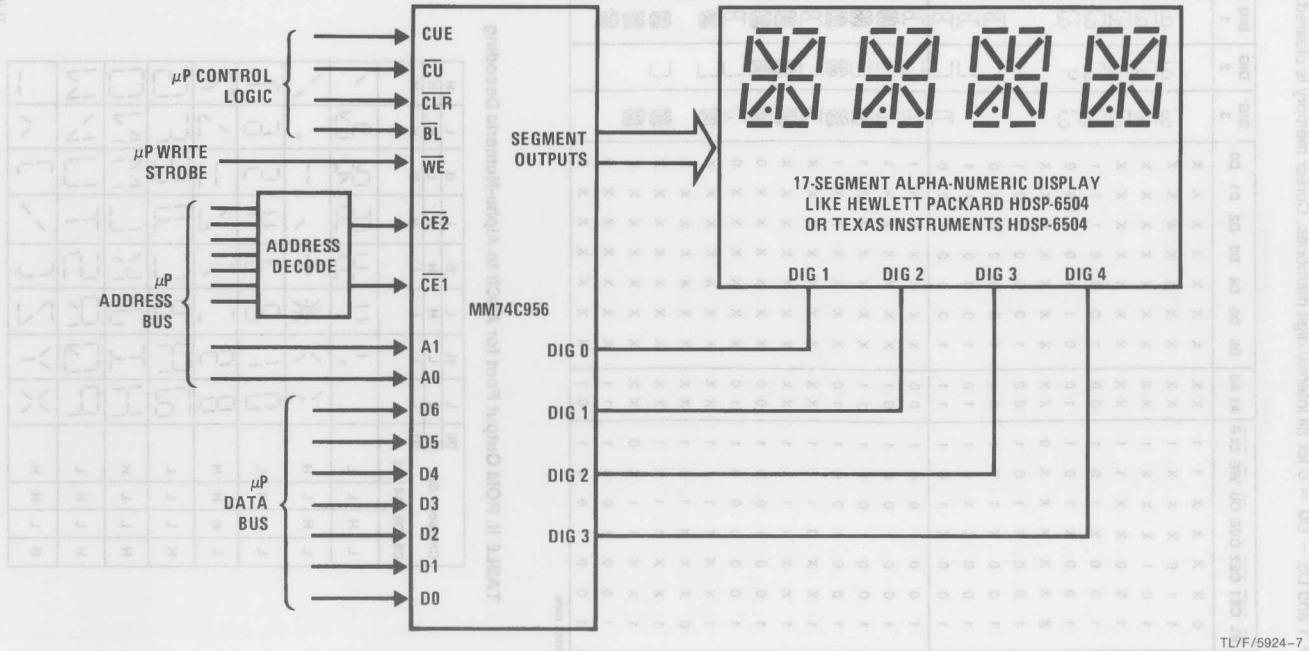
TL/F/5924–5

TABLE II. ROM Output Font for ASCII to Alpha-Numeric Decoding

Character Set	D0	L	H	L	H	L	H	L	H
	D1	L	L	H	H	L	L	H	H
	D2	L	L	L	L	H	H	H	H
D6 D5 D4 D3									
L H L L		!	"	#	$	%	&	'	
L H L H	(	)	*	+	,	-	.	/	
L H H L	0	1	2	3	4	5	6	7	
L H H H	8	9	:	;	<	=	>	?	
H L L L	@	A	B	C	D	E	F	G	
H L L H	H	I	J	K	L	M	N	O	
H L H L	P	Q	R	S	T	U	V	W	
H L H H	X	Y	Z	[	\	]	^	_	

TL/F/5924–6

Typical Application



TL/F/5924–7

National Semiconductor

MM78C29/MM88C29 Quad Single-Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

General Description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

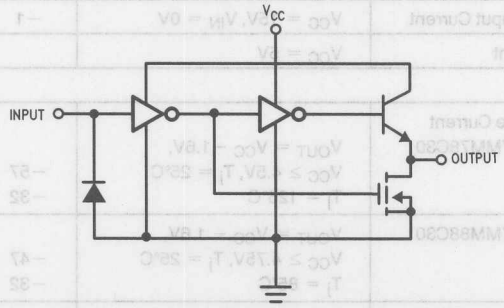
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver. Since the output ON resistance is a low 20Ω typ., the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

Features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low output ON resistance	20Ω (typ.)

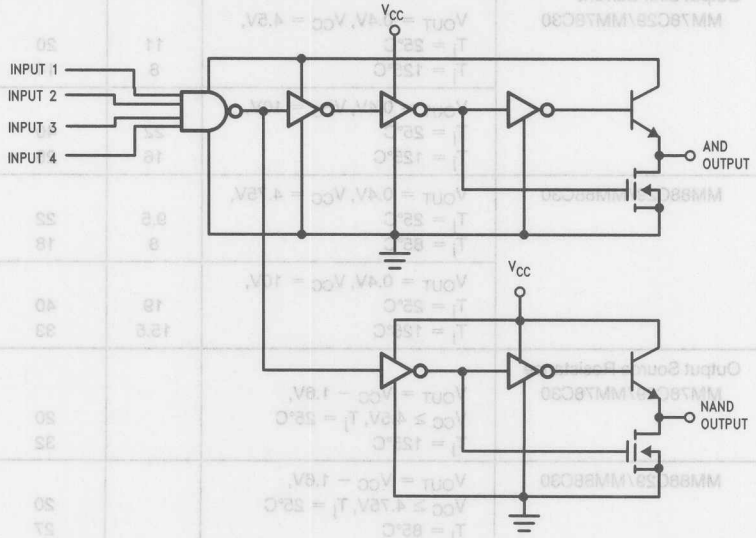
Logic Diagrams

1/4 MM78C29/MM88C29



TL/F/5908–1

1/2 MM78C30/MM88C30



TL/F/5908–2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +16V
Operating Temperature Range	
MM78C29/MM78C30	−55°C to +125°C
MM88C29/MM88C30	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Average Current at Output	
MM78C30/MM88C30	50 mA
MM78C29/MM88C29	25 mA
Maximum Junction Temperature, T_j	150°C
Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	100	mA
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V, V_{CC} ≥ 4.5V, T_j = 25°C	−57	−80		mA
		T_j = 125°C	−32	−50		mA
	MM88C29/MM88C30	V_{OUT} = V_{CC} − 1.6V, V_{CC} ≥ 4.75V, T_j = 25°C	−47	−80		mA
		T_j = 85°C	−32	−60		mA
	MM78C29/MM88C29 MM78C30/MM88C30	V_{OUT} = V_{CC} − 0.8V V_{CC} ≥ 4.5V	−2	−20		mA
I_{SINK}	Output Sink Current MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.5V, T_j = 25°C	11	20		mA
		T_j = 125°C	8	14		mA
		V_{OUT} = 0.4V, V_{CC} = 10V, T_j = 25°C	22	40		mA
		T_j = 125°C	16	28		mA
	MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V, T_j = 25°C	9.5	22		mA
		T_j = 85°C	8	18		mA
		V_{OUT} = 0.4V, V_{CC} = 10V, T_j = 25°C	19	40		mA
		T_j = 125°C	15.5	33		mA
I_{SOURCE}	Output Source Resistance MM78C29/MM78C30	V_{OUT} = V_{CC} − 1.6V, V_{CC} ≥ 4.5V, T_j = 25°C		20	28	Ω
		T_j = 125°C		32	50	Ω
	MM88C29/MM88C30	V_{OUT} = V_{CC} − 1.6V, V_{CC} ≥ 4.75V, T_j = 25°C		20	34	Ω
		T_j = 85°C		27	50	Ω

DC Electrical Characteristics

Min/Max limits apply across temperature range, unless otherwise noted (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (Continued)						
I_{SINK}	Output Sink Resistance					
	MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.50V,				
		T_j = 25°C		20	36	Ω
		T_j = 125°C		28	50	Ω
		V_{OUT} = 0.4V, V_{CC} = 10V,				
		T_j = 25°C		10	18	Ω
		T_j = 125°C		14	25	Ω
	MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V,				
		T_j = 25°C		18	41	Ω
		T_j = 85°C		22	50	Ω
		V_{OUT} = 0.4V, V_{CC} = 10V,				
		T_j = 25°C		10	21	Ω
		T_j = 85°C		12	26	Ω
	Output Resistance Temperature Coefficient					
	Source			0.55		%/°C
	Sink			0.40		%/°C
θ_{JA}	Thermal Resistance					
	MM78C29/MM78C30 (D-Package)			100		°C/W
	MM88C29/MM88C30 (N-Package)			150		°C/W

AC Electrical Characteristics* T_A = 25°C, C_L = 50 pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	(See *Figure 2*)				
	MM78C29/MM88C29	V_{CC} = 5V		80	200	ns
		V_{CC} = 10V		35	100	ns
	MM78C30/MM88C30	V_{CC} = 5V		110	350	ns
		V_{CC} = 10V		50	150	ns
t_{pd}	Differential Propagation Delay Time to Logical "1" or "0"	R_L = 100Ω, C_L = 5000 pF (See *Figure 1*)				
	MM78C30/MM88C30	V_{CC} = 5V			400	ns
		V_{CC} = 10V			150	ns
C_{IN}	Input Capacitance					
	MM78C29/MM88C29	(Note 3)		5.0		pF
	MM78C30/MM88C30	(Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacitance					
	MM78C29/MM88C29	(Note 3)		150		pF
	MM78C30/MM88C30	(Note 3)		200		pF

*AC Parameters are guaranteed by DC correlated testing.

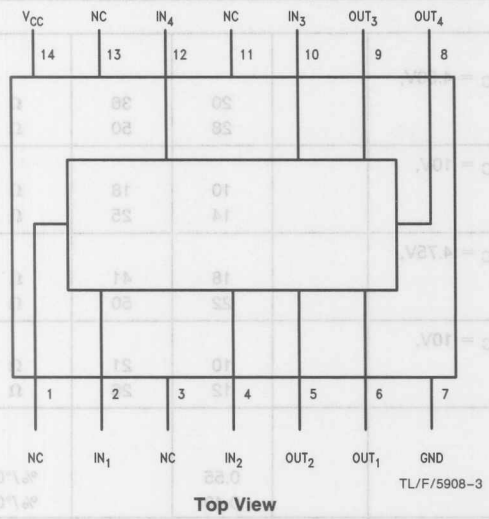
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Connection Diagrams

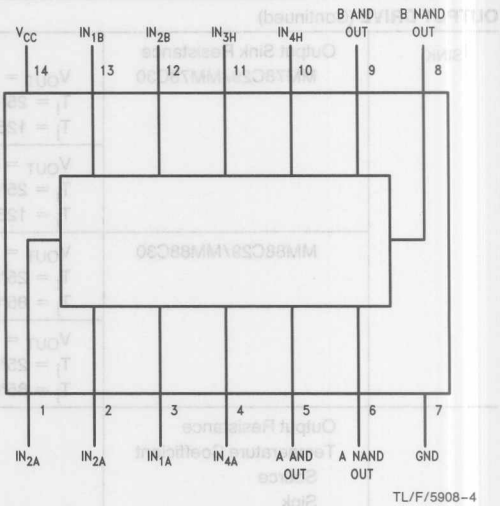
Dual-In-Line Package
MM78C29/MM88C29



Top View

Order Number MM78C29* or MM88C29*

Dual-In-Line Package
MM78C30/MM88C30



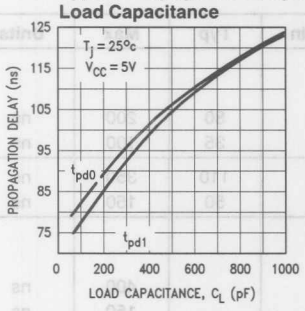
Top View

Order Number MM78C30J* or MM88C30J*

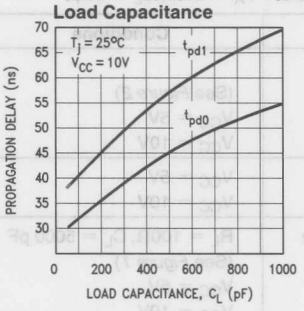
*Please look into Section 8, Appendix D for availability of various package types.

Typical Performance Characteristics

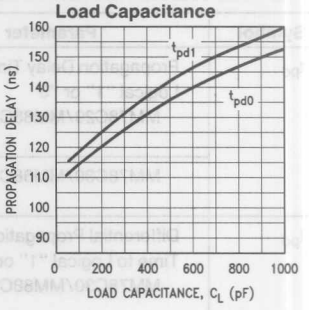
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



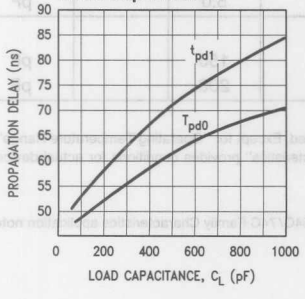
MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



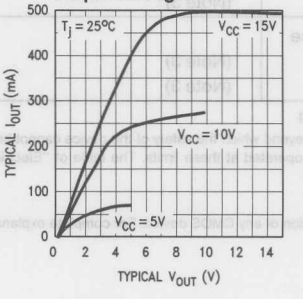
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



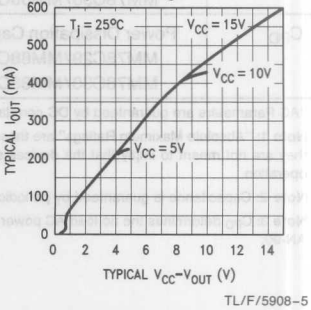
MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



Typical Sink Current vs Output Voltage

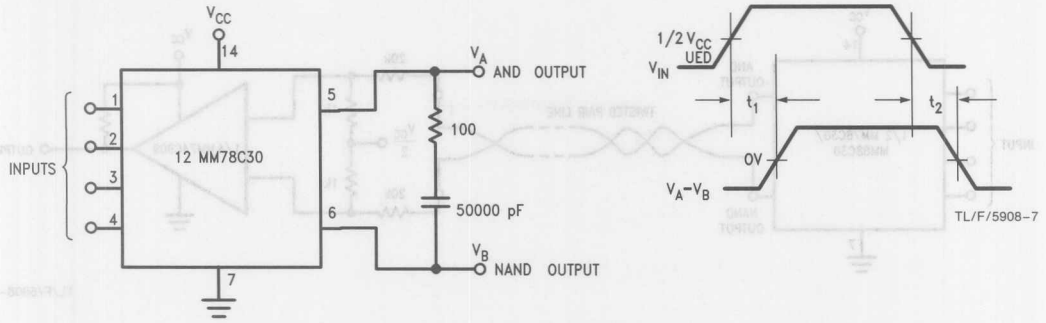


Typical Source Current vs Output Voltage



TL/F/5908–5

AC Test Circuits



TL/F/5908-6

FIGURE 1

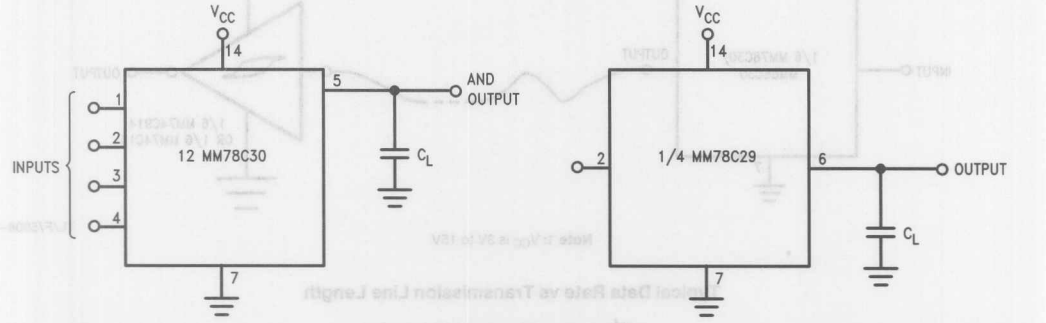
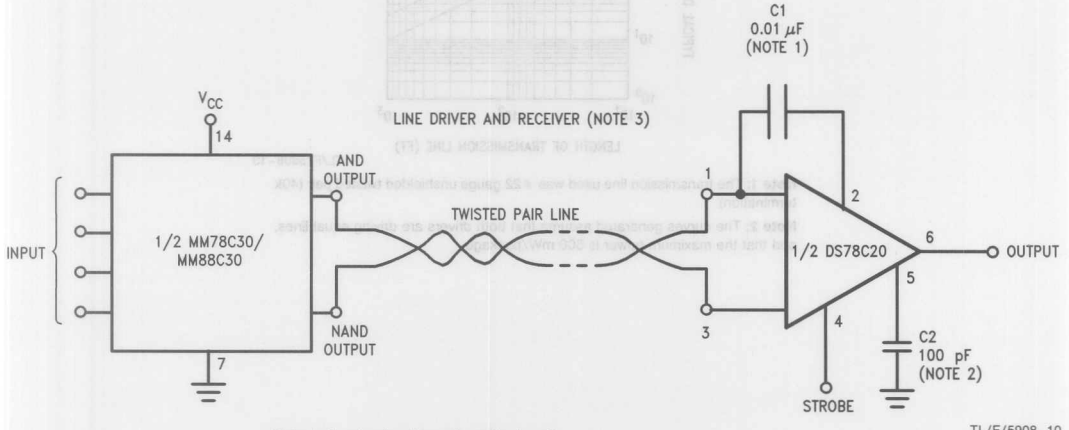


FIGURE 2

Typical Applications

Digital Data Transmission

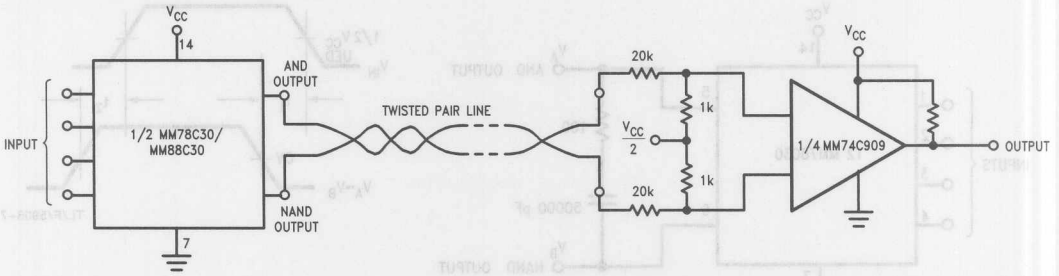


Note 1: Exact value depends on line length.

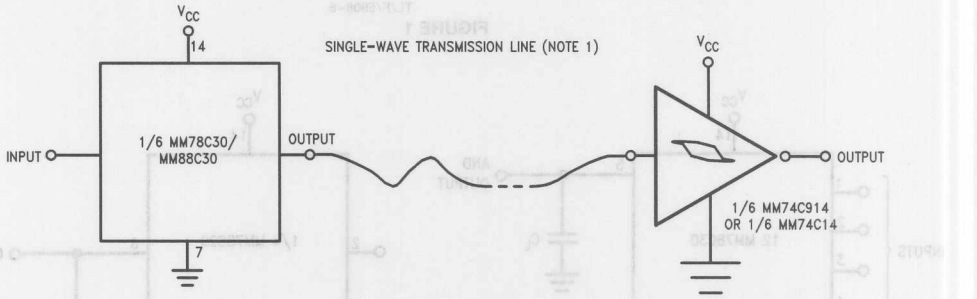
Note 2: Optional to control response time.

Note 3: V_{CC} to 4.5V to 5.5V for the DS7820.

Typical Applications (Continued)



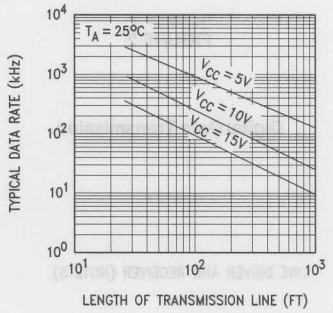
TL/F/5908–11



TL/F/5908–12

Note 1: V_{CC} is 3V to 15V

Typical Data Rate vs Transmission Line Length



TL/F/5908–13

Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

Section 7

Surface Mount

Section 7 Contents

Surface Mount 7-3

National Semiconductor

Section 7
Surface Mount

Cost pressures today are forcing many electronics manufacturers to automate their production lines. Surface mount technology plays a key role in this cost-savings trend because:

1. The mounting of devices on the PC board surface eliminates the expense of drilling holes;
2. The use of pick-and-place machines to assemble the PC boards greatly reduces labor costs;
3. The lighter and more compact assembled products resulting from the smaller dimensions of surface mount packages mean lower material costs.

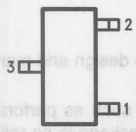
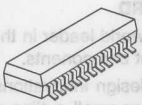
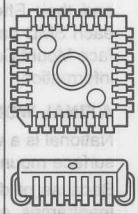
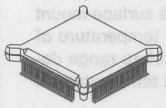
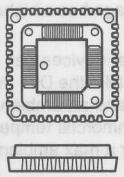
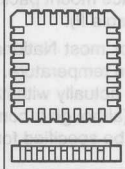
Production processes now permit both surface mount and insertion mount components to be assembled on the same PC board.

SURFACE MOUNT PACKAGING AT NATIONAL

To help our customers take advantage of this new technology, National has developed a line of surface mount packages. Ranging in lead counts from 3 to 360, the package offerings are summarized in Table I.

Lead center spacing keeps shrinking with each new generation of surface mount package. Traditional packages (e.g., DIPs) have a 100 mil lead center spacing. Surface mount packages currently in production (e.g., SOT, SOIC, PCC, LCC, LDCC) have a 50 mil lead center spacing. Surface mount packages in production release (e.g., PQFP) have a 25 mil lead center spacing. Surface mount packages in development (e.g., TAPEPAK™) will have a lead center spacing of only 12–20 mils.

TABLE I. Surface Mount Packages from National

Package Type	Small Outline Transistor (SOT)	Small Outline IC (SOIC)	Plastic Chip Carrier (PCC)	Plastic Quad Flat Pack (PQFP)	TAPEPAK™ (TP)	Leadless Chip Carrier (LCC) (LDCC)	Leaded Chip Carrier
							
Package Material	Plastic	Plastic	Plastic	Plastic	Plastic	Ceramic	Ceramic
Lead Bend	Gull Wing	Gull Wing	J-Bend	Gull Wing	Gull Wing	—	Gull Wing
Lead Center Spacing	50 Mils	50 Mils	50 Mils	25 Mils	20, 15, 12 Mils	50 Mils	50 Mils
Tape & Reel Option	Yes	Yes	Yes	tbd	tbd	No	No
Lead Counts	SOT-23 High Profile SOT-23 Low Profile	SO-8(*) SO-14(*) SO-14 Wide(*) SO-16(*) SO-16 Wide(*) SO-20(*) SO-24(*)	PCC-20 PCC-28 PCC-44 PCC-68 PCC-84 PCC-124	PQFP-84 PQFP-100 PQFP-132 PQFP-196 PQFP-244	TP-40 TP-68 TP-84 TP-132 TP-172 TP-220 TP-284 TP-360	LCC-18 LCC-20 LCC-28 LCC-32 LCC-44 LCC-48 LCC-52 LCC-68 LCC-84 LCC-124	LDCC-44 LDCC-68 LDCC-84 LDCC-124

*In production (or planned) for commercial CMOS logic products.

CMOS LOGIC PRODUCTS IN SURFACE MOUNT

A complete list of CMOS logic part numbers in surface mount is presented in Table III. Refer to the datasheet in the appropriate chapter of this databook for a complete description of the device. In addition, National is continually expanding the list of devices offered in surface mount. If the functions you need do not appear in Table III, contact the sales office or distributor branch nearest you for additional information.

Automated manufacturers can improve their cost savings by using Tape-and-Reel for surface mount devices. Simplified handling results because hundreds-to-thousands of semiconductors are carried on a single Tape-and-Reel pack (see ordering and shipping information—printed later in this section—for a comparison of devices/reel vs. devices/rail for those surface mount package types being used for CMOS logic products). With this higher device count per reel (when compared with less than a 100 devices per rail), pick-and-place machines have to be re-loaded less frequently and lower labor costs result.

With Tape-and-Reel, manufacturers save twice—once from using surface mount technology for automated PC board assembly and again from less device handling during shipment and machine set-up.

BOARD CONVERSION

Besides new designs, many manufacturers are converting existing printed circuit board designs to surface mount. The resulting PCB will be smaller, lighter and less expensive to manufacture; but there is one caveat—be careful about the thermal dissipation capability of the surface mount package.

Because the surface mount package is smaller than the traditional dual-in-line package, the surface mount package is not capable of conducting as much heat away as the DIP (i.e., the surface mount package has a higher thermal resistance—see Table II).

The silicon for most National devices can operate up to a 150°C junction temperature. Like the DIP, the surface mount package can actually withstand an ambient temperature of up to 125°C (although a commercial temperature range device will only be specified for a max ambient temperature of 85°C).

TABLE II: Surface Mount Package Thermal Resistance Range*

Package	Thermal Resistance** (θ_{jA}, °C/W)
SO-8	120–175
SO-14	100–140
SO-14 Wide	70–110
SO-16	90–130
SO-16 Wide	70–100
SO-20	60–90
SO-24	55–85

*Actual thermal resistance for a particular device depends on die size. Refer to the datasheet for the actual θ_{jA} value.

**Test conditions: PCB mount (FR4 material), still air (room temperature), copper traces (150 × 20 × 10 mils).

Given a max junction temperature of 150°C and a maximum allowed ambient temperature, the surface mount device will be able to dissipate less power than the DIP device. Although CMOS Logic devices dissipate very little power in the static mode, their power consumption may be significant when clocked at high frequencies. Therefore, the higher thermal resistance should be evaluated for new designs.

For board conversion, the DIP and surface mount devices would have to dissipate the same power. This means the surface mount circuit would have a lower maximum allowable ambient temperature than the DIP circuit. For DIP circuits where the maximum ambient temperature required is substantially lower than the maximum ambient temperature allowed, there may be enough margin for safe operation of the surface mount circuit with its lower maximum allowable ambient temperature. But where the maximum ambient temperature required of the DIP current is close to the maximum allowable ambient temperature, the lower maximum ambient temperature allowed for the surface mount circuit may fall below the maximum ambient temperature required. The circuit designer must be aware of this potential pitfall so that an appropriate work-around can be found to keep the surface mount package from being thermally overstressed in the application.

SURFACE MOUNT LITERATURE

National has published extensive literature on the subject of surface mount packaging. Engineers from packaging, quality, reliability, and surface mount applications have pooled their experience to provide you with practical hands-on knowledge about the construction and use of surface mount packages.

The applications note AN-450 "Surface Mounting Methods and their Effect on Product Reliability" is referenced on each SMD datasheet. In addition, "Wave Soldering of Surface Mount Components" is reprinted in this section for your information.

A FINAL WORD

National is a world leader in the design and manufacture of surface mount components.

Because of design innovations such as perforated copper leadframes, our small outline package is as reliable as our DIP—the laws of physics would have meant that a straight "junior copy" of the DIP would have resulted in an "S.O." package of lower reliability. You benefit from this equivalence of reliability. In addition, our ongoing vigilance at each step of the production process assures that the reliability we designed in stays in so that only devices of the highest quality and reliability are shipped to your factory.

Our surface mount applications lab at our headquarters site in Santa Clara, California continues to research (and publish) methods to make it even easier for you to use surface mount technology. Your problems are our problems.

When you think "Surface Mount"—think "National"!

TABLE III. CMOS Surface Mount Current Device Listing

CD4000	CD4538BCWM	MM74HC139M	MM74HC289M	MM74HC541WM	MM74HCT273WM
	CD4541BCWM	MM74HC14M	MM74HC299WM	MM74HC563WM	MM74HCT34M
CD4001BCM	CD4723BCM	MM74HC147M	MM74HC30M	MM74HC564WM	MM74HCT373WM
CD4002BCM		MM74HC149WM	MM74HC32M	MM74HC573WM	MM74HCT374WM
CD4007CM		MM74HC151M	MM74HC354WM	MM74HC574WM	MM74HCT521WM
CD4010CM		MM74HC153M	MM74HC356WM	MM74HC58M	MM74HCT533WM
CD4011BCM	**MM74C**	MM74HC154WM	MM74HC365WM	MM74HC589M	MM74HCT534WM
CD4013BCM		MM74HC157M	MM74HC366WM	MM74HC595M	MM74HCT540WM
CD4014CM	MM74C00M	MM74HC158M	MM74HC367WM	MM74HC597M	MM74HCT541WM
CD4016BCM	MM74C14M	MM74HC160M	MM74HC368WM	MM74HC640WM	MM74HCT640WM
CD4017BCM	MM74C154WM	MM74HC161M	MM74HC373WM	MM74HC643WM	MM74HCT643WM
CD4020BCM	MM74C193M	MM74HC162M	MM74HC374WM	MM74HC646WM	MM74HCT688WM
CD4021BCM	MM74C240WM	MM74HC163M	MM74HC390WM	MM74HC648WM	MM74HCT74M
CD4023BCM	MM74C244WM	MM74HC164M	MM74HC393M	MM74HC688WM	
CD4024BCM	MM74C32M	MM74HC165M	MM74HC4002M	MM74HC7266M	
CD4025BCM	MM74C373WM	MM74HC173M	MM74HC4016WM	MM74HC73M	
CD4027BCM	MM74C374WM	MM74HC174M	MM74HC4017M	MM74HC74AM	**MM74HCU**
CD4040BCM	MM74C74M	MM74HC175M	MM74HC4020M	MM74HC75M	
CD4041BCM	MM74C901M	MM74HC181WM	MM74HC4040M	MM74HC76M	MM74HCU04M
CD4042BCM	MM74C906M	MM74HC182M	MM74HC4046M	MM74HC85WM	
CD4043BCM	MM74C914M	MM74HC194WM	MM74HC4049M	MM74HC86M	
CD4047BCM		MM74HC195WM	MM74HC4050M		
CD4049UBCM		MM74HC20M	MM74HC4051WM		
CD4050BCM		MM74HC221AM	MM74HC4052WM		
CD4051BCM	**MM74HC**	MM74HC237M	MM74HC4053WM	**MM74HCT**	
CD4052BCM		MM74HC240WM	MM74HC4060M		
CD4053BCM	MM74HC00M	MM74HC241WM	MM74HC4066WM	MM74HCT00M	
CD4060BCM	MM74HC02M	MM74HC242M	MM74HC4075M	MM74HCT04M	
CD4066BCM	MM74HC03M	MM74HC243M	MM74HC4078M	MM74HCT05M	
CD4069UBCM	MM74HC04M	MM74HC24316WM	MM74HC42M	MM74HCT112M	
CD4070BCM	MM74HC08M	MM74HC244WM	MM74HC423AM	MM74HCT138M	
CD4071BCM	MM74HC10M	MM74HC245AWM	MM74HC4316WM	MM74HCT149WM	
CD4081BCM	MM74HC109AM	MM74HC251M	MM74HC4511M	MM74HCT151M	
CD4093BCM	MM74HC11M	MM74HC253M	MM74HC4514WM	MM74HCT153WM	
CD4094BCWM	MM74HC123AM	MM74HC257M	MM74HC4538M	MM74HCT164M	
CD4511BCWM	MM74HC125M	MM74HC259M	MM74HC4543M	MM74HCT240WM	
CD4512BCM	MM74HC126M	MM74HC266AM	MM74HC51M	MM74HCT241WM	
CD4514BCWM	MM74HC132M	MM74HC27M	MM74HC521WM	MM74HCT244WM	
CD4515BCWM	MM74HC133M	MM74HC273WM	MM74HC533WM	MM74HCT245WM	
CD4516BCWM	MM74HC137M	MM74HC280M	MM74HC534WM	MM74HCT251M	
CD4528BCM	MM74HC 138M	MM74HC283M	MM74HC540WM	MM74HCT253M	

7

that you will receive your devices in the following quantities per Tape-and-Reel pack: SMD devices can also be supplied in conventional conductive rails.

Package	Package Designator	Max/Rail	Per Reel*
SO-8	M	100	2500
SO-14	M	50	2500
SO-14 Wide	WM	50	1000
SO-16	M	50	2500
SO-16 Wide	WM	50	1000
SO-20 Wide	WM	40	1000
SO-24 Wide	WM	30	1000

*Incremental ordering quantities. (National Semiconductor reserves the right to provide a smaller quantity of devices per Tape-and-Reel pack to preserve lot or date code integrity. See example below.)

packs, each having 2500 MM74C00M ICs

- Case 2: 3,000 devices have date code A and 2,000 devices have date code B
  - You receive 3 SO-14 (Narrow) Tape-and-Reel packs as follows:

    Pack #1 has 2,500 MM74C00M ICs with date code A

    Pack #2 has 500 MM74C00M ICs with date code A

    Pack #3 has 2,000 MM74C00M ICs with date code B

Short-Form Procurement Specification

TAPE FORMAT

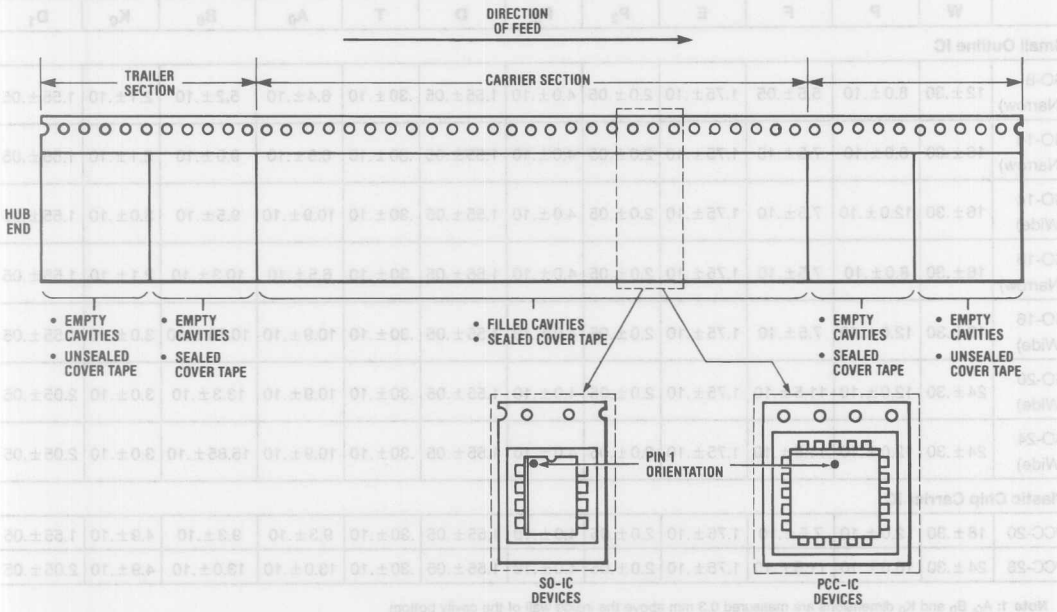
→ Direction of Feed

	Trailer (Hub End)*		Carrier*	Leader (Start End)*	
	Empty Cavities, min (Unsealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Filled Cavities (Sealed Cover Tape)	Empty Cavities, min (Sealed Cover Tape)	Empty Cavities, min (Unsealed Cover Tape)
Small Outline IC					
SO-8 (Narrow)	2	2	2500	5	5
SO-14 (Narrow)	2	2	2500	5	5
SO-14 (Wide)	2	2	1000	5	5
SO-16 (Narrow)	2	2	2500	5	5
SO-16 (Wide)	2	2	1000	5	5
SO-20 (Wide)	2	2	1000	5	5
SO-24 (Wide)	2	2	1000	5	5

***The following diagram identifies these sections of the tape and Pin #1 device orientation.**

Short-Form Procurement Specification (Continued)

DEVICE ORIENTATION

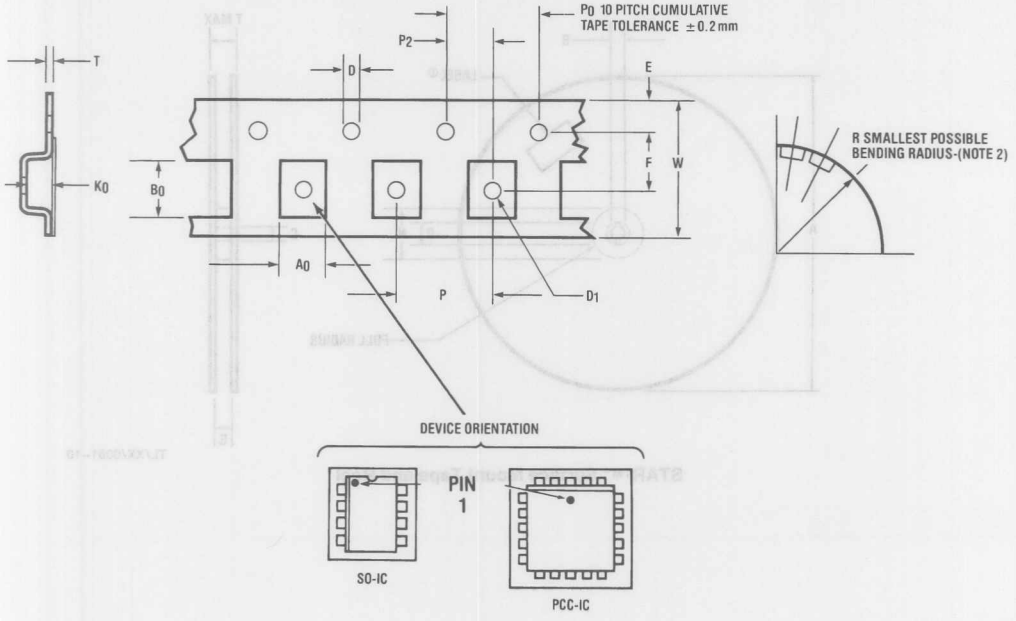


TL/XX/0061–8

MATERIALS

- Cavity Tape: Conductive PVC (less than 10^5 Ohms/Sq)
- Cover Tape: Polyester
  - (1) Conductive cover available
- Reel:
  - (1) Solid 80 pt fibreboard (standard)
  - (2) Conductive fibreboard available
  - (3) Conductive plastic (PVC) available

TAPE DIMENSIONS (24 Millimeter Tape or Less)



TL/XX/0061–9

Short-Form Procurement Specification (Continued)

	W	P	F	E	P_2	P_0	D	T	A_0	B_0	K_0	D_1	R
Small Outline IC													
SO-8 (Narrow)	12±.30	8.0±.10	5.5±.05	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.4±.10	5.2±.10	2.1±.10	1.55±.05	30
SO-14 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	9.0±.10	2.1±.10	1.55±.05	40
SO-14 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	9.5±.10	3.0±.10	1.55±.05	40
SO-16 (Narrow)	16±.30	8.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	6.5±.10	10.3±.10	2.1±.10	1.55±.05	40
SO-16 (Wide)	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	10.76±.10	3.0±.10	1.55±.05	40
SO-20 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	13.3±.10	3.0±.10	2.05±.05	50
SO-24 (Wide)	24±.30	12.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	10.9±.10	15.85±.10	3.0±.10	2.05±.05	50
Plastic Chip Carrier IC													
PCC-20	16±.30	12.0±.10	7.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	9.3±.10	9.3±.10	4.9±.10	1.55±.05	40
PCC-28	24±.30	16.0±.10	11.5±.10	1.75±.10	2.0±.05	4.0±.10	1.55±.05	.30±.10	13.0±.10	13.0±.10	4.9±.10	2.05±.05	50

Note 1: A_0, B_0 and K_0 dimensions are measured 0.3 mm above the inside wall of the cavity bottom.

Note 2: Tape with components shall pass around a mandril radius R without damage.

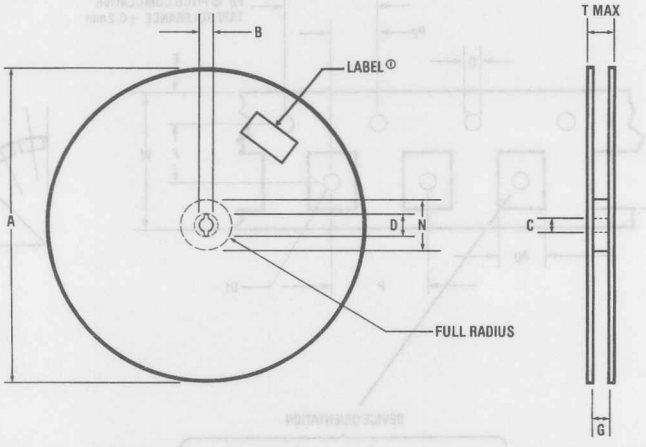
Note 3: Cavity tape material shall be PVC conductive (less than 10^5 Ohms/Sq).

Note 4: Cover tape material shall be polyester (30–65 grams peel-back force).

Note 5: D_1 Dimension is centered within cavity.

Note 6: All dimensions are in millimeters.

REEL DIMENSIONS



TL/XX/0061–10

STAR™* Surface Mount Tape and Reel

Short-Form Procurement Specifications (Continued)

		A (Max)	B (Min)	C	D (Min)	N (Min)	G	T (Max)
12 mm Tape	SO-8 (Narrow)	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.488^{+.078}_{-.000}$ 12.4^{+2}_{-0}	.724 18.4
16 mm Tape	SO-14 (Narrow) SO-14 (Wide) SO-16 (Narrow) SO-16 (Wide) PCC-20	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.646^{+.078}_{-.000}$ 16.4^{+2}_{-0}	.882 22.4
24 mm Tape	SO-20 (Wide) SO-24 (Wide) PCC-28	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$0.960^{+.078}_{-.000}$ 24.4^{+2}_{-0}	1.197 30.4
32 mm Tape	PCC-44	(13.00) (330)	.059 1.5	.512±.002 13±0.05	.795 20.2	1.969 50	$1.276^{+.078}_{-.000}$ 32.4^{+2}_{-0}	1.512 38.4

Units: Inches / Millimeters

Material: Paperboard (Non-Flaking)

LABEL

Human and Machine Readable Label is provided on reel. A variable (C.P.I) density code 39 is available. NSC STD label (7.6 C.P.I.)

FIELD

Lot Number

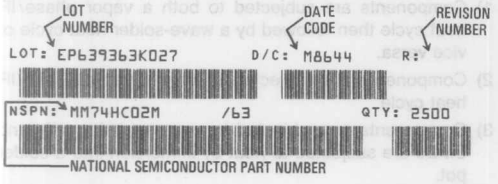
Date Code

Revision Level

National Part No. I.D.

Qty.

EXAMPLE



TL/XX/0061–11

Fields are separated by at least one blank space.

Future Tape-and-Reel packs will also include a smaller-size bar code label (high-density code 39) at the beginning of the tape. (This tape label is not available on current production.)

National Semiconductor will also offer additional labels containing information per your specific specification.

Wave Soldering of Surface Mount Components

ABSTRACT

In facing the upcoming surge of "surface mount technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this new process. However, as the availability of surface mount components is still limited, may have taken to mixing the lead-inserted standard dual-in-line packages (DIPs) with the surface mounted devices (SMDs). Furthermore, to take advantage of using both sides of the board, surface-mounted components are generally adhered to the bottom side of the board while the top side is reserved for the conventional lead-inserted packages. If processed through a wave solder machine, the semiconductor components are now subjected to extra thermal stresses (now that the components are totally immersed into the molten solder).

A discussion of the effect of wave soldering on the reliability of plastic semiconductor packages follows. This is intended to highlight the limitations which should be understood in the use of wave soldering of surface mounted components.

ROLE OF WAVE-SOLDERING IN APPLICATION OF SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave-soldering machine.

Wave Soldering of Surface Mount Components (Continued)

The reasons being:

1) Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.
2) Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.
3) Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW BOARD ASSEMBLY PROCEDURES

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

a) Whether to mount ICs on one or both sides of the board.
b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or combination of two or more methods.

The various processes that may be employed are:

A) Wave Solder before Vapor/IR reflow solder.
   1. Components on the same side of PW Board.
      Lead insert standard DIPS onto PW Board Wave solder (conventional)
      Wash and lead trim
      Dispense solder paste on SMD pads
      Pick and place SMDs onto PW Board
      Bake
      Vapor phase/IR reflow
      Clean
   2. Components on opposite side of PW Board.
      Lead insert standard DIPs onto PW Board
      Wave Solder (conventional)
      Clean and lead trim
      Invert PW Board
      Dispense solder paste on SMD pads
      Dispense drop of adhesive on SMD sites (optional for smaller components)
      Pick and place SMDs onto board
      Bake/Cure
      Invert board to rest on raised fixture
      Vapor/IR reflow soldering
      Clean

B) Vapor/IR reflow solder then Wave Solder.
   1. Components on the same side of PW Board.
      Solder paste screened on SMD side of Printed Wire Board
      Pick and place SMDs
      Bake
      Vapor/IR reflow
      Lead insert on same side as SMDs
      Wave solder
      Clean and trim underside of PCB

C) Vapor/IR reflow only.
   1. Components on the same side of PW Board.
      Trim and form standard DIPs in "gull wing" configuration
      Solder paste screened on PW Board
      Pick and place SMDs and DIPs
      Bake
      Vapor/IR reflow
      Clean
   2. Components on opposite sides of PW Board.
      Solder paste screened on SMD-side of Printed Wire Board
      Adhesive dispensed at central location of each component
      Pick and place SMDs
      Bake
      Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads
      Lead insert DIPs
      Vapor/IR reflow
      Clean and lead trim

D) Wave Soldering Only
   1. Components on opposite sides of PW Board.
      Adhesive dispense on SMD side of PW Board
      Pick and place SMDs
      Cure adhesive
      Lead insert top side with DIPs
      Wave solder with SMDs down and into solder bath
      Clean and lead trim

All of the above assembly procedures can be divided into three categories for I.C. Reliability considerations:

1) Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
2) Components are subjected to only a vapor phase/IR heat cycle.
3) Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a 'pallet' where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Wave Soldering of Surface Mount Components (Continued)

THERMAL CHARACTERISTICS OF MOLDED INTEGRATED CIRCUITS

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on lead frames, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of lead frame material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal lead frame in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the expoxy-metal interface. Howerver, if the package is subjected to temprature above its glass-transition temperature, the epoxy will begin to expand much faster than the metal and the probability of separation is greatly increased.

CONVENTIONAL WAVE-SOLDERING

Most wave-soldering operations occur at temperatures between 240–260°C. Conventional epoxies for encapsulation have glass-transition temperature between 140–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

1) The PW board has a certain amount of heat-sink effect and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
2) In conventional soldering, only the tip of each lead in a DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

EFFECT ON PACKAGE PERFORMANCE BY EPOXY-METAL SEPARATION

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metallization over time and premature failure of the device in the field.

VAPOR PHASE/IR REFLOW SOLDERING

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Operating temperatures are 215°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec–60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-lead frame interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

BIAS MOISTURE TEST

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a stream chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and

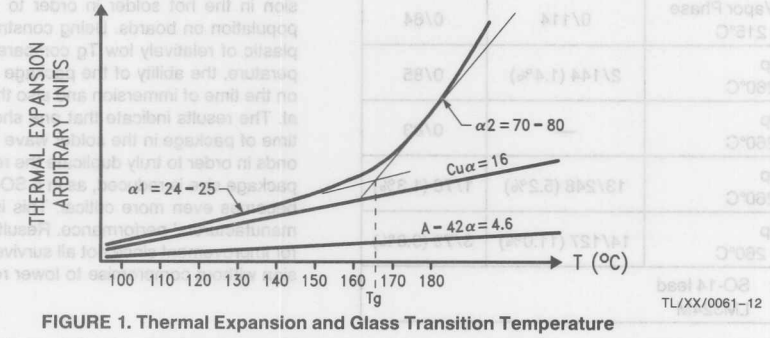


FIGURE 1. Thermal Expansion and Glass Transition Temperature

85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

TEST RESULTS

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave-soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec. exposure @ 215°C)
   = 9 failures/1723 samples
   = 0.5% (average over 32 sample lots)
2. Wave solder (2 sec total immersion @ 260°C)
   = 16 failures/1201 samples
   = 1.3% (average over 27 sample lots)

Package: SO-14 lead
Test: Bias moisture test 85% R.H., 85°C for 2000 hours
Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4000 hours 85/85 test. Results were compared for packages by itself against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results (85% R.H./85°C Bias Moisture Test, 2000 hours) (# Failures/Total Tested)

	Unmounted	Mounted
Control/Vapor Phase 15 sec @ 215°C	0/114	0/84
Solder Dip 2 sec @ 260°C	2/144 (1.4%)	0/85
Solder Dip 4 sec @ 260°C	—	0/83
Solder Dip 6 sec @ 260°C	13/248 (5.2%)	1/76 (1.3%)
Solder Dip 10 sec @ 260°C	14/127 (11.0%)	3/79 (3.8%)
Package: SO-14 lead Device: LM324M		

the mismatch in expansion, the results show the package being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6000 hours in a 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturers Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Tested)

Package SO-8	Vapor Phase 30 sec	Wave Solder 2 sec	Wave Solder 4 sec	Wave Solder 6 sec	Wave Solder 10 sec
Manuf A	8/30*	1/30*	0.30	12/30*	16/30*
Manuf B	2/30*	8/30*	2/30*	22/30*	20/30*
Manuf C	0/30	0/29	0/29	0/30	0/30
Manuf D	1/30*	0/30	12/30*	14/30*	2/30*
Manuf E	1/30**	0/30	0/30	0/30	0/30
Manuf F	0/30	0/30	0/30	0/30	0/30
Manuf G	0/30	0/30	0/30	0/30	0/30

*Corrosion-failures

**No Visual Defects—Non-corrosion failures

Test: Accelerated Bias Moisture Test; 85% R.H./85°C, 6000 equivalent hours.

SUMMARY

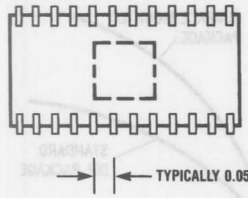
Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in a hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low Tg compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

Small Outline (SO) Package Surface Mounting Methods—Parameters and Their Effect on Product Reliability

The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

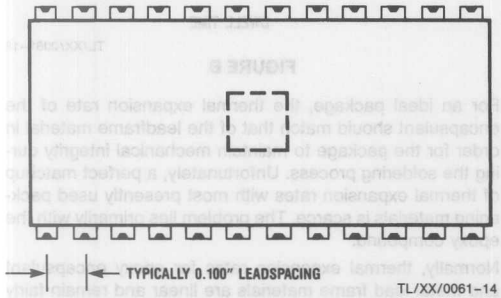
COMPONENT SIZE COMPARISON

S.O. Package



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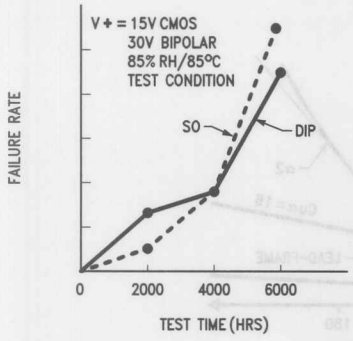
Standard DIP Package



TL/XX/0061–14

Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. *Figure A* is a summary of accelarated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.



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FIGURE A

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in *Figure A* no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

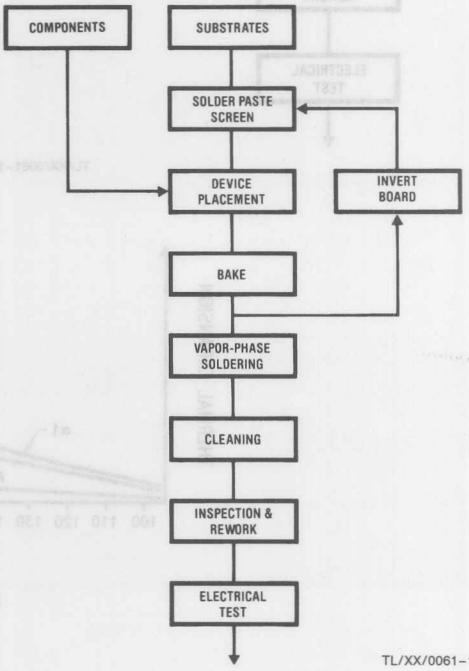
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

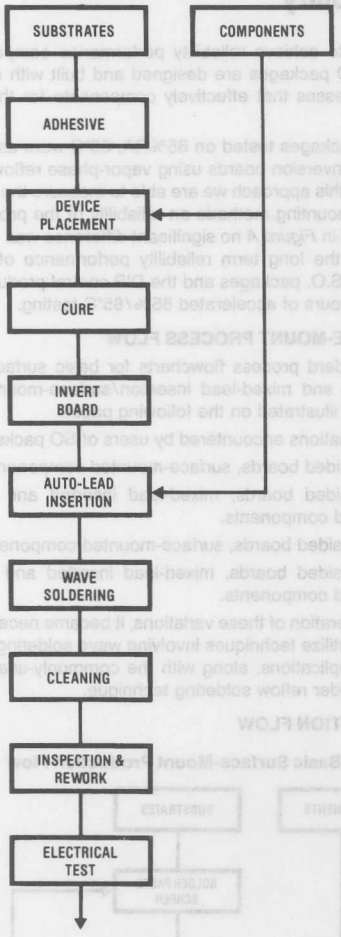
PRODUCTION FLOW

Basic Surface-Mount Production Flow



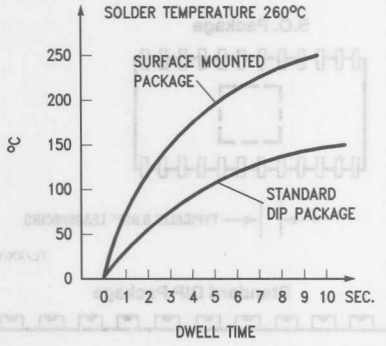
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Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



TL/XX/0061–17

Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP PC board mounting processes. *Figure B* illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).

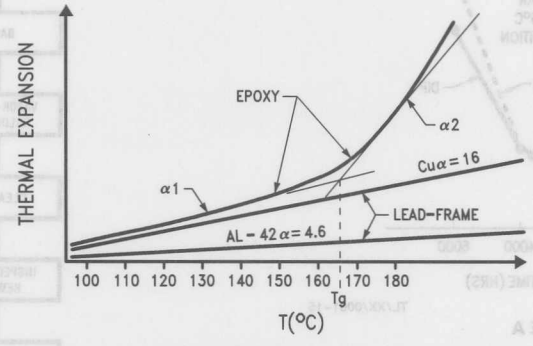


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FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect matchup of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160°C, *Figure C.* At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165°C), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.



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FIGURE C

When this happens during a conventional wave soldering process using flux and acid cleaners, process residues and even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws.

Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

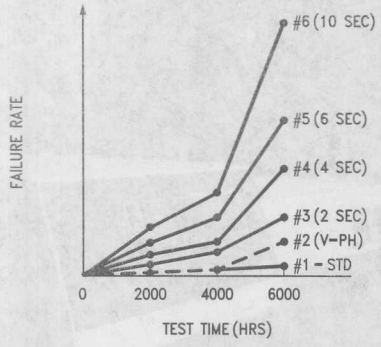
Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds



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FIGURE D

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferrably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

The basic component-placement systems available are classified as:

(a) In-line placement

— Fixed placement stations

— Boards indexed under head and respective components placed

(b) Sequential placement

— Either a X-Y moving table system or a θ, X-Y moving pickup system used

—Individual components picked and placed onto boards

(c) Simultaneous placement

— Multiple pickup heads

— Whole array of components placed onto the PCB at the same time

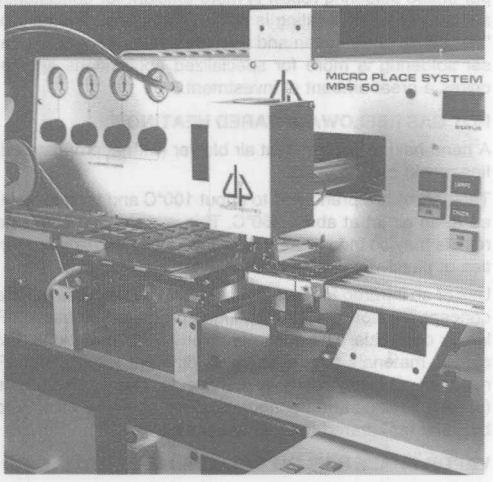
(d) Sequential/simultaneous placement

— X–Y moving table, multiple pickup heads system

— Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



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BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

Use of an infrared furnace is the next step to automating the concept, except that the heating is promoted by use of IR lamps or panels. The main objection to this method is that certain materials may heat up at different rates under IR radiation and may result in damage to these components (usually sockets and connectors). This could be minimized by using far-infrared (non-focused) system.

VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

The commonly used fluids (supplied by 3M Corp) are:

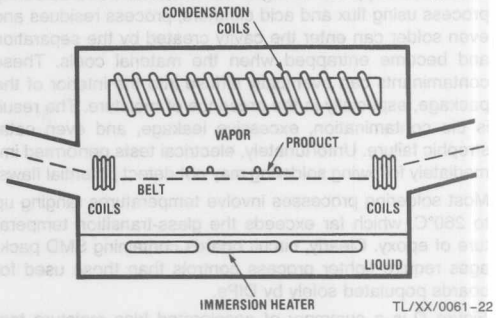
- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyorized systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).

In-Line Conveyorized Vapor-Phase Soldering



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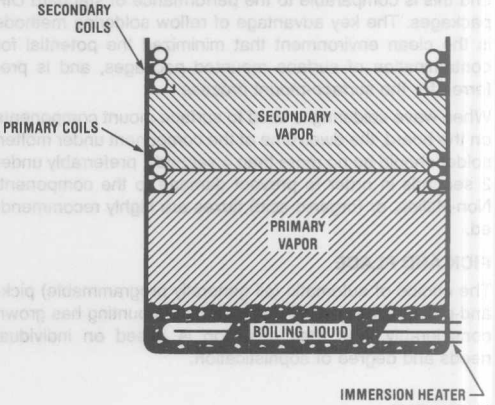
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace



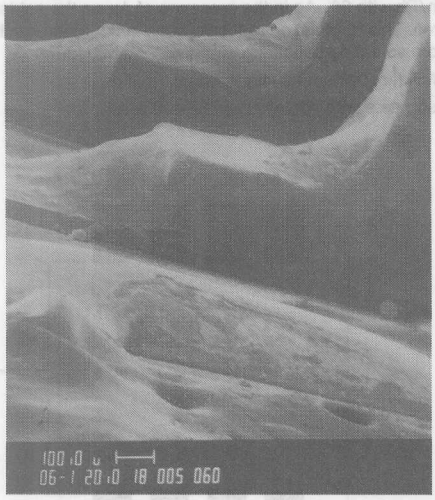
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Batch-Fed Production Vapor-Phase Soldering Unit



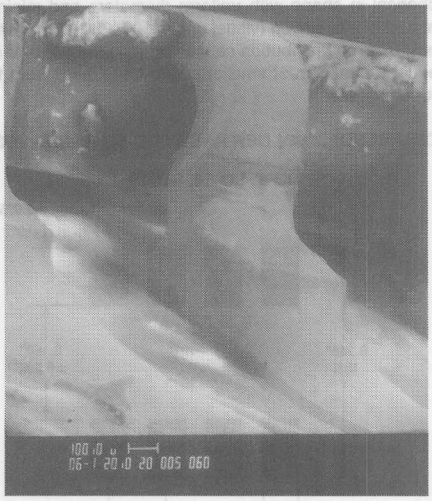
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Solder Joints on a SO-14 Package on PCB



TL/XX/0061–25

Solder Joints on a SO-14 Package on PCB



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PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polymide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

  The mask also protects circuits from processing chemical contamination and corrosion.

  If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

  Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

  General requirements for solder mask:

  — Good pattern resolution.

  — Complete coverage of circuit lines and resistance to flaking during soldering.

  — Adhesion should be excellent on substrate material to keep off moisture and chemicals.

  — Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050″ lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005″ usually used to achieve a solder paste thickness (wet) of about 0.008″ typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed 1/8″, to avoid damage to screens and minimize distortion.

SOLDER PASTE

Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see photographs below). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.

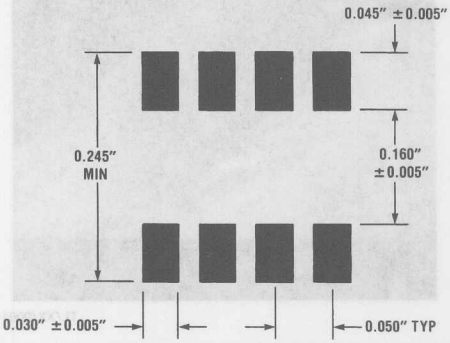
tion). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.

from soldering pads.

- RMA flux system usually used.
- Use paste with aproximately 88–90% solids.

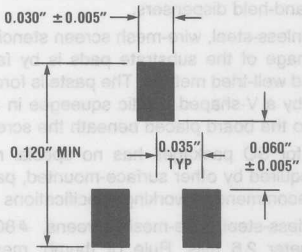
RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16



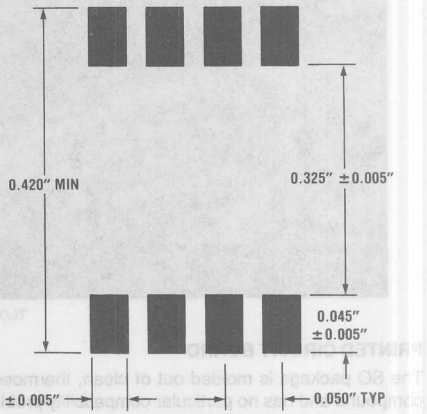
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SOT-23



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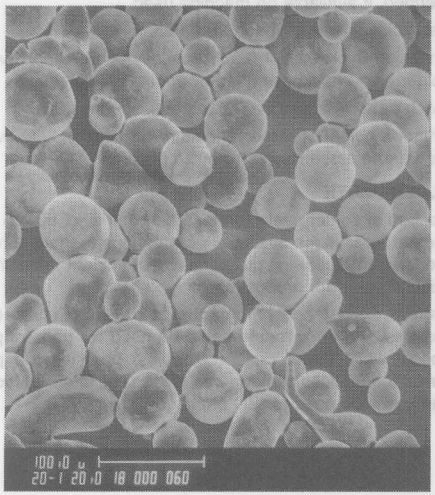
SO-16L, SO-20



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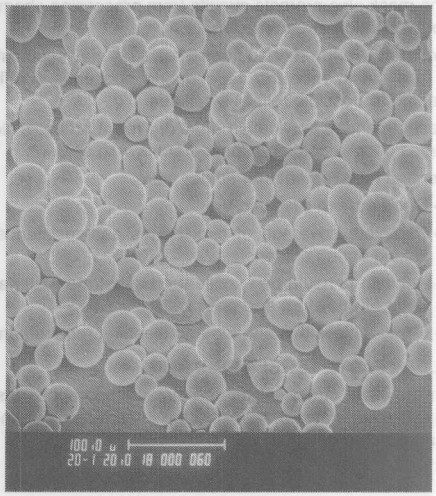
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)



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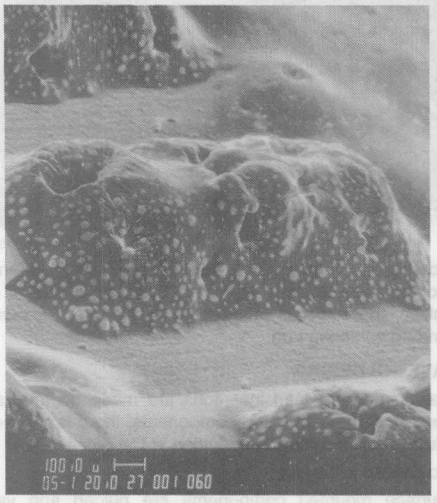
200 × Kester (63/37)



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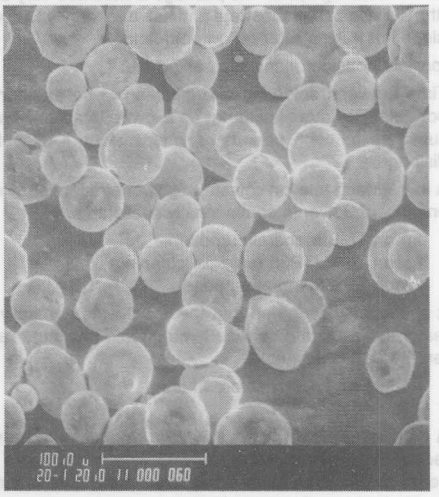
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



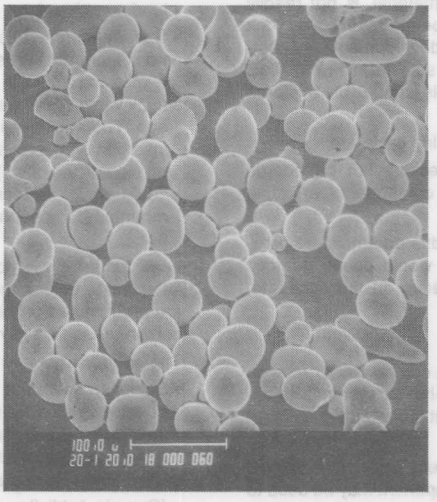
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200 × Fry Metal (63/37)



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200 ESL (63/37)



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CLEANING

The most critical process in surface mounting SO packages is in the cleaning cycle. The package is mounted very close to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. Solvents commercially available are:

  Freon TMS (general purpose)
  Freon TE35/TP35 (cold-dip cleaning)
  Freon TES (general purpose)

  It should also be noted that these solvents generally will leave the substrate surface hydrophobic (moisture repellent), which is desirable.

  Prelete or 1,1,1-Trichloroethane
  Kester 5120/5121
- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirments for low-volume production.
- For volume production, a conveyorized, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

The dangers of an inadequate cleaning cycle are:

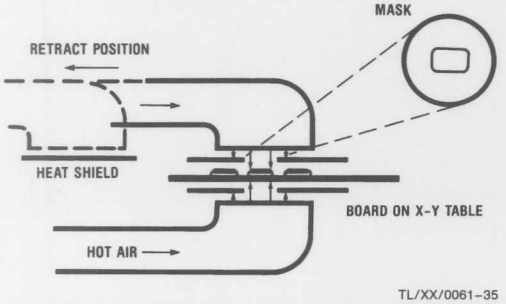
- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dentritic growth between close spacing traces on the substrate, resulting in failures (shorts).

REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

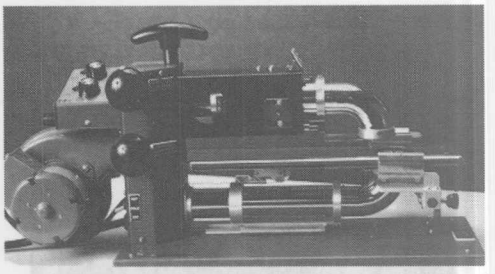
When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

Hot-Air Solder Rework Station



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Hot-Air Rework Machine



TL/XX/0061–36

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

Two options are used:

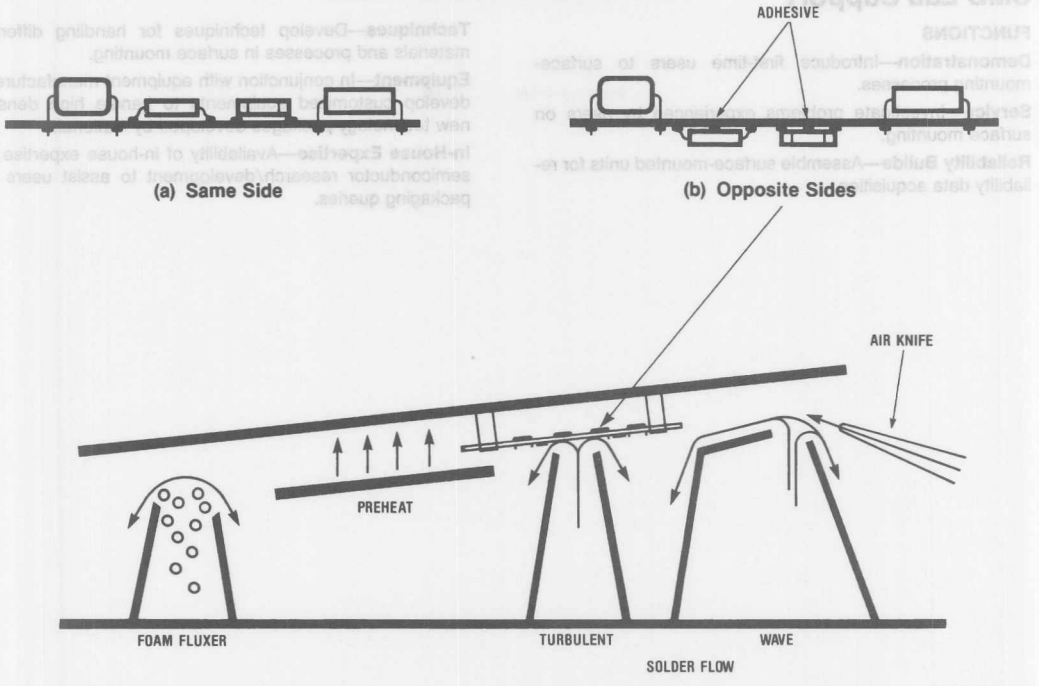
- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050″ vs 0.100″ for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.

Mixed Surface Mount and Lead Insertion



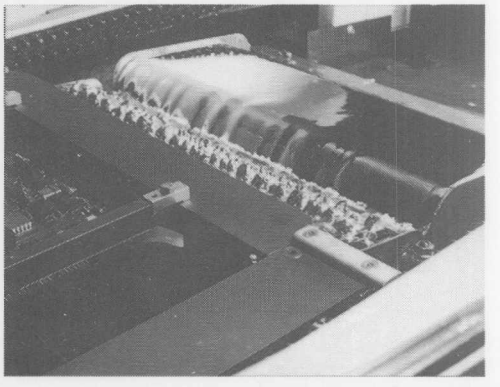
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A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyorized system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/XX/0061–38

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

7

Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.



Section 8

Appendices/ Physical Dimensions

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Appendix A
Military Aerospace Programs from National Semiconductor

This appendix is intended to provide a brief overview of military products available from National Semiconductor. For further information, refer to our *1987 Reliability Handbook.*

MIL-M-38510

The MIL-M-38510 Program, which is sometimes called the JAN IC Program, is administered by the Defense Electronics Supply Center (DESC). The purpose of this program is to provide the military community with standardized products that have been manufactured and screened to government-controlled specifications in government-certified facilities. All 38510 manufacturers must be formally qualified and their products listed on DESC's Qualified Products List (QPL) before devices can be marked and shipped as JAN product.

There are two processing levels specified within MIL-M-38510: Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems. National is a major supplier of both classes of devices. Screening requirements are outlined in Table III.

Tables I and II explain the JAN device marking system.

Copies of MIL-M-38510, the QPL, and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

DESC Specifications

DESC specifications are issued to provide standardized versions of devices which are not yet available as JAN product. MIL-STD-883 Class B screening is coupled with tightly controlled electrical specifications which have been written to allow a manufacturer to use his standard electrical tests. A current listing of National's DESC specification offerings can be obtained from our franchised distributors, sales offices, or DESC. DESC is located in Dayton, Ohio.

MIL-STD-883

Although originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-JAN military product. Revision C of this document defines the minimum requirements for a device to be marked and advertised as 883-compliant. Included are design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures. Details can be found in paragraph 1.2.1 of MIL-STD-883.

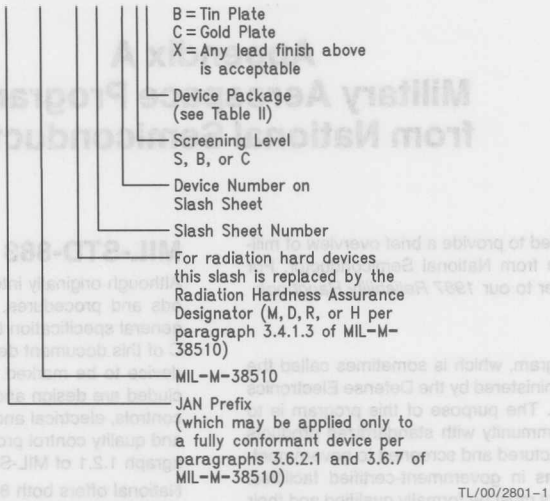
National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

As with DESC specifications, a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits, and test temperatures must be clearly documented. At National Semiconductor, this information is available via our RETS (Reliability Electrical Test Specification Program). The RETS document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military Screening Program (MSP)

National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly than is possible for JAN and 883 devices. Through this program, screened product is made available for prototypes and breadboards prior to or during the JAN or 883 qualification activities. MSP products receive the 100% screening of Table III but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.



TL/00/2801–1

TABLE II. JAN Package Codes

38510 Package Designation	Microcircuit Industry Description
A	14-Pin 1/4″ X 1/4″ (metal) flat pack
B	14-Pin 3/16″ X 1/4″ flat pack
C	14-Pin 1/4″ X 3/4″ dual-in-line
D	14-Pin 1/4″ X 3/8″ (ceramic) flat pack
E	16-Pin 1/4″ X 3/8″ dual-in-line
F	16-Pin 1/4″ X 3/8″ (metal or ceramic) flat pack
G	8-pin TO-99 can or header
H	10-pin 1/4″ x 1/4″ (metal) flat pack
I	10-pin TO-100 can or header
J	24-pin 1/2″ x 1-1/4″ dual-in-line
K	24-pin 3/8″ x 5/8″ flat pack
L	24-pin 1/4″ x 1-1/4″ dual-in-line
M	12-pin TO-101 can or header
N	(Note 1)
P	8-pin 1/4″ x 3/8″ dual-in-line
Q	40-pin 3/16″ x 2-1/16″ dual-in-line
R	20-pin 1/4″ x 1-1/16″ dual-in-line
S	20-pin 1/4″ x 1/2″ flat pack
T	(Note 1)
U	(Note 1)
V	18-pin 3/8″ x 15/16″ dual-in-line
W	22-pin 3/8″ x 1-1/8″ dual-in-line
X	(Note 1)
Y	(Note 1)
Z	(Note 1)
2	20-terminal 0.350″ x 0.350″ chip carrier
3	28-terminal 0.450″ x 0.450″ chip carrier

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

Screen	Class S		Class B	
	Method	Reqmt	Method	Reqmt
1. Wafer Lot Acceptance	5007	All Lots		—
2. Nondestructive Bond Pull	2023	100%		—
3. Internal Visual (Note 1)	2010, Condition A	100%	2010, Condition B	100%
4. Stabilization Bake	1008, Condition C, 24 hrs. Min.	100%	1008, Condition C, 24 hrs. Min.	100%
5. Temp. Cycling (Note 2)	1010, Condition C	100%	1010, Condition C	100%
6. Constant Acceleration	2001, Condition E (Min.) Y_1 Orientation Only	100%	2001, Condition E, (Min.), Y_1 Orientation Only	100%
7. Visual Inspection (Note 3)		100%		100%
8. Particle Impact Noise Detection (PIND)	2020, Condition A (Note 4)	100%		—
9. Serialization	(Note 5)	100%		—
10. Interim (Pre-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%	Per Applicable Device Specification (Note 6)	—
11. Burn-In Test	1015 240 Hrs. @ 125°C Min. (Cond. F Not Allowed)	100%	1015 160 Hrs. @ 125°C Min.	100%
12. Interim (Post-Burn-In) Electrical Parameters	Per Applicable Device Specification (Note 13)	100%		
13. Reverse Bias Burn-In (Note 7)	1015; Test Condition A, C, 72 Hrs. @ 150°C Min. (Cond. F Not Allowed)	100%		—
15. PDA Calculation	5% Parametric (Note 14), 3% Functional −25°C	All Lots	5% Parametric (Note 14)	All Lots
16. Final Electrical Test	Per Applicable Device Specification		Per Applicable Device Specification	
a) Static Tests				
1) 25°C (Subgroup 1, Table I, 5005)		100%		100%
2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005)		100%		100%
b) Dynamic Tests & Switching Tests, 25°C (Subgroups 4, 9, Table I, 5005)		100%		100%
c) Functional Test, 25°C (Subgroup 7, Table I, 5005)		100%		100%

TABLE III. 100% Screening Requirements (Continued)

Screen		Class S		Class B	
		Method	Reqmt	Method	Reqmt
17.	Seal Fine, Gross	1014	100%, (Note 8)	1014	100%, (Note 9)
18.	Radiographic (Note 10)	2012 Two Views	100%		—
19.	Qualification or Quality Conformance Inspection Test Sample Selection	(Note 11)	Samp.	(Note 11)	Samp.
20.	External Visual (Note 12)	2009	100%		100%

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock method 1011, test condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-M-38510, paragraph 4.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separate or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g. flatpacks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 19.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and Record when past burn-in delta measurements are specified.

Note 14: PDA shall apply to all static, dynamic, functional, and switching measurements at either 25°C or maximum rated operating temperature.

Military CMOS Products Available From National Semiconductor

Listed below are the military class B CMOS devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

	HC MIL/AERO Flows			
Device	-MIL	/883	DESC/SMD	JAN
HC00		x	x	x
HC02		x	x	x
HC03		x		
HC04		x	x	
HC05				
HC08		x	x	x
HC10		x	x	x
HC107		x	x	
HC109		x	x	
HC11		x	x	
HC112		x	x	
HC113		x		
HC123A		x	x	
HC125		x		
HC126		x	x	
HC132		x		x
HC133		x		
HC137				
HC138		x	x	x
HC139		x	x	
HC14		x	x	x
HC147		x	x	
HC148				
HC149				
HC151		x	x	
HC153		x	x	
HC154		x		
HC155				
HC157		x		
HC158		x		
HC160		x	x	
HC161		x	x	
HC162		x	x	
HC163		x		
HC164		x	x	
HC165		x	x	
HC166				
HC173		x	x	
HC174		x	x	

	HC MIL/AERO Flows			
Device	-MIL	/883	DESC/SMD	JAN
HC175		x	x	
HC181				
HC182				
HC190				
HC191				
HC192		x	x	
HC193		x		
HC194		x	x	
HC195		x	x	
HC20		x	x	x
HC221A		x		
HC237				
HC240		x		
HC241		x		
HC242		x		
HC243		x	x	
HC244		x	x	
HC245		x		
HC251		x	x	
HC253		x		
HC257		x	x	
HC258				
HC259		x	x	
HC266A		x		
HC27		x	x	
HC273		x		
HC280		x	x	
HC283		x		
HC298		x		
HC299		x		
HC30		x	x	x
HC32		x	x	x
HC34				
HC354		x		
HC356	x			
HC365		x	x	
HC366		x		
HC367		x	x	
HC368		x	x	

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

HC MIL/AERO Flows

Device	-MIL	/883	DESC/SMD	JAN
HC373		x	x	
HC374		x	x	
HC390		x	x	
HC393		x	x	
HC4002		x	x	
HC4016				
HC4017		x	x	
HC4020		x		
HC4040		x		
HC4046				
HC4049		x	x	
HC4050		x	x	
HC4051				
HC4052				
HC4053				
HC4060		x		
HC4066				
HC4075		x		
HC4078		x		
HC42		x	x	
HC423A		x		
HC4316				
HC4511		x		
HC4514		x		
HC4538		x		
HC4543		x		
HC51		x		
HC521				
HC533		x	x	
HC534	x			
HC540				
HC541				
HC563		x		
HC564		x		
HC573		x		
HC574		x		
HC58		x		
HC589				
HC595				

HC MIL/AERO Flows

Device	-MIL	/883	DESC/SMD	JAN
HC597				
HC620				
HC623				
HC640		x		
HC643		x		
HC646		x		
HC648				
HC688		x		
HC7266		x		
HC73		x	x	
HC74		x	x	
HC75		x	x	
HC76		x		
HC85		x	x	
HC86		x	x	
HCT00				
HCT03				
HCT04		x		
HCT05				
HCT08				
HCT109				
HCT112				
HCT138		x		
HCT139				
HCT147				
HCT148				
HCT149				
HCT151				
HCT153				
HCT155				
HCT157				
HCT158				
HCT160				
HCT161				
HCT162				
HCT163				
HCT164				
HCT166				
HCT168				

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Military CMOS Products Available From National Semiconductor

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HC MIL/AERO Flows

Device	-MIL	/883	DESC/SMD	JAN
HCT169		x		
HCT190		x		
HCT191		x		
HCT192		x		
HCT193		x		
HCT240		x		
HCT241		x		
HCT244		x		
HCT245		x		
HCT251		x		
HCT253		x		
HCT257		x		
HCT258		x		
HCT273		x		
HCT32		x		

HC MIL/AERO Flows

Device	-MIL	/883	DESC/SMD	JAN
HCT34		x		
HCT373		x		
HCT374		x		
HCT521	x	x		
HCT533		x		
HCT534			x	
HCT540		x		
HCT541		x		
HCT640			x	
HCT643		x		
HCT688		x		
HCT74		x		
HCT76			x	
HCU04		x	x	

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Military CMOS Products Available From National Semiconductor

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	C MIL/AERO Flows			
Device	-MIL	/883C	DESC/SMD	JAN
MM54C00		x		
MM54C02		x		
MM54C04		x		
MM54C08		x	x	
MM54C10		x		
MM54C107	x			
MM54C14		x		
MM54C151		x		
MM54C154	x			
MM54C157		x		
MM54C160		x		
MM54C161		x		
MM54C162	x			
MM54C163		x		
MM54C164		x		
MM54C165	x			
MM54C173		x		
MM54C174		x		
MM54C175		x		
MM54C192		x		
MM54C193		x		
MM54C195		x		
MM54C200		x		
MM54C221		x		
MM54C244	x			
MM54C30		x		

	C MIL/AERO Flows			
Device	-MIL	/883C	DESC/SMD	JAN
MM54C32		x		
MM54C373		x		
MM54C374		x		
MM54C42		x		
MM54C48		x		
MM54C74		x		
MM54C76		x		
MM54C83		x		
MM54C85		x		
MM54C86		x		
MM54C89		x		
MM54C90		x		
MM54C901		x		
MM54C902		x		
MM54C905		x		
MM54C906		x		
MM54C907		x		
MM54C914		x		
MM54C922		x		
MM54C923	x			
MM54C941	x			
MM70C95	x			
MM70C97	x			
MM70C98	x			
MM78C29	x			
MM78C30	x			

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

Military CMOS Products Available From National Semiconductor

Listed below are the military class B CMOS devices available from National Semiconductor. Many of these are also available as Class S product. Additional information including new product plans can be obtained from our sales offices.

CD4000 MIL/AERO Flows

Device	-MIL	/883	DESC/SMD	JAN
CD4001B		x		
CD4002A				x
CD4002B		x		
CD4006A				x
CD4006B		x		
CD4007A		x		x
CD4008B				
CD4009A		x		
CD4010A				
CD4011A				x
CD4011B		x		
CD4012A				x
CD4012B		x		
CD4013A				x
CD4013B		x		x
CD4014A				x
CD4014B		x		
CD4015A				x
CD4015B				
CD4016B	x			
CD4017A				x
CD4017B		x		
CD4018A				x
CD4018B	x			x
CD4019A				x
CD4019B		x		x
CD4020A				x
CD4020B		x		
CD4021A				x
CD4021B				
CD4022A				x
CD4022B				
CD4023A				x
CD4023B		x		
CD4024A				x
CD4024B				
CD4025A				x
CD4025B		x		x

CD4000 MIL/AERO Flows

Device	-MIL	/883	DESC/SMD	JAN
CD4027A				x
CD4027B		x		
CD4028B		x		
CD4029B		x	x	
CD4030A		x		x
CD4031B	x			
CD4034B	x			
CD4040B		x	x	
CD4041A		x		
CD4042B				
CD4043B				
CD4044B				
CD4046B				
CD4047B		x		
CD4048B	x			
CD4049A				x
CD4049UB		x		
CD4050A				x
CD4050B		x		x
CD4051B		x		
CD4052B		x	x	
CD4053B		x		
CD4060B	x			
CD4066B		x		
CD4069A		x		
CD4070B		x		
CD4071B		x		
CD4072B				
CD4073B		x		
CD4075B		x		
CD4076B		x		
CD4081B		x		
CD4082B				
CD4089B				
CD4093B		x	x	
CD4094B				
CD4099B		x		

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

CD40106B		x	x	
CD40160B	x			
CD40161B		x		
CD40162B	x			
CD40163B		x		
CD40174B		x	x	
CD40175B		x		
CD40192B		x		
CD40193B		x		
CD40195B	x			
CD4503B		x		
CD4510B				
CD4511B		x		
CD4512B		x		
CD4514B				

CD4515B				
CD4516B				
CD4518B				
CD4519B				
CD4520B		x	x	
CD4522B				
CD4526B				
CD4527B				
CD4528B		x		
CD4529B				
CD4538B				
CD4541B				
CD4543B	x			
CD4723B				
CD4724B	x			

*Some older products are not completely compliant with MIL-STD-883 but are still required for use in military systems. These devices are screened to the same stringent requirements as 883 product but are marked "-MIL".

National Semiconductor

Appendix B
National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who need better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction; the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.



SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

National's A+ Program (Continued)

Five Temperature Cycles (0°C to 100°C)

Exercising each device over a 100°C temperature range provides an additional die and package stress.

High Temperature (100°C)

Functional Electrical Test

A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C—15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing

Every device is tested at 25°C for functional and DC parameters.

Burn-In Test

Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96 eV activation energy (i.e., 23 hours at +155°C). All burn-in done under steady-state conditions unless otherwise specified.

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-Than-Normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

National Semiconductor

Appendix C
National's Standard Processing Program

Standard Program: A comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

National's Standard Program Gets It All Together

With the exception of the final QC inspection, which is sampled, all steps of the process are performed on 100 percent of the program parts. The following flow chart shows how we do it step by step.



SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

High Temperature (100°C) Functional Electrical Test

A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C—15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittants, we perform this test to ensure against even the remotest possibility of such a problem.



Five Temperature Cycles (0°C to 100°C)

Exercising each device over a 100°C temperature range provides an additional die and package stress.

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-Than-Normal QC Inspection Plans

Sample parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max.

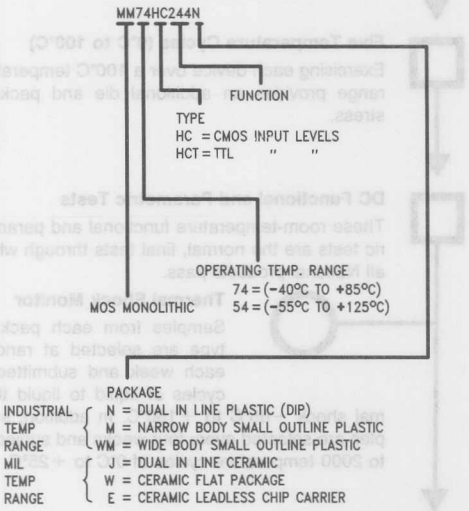
Ship Parts

Here are the QC sample plans used in our Standard Test Program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

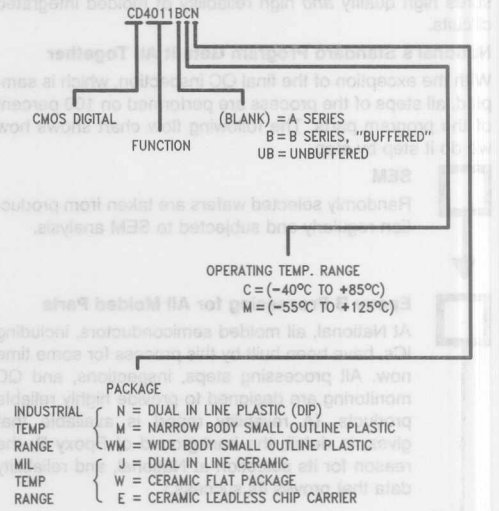
Appendix D
CMOS Ordering Information

High Speed CMOS



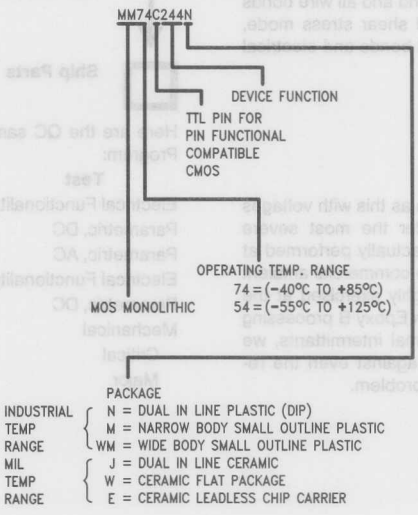
TL/XX/0062–1

Metal Gate CMOS



TL/XX/0062–2

Metal Gate CMOS



TL/XX/0062–3

CMOS Ordering Information
Industrial Temp. Range

Package ID	N14A	M14A	M14B	N16E	M16A	M16B	N24A	N24C	M24B
Suffix	N	M	WM	N	M	WM	N	N	WM
CD4000C	***								
CD4001BC	***	***							
CD4001C	***	***							
CD4011BC	***	***							
CD4002BC	***	***							
CD4012C	***								
CD4006BC	***								
CD4007C	***	***							
CD4008BC				***					
CD4009C				***					
CD4010C				***	***				
CD4013BC	***	***							
CD4014BC				***	***				
CD4015BC				***	***				
CD4016BC	***	***							
CD4017BC				***	***				
CD4022BC				***					
CD4018BC				***					
CD4019BC				***	***				
CD4020BC				***	***				
CD4040BC				***	***				
CD4060BC				***	***				
CD4021BC				***	***				
CD4023BC	***	***							
CD4025BC	***	***							
CD4024BC	***	***							
CD4027BC				***	***				
CD4028BC				***	***				
CD4029BC				***					
CD4030C	***								
CD4031BC				***					
CD4034BC							***		
CD4035BC				***					
CD4041UBC	***	***							
CD4042BC				***	***				
CD4043BC				***	***				
CD4044BC				***	***				
CD4046BC				***		***			
CD4047BC	***	***							
CD4048BC				***					
CD4049UBC				***	***				
CD4050BC				***	***				
CD4051BC				***	***				
CD4052BC				***	***				
CD4053BC				***	***				
CD4066BC	***	***							

CMOS Ordering Information
Industrial Temp. Range (Continued)

Package ID	N14A	M14A	M14B	N16E	M16A	M16B	N24A	N24C	M24B
Suffix	N	M	WM	N	M	WM	N	N	WM
CD4069UBC	***	***							
CD4070BC	***	***							
CD4071BC	***	***							
CD4081BC	***	***							
CD4072BC	***								
CD4082BC	***								
CD4073BC	***	***							
CD4075BC	***								
CD4076BC	***								
CD4089BC				***					
CD4527BC				***					
CD4093BC	***	***							
CD4094BC				***		***			
CD4099BC				***					
CD40106BC	***	***							
CD40160BC				***					
CD40161BC				***					
CD40162BC				***					
CD40163BC				***					
CD40174BC				***					
CD40175BC				***					
CD40192BC				***					
CD40193BC				***					
CD4503BC				***	***				
CD4510BC				***					
CD4516BC				***		***			
CD4511BC				***		***			
CD4512BC				***	***				
CD4514BC							***		***
CD4515BC							***		***
CD4518BC				***					
CD4520BC				***		***			
CD4519BC				***					
CD4522BC				***					
CD4526BC				***					
CD4528BC				***	***				
CD4529BC				***					
CD4538BC				***		***			
CD4541BC	***	***							
CD4543BC				***					
CD4584BC	***	***							
CD4723BC				***	***				
CD4724BC				***					

CMOS Ordering Information
Industrial Temp. Range (Continued)

Package ID	N08E	N14A	M14A	M14B	N16E	M16A	M16B	N18A	N20A	M20B	N24A	N24C	M24B	N28B	N40A
Suffix	N	N	M	WM	N	M	WM	N	N	WM	N	N	WM	N	N
MM74C00		***	***												
MM74C02		***													
MM74C04		***	***												
MM74C10		***													
MM74C20		***													
MM74C08		***													
MM74C14		***	***												
MM74C30		***													
MM74C32		***	***												
MM74C42					***										
MM74C48					***										
MM74C73		***													
MM74C76					***										
MM74C107		***													
MM74C74		***	***												
MM74C83					***										
MM74C85					***										
MM74C86		***	***												
MM74C89					***										
MM74C90		***													
MM74C93		***													
MM74C95		***													
MM74C150											***				
MM82C19											***				
MM74C151					***										
MM74C154											***		***		
MM74C157					***										
MM74C160					***										
MM74C161					***										
MM74C162					***										
MM74C163					***										
MM74C164		***													
MM74C165					***										
MM74C173					***										
MM74C174					***		***								
MM74C175					***										
MM74C192					***										
MM74C193					***	***									
MM74C195					***										
MM74C200	Call Factory														
MM74C221					***										
MM74C240									***	***					
MM74C244									***	***					

Suffix	N	N	M	WM	N	M	WM	N	N	WM	N	N	WM	N	N
MM74C373									***	***					
MM74C374									***	***					
MM74C901		***	***												
MM74C902		***													
MM74C903		***													
MM74C904		***													
MM74C905											***				
MM74C906		***	***												
MM74C907		***													
MM74C910								***							
MM74C914		***	***												
MM74C915								***							
MM74C922								***							
MM74C923									***	***					
MM74C932	***														
MM74C941									***						
MM74C989					***										
MM80C95					***										
MM80C96					***										
MM80C97					***	***									
MM80C98					***										
MM74C908	***														
MM74C918		***													
MM74C911														***	
MM74C912														***	
MM74C917														***	
MM74C925					***										
MM74C926								***							
MM74C927								***							
MM74C928								***							
MM74C945															***
MM74C947															***
MM74C946															***
MM74C956															***
MM88C29		***													
MM88C30		***													
MM74C924															***
MM74C934														***	
MM74C935														***	
MM74C936														***	
MM74C937											***				
MM74C938											***				
MM74C948															***
MM74C949														***	

CMOS Ordering Information
Industrial Temp. Range (Continued)

Package ID	N14A	M14A	M14B	N16E	M16A	M16B	N20A	M20B	N24C	M24B
Suffix	N	M	WM	N	M	WM	N	WM	N	WM
MM74HC00	***	***								
MM74HC02	***	***								
MM74HC03	***	***								
MM74HC04	***	***								
MM74HC05	***									
MM74HC08	***	***								
MM74HC10	***	***								
MM74HC11	***	***								
MM74HC14	***	***								
MM74HC20	***	***								
MM74HC27	***	***								
MM74HC30	***	***								
MM74HC32	***	***								
MM74HC34	***									
MM74HC42				***	***					
MM74HC51	***	***								
MM74HC58	***	***								
MM74HC73	***	***								
MM74HC74A	***	***								
MM74HC75				***	***					
MM74HC76				***	***					
MM74HC85				***		***				
MM74HC86	***	***								
MM74HC107	***									
MM74HC109A	***									
MM74HC112				***						
MM74HC113	***									
MM74HC123A				***	***					
MM74HC125	***	***								
MM74HC126	***	***								
MM74HC132	***	***								
MM74HC133				***	***					
MM74HC137				***	***					
MM74HC138				***	***					
MM74HC139				***	***					
MM74HC147				***	***					
MM74HC148				***						
MM74HC149							***	***		
MM74HC151				***	***					
MM74HC153				***	***					
MM74HC154									***	***
MM74HC155				***	***					
MM74HC157				***	***					
MM74HC158				***	***					
MM74HC160				***	***					
MM74HC161				***	***					

CMOS Ordering Information
Industrial Temp. Range (Continued)

Package ID	N14A	M14A	M14B	N16E	M16A	M16B	N20A	M20B	N24C	M24B
Suffix	N	M	WM	N	M	WM	N	WM	N	WM
MM74HC162				***	***					
MM74HC163				***	***					
MM74HC164				***	***					
MM74HC165				***	***					
MM74HC166				***	***					
MM74HC173				***	***					
MM74HC174				***	***					
MM74HC175				***	***					
MM74HC181									***	***
MM74HC182				***	***					
MM74HC190				***						
MM74HC191				***						
MM74HC192				***						
MM74HC193				***						
MM74HC194				***		***				
MM74HC195				***		***				
MM74HC221A				***	***					
MM74HC237				***	***					
MM74HC240							***	***		
MM74HC241							***	***		
MM74HC242	***	***								
MM74HC243	***	***								
MM74HC244							***	***		
MM74HC245A							***	***		
MM74HC251				***	***					
MM74HC253				***	***					
MM74HC257				***	***					
MM74HC258				***						
MM74HC259				***	***					
MM74HC266A	***	***								
MM74HC273							***	***		
MM74HC280	***	***								
MM74HC283				***	***					
MM74HC298				***	***					
MM74HC299							***	***		
MM74HC354							***	***		
MM74HC356							***	***		
MM74HC365				***		***				
MM74HC366				***		***				
MM74HC367				***		***				
MM74HC368				***		***				
MM74HC373							***	***		
MM74HC374							***	***		
MM74HC390				***		***				

CMOS Ordering Information
Industrial Temp. Range (Continued)

Package ID	N14A	M14A	M14B	N16E	M16A	M16B	N20A	M20B	N24C	M24B
Suffix	N	M	WM	N	M	WM	N	WM	N	WM
MM74HC393	***	***								
MM74HC423A				***	***					
MM74HC521							***	***		
MM74HC533							***	***		
MM74HC534							***	***		
MM74HC540							***	***		
MM74HC541							***	***		
MM74HC563							***	***		
MM74HC564							***	***		
MM74HC573							***	***		
MM74HC574							***	***		
MM74HC589				***	***					
MM74HC595				***	***					
MM74HC597				***	***					
MM74HC620							***	***		
MM74HC623							***	***		
MM74HC640							***	***		
MM74HC643							***	***		
MM74HC646									***	***
MM74HC648									***	***
MM74HC4002	***	***								
MM74HC4016	***		***							
MM74HC4017				***	***					
MM74HC4020				***	***					
MM74HC4040				***	***					
MM74HC4046				***	***					
MM74HC4049				***	***					
MM74HC4050				***	***					
MM74HC4051				***		***				
MM74HC4052				***		***				
MM74HC4053				***		***				
MM74HC4060				***	***					
MM74HC4066	***		***							
MM74HC4075	***	***								
MM74HC4078	***	***								
MM74HC4316				***		***				
MM74HC4511				***	***					
MM74HC4514									***	***
MM74HC4538				***	***					
MM74HC4543				***	***					
MM74HC942							***	***		
MM74HC943							***	***		
MM74HC7266	***	***								
MM74HCT00	***	***								

Package ID	N14A	M14A	M14B	N16E	M16A	M16B	N20A	M20B	N24C	M24B
Suffix	N	M	WM	N	M	WM	N	WM	N	WM
MM74HCT03	***						***	***		
MM74HCT04	***	***		***	***					
MM74HCT05	***	***								
MM74HCT08	***	***								
MM74HCT32	***	***								
MM74HCT34	***	***								
MM74HCT74	***	***								
MM74HCT76	***	***		***						
MM74HCT109	***	***		***						
MM74HCT112	***	***		***						
MM74HCT138	***	***		***	***					
MM74HCT139				***	***					
MM74HCT147				***	***					
MM74HCT148				***	***					
MM74HCT149	***	***					***	***		
MM74HCT151	***	***		***	***					
MM74HCT153	***	***		***		***				
MM74HCT155	***	***		***						
MM74HCT157				***	***					
MM74HCT158				***	***					
MM74HCT164	***	***					***	***		
MM74HCT166				***		***		***		
MM74HCT190				***	***					
MM74HCT191				***	***					
MM74HCT192				***	***					
MM74HCT193				***	***					
MM74HCT240				***	***		***	***		
MM74HCT241				***	***		***	***		
MM74HCT244			***		***		***	***		
MM74HCT245			***		***		***	***		
MM74HCT251			***	***	***					
MM74HCT253				***	***	***				
MM74HCT257				***		***		***		
MM74HCT273							***	***		
MM74HCT373							***	***		
MM74HCT374			***		***		***	***		
MM74HCT521				***	***		***	***		
MM74HCT533							***	***		
MM74HCT534				***	***		***	***		
MM74HCT540				***	***		***	***		
MM74HCT541	***	***					***	***		
MM74HCT640	***	***					***	***		
MM74HCT643							***	***		
MM74HCT688							***	***		

CMOS Ordering Information
Mil. Temp. Range

Package ID	J14A	W14B	J16A	W16A	E20A	J24F
Suffix	J	W	J	W	E	J
MM54HC00	***	***			***	
MM54HC02	***	***			***	
MM54HC03	***				***	
MM54HC04	***	***			***	
MM54HC05						
MM54HC08	***	***			***	
MM54HC10	***	***			***	
MM54HC11	***	***			***	
MM54HC14	***	***			***	
MM54HC20	***	***			***	
MM54HC27	***	***			***	
MM54HC30	***	***			***	
MM54HC32	***	***			***	
MM54HC34						
MM54HC42			***	***	***	
MM54HC51	***	***			***	
MM54HC58	***	***			***	
MM54HC73	***	***			***	
MM54HC74A	***	***			***	
MM54HC75			***	***	***	
MM54HC76			***	***	***	
MM54HC85			***	***	***	
MM54HC86	***	***			***	
MM54HC107	***	***			***	
MM54HC109A	***	***			***	
MM54HC112	***	***			***	
MM54HC113	***	***			***	
MM54HC123A			***	***	***	
MM54HC125	***	***			***	
MM54HC132	***	***			***	
MM54HC133			***	***	***	
MM54HC137						
MM54HC138			***	***	***	
MM54HC139			***	***	***	
MM54HC147			***	***	***	
MM54HC148						
MM54HC149						
MM54HC151			***	***	***	
MM54HC153			***	***	***	
MM54HC154						***
MM54HC155						
MM54HC157			***	***	***	
MM54HC158			***	***	***	
MM54HC160			***	***	***	
MM54HC161			***	***	***	
MM54HC162			***	***	***	

CMOS Ordering Information
Mil. Temp. Range

Package ID	J14A	W14B	J16A	W16A	E20A	J20A
Suffix	J	W	J	W	E	J
MM54HC163			***	***	***	
MM54HC164	***	***			***	
MM54HC165			***	***	***	
MM54HC166						
MM54HC173			***	***	***	
MM54HC174			***	***	***	
MM54HC175			***	***	***	
MM54HC181						
MM54HC182						
MM54HC190						
MM54HC191						
MM54HC192			***	***	***	
MM54HC193			***	***	***	
MM54HC194			***	***	***	
MM54HC195			***	***	***	
MM54HC221A			***	***	***	
MM54HC237						
MM54HC240					***	***
MM54HC241					***	***
MM54HC242	***	***			***	
MM54HC243	***	***			***	
MM54HC244					***	***
MM54HC245A					***	***
MM54HC251			***	***	***	
MM54HC253			***	***	***	
MM54HC257			***	***	***	
MM54HC258						
MM54HC259			***	***	***	
MM54HC266A	***	***			***	
MM54HC273						
MM54HC280	***	***			***	
MM54HC283			***	***	***	
MM54HC298			***	***	***	
MM54HC299					***	***
MM54HC354					***	***
MM54HC356						
MM54HC365			***	***	***	
MM54HC366			***	***	***	
MM54HC367			***			
MM54HC368			***	***	***	
MM54HC373					***	***
MM54HC374					***	***
MM54HC390			***	***	***	
MM54HC393	***	***			***	
MM54HC423A			***	***	***	

CMOS Ordering Information
Mil. Temp. Range

Package ID	J14A	W14B	J16A	W16A	E20A	J20A	J24F
Suffix	J	W	J	W	E	J	J
MM54HC521							
MM54HC533					***	***	
MM54HC534							
MM54HC540							
MM54HC541							
MM54HC563					***	***	
MM54HC564					***	***	
MM54HC573					***	***	
MM54HC574					***	***	
MM54HC589							
MM54HC595							
MM54HC597							
MM54HC620							
MM54HC623							
MM54HC640					***	***	
MM54HC643					***	***	
MM54HC646							
MM54HC688					***	***	
MM54HC4002	***	***			***		
MM54HC4016							
MM54HC4017			***	***	***		
MM54HC4020							
MM54HC4040							
MM54HC4046							
MM54HC4049			***	***	***		
MM54HC4050			***	***	***		
MM54HC4051							
MM54HC4052							
MM54HC4053							
MM54HC4060							
MM54HC4066							
MM54HC4075	***	***			***		
MM54HC4078	***	***			***		
MM54HC4316							
MM54HC4511			***	***	***		
MM54HC4514							***
MM54HC4538							
MM54HC4543			***	***	***		
MM54HC942							
MM54HC943							
MM54HC7266	***	***			***		
MM54HCT00							
MM54HCT03							
MM54HCT04							
MM54HCT05							

CMOS Ordering Information
Mil. Temp. Range

Package ID	J14A	W14B	J16A	W16A	E20A	J20A
Suffix	J	W	J	W	E	J
MM54HCT08						
MM54HCT32						
MM54HCT34						
MM54HCT74						
MM54HCT76						
MM54HCT109						
MM54HCT112						
MM54HCT138						
MM54HCT139						
MM54HCT147						
MM54HCT148						
MM54HCT149						
MM54HCT151						
MM54HCT153						
MM54HCT155						
MM54HCT157						
MM54HCT158						
MM54HCT164						
MM54HCT166						
MM54HCT190						
MM54HCT191						
MM54HCT192						
MM54HCT193						
MM54HCT240					***	***
MM54HCT241						
MM54HCT245						
MM54HCT251						
MM54HCT253						
MM54HCT257						
MM54HCT273						
MM54HCT373					***	***
MM54HCT374					***	***
MM54HCT521						
MM54HCT533						
MM54HCT534						
MM54HCT540						
MM54HCT541						
MM54HCT563						
MM54HCT564						
MM54HCT573						
MM54HCT574						
MM54HCT640						
MM54HCT643						
MM54HCT688						
CD4000M						

CMOS Ordering Information
Mil. Temp. Range

Package ID	J14A	W14B	J16A	W16A	J24A	F24C
Suffix	J	W	J	W	J	F
CD4001BM	***	***				
CD4011B	***	***				
CD4002BM	***	***				
CD4012BM	***	***				
CD4006B	***	***				
CD4007	***	***				
CD4008BM						
CD4009M			***	***		
CD4010M			***			
CD4013BM	***	***				
CD4014BM			***	***		
CD4015BM						
CD4016BM	***	***				
CD4017BM			***	***		
CD4022BM						
CD4018BM			***	***		
CD4019BM			***	***		
CD4020BM			***	***		
CD4040BM			***	***		
CD4060BM						
CD4021BM						
CD4023BM	***	***				
CD4025BM	***	***				
CD4024BM						
CD4027BM			***	***		
CD4028BM			***	***		
CD4029BM			***	***		
CD4030M	***	***				
CD4031BM			***	***		
CD4034BM					***	***
CD4035BM						
CD4041	***	***				
CD4042BM						
CD4043BM						
CD4044BM						
CD4046BM						
CD4047BM	***	***				
CD4048BM			***	***		
CD4049UBM			***	***		
CD4050BM			***	***		
CD4051BM			***	***		
CD4052BM			***	***		
CD4053BM			***	***		
CD4066BM	***	***				
CD4069	***	***				

CD4070BM	***	***				
CD4071BM	***	***				
CD4081BM	***	***				
CD4072BM						
CD4082BM						
CD4073BM	***	***				
CD4075BM	***	***				
CD4076BM			***	***		
CD4089BM						
CD4527BM						
CD4093BM	***	***				
CD4094BM						
CD4099BM			***	***		
CD40106BM	***	***				
CD40160BM			***	***		
CD40161BM			***	***		
CD40162BM			***	***		
CD40163BM			***	***		
CD40174BM			***	***		
CD40175BM			***	***		
CD40192BM			***	***		
CD40193BM			***	***		
CD4503BM						
CD4510BM						
CD4516BM						
CD4511BM			***	***		
CD4512BM			***	***		
CD4514BM						
CD4515BM						
CD4518BM						
CD4520BM			***	***		
CD4519BM						
CD4522BM						
CD4526BM						
CD4528BM			***	***		
CD4529BM						
CD4538BM						
CD4541BM						
CD4543BM			***	***		
CD4584BM						
CD4723BM						
CD4724BM			***			
MM54C00	***	***				
MM54C02	***	***				
MM54C04	***	***				

CMOS Ordering Information
Mil. Temp. Range

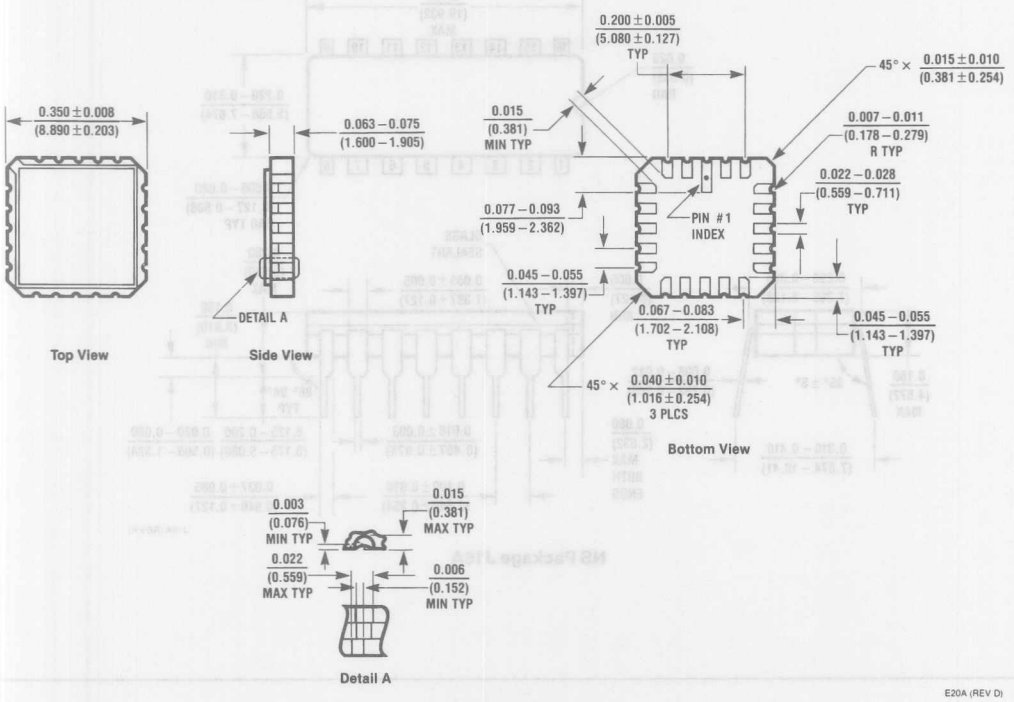
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Suffix	J	W	J	W	D	J
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MM54C20						
MM54C08		***				
MM54C14	***			***		
MM54C30	***			***		
MM54C32	***					
MM54C42				***		
MM54C48	***					
MM54C73						
MM54C76				***		
MM54C107						
MM54C74	***					
MM54C83	***					
MM54C85				***		
MM54C86	***					
MM54C89	***			***		
MM54C90	***			***		
MM54C93						
MM54C95						
MM54C150						
MM82C19						
MM74C151	***					
MM54C154						
MM54C157			***	***		
MM54C160						
MM54C161			***	***		
MM54C162						
MM54C163			***	***		
MM54C164	***					
MM54C165						
MM54C173			***	***		
MM54C174			***	***		
MM54C175	***					
MM54C192			***	***		
MM54C193			***	***		
MM54C195	***					
MM54C200					***	
MM54C221			***	***		
MM54C240						
MM54C244						
MM54C373						***
MM54C374						***
MM54C901	***					
MM54C902			***	***		
MM54C903	***	***				

CMOS Ordering Information
Mil. Temp. Range

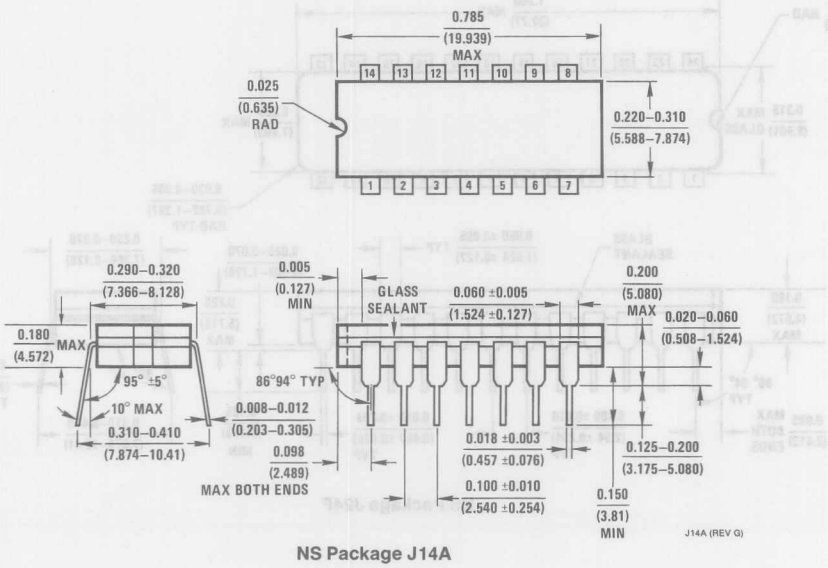
Package ID	J14A	W14B	J16A	W16A	J18A	J20A
Suffix	J	W	J	W	J	J
MM54C904						
MM54C905	***					
MM54C906	***	***				
MM54C907	***	***				
MM54C910						
MM54C914	***	***				
MM54C915						
MM54C922					***	
MM54C923						***
MM54C932						
MM54C941						
MM54C989						
MM70C95			***	***		
MM70C96						
MM70C97			***	***		
MM70C98			***	***		
MM54C908						
MM54C918						
MM54C911						
MM54C912						
MM54C917						
MM54C925						
MM54C926						
MM54C927						
MM54C928						
MM54C945						
MM54C947						
MM54C946						
MM54C956						
MM78C29						
MM78C30						

National Semiconductor

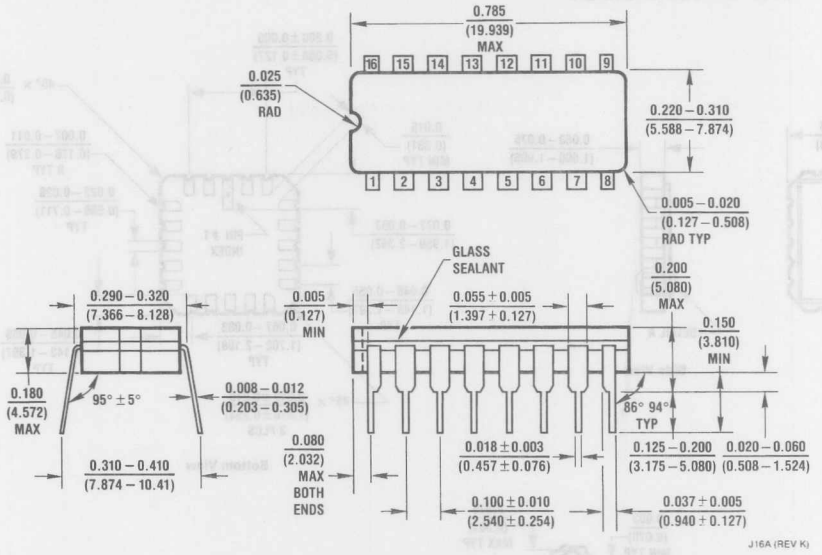
All dimensions are in inches (millimeters)



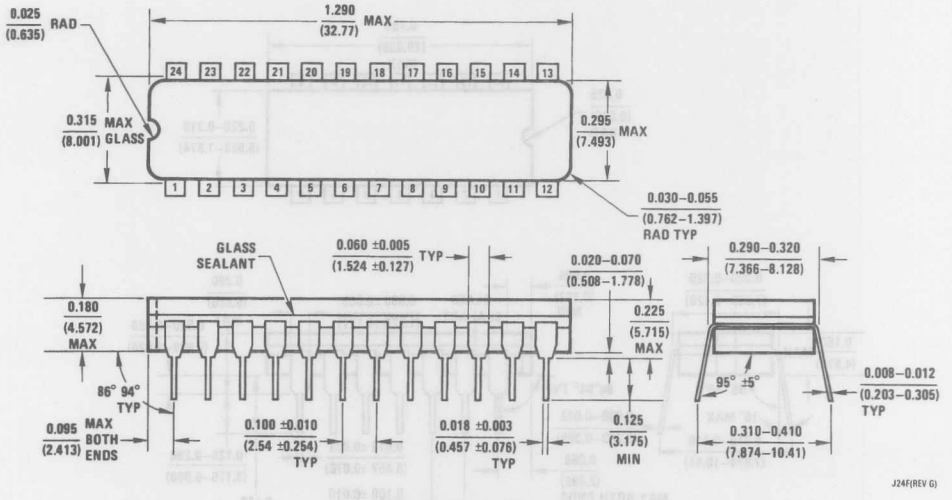
NS Package E20A



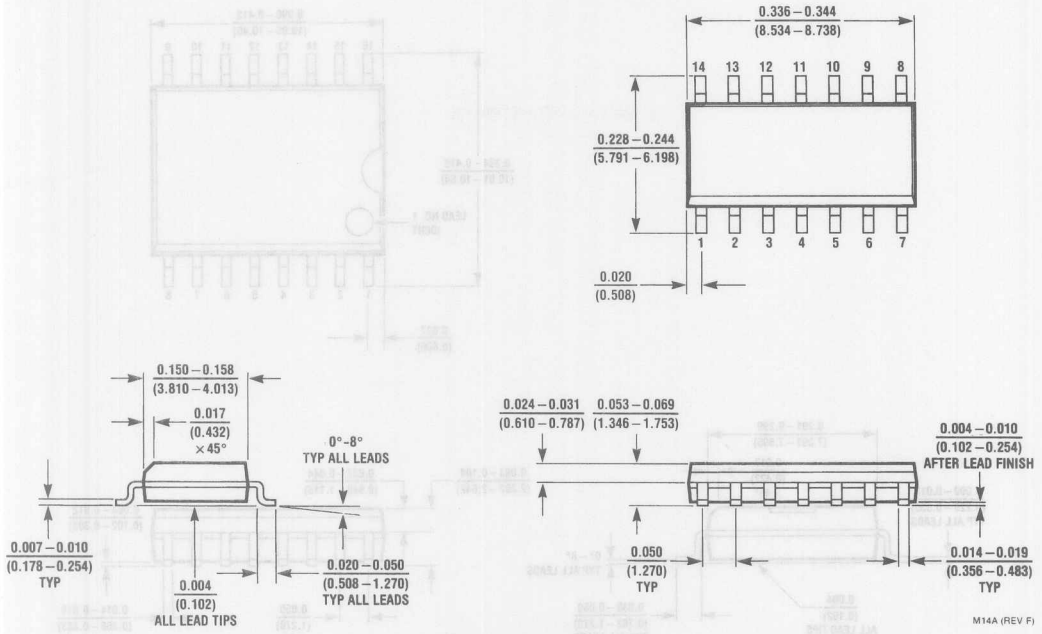
NS Package J14A



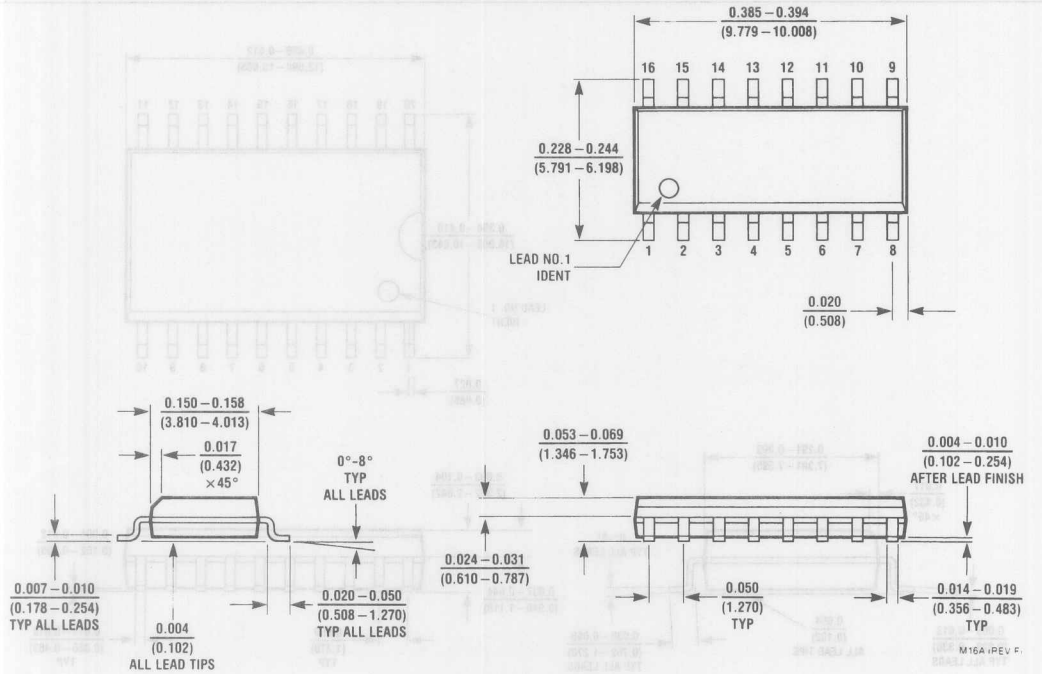
NS Package J16A



NS Package J24F

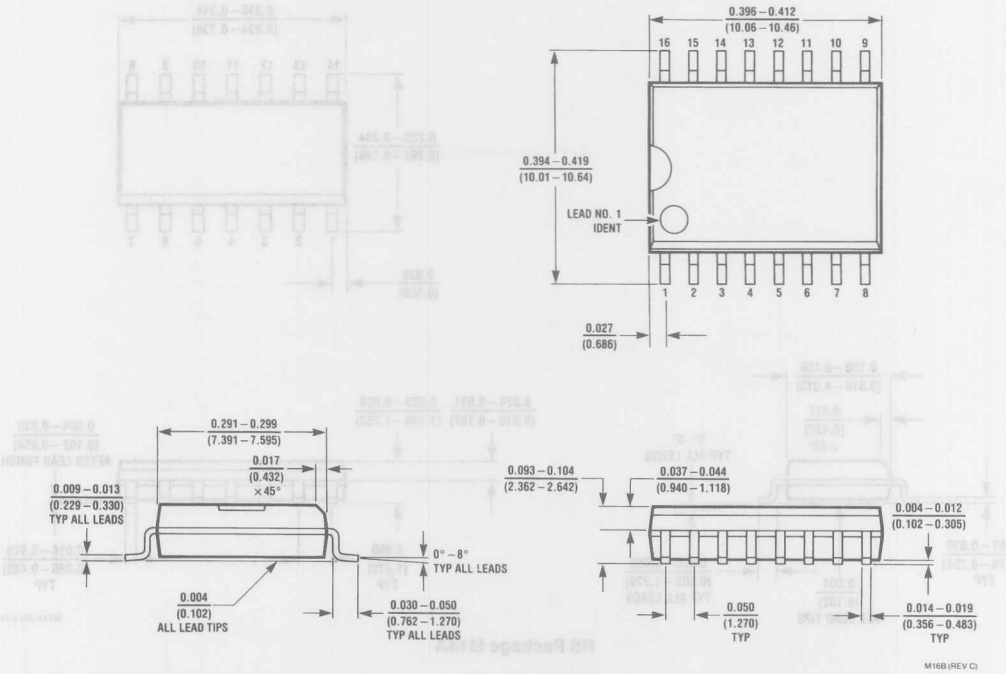


NS Package M14A

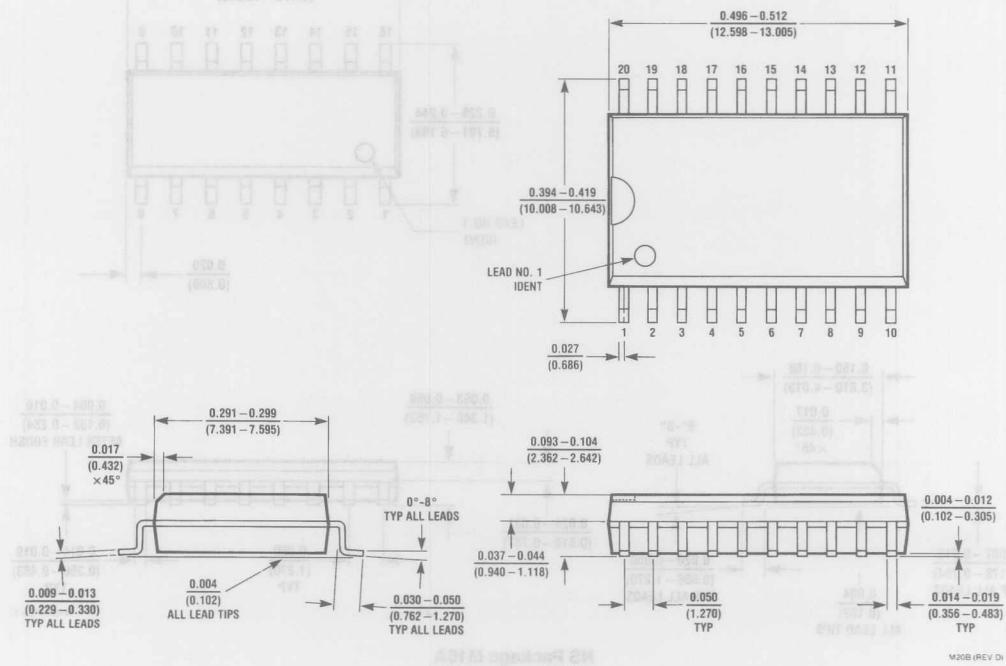


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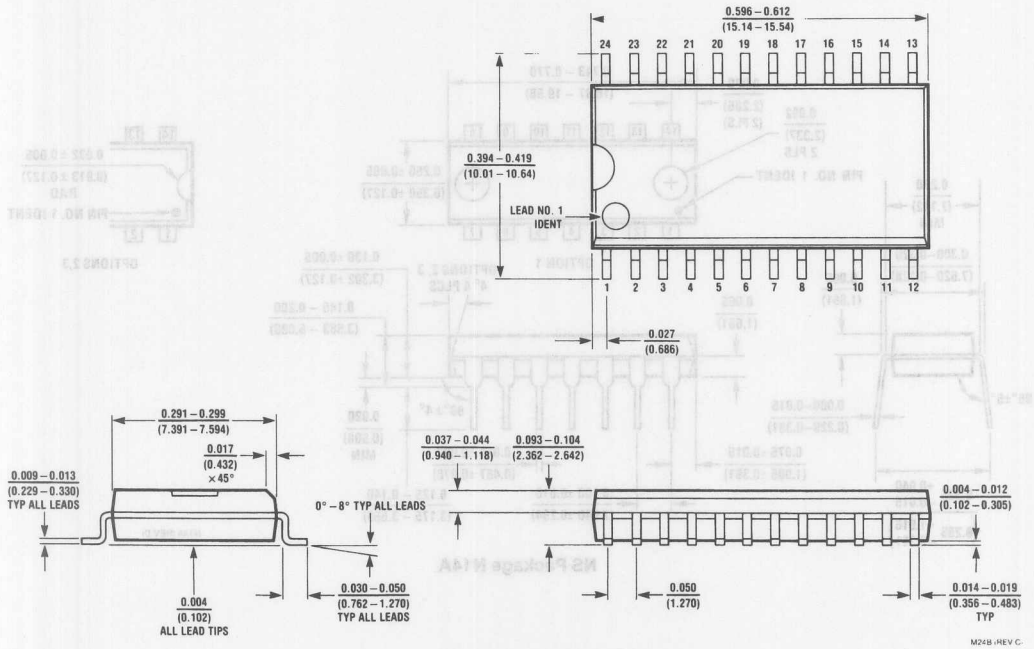
8



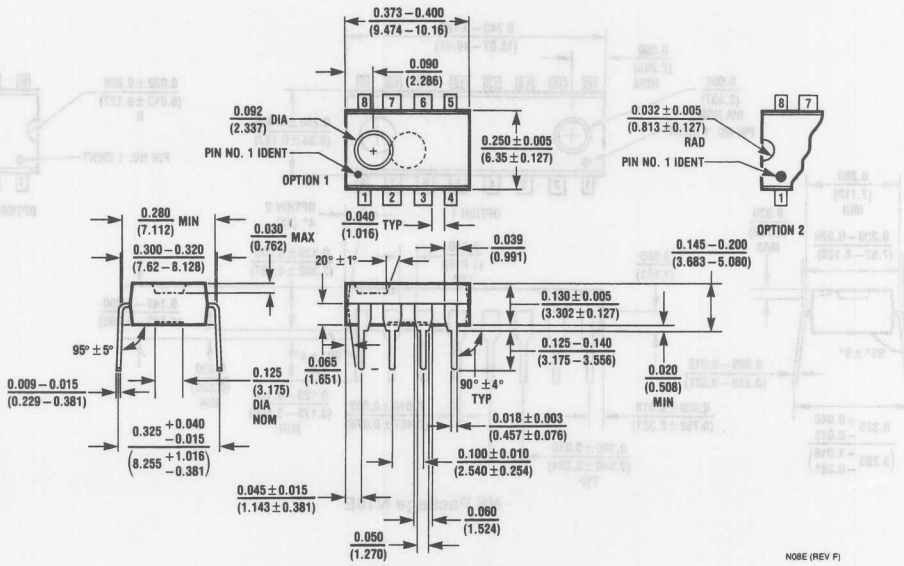
NS Package M16B



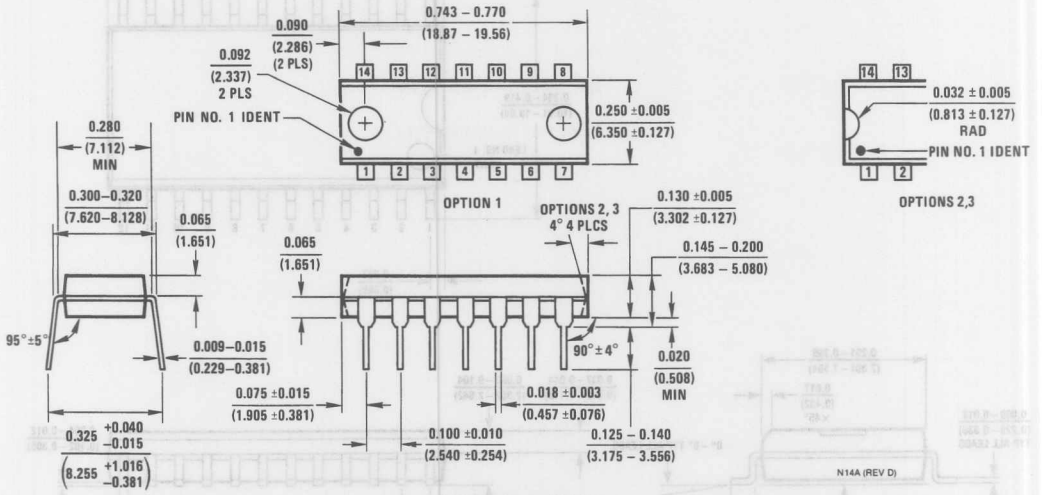
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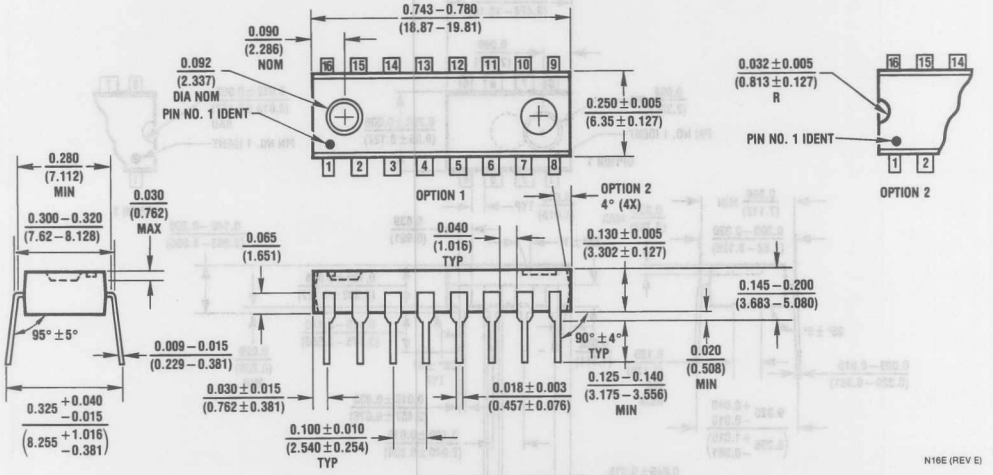
NS Package M24B



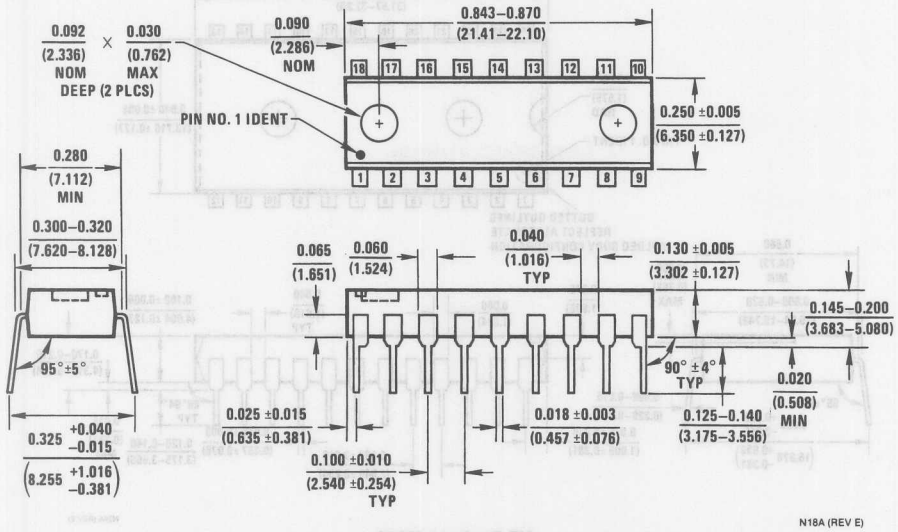
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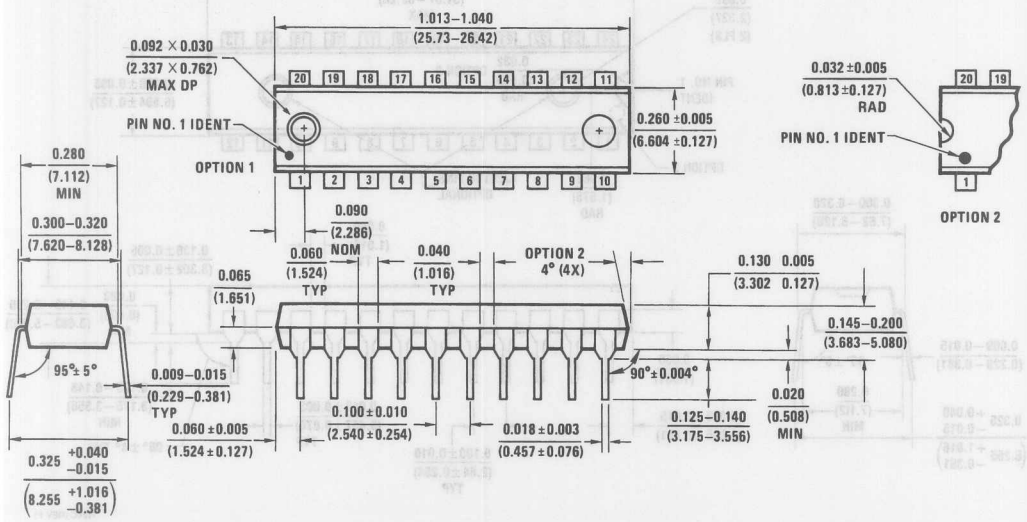
NS Package N14A



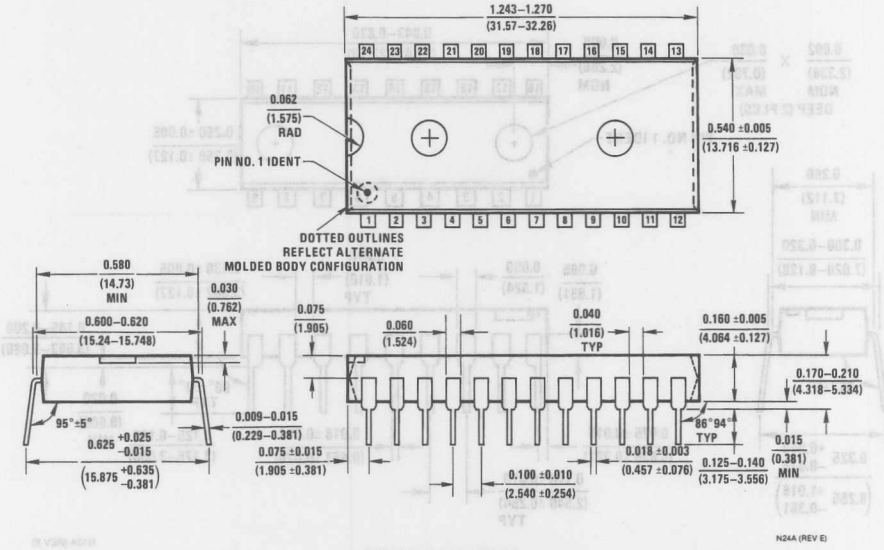
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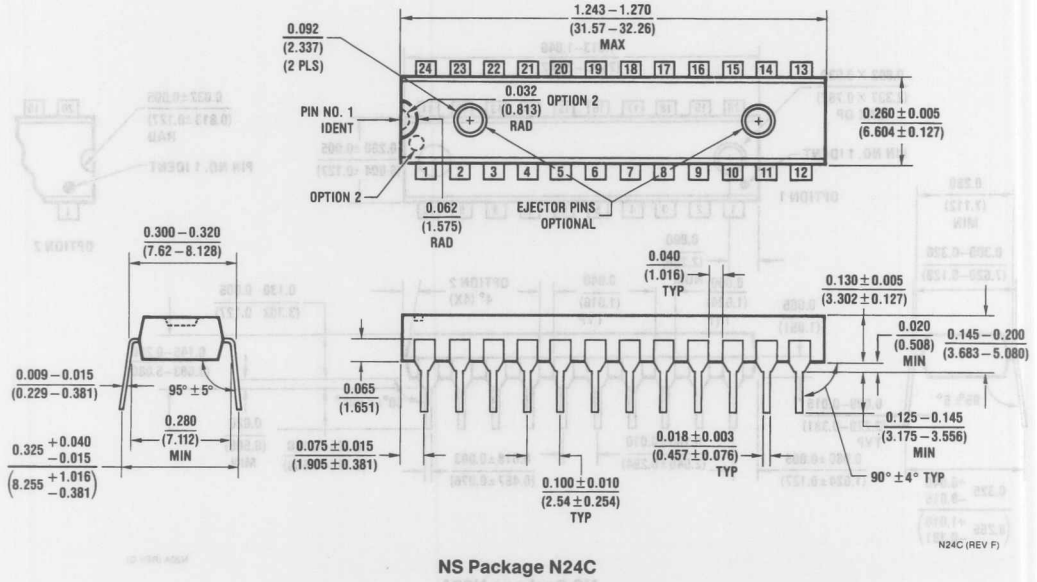
NS Package N18A



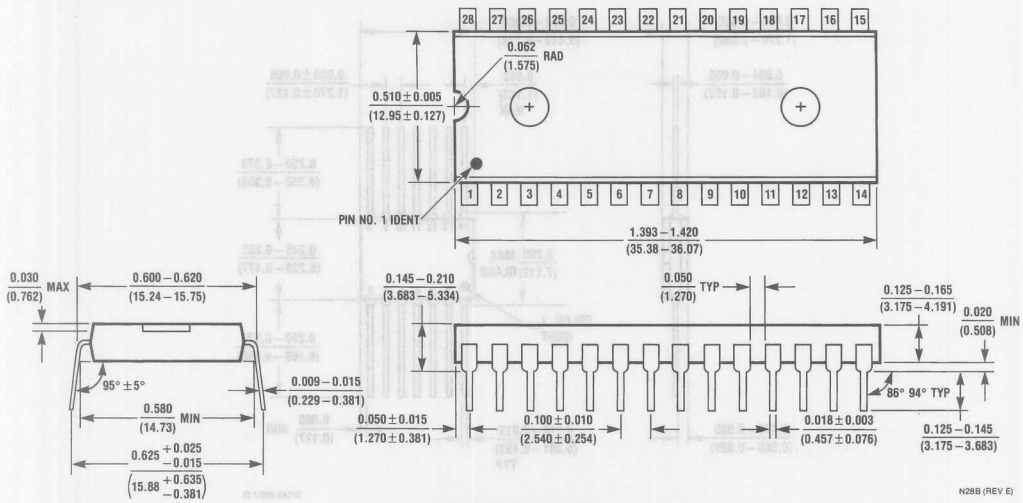
NS Package N20A



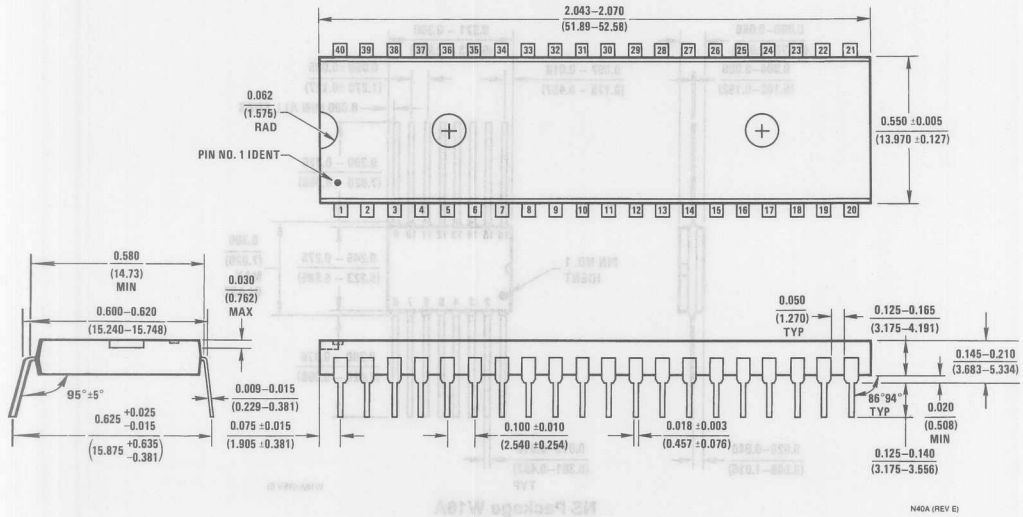
NS Package N24A



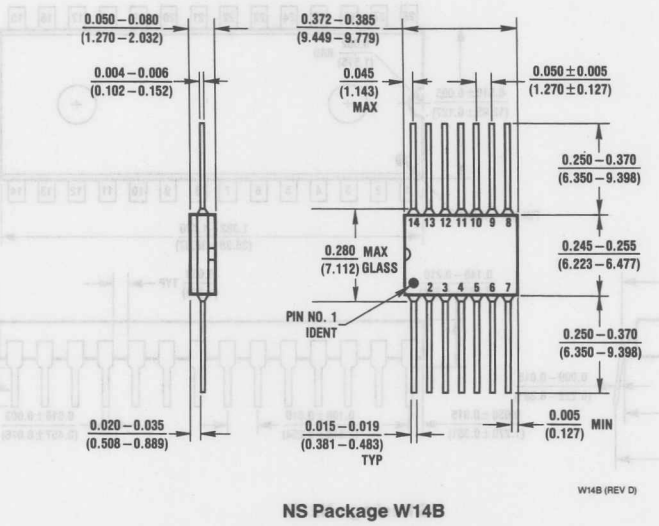
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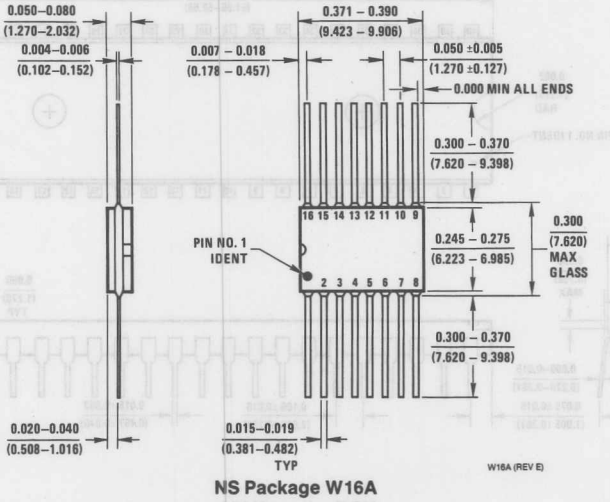
NS Package N28B



NS Package N40A



NS Package W14B



NS Package W16A